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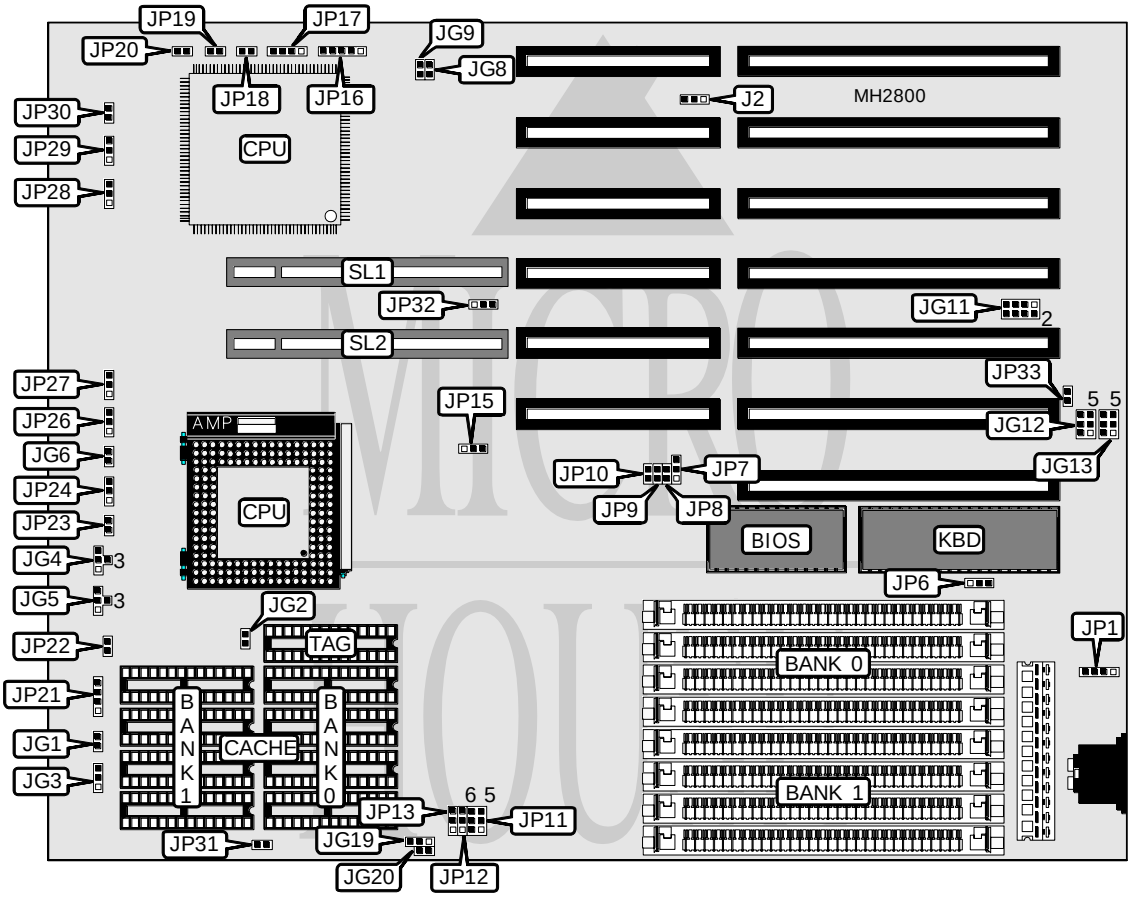
2VLG-A486A

Processor	CX486M6/80486SX/SL80486SX/80487SX/CX486M7/AM486DXL/80486DX/ SL80486DX2/80486DX2/Pentium Overdrive
Processor Speed	25/33/40/50(internal)/50/66(internal)MHz
Chip Set	Unidentified
Max. Onboard DRAM	128MB
Cache	32/64/128/256KB
BIOS	AMI
Dimensions	254mm x 218mm
I/O Options	32-bit VESA local bus slots (2), green PC connector
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
Modem ring in signal interface	JG8	Speaker	JP17
Green PC connector	JG9	Turbo switch	JP18
Green PC connector (monitor)	JG11 pins 5 & 6	Turbo LED	JP19
Green PC connector (fan)	JG11 pins 7 & 8	Reset switch	JP20
External battery	JP1	32-bit VESA local bus slots	SL1 & SL2
Power LED & keylock	JP16		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í CX487S not installed	J2	pins 2 & 3 closed
CX487S installed	J2	pins 1 & 2 closed
í Monitor type select monochrome	JP6	pins 1 & 2 closed
Monitor type select color	JP6	pins 2 & 3 closed
í CMOS memory normal operation	JP33	Open
CMOS memory clear	JP33	Closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
32MB	(4) 4M x 9	(4) 4M x 9
64MB	(4) 16M x 9	NONE
128MB	(4) 16M x 9	(4) 16M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
32KB	(4) 8K x 8	NONE	(1) 8K x 8
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 16K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION						
Size	JG19	JG20	JP11	JP12	JP13	JP31
32KB	1 & 2	Closed	Open	2 & 3	2 & 3	Open
64KB	1 & 2	Closed	Open	1 & 2	1 & 2	Closed
128KB	1 & 2	Closed	1 & 2, 3 & 4	2 & 3	1 & 2	Closed
256KB	2 & 3	Open	1 & 2, 3 & 4, 5 & 6	1 & 2	1 & 2	Closed
256KB	1 & 2	Closed	1 & 2, 3 & 4, 5 & 6	1 & 2	1 & 2	Closed
Note: Pins designated should be in the closed position.						

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CPU TYPE CONFIGURATION					
Type	JG1	JG2	JG3	JG4	JG5
CX486M6 1x	Closed	Open	1 & 2	2 & 4	2 & 4
CX486M6 2x	Closed	Open	1 & 2	2 & 4	2 & 4
80486SX	Open	Open	Open	Open	Open
SL80486SX	Open	Closed	2 & 3	1 & 2	1 & 2
80487SX	Open	Open	Open	Open	Open
CX486M7 1x	Closed	Open	1 & 2	2 & 4	2 & 4
CX486M7 2x	Closed	Open	1 & 2	2 & 4	2 & 4
AM486DXL	Open	Open	Open	2 & 3	2 & 3
80486DX	Open	Open	Open	Open	Open
SL80486DX	Open	Closed	2 & 3	1 & 2	1 & 2
80486DX2	Open	Open	Open	Open	Open
SL80486DX2	Open	Closed	2 & 3	1 & 2	1 & 2
P24T	Open	Open	Open	2 & 3	2 & 3
Note: Pins designated should be in the closed position.					

CPU TYPE CONFIGURATION (CON'T)						
Type	JG6	JP8	JP9	JP10	JP21	JP22
CX486M6 1x	Open	Closed	Open	Closed	3 & 4	Open
CX486M6 2x	Closed	Closed	Open	Closed	3 & 4	Open
80486SX	Open	Closed	Closed	Open	3 & 4	Closed
SL80486SX	Open	Closed	Closed	Open	3 & 4	Closed
80487SX	Open	Closed	Closed	Open	1 & 2	Closed
CX486M7 1x	Open	Closed	Open	Open	2 & 3	Closed
CX486M7 2x	Closed	Closed	Open	Open	2 & 3	Closed
AM486DXL	Open	Closed	Closed	Open	2 & 3	Closed
80486DX	Open	Closed	Closed	Open	2 & 3	Closed
SL80486DX	Open	Closed	Closed	Open	2 & 3	Closed
80486DX2	Open	Closed	Closed	Open	2 & 3	Closed
SL80486DX2	Open	Closed	Closed	Open	2 & 3	Closed
P24T	Open	Open	Closed	Open	1 & 2	Closed
Note: Pins designated should be in the closed position.						

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CPU TYPE CONFIGURATION (CON'T)					
Type	JP23	JP24	JP26	JP27	JP30
CX486M6 1x	Open	1 & 2	1 & 2	1 & 2	Closed
CX486M6 2x	Open	1 & 2	1 & 2	1 & 2	Closed
80486SX	Closed	1 & 2	1 & 2	1 & 2	Open
SL80486SX	Closed	1 & 2	2 & 3	1 & 2	Open
80487SX	Closed	2 & 3	1 & 2	1 & 2	Open
CX486M7 1x	Closed	2 & 3	2 & 3	1 & 2	Closed
CX486M7 2x	Closed	2 & 3	2 & 3	1 & 2	Closed
AM486DXL	Closed	2 & 3	1 & 2	1 & 2	Closed
80486DX	Closed	2 & 3	1 & 2	1 & 2	Open
SL80486DX	Closed	2 & 3	2 & 3	1 & 2	Open
80486DX2	Closed	2 & 3	1 & 2	1 & 2	Open
SL80486DX2	Closed	2 & 3	2 & 3	1 & 2	Open
P24T	Closed	2 & 3	1 & 2	1 & 2	Closed
Note: Pins designated should be in the closed position.					

CPU SMI CONFIGURATION	
Type	JG12
Cyrix	pins 5 & 6 closed
Texas Instruments	pins 1 & 2, 5 & 6 closed
AMD	pins 3 & 4 closed
Intel S-series	pins 1 & 2 closed
Intel	Open

CPU SPEED CONFIGURATION				
Speed	JG13	JP7	JP15	JP32
25MHz	1 & 2, 5 & 6	1 & 2	2 & 3	2 & 3
33MHz	1 & 2, 3 & 4	1 & 2	2 & 3	2 & 3
40MHz	3 & 4, 5 & 6	2 & 3	1 & 2	1 & 2
50iMHz	1 & 2, 5 & 6	1 & 2	2 & 3	2 & 3
50MHz	1 & 2, 5 & 6	2 & 3	1 & 2	1 & 2
66iMHz	1 & 2, 3 & 4	1 & 2	2 & 3	2 & 3
Note: Pins designated should be in the closed position.				

BUS SPEED CONFIGURATION		
CPU speed	JP28	JP29
<= 33MHz	pins 1 & 2 closed	pins 1 & 2 closed
> 33MHz	pins 2 & 3 closed	pins 2 & 3 closed