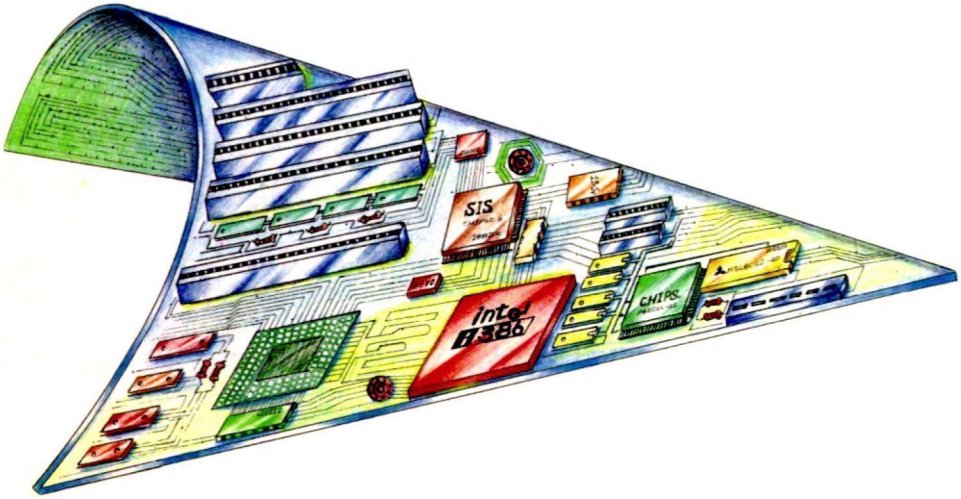
325S/333S/333SC/340SC



U S E R ' S ▪ H A N D B O O K

325S/333S/333SC/340SC
V04 1991 SEP.

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PREFACE

We, the manufacturers, would like to congratulate you on, what we think was a very wise decision to purchase the 325S/333S/333SC/340SC main board.

No matter what walk of life, the 325S/333S/333SC/340SC will perform beyond the call of duty giving you not only value for money but performance second to none.

We hope that this manual will provide all the information that you will need to operate your PC/AT. However, should you require any further information, please contact your dealer who will be pleased to assist you.

TABLE OF CONTENTS

1 INTRODUCTION

325S/333S/333SC/340SC is a high-performance AT-compatible system board that provides incredible speed of processing while maintaining full compatibility with the IBM* PC /AT*. The system board is designed to be mounted in a standard PC / XT*, Baby AT, or PC/AT-type enclosure and uses industry-standard power supply inputs, connectors, expansion board sockets, and so forth. In other words, you can design a new system or upgrade your existing system with no modifications to existing or available components.

The following sections will provide a quick and precise information for the end user to understand and properly use the 325S/333S/333SC/340SC motherboard.

1-1 SPECIFICATIONS

CPU	: Intel80386DX-25 for 325S AMD or Intel80386DX-33 for 333S/333SC AMD80386DX-40 for 340SC
CPU CLOCK	: Programmable CPU clock which has options divided by 2, by 3, and by 4 (BIOS setup)

COPROCESSORS: Socket for Weitek 3167 or Intel 80387DX

MEMORY : Up to 16MB on boar with fast paging mode for 333SC/340SC. Up to 8MB on board with fast paging mode for 325S or 333S

CACHE SIZE : 128 byte for 325S/333S, 128 byte or 64K byte for 333SC/340SC

BIOS : AMI (single 64K EPROM configuration)

I/O SLOTS : 16-bit x 6, 8-bit x 2

JUMPER ON BOARD :

. H/W reset (J14)
. Power LED & keylock(J10)
. Speaker (J13)
. External battery (J1)
. Turbo LED (J11)
. H/W speed selector (J12)
. Mono/color selector (J3)

LANDMARK SPEED (V0.99):

43.5MH (325S), 58.7MHz (333S), 58.7MHz (333SC),

LANDMARK SPEED (V1.14):

65.4MHz (340SC)

POWER METER (V1.2) :

4.047MIPS (325S),
5.368MIPS (333S)
7.842MIPS (333SC)
9.483MIPS (340SC)

NORTON SI (V 4.0) :

30.5 (325S), 39.7 (333S)
40.3 (333SC), 48.5 (340SC)

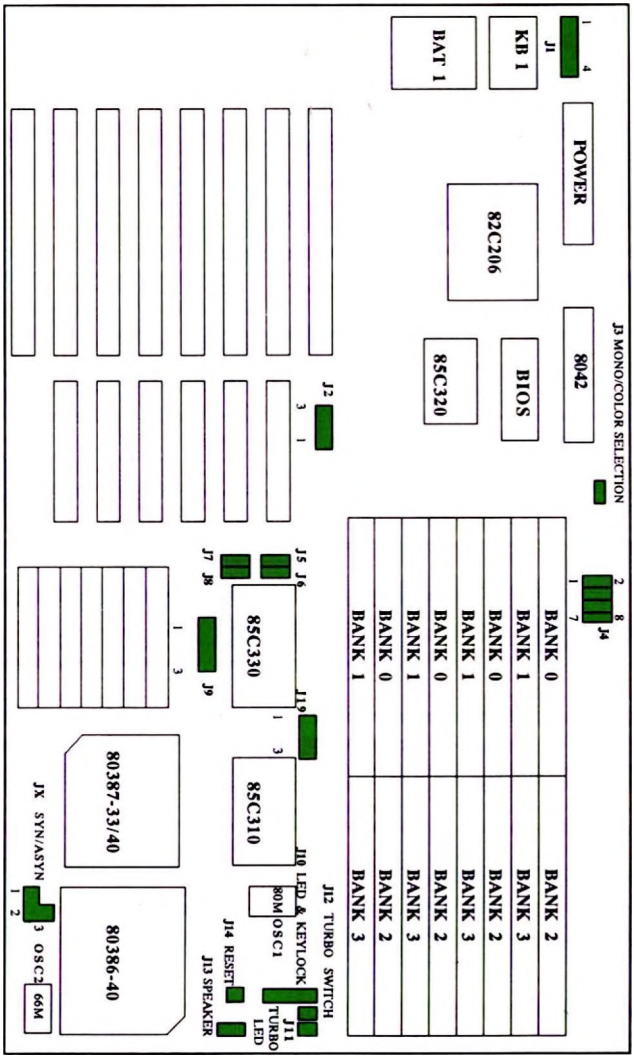
SHADOW RAM : System BIOS , video BIOS, and adapter BIOS

SHADOW CACHE: System BIOS, video BIOS, and adapter BIOS
SIZE : 33cm x 21.7cm

1-2 FEATURES

- 100% IBM* PC/AT* compatible
- Supports EMS version 4.0
- Programmable CPU clock for high/low speed change
- Programmable shadow RAM & shadow cache and optional shadow block size
- Flexible cache size cache controller with different line size for cache update
- Add wait states to DRAM read/write access by BIOS setting
- Rechargeable battery and external battery connector
- Network : NOVELL (3.01)
- OS : MS-DOS (3.3, 4.01) or MS-OS/2 (1.20), SCO XENIX (R 2.3.1) SCO UNIX (R 3.2.1)
- Software Appications :
  - Window (3.0)
  - Auto-CAD (R10)
  - PC-tools (5.5)
  - Lotus-123 (R3.0)
  - WordPerfect(5.0)
  - Telix (3.10)
  - dBASE III PLUS
  - Procomm (V2.4.2)
  - ET(2.0),
  - PEII...etc.

1-3 BOARD LAYOUT FOR 325S/ 333S/333SC /340SC



1-4 JUMPER SETTING FOR 325S/ 333S/333SC/ 340SC

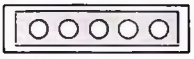
[J3] Mono/color selection

 Open: mono  Short: color

[J11] Turbo LED

+

[J10] PowerLED & keylock



5 1

1. LED output
2. No connect
3. GND
4. Keylock
5. GND

[J13] Speaker jumper

4 1

1. Speaker out
2. GND
3. GND
4. +5VDC

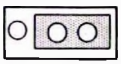
[J1] External battery jumper

1

1. +VDD (External battery power input)
2. 3.6V (Battery)
3. +VDD (Internal battery power input)
4. GND

1 & 4 are connectors for external battery
2 & 3 short : internal battery used
2 & 3 open : discharge XCMOS setup

[J19] default condition



1

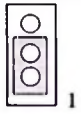
[J12] Turbo switch

open : low speed or

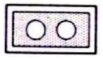
short : high speed

[CTRL][ALT][+] high speed
[CTRL][ALT][-] low speed

[J2] default condition

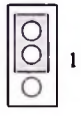


[J14] Reset switch

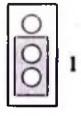


1. GND
2. Power good

[J9] Cache size selection
(for 333SC/340SC only)



1-2 short : 32KB cache



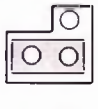
2-3 short : 64KB cache

[J5,J6,J7,J8] All short : For model 333S/325S
All open : For model 333SC/340SC

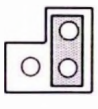
[J4] 8042 Speed control pin selection

8042 pin	J4 short header	
23	5-6	
24	7-8	
29	1-2	default :
30	3-4	header 5-6 short

[JX] Coprocessor SYNC/ASYNC selection (for model 340SC only)



1-2 SYNC: Use a 40MHz coprocessor



2-3 ASYNC: Use a 33MHz coprocessor

2 CONFIGURATION

This chapter briefly describes the major features of the 325S/333S/333SC/340SC system board. It covers the following topics.

. Microprocessor
. Math Coprocessor
. Main Memory
. Cache Memory
. The SIS 85C310/SIS 85C320/SIS 85C330 Chip Set
. Shadow RAM & Memory Remapping
. DMA controller
. Interrupt Controller
. Timer
. Real-Time Clock and Nonvolatile RAM
. Keyboard Controller
. I/O Port Address MAP
. I/O Channel Pin Assignments
. I/O Channel Signal Description

2-1 MICROPROCESSOR

The 325S/333S/333SC/340SC motherboa uses an AMD or Intel 80386DX microprocessor to run at 25MHz, 33MHz, or 40MHz. The 80386DX is an advanced 32-bit microprocessor designed for ap-

plications needing very high performance and optimized for multi-tasking operating systems. The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes of virtual memory. The integrated memory management and protection architecture includes address translation registers, advanced multitasking hardware and a protection mechanism to support operating systems. In addition, the 80386DX allows the simultaneous running of multiple operating systems. Instruction pipelining, on chip address translation, and high bus bandwidth ensure short average instruction execution times and high system throughput.

2-2 MATH COPROCESSOR

The system's numeric processing power may be enhanced by adding an optional 80387 DX or Weitek 3167 coprocessor into a PGA(pin grid array) socket located beside the 80386 CPU.

NOTE:
Before inserting a coprocessor in the socket please make sure the system power is turned off and coprocessor pin 1 is in right position; otherwise, the system board will be damaged. Moreover, the math coprocessor's clock speed should match your CPU's speed.

2-3 MAIN MEMORY

The following table lists the possible memory configurations.

DRAM TYPE	On Board SIM Module				Total
CFG	Bank0	Bank1	Bank2	Bank3	Memory
1	0	0	0	0	0
2	256Kx4	0	0	0	1M
3	256Kx4	256Kx4	0	0	2M
4	1Mx4	0	0	0	4M
5	256Kx4	1Mx4	0	0	5M
6	1Mx4	1Mx4	0	0	8M
7	1Mx4	1MX4	1MX4	0	12M
8	1MX4	1MX4	1MX4	1MX4	16M

Please use 256KB/1MB RAM modules with 70ns or 80ns propagation delay time. Please do not use NMBS DRAMS. Memory banks are as follows:

BANK0	BANK2
BANK1	BANK3
BANK0	BANK2
BANK1	BANK3
BANK0	BANK2
BANK1	BANK3
BANK0	BANK2
BANK1	BANK3

2-4 CACHE MEMORY

If you select the model 325S/333S, we support 128 bytes of internal cache RAM in a SIS 85C310 chip. It provides higher performance than a pure non-cache system. If you select model 333SC/340SC, in addition to the 128 bytes of internal cache RAM, another 64K bytes cache RAM will be supported.

2-5 THE SIS 85C310 / 85C320 / 85C330 CHIP SET

The SIS 386 chipset from SIS allows the programming of many system board functions. The set comprises two VLSI (Very Large Scale Integration) chips that enable the CPU and AT bus clock rates to be programmed as well as the memory and I/O wait states. The Shadow RAM capability can be set. The Chipset consists of the

SIS85C310	Cache/Memory Controller
SIS85C320	Bus Controller
SIS85C330	Data Buffer
82C206	Integrated Peripherals Controller

2-6 SHADOW RAM & MEMORY REMAPPING

The SIS 85C310 has built-in support for shadowing different areas of memory (which include system BIOS and video BIOS.)

The SIS 85C310 supports shadow RAM in one of the following four options:

Option	BIOS	BIOS Address	Video	Video Address
1	64K	0F0000-0FFFFF	0	
2	128K	0E0000-0FFFFF	0	
3	64K	0F0000-0FFFFF	64K	0C0000-0CFFFF
4	128K	0E0000-0FFFFF	128K	0C0000-0DFFFF

All shadow memory has to be initialized by enabling a write to the specified shadow area. After initialization, the shadowed area becomes read-only. Reads to these areas are considered main memory accesses and, therefore, are cacheable. A write to this area is considered an off board memory cycle (AT cycle) and ATCYC* will be active.

The rest of the 384K shadow area can be remapped to extended memory (from 1MB to 16MB) automatically. The remapping area is arranged as follows:

Condition (1)

Shadow RAM Disable	Remapping Memory Size
1M DRAM used	384K
2M DRAM used	384K
4M DRAM used	256K
Over 4M DRAM used	0

Condition (2)

Shadow RAM Enable	Remapping Memory Size
64K (ROM Space)	256K
128K (ROM Space)	256K
64K + 64K (I/O Bus + ROM)	256K
128K + 128K (I/O Bus + ROM)	0

2-7 DMA CONTROLLER

The equivalents of two 8237A DMA Controllers are implemented in the 82C206. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high speed information transfer with less CPU intervention.

The two DMA Controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1), and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

DMA Channel 0 : spare
DMA Channel 1 : IBM SDLC
DMA Channel 2 : Diskette adapter
DMA Channel 3 : spare
DMA Channel 4 : cascade for DMA controller 1
DMA Channel 5 : spare
DMA Channel 6 : spare
DMA Channel 7 : spare

2-8 INTERRUPT CONTROLLER

The equivalents of two 8259 Programmable Interrupt Controllers (PICs) are included in the 82C206. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide a vector which is used as an acceptance index by the CPU to determine which interrupt service routine to execute.

Interrupt Level	Description
NMI	Parity check error
IRQ0	System timer interrupt from timer 8254-2
IRQ1	Keyboard output buffer full
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	Paralled printer port 2
IRQ6	Floppy disk adapter
IRQ7	Paralled printer port 1
IRQ8	Clock/Calendar
IRQ9	Rerounting to INT 10 from hardware IRQ2
IRQ10	Spare
IRQ11	Spare
IRQ12	Spare
IRQ13	Math Coprocessor 80387
IRQ14	Hard disk adapter
IRQ15	Spare

2-9 TIMERS

The 82C206 chip can provide three programmable timers, each with the same timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0 (IRQ0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone. Application programs can load different counts into this timer to generate various sound frequencies.

2-10 REAL-TIME CLOCK AND NONVOLATILE RAM

The 82C206chip contains a real-time clock component that maintains data and time information in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 50 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time with an inexpensive battery (one rechargeable battery and one 6Vexternal bat tery connector on the main board).

Adrs	Description	Adrs	Description
00	Seconds	10	Diskette drive type byte-drives A and B
01	Second alarm	11	Reserved
02	Minutes	12	Mixed disk type byte-drives C and D
03	Minute alarm	13	Reserved
04	Hours	14	Equipment byte
05	Hour alarm	15	Low-base memory
06	Day of week	16	High-base memory
07	Data of Month	17	Low-expansion memory
08	Month	18	High-expansion memory byte
09	Year		
0A	Status Register A	19-2D	Reserved

(Continual)

Adrs	Description	Adrs	Description
0B	Status Register B	2E-2F	2-byte CMOS check sum
0C	Status Register C	30	Low-expansion memory byte
0D	Status Register D	31	High-expansion memory byte
0E	Diagnostic status	32	Data century byte
0F	Shutdown	33	Information flags (set during power on)
		34-3F	Reserved

2-11 KEYBOARD CONTROLLER

The keyboard controller is a single-chip 8742 or 8042 microprocessor programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data is sent to the keyboard by first polling the controller's status register to determine when the input buffer is ready to accept data and then writing to the input buffer.

Each byte of data is sent to the keyboard serially with an odd parity bit automatically inserted. The keyboard is required to acknowledge all data transmissions; another byte of data should not be sent to the keyboard until acknowledgment is received for the previous byte sent. The "output buffer full" interrupt may be used for both send and receive routines.

2-12 I/O PORT ADDRESS MAP

Hex Range	Devices	Usage
000-01F	DMA controller 1, 8237A-5	System
020-03F	Interrupt controller 1, 8259A	System
040-05F	Timer, 8254-2	System
060-06F	Keyboard I/O	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register, 74LS612	System
0A0-0BF	Interrupt controller 2, 8259A	System
0C0-0DF	DMA controller 2, 8237A-5	System
0F0	Clear Math Coprocessor Busy	System
0F1	Reset Math Coprocessor	System
0F8-0FF	Math Coprocessor	System

Hex Range	Devices	Usage
1F0 - 1F8	Fixed Disk	I/O
200 - 207	Game I/O	I/O
278 - 27F	Parallel printer port 2	I/O
2F8 - 2FF	Serial port 2	I/O
300 - 31F	Prototype card	I/O
360 - 36F	Reserved	I/O
378 - 37F	Parallel printer port 1	I/O
380 - 38F	SDLC, bisynchronous 2	I/O
3A0 - 3AF	Bisynchronous 1	I/O
3B0 - 3BF	Monochrome display printer adapter	I/O
3C0 - 3CF	Reserved	I/O
3D0 - 3DF	Color/Graphic monitor adapter	I/O
3F0 - 3F7	Floppy diskette controller	I/O
3F8 - 3FF	Serial port 1	I/O

2-13 I/O CHANNEL PIN ASSIGNMENTS

Pin-Out Specifications for 8-Bit Expansion Slots

Signals	I/O	Pin No.		Signals	I/O
Ground		B1	A1	-I/O CH CK	[I]
Reset Drive	[O]	B2	A2	SD7	[I/O]
+5V DC		B3	A3	SD6	[I/O]
IRQ9	[I]	B4	A4	SD5	[I/O]
-5V DC		B5	A5	SD4	[I/0]
DRQ2	[I]	B6	A6	SD3	[I/O]
-12V DC		B7	A7	SD2	[I/O]
0WS	[I]	B8	A8	SD1	[I/O]
+12V DC		B9	A9	SD0	[I/O]
Ground		B10	A10	-I/O CH DRY	[I]
-SMEMW	[O]	B11	A11	AEN	[O]
-SMEMR	[O]	B12	A12	SA19	[I/O]
-IOW	[I/O]	B13	A13	SA18	I/O]
-IOR	[I/O]	B14	A14	SA17	[I/O]
-DACK3	[O]	B15	A15	SA16	[I/O]
DRQ3	[I]	B16	A16	SA15	[I/O]
-DACK1	[O]	B17	A17	SA14	[I/O]
DRQ1	[I]	B18	A18	SA13	[I/O]
-Refresh	[I/O]	B19	A19	SA12	[I/O]
CLK	[O]	B20	A20	SA11	[I/O]
IRQ7	[I]	B21	A21	SA10	[I/O]
IRQ6	[I]	B22	A22	SA9	[I/O]
IRQ5	[I]	B23	A23	SA8	[I/O]
IRQ4	[I]	B24	A24	SA7	[I/O]
IRQ3	[I]	B25	A25	SA6	[I/O]
-DACK2	[O]	B26	A26	SA5	[I/O]
T/C	[O]	B27	A27	SA4	[I/O]
BALE	[O]	B28	A28	SA3	[I/O]

Pin-Out Specifications for 16-Bit Expansion Slots

Signals	I/O	Pin No.		Signals	[I/O]
+5VDC		B29	A29	SA2	[I/O]
OSC	[O]	B30	A30	SA1	[I/O]
Ground		B31	A31	SA0	[I/O]
-MEM CS16	[I]	D1	C1	SBHE	[I/O]
-I/O CS16	[I]	D2	C2	LA23	[I/O]
IRQ10	[I]	D3	C3	LA22	[I/O]
IRQ11	[I]	D4	C4	LA21	[I/O]
IRQ12	[I]	D5	C5	LA20	[I/O]
IRQ15	[I]	D6	C6	LA19	[I/O]
IRQ14	[I]	D7	C7	LA18	[I/O]
-DACK0	[O]	D8	C8	LA17	[I/O]
DRQ0	[I]	D9	C9	-MEMR	[I/O]
-DACK5	[O]	D10	C10	-MEMW	[I/O]
DRQ5	[I]	D11	C11	SD8	[I/O]
-DACK6	[O]	D12	C12	SD9	[I/O]
DRQ6	[I]	D13	C13	SD10	[I/O]
-DACK7	[O]	D14	C14	SD11	[I/O]
DRQ7	[I]	D15	C15	SD12	[I/O]
+5VDC		D16	C16	SD13	[I/O]
-Master	[I]	D17	C17	SD14	[I/O]
Ground		D18	C18	SD15	[I/O]

2-14 I/O CHANNEL SIGNAL DESCRIPTION

All signal lines are TTL-compatible with a maximun loading of two Low-Power Shockty [LS] devices.

CLK [Output]
The CLK signals of the I/O slot are synchronous to those of CPU CLK.

RESET DRV [Output]
This signal goes high during power-up, low line-voltage, or hardware reset.

SA0-19 [Input/output]
The System Address Lines run from bit 0 to 19. They are latched on to the falling edge of "BALE".

LA17-23 [Input/Output]
The Unlatched Address Lines run from bit 17 to 23.

SD0-15 [Input/Output]
System data bits 0 to 15.

BALE [Output]
The Buffered Address Latch Enable is used to latch SA0-SA19 on to the falling edge. This signal is forced high during DMA cycles.

I/O CHCK [Input]
The I/O Channel Check is an active low signal which indicates that a parity error exists on the I/O board.

I/O CH RDY [Input]
This signal lengthens the I/O or memory read/write cycle and should be held low with a valid address. It can only be held low for a maximum of 2.5 microseconds.

IRQ3-7, 9-12, 14-15 [Input]
The interrupt Request signals indicate I/O service request attention. They are prioritized in the following sequence: HIGHEST IRQ9, 10, 11, 12, 14, 15, 3,

4, 5, 6, 7 Lowest.

-I/OR [Input/Output]
The I/O read Signal is an active low signal which instructs the I/O device to drive its data onto the data bus.

-I/OW [Input/Output]
The I/O write is an active low signal which instructs the I/O device to read data from the data bus.

-SMEMR [Output]
The system Memory Read is low while the low 1 mega byte of memory is being used.

-MEMR [Input/Output]
The Memory Read Signal is low while any memory location is being read.

-SMEMW [Output]
The System Memory Write is low while the low 1 mega byte of memory is being written.

-MEMW [Input/Output]
Memory Write is low while any memory location is being written.

DRQ Request channels 0 to 3 are for 8-bit data transfer.

DMA Request channels 5 to 7 are for 16-bit data transfer.

DMA Request channel 4 is used internally on the

system board.

A DMA Request should be held high until the corresponding DMA.

Their priority is in the following sequence: Highest DRQ0,1,2,3,5,6,7 Lowest.

-DACK 0-3, 5-7 [Output]
The DMA Acknowledge 0 to 3, 5 to 7 are the corre sponding acknowledge signals for DRQ 0 TO 3, 5-7.

AEN [Output]
The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the 80286 CPU is driving the address bus.

- REFRESH [Input/Output]
This signal is used to indicate a memory refresh cycle and can be driven by a microprocessor on the I/O channel.

T/C [Output]
Terminal Count provides a pulse when the terminal-count for any DMA channel is reached.

SBHE [Input/Output]
The System Bus HIGH Enable indicates the high bytes SD8-SD15 on the data bus.

-MASTER [Input]
The Master is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh.

-MEM CS16 [Input, Open collector]
The memory chip Select 16 indicates that the present data transfer is a 1-Wait State 16-bit data memory operation.

-I/O CS16 [Input, Open collector]
The I/O Chip Select indicates the present data transfer is a 1-Wait State 16-bit data I/O operation.

OSC [Output]
The Oscillator is a 14.31818 MHz signal used for the color graphic board.

0WS [Input, Open collector]
The 0-Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting an additional wait state.

3 INSTALLATION

This chapter provides the information for you to set up a working system based on the 325S/333S/333SC/340SC mainboard. Before removing the board from its anti-static bag read the section below about static electricity precautions.

3-1 STATIC PRECAUTIONS

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on the system board. It is therefore important to observe basic precautions whenever you are going to handle or use computer components. Although areas with a humid climate are much less prone to static build-up, it is best to always safeguard against accidental damage that may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

. Touch a grounded metal object to discharge the static electricity in your body (or, preferably, wear a grounded wrist strap).

. When unpacking and handling the board and other system components, all materials should be placed on a anti-static surface.

When handling individual cards or boards or modules, be careful to avoid contact with the components on them and also with the "golden finger" connectors that plug into the expansion bus.

3-2 PERIPHERALS REQUIRED

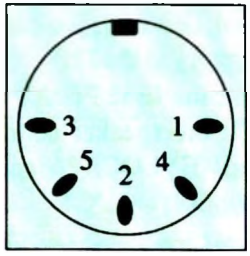
. The 325S, 333S, 333SC, or 340SC mainboard.
. An IBM-AT power supply or compatible; we recommend that you use at least a 180 watt power supply for the system.
. An IBM-AT keyboard or compatible.
. An IBM-AT fixed disk/floppy disk controller or compatible.
. At least one floppy disk drive [360K, 720K, 1.2M, 1.44M..]
. An IBM-AT display card: CGA,MDA,EGA,VGA or compatible.
. A monitor that corresponds to the display card.
. MS-DOS version 3.10 or later, PC-DOS version 3.10 or later,or OS/2.

3-3 BUILDING UP A SYSTEM

1) Install the SIMM DRAM card on the mainboard.
2) Put the mainboard into computer case and secure it.
3) Plug in the keyboard connector to the keyboard at the back of the system unit as in Figure 3-1.
4) Install an MDA, CGA, EGA, VGA, display card in the I/O slot.
5) Select monochrome or color on switch J3 to match the card installed in step (4).
6) Connect the monitor cable to the display card.
7) Connect the power supply connectors to the

Power Connector as show in Figure 3-2.

8) The 325S, 333S, 333SC or 340SC has a rechargeable battery on board; however, you can plug in an external backup battery to the J1.
9) For those who have the IBM PC/AT chassis or equivalent, plug in the speaker connector and the "Power LED and KEYLOCK" connector at the front of the system unit.
10) Turn on the monitor.
11) Turn on the power supply.



Pin	Description
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	SPARE
4	GROUND
5	+5VDC

Figure 3-1 Keyboard Connector

1	POWER GOOD	Orange
2	+5V	Red
3	+12V	Yellow
4	- 12V	Blue
5	GROUND	Black
6	GROUND	Black
1	GROUND	Black
2	GROUND	Black
3	- 5V	White
4	+5V	Red
5	+5V	Red
6	+5V	Red

Figure 3-2 Power Supply Connector

4 POWER-ON SELF TEST

The Power-On Self Test (POST) is a diagnostic test that resides in the ROM-BIOS and runs automatically whenever you turn on or reset your system. The POST checks the processor, the memory, and the peripheral devices connected to the computer (Keyboard, monitor, disk drives, and others).

4-1 ERROR MESSAGES FROM SPEAKER OR DISPLAY

AMI-BIOS performs various diagnostic tests at the time the system is powered up. Whenever an error is encountered during these tests, there will be either a few short beeps or an error message displayed on the monitor. If the error occurs before the display device is initialized the system reports the error with several short beeps.

If the error is FATAL the system halts after reporting the FATAL error. If the error is NON-FATAL the process continues after reporting the error.

4-2 ERROR MESSAGES FROM SPEAKER

Fatal Errors Through Beeps

These errors are conveyed through a number of beeps in an infinite process,but there is enough time between two subsequent sets of error beeps to tell the number in each set.

Beep Count	Meaning
1	DRAM refresh failure
3	Base 64-Kbyte RAM failure
4	System Timer Failure
5	Processor Failure
6	Keyboard Controller-Gate A20 error
7	Virtual Mode Exception Error
9	ROM-BIOS CheckSum Failure

Non-Fatal Errors Through Beeps

These errors are conveyed as one long beep followed by several short beeps.

Beep Count	Meaning
3	Conventional and Extended test failure
8	Display test and vertical and horizontal retrace test failure

4-3 ERROR MESSAGE FROM DISPLAY

Fatal Errors shown in Display

When these errors are displayed the screen is cleared, and the error message display is followed by a line saying "SYSTEM HALTED".

CMOS INOPERATIONAL indicates failure of the CMOS shutdown register test

8042 GATE-A20 ERROR , an error in getting into protected mode

INVALID SWITCH MEMORY FAILURE

DMA ERROR, DMA controller page register test failure.

DMA #1 ERROR, DMA Unit 1 register test failed.

DMA #2 ERROR, DMA Unit 2 register test failed.

Non-Fatal Errors shown in Display

There are two types of errors in this category:

1. Ones that wait for the F1 key to be pressed and give the option to run SETUP.
2. Ones that wait for the F1 key to be pressed and don't give a SETUP option.

Errors With Setup Option

CMOS battery state low indicates failure of CMOS battery, or a failure in the set and checksum tests.

CMOS system options not set indicates failure of CMOS battery, or failure in set and checksum tests.

CMOS checksum failure indicates CMOS battery low or a failure in set and checksum tests.

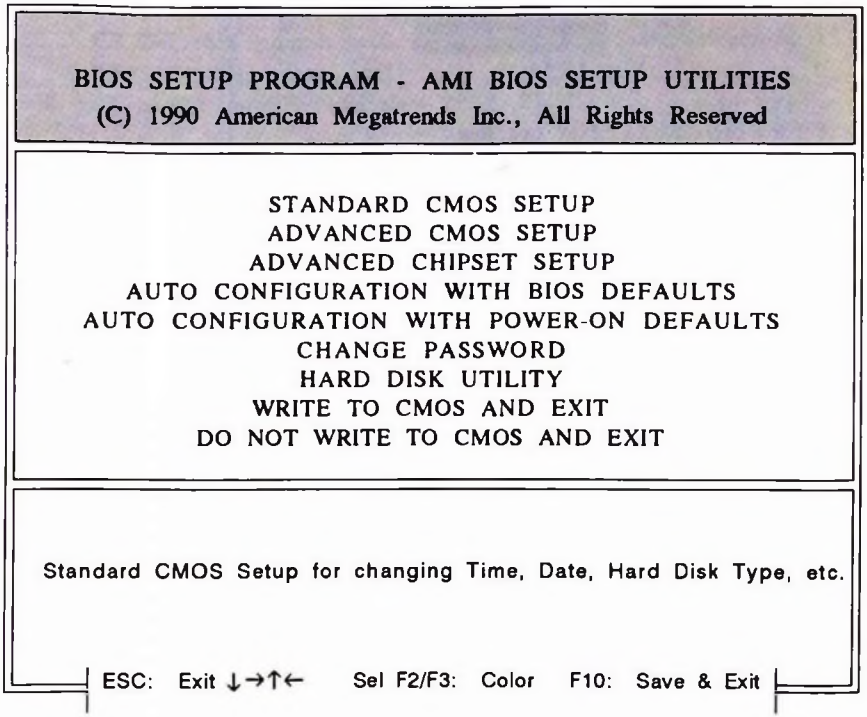
CMOS display type mismatch indicates failure of display verification.
CMOS memory size mismatch indicates a System Configuration and setup failure.
CMOS time & date not set indicates a System Configuration verification error and setup error (in timer).

Errors Without Setup Option

CH-2 timer error indicates channel 2,1,0 timer test failure.
Keyboard error indicates keyboard test failure.
KB/Interface error indicates keyboard test failure.
Display switch setting not proper indicates display type verification error.
Keyboard is locked... Unlock it.
HDD controller error indicates system Configuation verification error in hard disk setup.
C : Drive error indicates hard disk setup error
D : Drive error indicates hard disk setup error
D : Drive failure indicates hard disk failure.

5 AMI BIOS SETUP

AMI BIOS is designed in to the 325S/333S/333SC/340SC motherboard so that users can configure their system easily. After the memory test has been completed, press the <ESC> key and the following diagram will appear in a few seconds.



5-1 STANDARD CMOS SETUP

This is a general setup for the user to configure his system components such as floppy drive, hard disk, display, and memory. Once a field is highlighted there will be online help information shown in the left bottom of the menu. Figure 5-1 is a sample menu for the STANDARD CMOS SETUP.

Figure 5-1 CMOS Setup Screen

BIOS SETUP PROGRAM -STANDARD CMOS SETUP
(C) 1990 American Megatrends Inc.; All Rights Reserved

Date (mn/date/year); Fri, Jan 04 1991
Time (hour/min/sec);18:35:40
Floppy drive A : : 1.2 MB, 5.25"
Floppy drive B : : Not Installed
Hard disk C :type : Not Installed
Hard disk D : type : Not Installed
Primary display : Monochrome
Keyboard : Installed

Base memory size :640 KB
Ext. memory size : 3328KB

Cyln	Head	WPcom	LZone	Sect	Size

Sun	Mon	Tue	Wed	Thu	Fri	Sat
31	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31	1	2	3
4	5	6	7	8	9	10

Month : Jan,Feb,..... Dec
Date : 01,02,03,.....31
Year : 1901,1902,.....2099

ESC:Exit,↓→↑← :Select,PgUp/Pg/Dn=Modify

AMI Hard Disk Types Reference

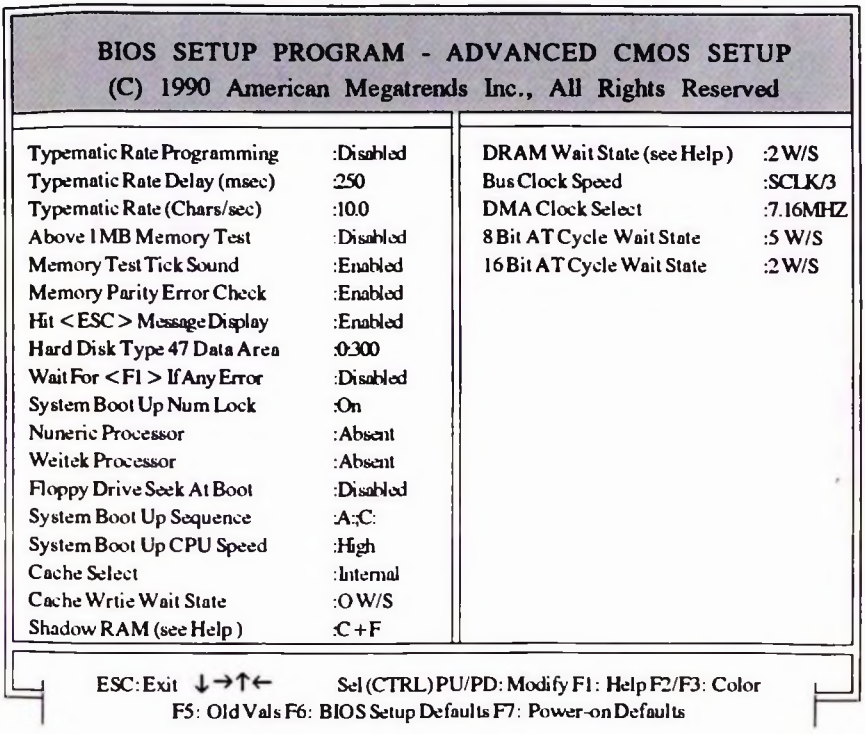
Type	Cylinders	Heads	Write-Precomp	Landing Zone	Capacity (Mbytes)
1	306	4	128	305	10
2	615	4	300	615	20
3	615	6	300	615	31
4	940	8	512	940	62
5	940	6	512	940	47
6	615	4	65535	615	20
7	462	8	256	511	31
8	733	5	65535	733	30
9	900	15	65535	901	112
10	820	3	65535	820	20
11	855	5	65535	855	35
12	855	7	65535	855	50
13	306	8	128	319	20
14	733	7	65535	733	43
15	000	0	000	000	00
16	612	4	0000	663	20
17	977	5	300	977	41
18	977	7	65535	977	57
19	1024	7	512	1023	60
20	733	5	300	732	30
21	733	7	300	732	43
22	733	5	300	733	30
23	306	4	0000	336	10
24	325	7	0000	925	54
25	925	9	65535	925	69
26	754	7	754	754	44
27	754	11	65535	754	69
28	699	7	256	699	41
29	823	10	65535	823	68
30	918	7	818	918	53
31	1024	11	65535	1024	94

Type	Cylinders	Heads	Write-Precomp	Landing Zone	Capacity (Mbytes)
32	1024	15	65535	1024	128
33	1024	5	1024	1024	43
34	612	2	128	612	10
35	1024	9	65535	1024	77
36	1024	8	512	1024	68
37	615	8	128	615	41
38	987	3	987	987	25
39	987	7	987	987	57
40	820	6	820	820	41
41	977	5	977	977	41
42	981	5	981	981	41
43	830	7	512	830	48
44	830	10	65535	830	69
45	917	15	65535	918	114
46	1224	15	65535	1223	152

5-2 ADVANCED CMOS SETUP

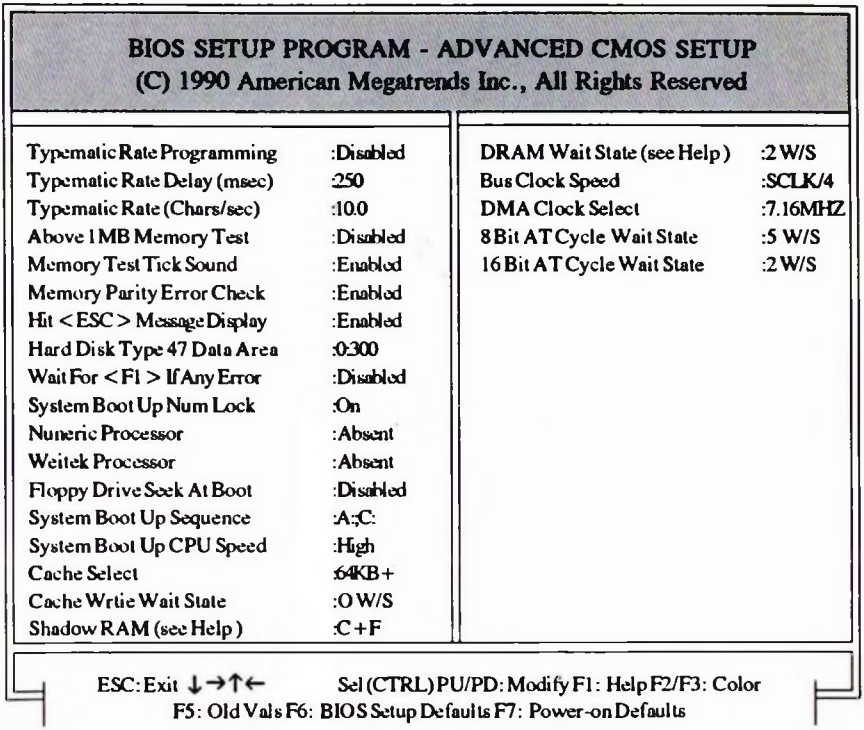
Choose the second option "ADVANCD CMOS SETUP" at the beginning to enter the Advance CMOS Setup Program. Figure 5-2 is a sample menu with the manufacturer's default values for the 325S/333S. Figure 5-3 is a sample menu and with manufacturer's default values for the 333SC/340SC.

Figure 5-2 ADVANCED SETUP SCREEN FOR 325S/333S



Note: Bus Clock Speed: SCLK/3 for 325S
SCLK/4 for 333S

Figure 5-3 ADVANCED SETUP SCREEN FOR 333SC/340SC



Note:DRAM Wait State: 2 W/S for 333SC
3 W/S for 340SC