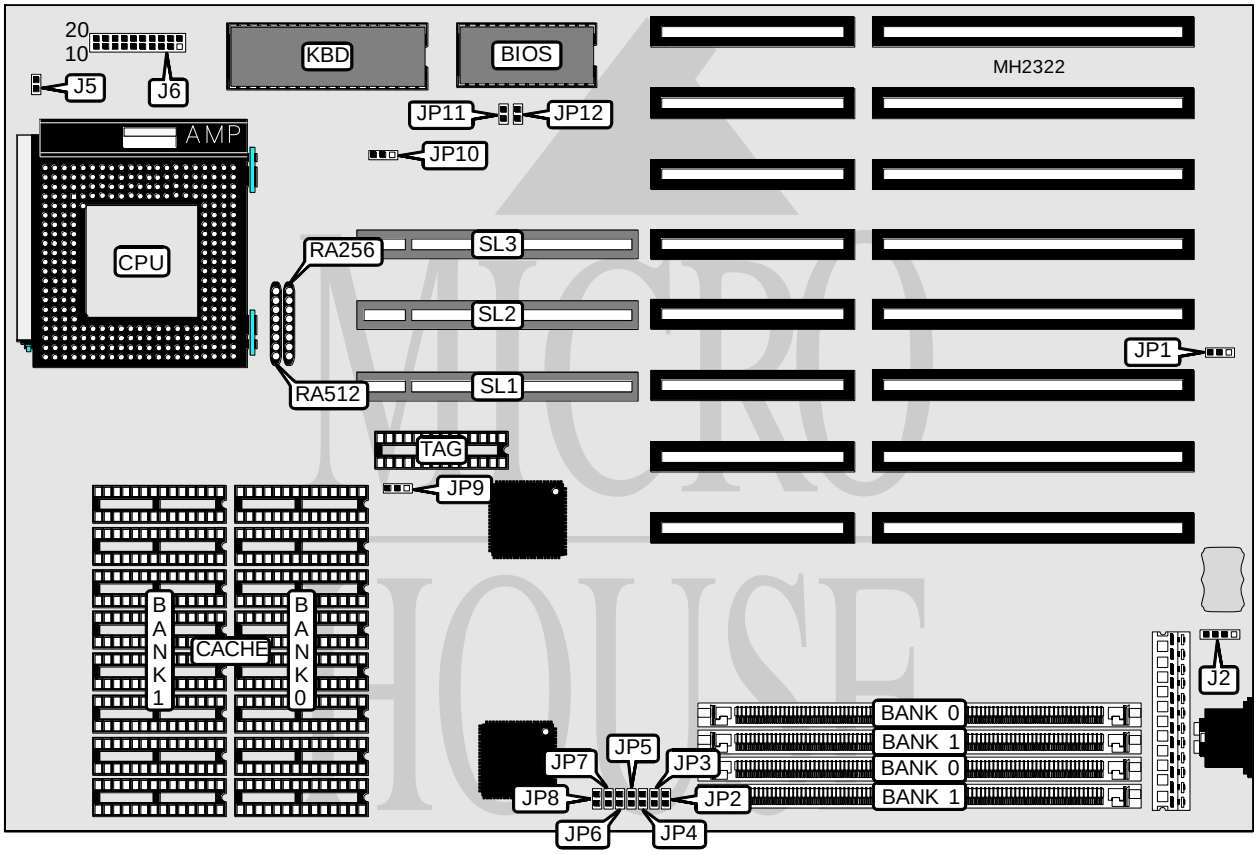
TMC RESEARCH CORPORATION
P A T 5 4 P V (V E R 1 . 0 A , 1 . 1 A)

Processor	Pentium
Processor Speed	75/90/100MHz
Chip Set	OPTI
Max. Onboard DRAM	128MB
Cache	256/512KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit VESA local bus slots (3)
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J2	Reset switch	J6 (pins 9 - 19)
IDE interface LED	J5	IDE interface LED	J6 (pins 10 - 20)
Speaker	J6 (pins 1 - 4)	Power LED & keylock	J6 (pins 11 - 15)
Turbo LED	J6 (pins 8 - 18)	32-bit VESA local bus slots	SL1 - SL3

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Battery type select internal	JP1	pins 2 & 3 closed
Battery type select external	JP1	Open
CMOS memory clear	JP1	pins 1 & 2 closed
í Monitor type select monochrome	JP7	Open
Monitor type select color	JP7	Closed
í Back-to-back I/O delay enabled	JP8	Closed
Back-to-back I/O delay disabled	JP8	Open

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
2MB	(2) 256K x 36	NONE
4MB	(2) 512K x 36	NONE
6MB	(2) 256K x 36	(2) 512K x 36
8MB	(2) 1M x 36	NONE
8MB	(2) 512K x 36	(2) 512K x 36
10MB	(2) 256K x 36	(2) 1M x 36
12MB	(2) 512K x 36	(2) 1M x 36
16MB	(2) 1M x 36	(2) 1M x 36
16MB	(2) 2M x 36	NONE
18MB	(2) 256K x 36	(2) 2M x 36
20MB	(2) 512K x 36	(2) 2M x 36
24MB	(2) 1M x 36	(2) 2M x 36
32MB	(2) 4M x 36	NONE
32MB	(2) 2M x 36	(2) 2M x 36
34MB	(2) 256K x 36	(2) 4M x 36
36MB	(2) 512K x 36	(2) 4M x 36
40MB	(2) 1M x 36	(2) 4M x 36
48MB	(2) 2M x 36	(2) 4M x 36
64MB	(2) 4M x 36	(2) 4M x 36
64MB	(2) 8M x 36	NONE
66MB	(2) 256K x 36	(2) 8M x 36
68MB	(2) 512K x 36	(2) 8M x 36
72MB	(2) 1M x 36	(2) 8M x 36
80MB	(2) 2M x 36	(2) 8M x 36
96MB	(2) 4M x 36	(2) 8M x 36
128MB	(2) 8M x 36	(2) 8M x 36

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
256KB	(8) 32K x 8	NONE	(1) 32K x 8
512KB	(8) 32K x 8	(8) 32K x 8	(1) 32K x 8

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CACHE JUMPER CONFIGURATION		
Size	RA256	RA512
256KB	Installed	Not installed
512KB	Not installed	Installed

CPU SPEED CONFIGURATION	
Speed	JP18
75MHz	pins 1 & 2 closed
90MHz	pins 3 & 4 closed
100MHz	pins 1 & 2, 5 & 6 closed
Note: The location of JP18 is unidentified.	

VESA CLOCK SPEED CONFIGURATION						
CPU Type	JP4	JP6	JP9	JP10	JP11	JP12
33MHz	Open	Open	1 & 2	2 & 3	Open	Closed
40MHz	Closed	Closed	1 & 2	1 & 2	Closed	Closed
50MHz	Closed	Closed	2 & 3	1 & 2	Closed	Open
Note: Pins designated should be in the closed position.						

BUS CLOCK FREQUENCY CONFIGURATION			
ATCLK frequency	VLCLK frequency	JP2	JP3
8MHz	33MHz	Closed	Open
8MHz	40MHz	Closed	Closed
10MHz	50MHz	Closed	Closed

VESA WAIT STATE CONFIGURATION	
Wait states	JP5
0 wait states	Open
1 wait state	Closed

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