CHAINTECH COMPUTER COMPANY, LTD. 486SCSL/486SCSI

CX486S/CX486S & CX487S/80486SX/80487SX/AMD486DX/80486DX/ **Processor**

ODP486SX/ 80486DX2

25/33/40/50(internal)/50/66(internal)MHz **Processor Speed**

Chip Set SIS Max. Onboard DRAM 32MB

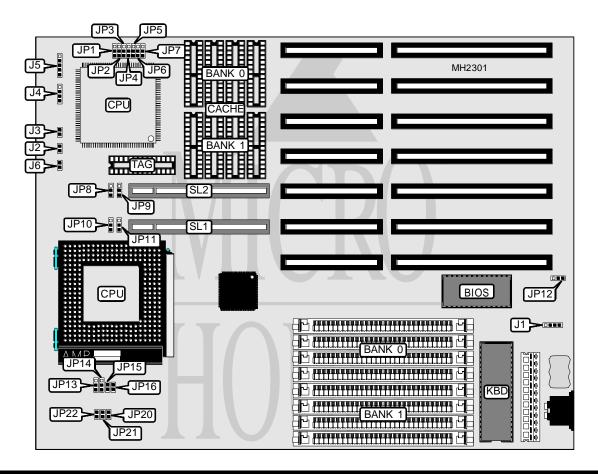
Cache 64/128/256KB

BIOS AMI

Dimensions 265mm x 220mm

I/O Options 32-bit VESA local bus slots (2) (486SCSL only)

NPU Options



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J1	Power LED & keylock	J5
Turbo LED	J2	Reset switch	J6
Turbo switch	J3	32-bit VESA local bus slots	SL1 & SL2
Speaker	J4		

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USER CONFIGURABLE SETTINGS			
Function	Jumper	Position	
í Turbo switch select low	J3	Open	
Turbo switch select high	J3	Closed	
í CMOS memory normal operation	JP12	pins 1 & 2 closed	
CMOS memory clear	JP12	pins 2 & 3 closed	
í PQFP CPU disabled	JP16	Closed	
PQFP CPU enabled	JP16	Open	

	DRAM CONFIGURATION	
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 16K x 8 or (1) 32K x 8

	CACHE JUMPER CONFIGURATION						
Size	JP1	JP2	JP3	JP4	JP5	JP6	JP7
64KB	1 & 2	1 & 2	1 & 2	1 & 2	2 & 3	Open	1 & 2
128KB	2 & 3	1 & 2	2 & 3	1 & 2	1 & 2	1 & 2	2 & 3
256KB	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3
Note: Pins designated should be in the closed position.							

CPU TYPE CONFIGURATION				
Type	JP13	JP14	JP15	
CX486S	Open	pins 2 & 3 closed	Open	
CX486S & CX487S	pins 1 & 2 closed	pins 1 & 2 closed	Closed	
80486SX (PQFP)	Open	pins 2 & 3 closed	Open	
80486SX (PGA)	Open	pins 2 & 3 closed	Open	
ODP486SX	pins 2 & 3 closed	pins 1 & 2 closed	Closed	
80487SX	pins 2 & 3 closed	pins 1 & 2 closed	Closed	
AMD486DX	pins 1 & 2 closed	pins 1 & 2 closed	Closed	
80486DX	pins 1 & 2 closed	pins 1 & 2 closed	Closed	
80486DX2	pins 1 & 2 closed	pins 1 & 2 closed	Closed	

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CPU SPEED CONFIGURATION				
Speed	JP20	JP21	JP22	
25MHz	Closed	Open	Open	
33MHz	Open	Open	Closed	
40MHz	Open	Closed	Closed	
50iMHz	Closed	Open	Open	
50MHz	Open	Closed	Open	
66iMHz	Open	Open	Closed	

VESA WAIT STATE CONFIGURATION (SCSL ONLY)		
Wait states JP9/11		
0 wait states	pins 1 & 2 closed	
1 wait state	pins 2 & 3 closed	

BUS SPEED CONFIGURATION (SCSL ONLY)		
CPU speed JP8/10		
<= 33MHz	pins 1 & 2 closed	
> 33MHz	pins 2 & 3 closed	