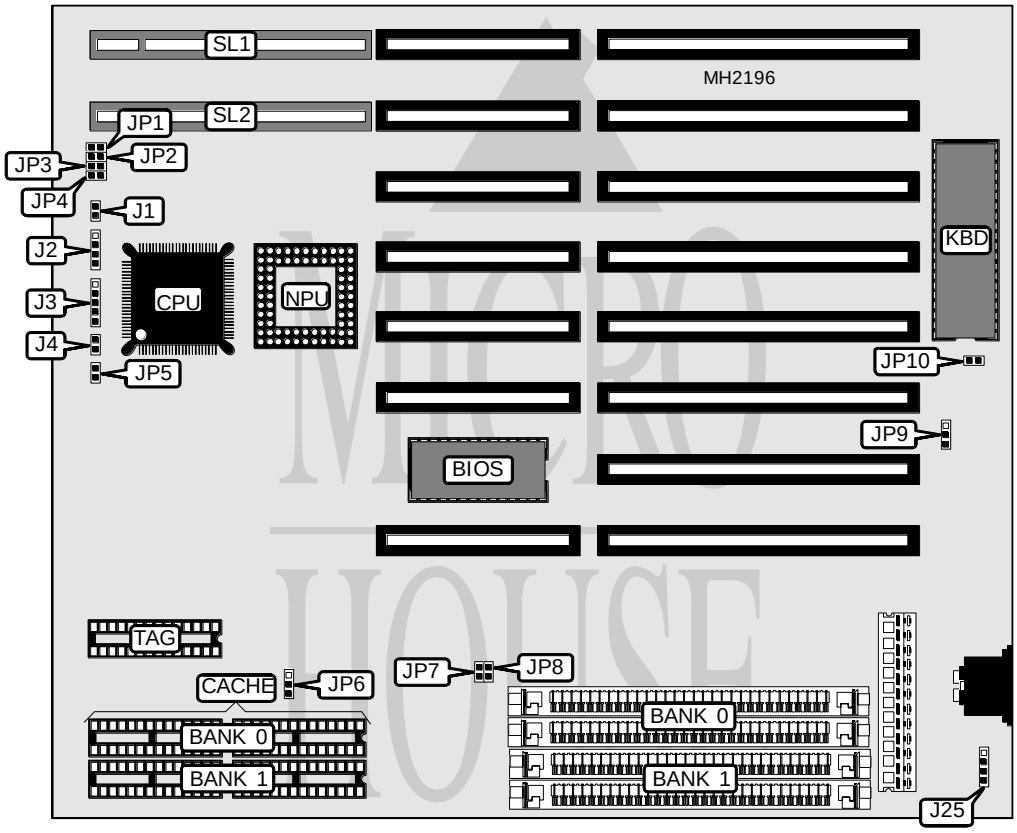
IBM CORPORATION
O P A L 4 8 6 S L C 2 R E V C

Processor	CX486SLC2
Processor Speed	50(internal)/66(internal)MHz
Chip Set	IBM
Max. Onboard DRAM	16MB
Cache	64/128KB
BIOS	AMI/MR
Dimensions	254mm x 218mm
I/O Options	32-bit VESA local bus slots (2)
NPU Options	80387SX



CONNECTIONS			
Purpose	Location	Purpose	Location
Reset switch	J1	Turbo switch	J4
Speaker	J2	External battery	J25
Power LED & keylock	J3	32-bit VESA local bus slots	SL1 & SL2

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í CMOS memory normal operation	JP9	pins 2 & 3 closed
CMOS memory clear	JP9	pins 1 & 2 closed
í Password enabled(MR BIOS only)	JP10	Closed
Password disabled (MR BIOS only)	JP10	Open

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
512KB	(2) 256K x 9	NONE
1MB	(2) 256K x 9	(2) 256K x 9
2MB	(2) 1M x 9	NONE
4MB	(2) 1M x 9	(2) 1M x 9
8MB	(2) 4M x 9	NONE
10MB	(2) 1M x 9	(2) 4M x 9
16MB	(2) 4M x 9	(2) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
64KB	(2) 32K x 8	NONE	(1) 8K x 8
128KB	(2) 32K x 8	(2) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION	
Size	JP6
64KB	pins 2 & 3 closed
128KB	pins 1 & 2 closed

CPU SPEED CONFIGURATION		
Speed	JP7	JP8
50iMHz	Open	Closed
66iMHz	Closed	Open

BUS SPEED CONFIGURATION	
CPU speed	JP5
<=33MHz	Open
>33MHz	Closed

VESA ID CONFIGURATION				
ID	JP1	JP2	JP3	JP4
ID0	Open	Open	Open	Closed
ID1	Closed	Closed	Open	Closed
ID2	Closed	Open	Closed	Closed
ID3	Open	Closed	Closed	Closed