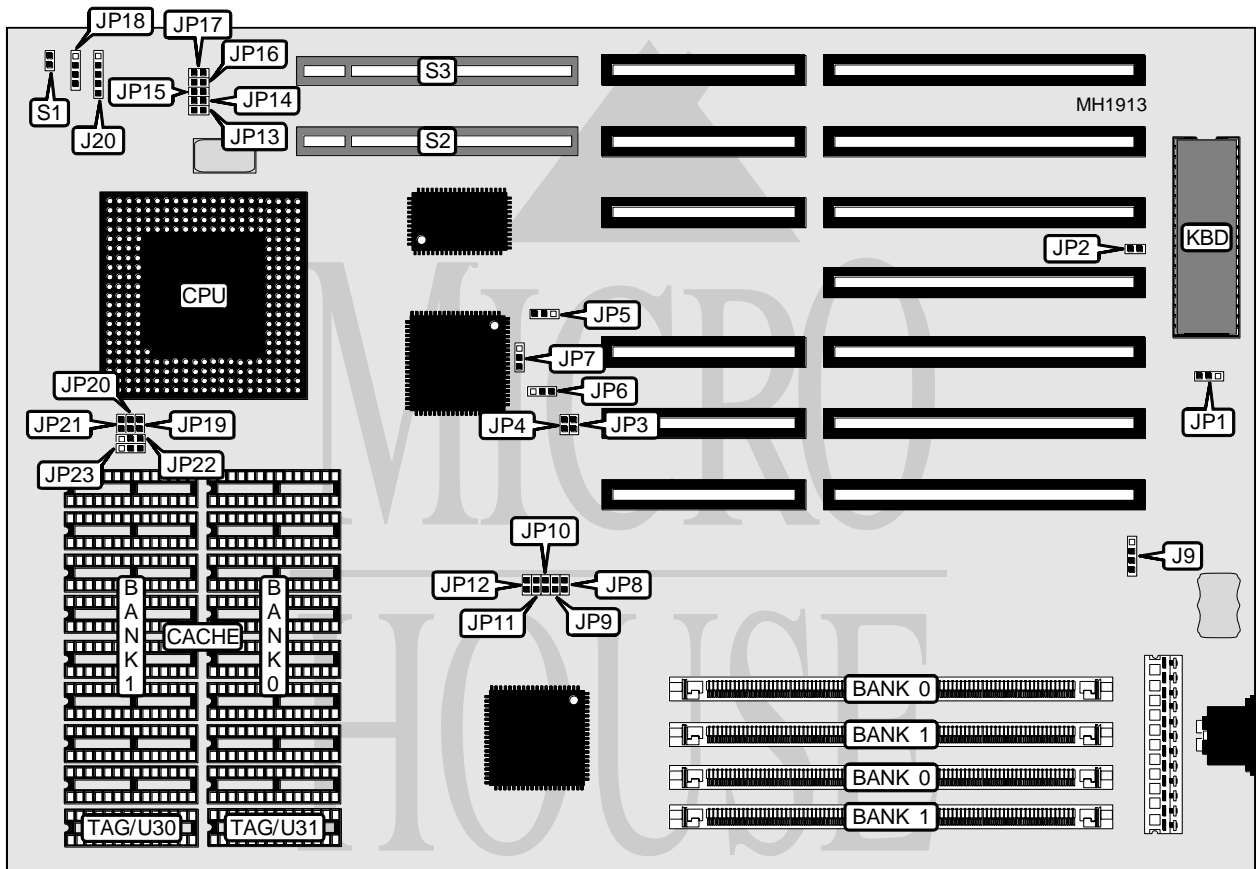


QDI COMPUTER, INC. V5P596P2 PENTIUM VL

Processor	Pentium
Processor Speed	60/66MHz
Chip Set	OPTi
Max. Onboard DRAM	64MB
Cache	64/128/256/512KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit VESA local bus slots (2)
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J9	Reset switch	S1
Power LED & keylock	J20	32-bit VESA Local bus slot	S2
Speaker	JP18	32-bit VESA Local bus slot	S3

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í CMOS memory normal operation	JP1	pins 2 & 3 closed
CMOS memory clear	JP1	pins 1 & 2 closed
í Monitor type select color	JP2	Closed
Monitor type select monochrome	JP2	Open
í Signal goes high at beginning of last T2	JP3	Closed
Signal goes high at end of last T2	JP3	Open
í AT controller back - back I/O delay enabled	JP10	Closed
AT controller back - back I/O delay disabled	JP10	Open
í VL bus power-up signal sample end of 1st T2	JP11	Open
VL bus power-up signal sample end of 2nd T2	JP11	Closed
VESA local bus enabled	JP12	Open
VESA local bus disabled	JP12	Closed
í Factory configured - do not alter	JP13	N/A
í Factory configured - do not alter	JP14	N/A
í Factory configured - do not alter	JP17	Open

DRAM CONFIGURATION		
Size	Bank 0	Bank 3
2MB	(2) 256K x 36	NONE
4MB	(2) 2M x 36	NONE
4MB	(2) 256K x 36	(2) 256K x 36
8MB	(2) 1M x 36	NONE
8MB	(2) 2M x 36	(2) 2M x 36
16MB	(2) 4M x 36	NONE
16MB	(2) 1M x 36	(2) 1M x 36
32MB	(2) 2M x 36	(2) 2M x 36
32MB	(2) 4M x 36	NONE
64MB	(2) 4M x 36	(2) 4M x 36

CACHE CONFIGURATION				
Size	Bank 0	Bank 1	TAG/U30	TAG/U31
64KB	(8) 8K x 8	NONE	NONE	(1) 8K x 8
128KB	(8) 8K x 8	(8) 8K x 8	NONE	(1) 8K x 8
256KB	(8) 32K x 8	NONE	NONE	(1) 8K x 8
512KB	(8) 32K x 8	(8) 32K x 8	(1) 8K x 8	(1) 8K x 8

Note: The exact locations of Bank 0 & Bank 1 are unknown, as well as the exact locations for both TAG chips.

CACHE JUMPER CONFIGURATION						
Size	JP6	JP19	JP20	JP21	JP22	JP23
64KB	pins 1 & 2	Open	Open	Open	pins 1 & 2	pins 1 & 2
128KB	pins 2 & 3	Closed	Open	Open	pins 2 & 3	pins 2 & 3
256KB	pins 1 & 2	Closed	Closed	Open	pins 1 & 2	pins 1 & 2
512KB	pins 2 & 3	Closed	Closed	Closed	pins 2 & 3	pins 2 & 3

Note: Pins designated should be in the closed position.

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VESA WAIT STATE/BUS SPEED CONFIGURATION			
CPU speed	Wait states	JP15	JP16
≤ 33MHz	0 wait states	Open	Open
> 33MHz	1 wait state	Closed	Closed

AT CLOCK SELECTION		
Clock	JP8	JP9
LCLK/5	Closed	Closed
LCLK/4	Open	Closed
LCLK/3	Closed	Open
LCLK/2	Open	Open

CLOCK TYPE CONFIGURATION			
Type	JP4	JP5	JP7
Internal	Closed	pins 1 & 2 closed	pins 1 & 2 closed
External	Open	pins 2 & 3 closed	pins 2 & 3 closed