TYAN COMPUTER CORPORATION
S1441 PENTIUM-VL (REVISION 1.1)

Processor	Pentium
Processor Speed	60/66MHz
Chip Set	OPTi
Max. Onboard DRAM	128MB
Cache	64/128/256/512/1024/2024KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit VESA local bus slots (3)
NPU Options	None
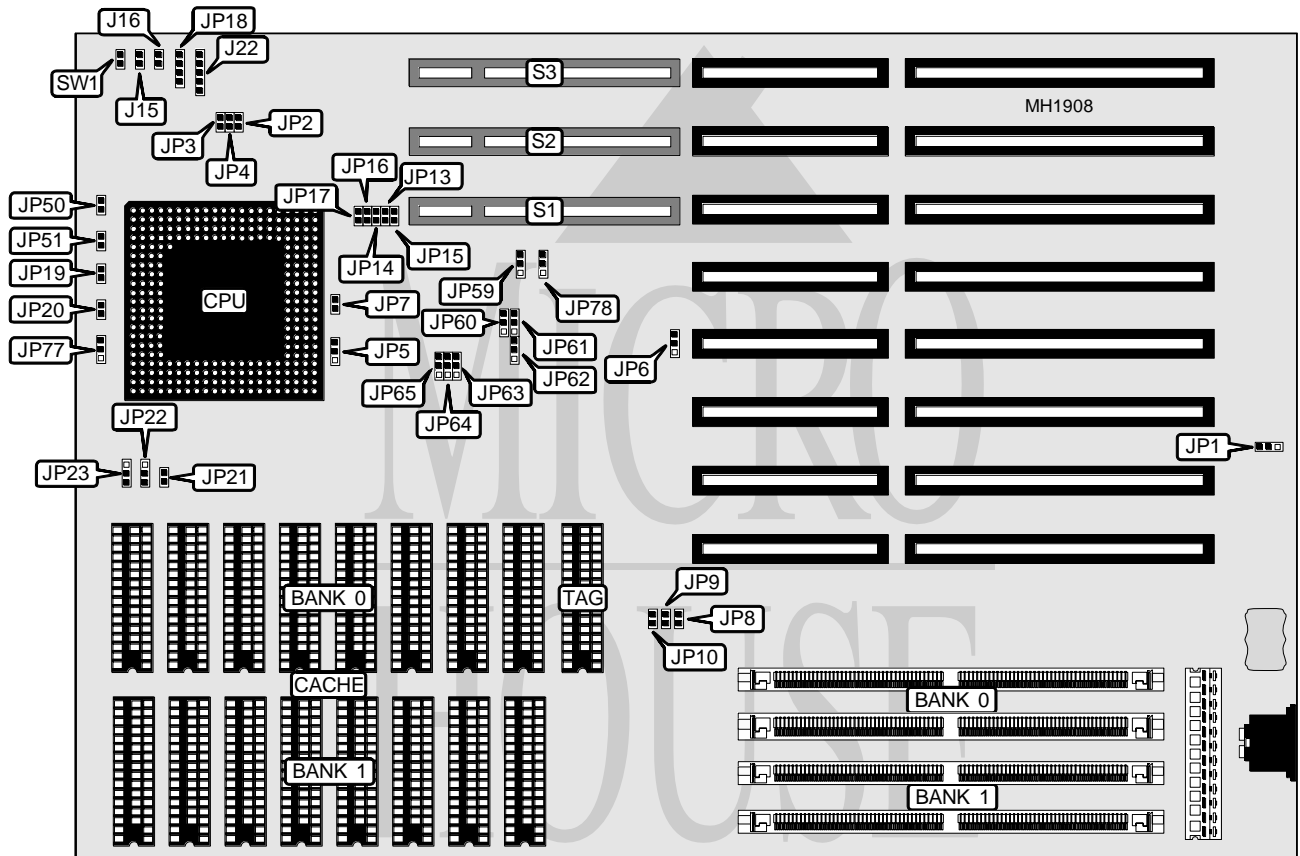
CONNECTIONS			
Purpose	Location	Purpose	Location
Turbo LED	J15	32-bit VESA Local bus slots	S1 - S3
Turbo switch	J16	Reset switch	SW1
Power LED & keylock	J22		
Speaker	JP18		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	J11	Open
í Factory configured - do not alter	J12	Open
í Factory configured - do not alter	J13	Closed
í Factory configured - do not alter	J15	Closed
í Factory configured - do not alter	J17	Closed
í CMOS memory normal operation	JP1	pins 2 & 3 closed
CMOS memory clear	JP1	pins 1 & 2 closed
í Monitor type select color	JP2	Open
Monitor type select monochrome	JP2	Closed
í Factory configured - do not alter	JP3	Closed
í AT back - to - back I/O delay enabled	JP10	Closed
AT back - to - back I/O delay disabled	JP10	Open

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
8MB	(2) 1M x 36	NONE
16MB	(2) 2M x 36	NONE
16MB	(2) 1M x 36	(2) 2M x 36
24MB	(2) 1M x 36	(2) 2M x 36
32MB	(2) 4M x 36	NONE
32MB	(2) 2M x 36	(2) 2M x 36
40MB	(2) 1M x 36	(2) 4M x 36
48MB	(2) 2M x 36	(2) 4M x 36
64MB	(2) 8M x 36	NONE
64MB	(2) 4M x 36	(2) 4M x 36
72MB	(2) 1M x 36	(2) 8M x 36
80MB	(2) 2M x 36	(2) 8M x 36
96MB	(2) 4M x 36	(2) 8M x 36
128MB	(2) 8M x 36	(2) 8M x 36

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
64KB	(8) 8K x 8	NONE	(1) 8K x 8
128KB	(8) 8K x 8	(8) 8K x 8	(1) 8K x 8
256KB	(8) 32K x 8	NONE	(1) 8K x 8
512KB	(8) 32K x 8	(8) 32K x 8	(1) 32K x 8
1024KB	(8) 128K x 8	NONE	(1) 32K x 8
2024KB	(8) 128K x 8	(8) 128K x 8	(1) 128K x 8

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CACHE JUMPER CONFIGURATION									
Size	JP6	JP19	JP20	JP21	JP22	JP23	JP50	JP51	JP77
64KB	1 & 2	Open	Open	Open	1 & 2	1 & 2	Open	Open	Open
128KB	2 & 3	Closed	Open	Open	2 & 3	2 & 3	Open	Open	Open
256KB	1 & 2	Closed	Closed	Open	1 & 2	1 & 2	Open	Open	Open
512KB	2 & 3	Closed	Closed	Closed	2 & 3	2 & 3	Open	Open	Open
1024KB	1 & 2	Closed	Closed	Closed	1 & 2	1 & 2	Closed	Open	1 & 2
2024KB	2 & 3	Closed	Closed	Closed	2 & 3	2 & 3	Closed	Closed	2 & 3
Note: Pins designated should be in the closed position.									

VESA BUS CLOCK CONFIGURATION			
Speed	JP63	JP64	JP65
20MHz	pins 2 & 3	pins 1 & 2	pins 1 & 2
25MHz	pins 1 & 2	pins 2 & 3	pins 1 & 2
33MHz	pins 1 & 2	pins 1 & 2	pins 2 & 3
40MHz	pins 2 & 3	pins 2 & 3	pins 1 & 2
50MHz	pins 2 & 3	pins 1 & 2	pins 2 & 3

VESA BUS CLOCK SOURCE			
Source	JP4	JP5	JP7
Internal clock from chip	Open	pins 2 & 3 closed	Open
External clock	Closed	pins 1 & 2 closed	Closed

AT BUS CLOCK CONFIGURATION		
CPU speed divided by:	JP8	JP9
2	Open	Open
3	Closed	Open
4	Open	Closed
5	Closed	Closed

CPU SPEED CONFIGURATION					
Speed	JP59	JP60	JP61	JP62	JP78
60MHz	pins 1 & 2	pins 2 & 3	pins 1 & 2	pins 1 & 2	pins 1 & 2
66MHz	pins 2 & 3	pins 1 & 2	pins 2 & 3	pins 2 & 3	pins 2 & 3
Note: Pins designated should be in the closed position.					

VESA WAIT STATE/BUS SPEED (ID2 & ID3) CONFIGURATION			
CPU speed	Wait states	JP15 (ID3)	JP16 (ID2)
$\leq$ 33MHz	0 wait states	Open	Open
$>$ 33MHz	1 wait state	Closed	Closed