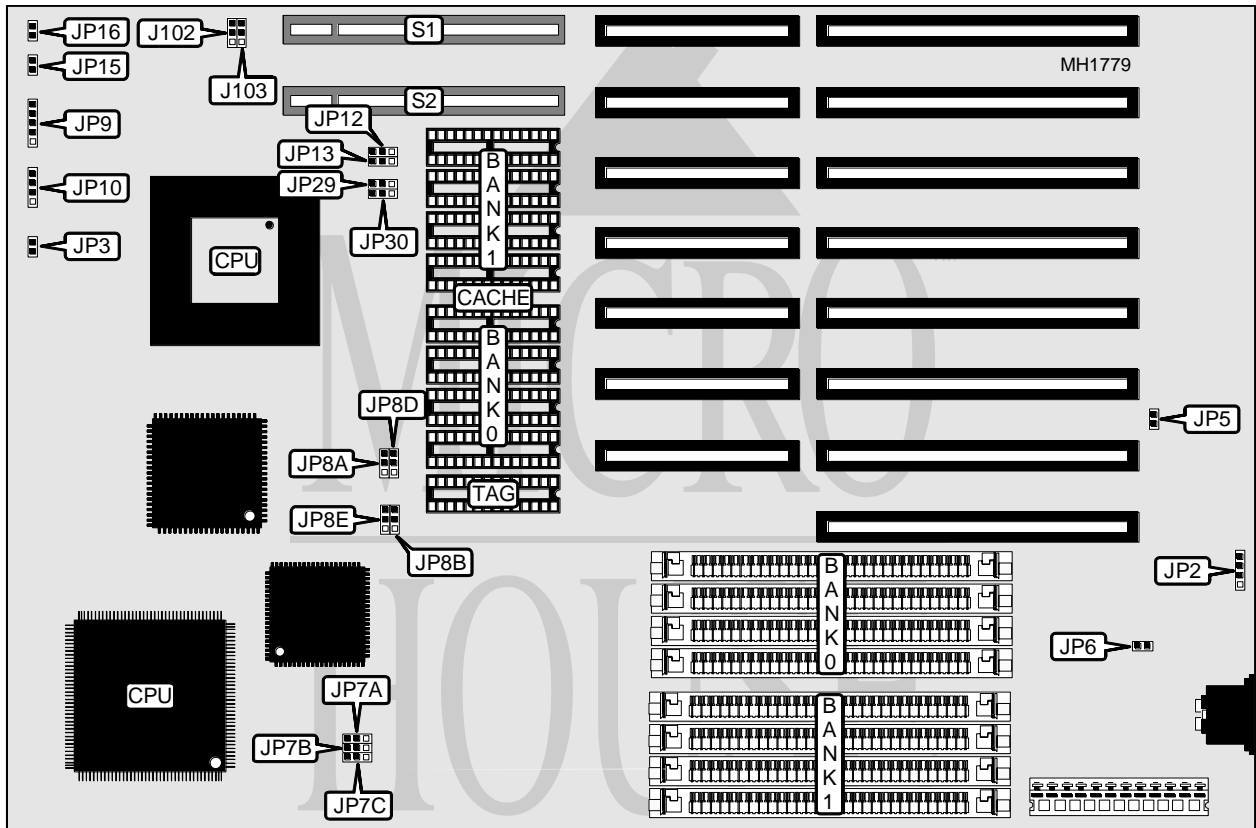


INFORMTECH INTERNATIONAL, INC.
IT486SMV MINI
KT TECHNOLOGY PTE LTD.
KT433 FX3C-WB/VESA

Processor	80486SX/80487SX/80486DX/ODP486SX/80486DX2
Processor Speed	20/25/33/50(internal)/66(internal)MHz
Chip Set	Forex
Max. Onboard DRAM	32MB
Cache	64/128/256KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit VESA local bus slots (2)
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	JP2	Turbo switch	JP15
Reset switch	JP3	Turbo LED	JP16
Power LED & keylock	JP9	32-bit VESA Local bus slot	S1
Speaker	JP10	32-bit VESA Local bus slot	S2

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USER CONFIGURABLE SETTINGS

Function	Jumper	Position
í Factory configured - do not alter	JP5	Open
í CMOS memory normal operation	JP6	Open
CMOS memory clear	JP6	Closed

DRAM CONFIGURATION

Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION

Size	Max Cachable	Bank 0	Bank 1	TAG
64KB	16MB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	32MB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	32MB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION

Size	JP8A	JP8B	JP8D	JP8E
64KB	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
128KB	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
256KB	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed

CPU TYPE CONFIGURATION

Type	JP12	JP13	JP29	JP30
80486SX	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
80487SX	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
80486DX	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
ODP486SX	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
80486DX2	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed

CPU SPEED CONFIGURATION

Speed	JP7A	JP7B	JP7C
20MHz	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
25MHz	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed
33MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
50i MHz	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed
66i MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed

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VESA WAIT STATE/BUS SPEED CONFIGURATION			
CPU speed	Wait states	JP102	JP103
≤ 33MHz	0 wait states	pins 1 & 2 closed	pins 1 & 2 closed
> 33MHz	1 wait state	pins 2 & 3 closed	pins 2 & 3 closed