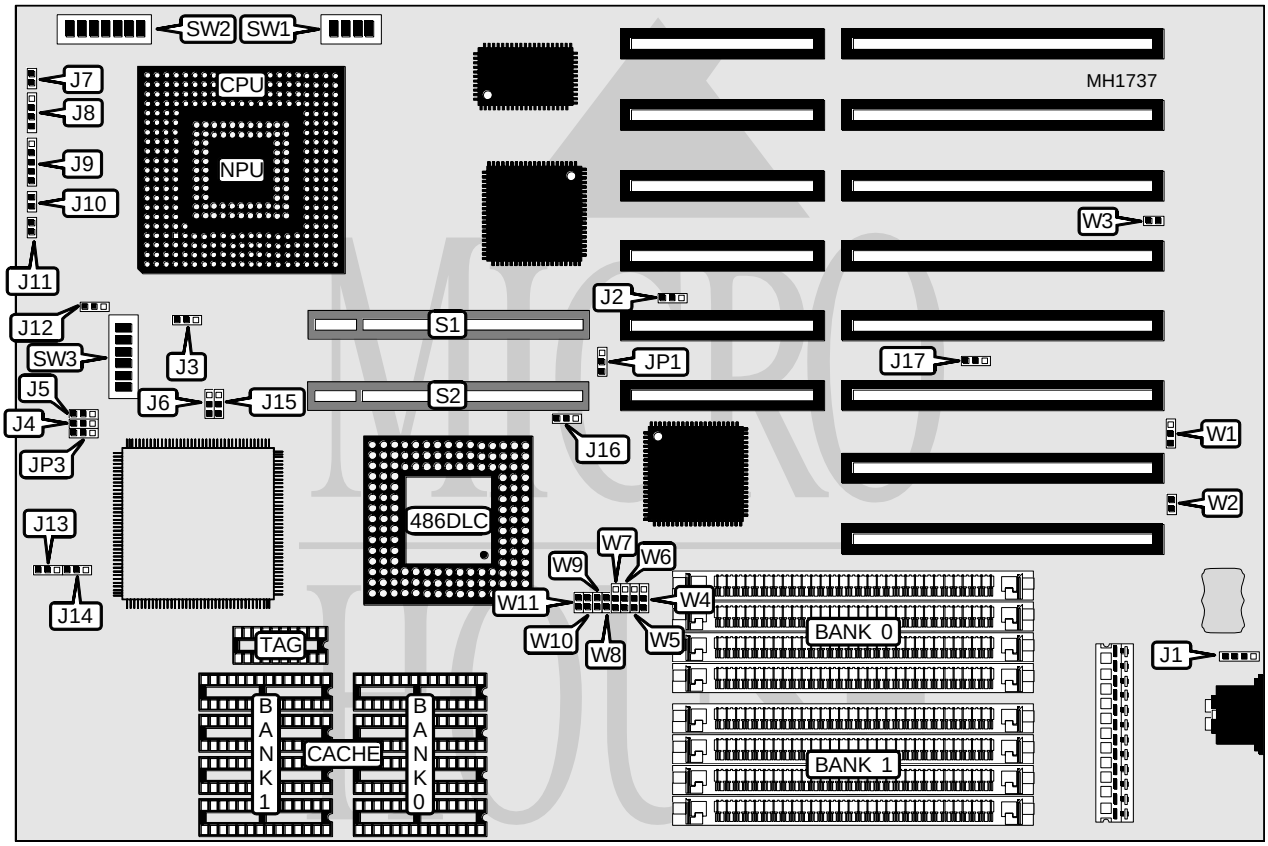
EFA CORPORATION
3 4 M 5 0 H L 2

Processor	CX486DLC/80486SX/80486DX/ODP486SX/80486DX2
Processor Speed	16/20/25/33/40/50(internal)/50/66(internal)MHz
Chip Set	UMC
Max. Onboard DRAM	32MB
Cache	64/128/256KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit VESA local bus slots (2)
NPU Options	80387DX



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J1	Reset switch	J10
Turbo LED	J7	Turbo switch	J11
Speaker	J8	32-bit VESA Local bus slot	S1
Power LED & keylock	J9	32-bit VESA Local bus slot	S2

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EFA CORPORATION
3 4 M 5 0 H L 2

. . . continued from previous page

USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í CMOS memory normal operation	W1	pins 1 & 2 closed
CMOS memory clear	W1	pins 2 & 3 closed
í Battery select internal	W2	Closed
Battery select external	W2	Open
í Monitor type select color	W3	Open
Monitor type select monochrome	W3	Closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION				
Size	Max Cachable	Bank 0	Bank 1	TAG
64KB	16MB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	32MB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	64MB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION								
Size	W4	W5	W6	W7	W8	W9	W10	W11
64KB	1 & 2	1 & 2	1 & 2	Open	Open	Open	Open	Open
128KB	2 & 3	1 & 2	2 & 3	1 & 2	Open	Closed	Open	Closed
256KB	2 & 3	2 & 3	1 & 2	2 & 3	Closed	Closed	Closed	Closed
Note: Pins designated should be in the closed position.								

CPU TYPE CONFIGURATION									
Type	J2	J6	J13	J14	J15	J16	J17	JP1	JP3
CX486DLC	1 & 2	2 & 3	1 & 2	2 & 3	2 & 3	1 & 2	1 & 2	1 & 2	2 & 3
80486SX	2 & 3	2 & 3	2 & 3	1 & 2	2 & 3	2 & 3	1 & 2	1 & 2	2 & 3
80486DX	2 & 3	2 & 3	2 & 3	1 & 2	2 & 3	2 & 3	1 & 2	1 & 2	2 & 3
ODP486SX	2 & 3	2 & 3	2 & 3	1 & 2	2 & 3	2 & 3	1 & 2	1 & 2	2 & 3
80486DX2	2 & 3	2 & 3	2 & 3	1 & 2	2 & 3	2 & 3	1 & 2	1 & 2	2 & 3
Note: Pins designated should be in the closed position.									

VESA LOCAL BUS IDE CONTROLLER CONFIGURATION		
Type	J6	J15
Promise Tech. (chip #PDC2013A)	pins 1 & 2 closed	pins 1 & 2 closed
Any other	pins 2 & 3 closed	pins 2 & 3 closed

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EFA CORPORATION
3 4 M 5 0 H L 2

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CPU TYPE CONFIGURATION (CONT.)							
Type	Package	SW3/1	SW3/2	SW3/3	SW3/4	SW3/5	SW3/6
CX486DLC	PGA	Off	On	On	Off	Off	Off
80486SX	PGA	Off	Off	Off	On	On	Off
80486SX	PQFP	Off	Off	Off	Off	Off	Off
80486DX	PGA	Off	On	On	Off	Off	Off
80486DX	PQFP	On	Off	Off	Off	Off	On
ODP486SX	PGA	Off	On	On	Off	Off	Off
80486DX2	PGA	Off	On	On	Off	Off	Off

CPU TYPE CONFIGURATION (CONT.)						
Type	SW2/1	SW2/2	SW2/3	SW2/4	SW2/5	SW2/6
CX486DLC	On	On	On	On	On	On
80486SX	Off	Off	Off	Off	Off	Off
80486DX	Off	Off	Off	Off	Off	Off
ODP486SX	Off	Off	Off	Off	Off	Off
80486DX2	Off	Off	Off	Off	Off	Off

CPU TYPE CONFIGURATION	
Type	J12
ODP486SX enabled	pins 1 & 2 closed
80486SX enabled	pins 2 & 3 closed
80486DX enabled	pins 2 & 3 closed
80486DX2 enabled	pins 2 & 3 closed
Note: This only applies when the 80486SX/DX PQFP is disabled.	

CPU PIN NUMBER CONFIGURATION		
Type	Pins	J3
CX486DLC	64	N/A
80486SX	168	Open
ODP486SX	169	pins 2 & 3 closed
ODP486SX	168	pins 1 & 2 closed
80486DX	168	pins 1 & 2 closed
80486DX2	168	pins 1 & 2 closed

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EFA CORPORATION
3 4 M 5 0 H L 2

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CPU SPEED CONFIGURATION							
CPU	Speed	OSC.	SW1/1	SW1/2	SW1/3	SW1/4	SW3/4
CX486DLC	16MHz	16MHz	On	On	On	On	Off
CX486DLC	20MHz	20MHz	On	On	On	Off	Off
CX486DLC	16MHz	32MHz	Off	Off	On	On	Off
CX486DLC	33MHz	66MHz	Off	Off	Off	On	Off
CX486DLC	40MHz	80MHz	On	Off	Off	Off	Off
80486SX	20MHz	40MHz	Off	Off	On	Off	On
80486SX	25MHz	25MHz	On	On	Off	On	On
80487SX	20MHz	40MHz	Off	Off	On	Off	N/A
80487SX	25MHz	25MHz	On	On	Off	On	N/A
80486DX	25MHz	25MHz	On	On	Off	On	Off
80486DX	33MHz	33MHz	On	Off	On	On	Off
80486DX	50MHz	50MHz	Off	Off	Off	Off	Off
ODP486SX	50i MHz	25MHz	On	On	Off	On	Off
ODP486SX	66i MHz	33MHz	On	Off	On	On	Off
80486DX2	50i MHz	25MHz	On	On	Off	On	Off
80486DX2	66i MHz	33MHz	On	Off	On	On	Off

NPU CONFIGURATION	
80387DX	SW2/switch 7
Disabled	Off
Enabled	On
Note: The 80387DX can only be used with a CX486DLC CPU. The NPU must be disabled if any other CPU is used	

VESA WAIT STATE/BUS SPEED CONFIGURATION			
CPU speed	Wait states	J4 (ID2)	J5 (ID3)
$\leq$ 33MHz	0 wait states	pins 1 & 2 closed	pins 1 & 2 closed
$>$ 33MHz	1 wait state	pins 2 & 3 closed	pins 2 & 3 closed

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