INTERCOMP, INC.
ILC VL33/486

Processor	80386DX/CX486DLC/80486SX/80486DX/80486DX2
Processor Speed	20/25/33/40/50(Internal)/50/66(Internal)MHz
Chip Set	Intercomp
Max. onboard DRAM	128MB
Cache	64/128/256KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit VESA local bus slots (2)
NPU Options	80387DX/3167
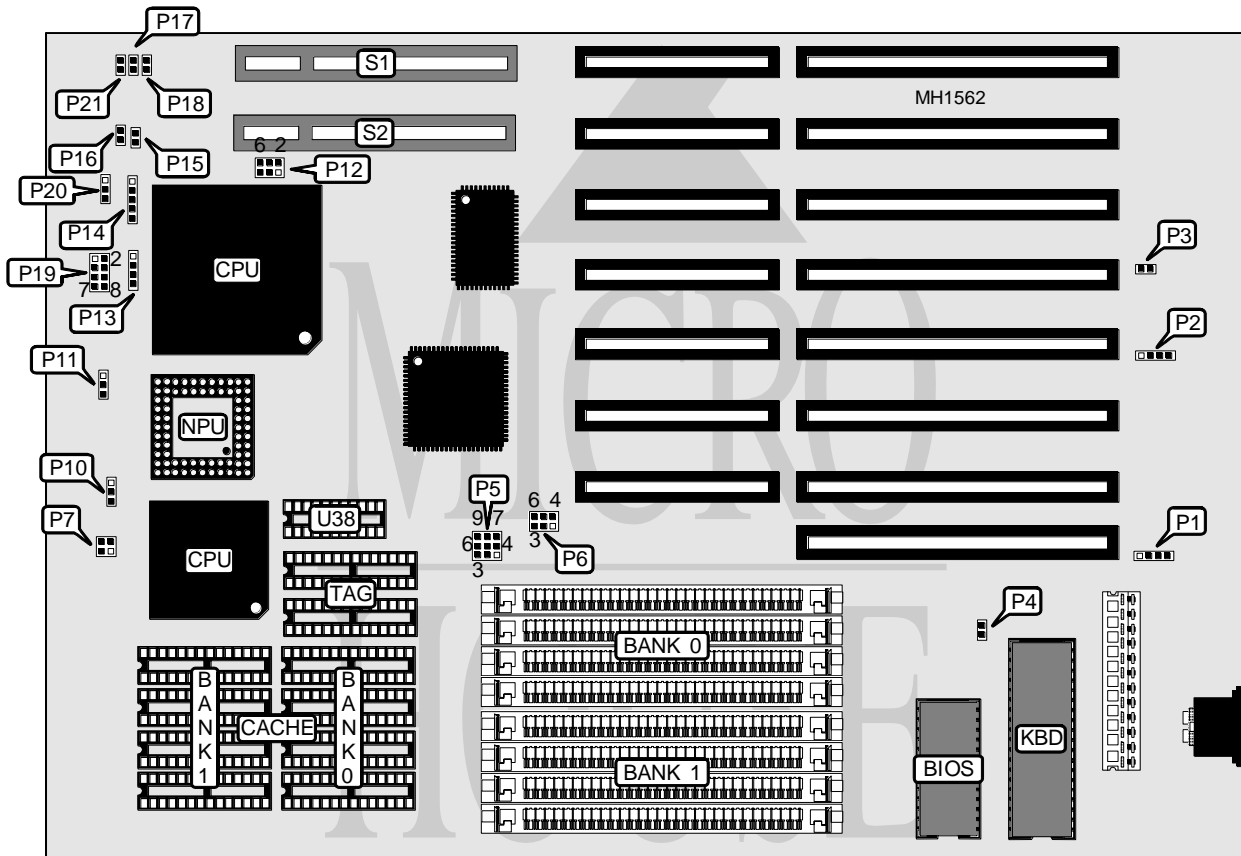
CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	P1	Turbo LED	P16
Speaker	P13	Turbo switch	P17
Power LED & keylock	P14	32-bit VESA local bus slot	S1
Reset switch	P15	32-bit VESA local bus slot	S2

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í CMOS memory normal operation (Internal Battery)	P2	pins 2 & 3 closed
CMOS memory normal operation (External Battery)	P2	pins 1 & 2 closed
CMOS memory clear	P2	pins 3 & 4 closed
í 80486/50MHz CPU enabled	P3	Closed
80486/50Mhz CPU disabled	P3	Open
í Factory configured do not alter	P4	Open
í VESA local bus enable	P7	pins 1 & 2, 3 & 4 open
VESA local bus disable	P7	pins 1 & 2, 3 & 4 closed
í Factory configured do not alter	P12	pins 3 & 6 closed
í NPU disabled (80387)	P20	pins 2 & 3 closed
NPU enabled (80387)	P20	pins 1 & 2 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
17MB	(4) 256K x 9	(4) 4M x 9
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9
64MB	(4) 16M x 9	NONE
65MB	(4) 256K x 9	(4) 16M x 9
68MB	(4) 1M x 9	(4) 16M x 9
80MB	(4) 4M x 9	(4) 16M x 9
128MB	(4) 16M x 9	(4) 16M x 9
Note: If SIMMs on bank 0 are not present SIMMs located on bank 1 will be automatically re-mapped to Bank O.		

CACHE CONFIGURATION				
Size	Bank 0	Bank 1	TAG	Dirty bit (U38)
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8	(1) 16K x 4
128KB	(4) 32K x 8	NONE	(1) 8K x 8	(1) 16K x 4
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8	(1) 16K x 4

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CACHE JUMPER CONFIGURATION			
CACHE	Main Memory	P5	P6
64KB	≤16MB	pins 1 & 2, 4 & 5, 7 & 8 closed	pins 1 & 2, 4 & 5 closed
64KB	>16MB, ≤=32MB	pins 1 & 2, 4 & 5, 7 & 8 closed	pins 1 & 2, 4 & 5 closed
128KB	≤32MB	pins 2 & 3, 4 & 5, 8 & 9 closed	pins 2 & 3, 4 & 5 closed
128KB	>32MB, ≤=64MB	pins 2 & 3, 4 & 5, 7 & 8 closed	pins 2 & 3, 4 & 5 closed
256KB	≤32MB	pins 2 & 3, 5 & 6, 8 & 9 closed	pins 2 & 3, 5 & 6 closed
256KB	>32MB, ≤=64MB	pins 2 & 3, 5 & 6, 7 & 8 closed	pins 2 & 3, 5 & 6 closed

CPU SPEED CONFIGURATION		
Speed	P3	P19
80386DX20/25	Open	pins 1 & 5, 2 & 6, 4 & 8 closed
80386DX/33	Open	pins 1 & 5, 3 & 7, 4 & 8 closed
CX486DLC/40	Open	pins 1 & 5, 2 & 6 closed
80486SX/20	Open	pins 2 & 6, 3 & 7 closed
80486SX/25	Open	pins 2 & 6, 4 & 8 closed
80486DX25	Open	pins 2 & 6, 4 & 8 closed
80486DX33	Open	pins 3 & 7, 4 & 8 closed
80486DX50	Closed	pins 3 & 7 closed
80486DX2/66	Open	pins 3 & 7, 4 & 8 closed

CPU TYPE CONFIGURATION				
CPU	P10	P11	P18	P21
80386DX	pins 1 & 2 closed	Open	Open	Closed
80486SX	pins 2 & 3 closed	pins 1 & 2 closed	Closed closed	Open
80486DX	pins 2 & 3 closed	pins 2 & 3 closed	Closed closed	Open
80486DX2	pins 2 & 3 closed	pins 2 & 3 closed	Closed closed	Open
Note: The VESA slots are disabled (by P10) when using a 80386 or CX486DLC				

NPU CONFIGURATION	
NPU	P20
None	pins 2 & 3 closed
80387	pins 1 & 2 closed
3167	pins 2 & 3 closed