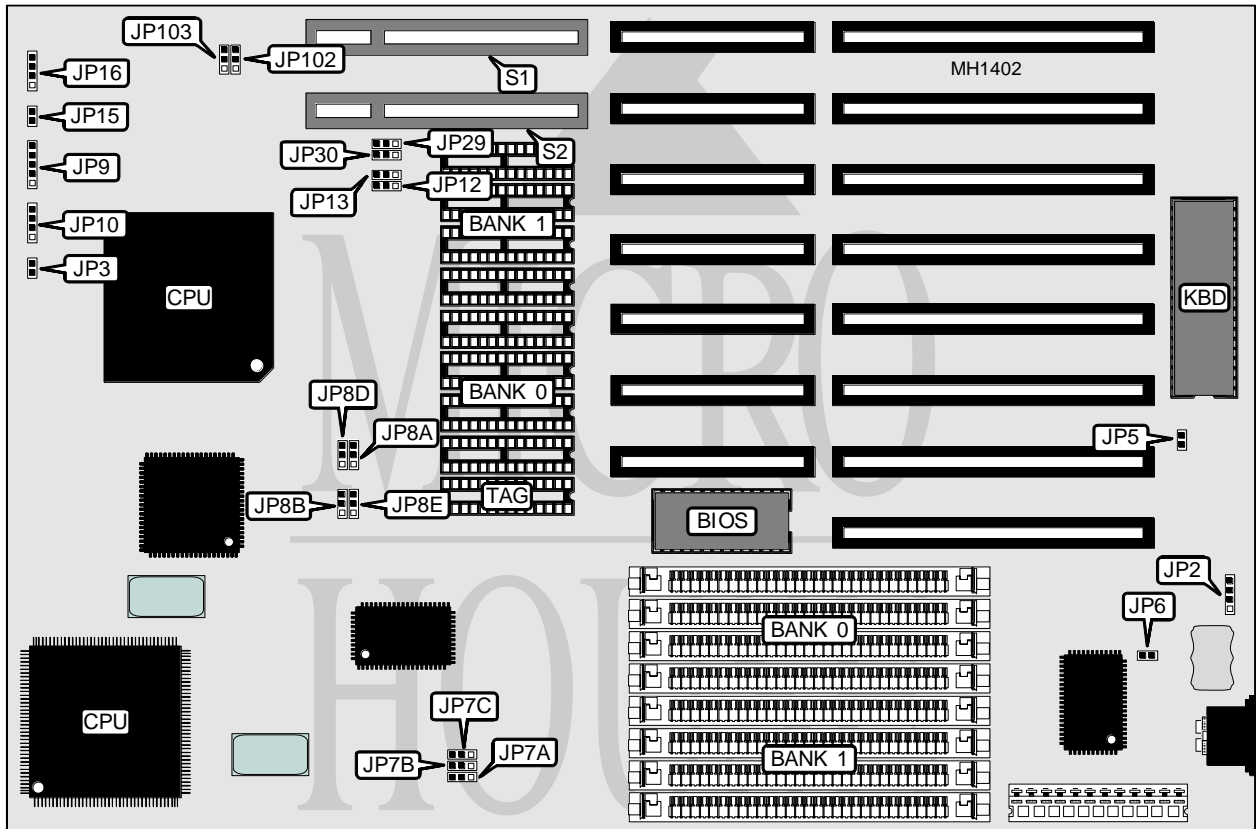


# JETPRO INFOTECH COMPANY, LTD.

## MB-4F3 (MB-450C4FV)

<b>Processor</b>	80486SX/80487SX/80486DX/ODP486SX/80486DX2
<b>Processor Speed</b>	20/25/33/50(internal)/50/66(internal)MHz
<b>Chip Set</b>	FOREX
<b>Max. Onboard DRAM</b>	32MB
<b>SRAM Cache</b>	64/128/256KB
<b>BIOS</b>	AMI/AWARD
<b>Dimensions</b>	254mm x 218mm
<b>I/O Options</b>	32-bit VESA local bus slots (2)
<b>NPU Options</b>	None



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	JP2	Turbo switch	JP15
Reset switch	JP3	Turbo LED	JP16
Power LED & keylock	JP9	32-bit VESA card (2)	S1 & S2
Speaker	JP10		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Battery select internal	JP2	pins 2 & 3 closed
Battery select external	JP2	connected
í Factory configured - do not alter	JP5	closed
í CMOS memory normal operation	JP6	open
CMOS memory clear	JP6	closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CPU SPEED CONFIGURATION					
CPU speed	JP7A	JP7B	JP7C	JP102	JP103
66MHz(internal)	pins 1 & 2	pins 1 & 2	pins 2 & 3	pins 1 & 2	pins 1 & 2
50MHz	pins 2 & 3	pins 1 & 2	pins 2 & 3	pins 2 & 3	pins 2 & 3
50MHz(internal)	pins 1 & 2	pins 2 & 3	pins 1 & 2	pins 1 & 2	pins 1 & 2
33MHz	pins 1 & 2	pins 1 & 2	pins 2 & 3	pins 1 & 2	pins 1 & 2
25MHz	pins 1 & 2	pins 2 & 3	pins 1 & 2	pins 1 & 2	pins 1 & 2
20MHz	pins 2 & 3	pins 1 & 2	pins 1 & 2	pins 1 & 2	pins 1 & 2

Note: JP102 controls VESA Bus wait states. JP103 controls VESA bus speed

CPU TYPE CONFIGURATION				
CPU Type	JP12	JP13	JP29	JP30
80486DX2	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
80486DX2(PQFP)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
ODP486SX	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
80486DX(PQFP)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
80486DX(PGA)	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
80487SX	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
80486SX(PQFP)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed

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SRAM CONFIGURATION			
Size	Cache SRAM	Location	TAG
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8
128KB	(4) 32K x 8	Bank 0	(1) 8K x 8
256KB	(8) 32K x 8	Banks 0 & 1	(1) 32K x 8

SRAM JUMPER CONFIGURATION				
Size	JP8A	JP8B	JP8D	JP8E
64KB	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
128KB	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
256KB	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed