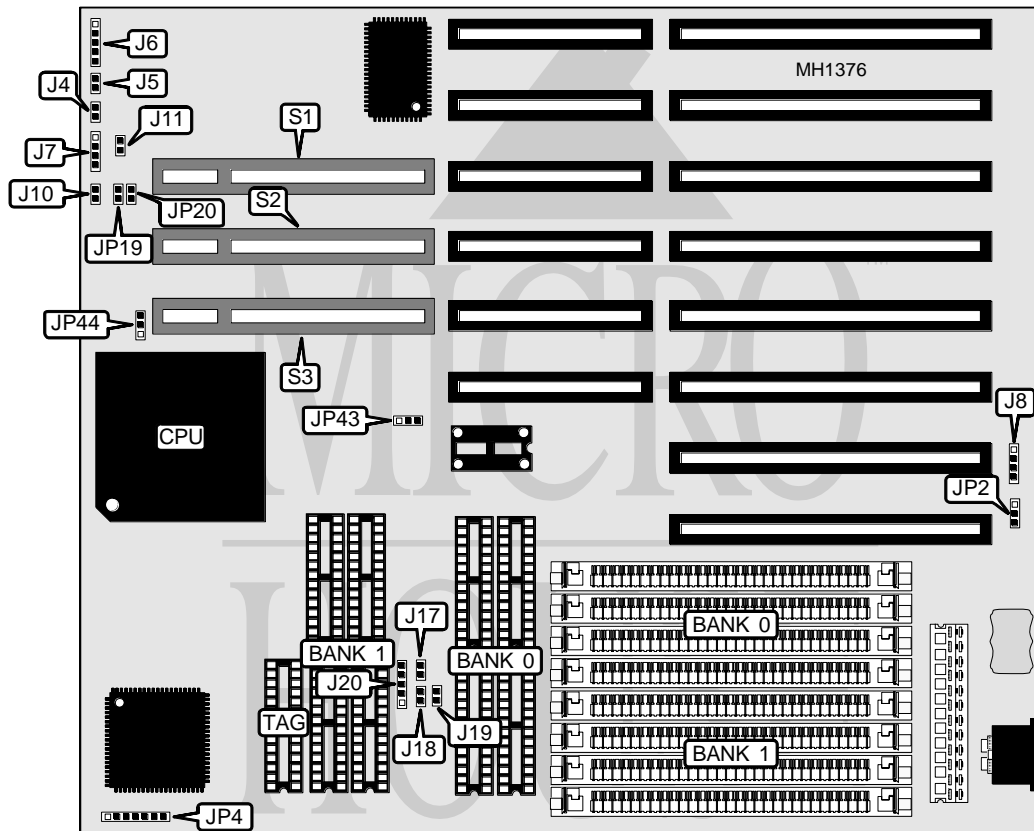


# UPDATE TECHNOLOGY, INC. VL-BUS MAINBOARD

<b>Processor</b>	80486SX/80487SX/80486DX/ODP486SX/80486DX2
<b>Processor Speed</b>	20/25/33/50(internal)/50/66(internal)MHz
<b>Chip Set</b>	UNI
<b>Max. Onboard DRAM</b>	32MB
<b>SRAM Cache</b>	32/64/128/256KB
<b>BIOS</b>	AMI
<b>Dimensions</b>	254mm x 218mm
<b>I/O Options</b>	32-bit VESA local-bus card slots (3)
<b>NPU Options</b>	None



CONNECTIONS			
Purpose	Location	Purpose	Location
Turbo switch	J4	External battery	J8
Turbo LED	J5	Reset switch	J10
Speaker	J6	32-bit VESA local-bus cards (3)	S1 - S3
Power LED & keylock	J7		

Continued on next page . . .

# UPDATE TECHNOLOGY, INC.

## VL-BUS MAINBOARD

... continued from previous page

USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Monitor type select color	J11	closed
Monitor type select monochrome	J11	open
í CMOS memory normal operation (internal battery)	JP2	pins 1 & 2 closed
CMOS memory normal operation (external battery)	JP2	open
CMOS memory clear	JP2	pins 2 & 3 closed
í VESA local bus speed select (CPU ≤ 33MHz)	JP19	closed
VESA local bus speed select (CPU > 33MHz)	JP19	open
í VESA local bus wait states select 0 (CPU >33MHz)	JP20	closed
VESA local bus wait state select 1 (CPU ≤ 33MHz)	JP20	open
í VESA local bus speed select CPU/1	JP43	pins 1 & 2 closed
VESA local bus speed select CPU/2	JP43	pins 2 & 3 closed
í CPU speed select ≤ 33MHz	JP44	pins 2 & 3 closed
CPU speed select > 33MHz	JP44	pins 1 & 2 closed

CPU TYPE CONFIGURATION	
CPU	J4
80486DX2	pins 1 & 2, 4 & 5, and 6 & 7 closed
ODP487SX	pins 2 & 3, 4 & 5, and 6 & 7 closed
80486DX	pins 1 & 2, 4 & 5, and 6 & 7 closed
80487SX	pins 5 & 6 closed
80486SX	pins 2 & 3, 4 & 5, and 6 & 7 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

Continued on next page ...

# UPDATE TECHNOLOGY, INC.

## VL-BUS MAINBOARD

... continued from previous page

SRAM CONFIGURATION			
Size	Cache	Location	TAG
32KB	(4) 8K x 8	Bank 0	(1) 8K x 8
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8
128KB	(4) 32K x 8	Bank 0	(1) 32K x 8
256KB	(8) 32K x 8	Banks 0 & 1	(1) 32K x 8

SRAM JUMPER CONFIGURATION				
Size	J17	J18	J19	J20
32KB	open	open	open	pins 2 & 3 closed
64KB	open	closed	open	pins 1 & 2 closed
128KB	open	closed	closed	pins 1 & 2 and 3 & 4 closed
256KB	closed	closed	closed	pins 1 & 2 and 4 & 5 closed