INFORMTECH INTERNATIONAL, INC.
IT486SMV MINI (VER. 1.00)

Processor	80486SX/80487SX/80486DX/ODP486SX/80486DX2
Processor Speed	20/25/33/50(internal)/66(internal)MHz
Chip Set	OPTI
Max. Onboard DRAM	32MB
SRAM Cache	64/128/256KB
BIOS	AMI
Dimensions	220mm x 230mm
I/O Options	32-bit VESA card slot (2)
NPU Options	None
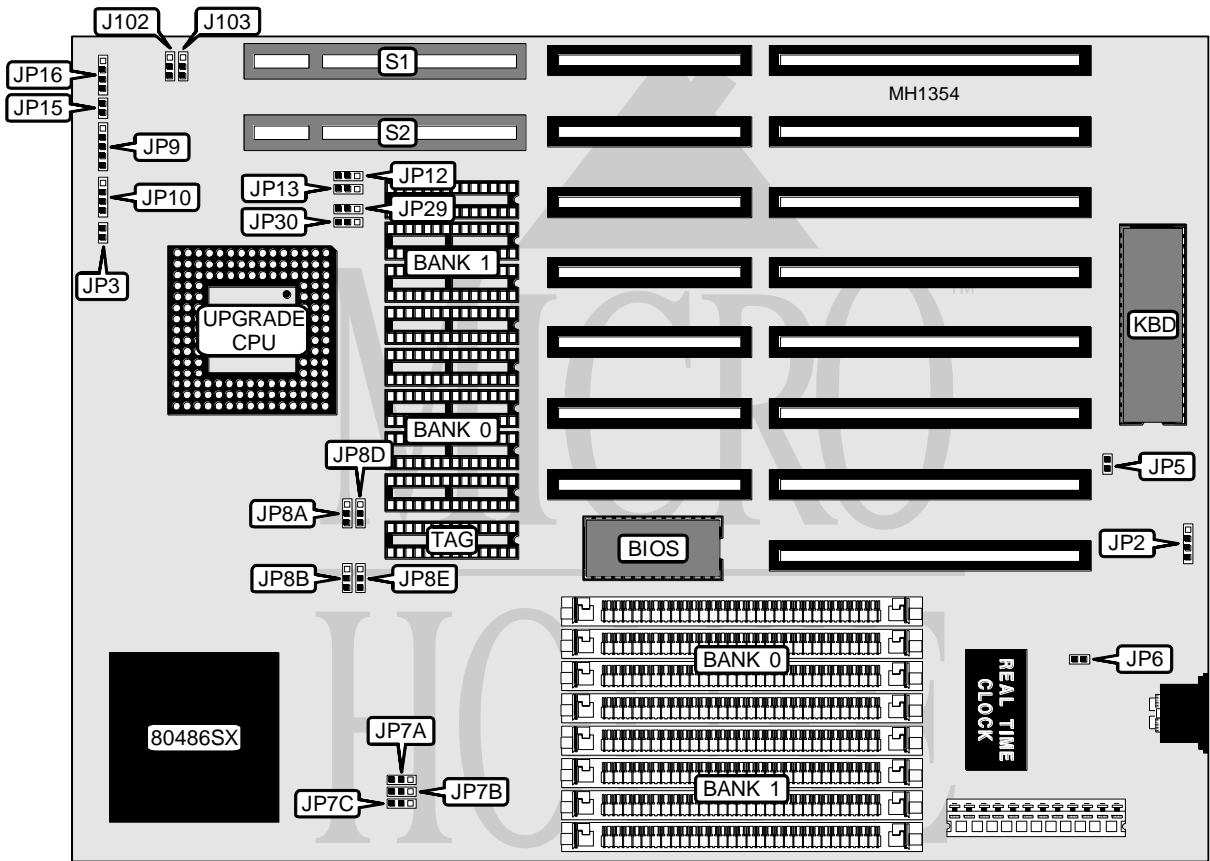
CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	JP2	Turbo switch	JP15
Reset switch	JP3	Turbo LED	JP16
Power LED & keylock	JP9	32-bit VESA local bus slots	S1 & S2
Speaker	JP10		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	JP5	open
í CMOS memory normal operation	JP6	open
CMOS memory clear	JP6	closed
í Wait states select zero	JP102	pins 1 & 2 closed
Wait state select one	JP102	pins 2 & 3 closed
í Local bus speed select ≤ 33MHz	JP103	pins 1 & 2 closed
Local bus speed select > 33MHz	JP103	pins 2 & 3 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CPU TYPE CONFIGURATION		
Type	Jumper JP12 & JP13	Jumper JP29 & JP30
80486DX2	pins 1 & 2 closed	pins 1 & 2 closed
ODP486SX	pins 1 & 2 closed	pins 2 & 3 closed
80486DX	pins 1 & 2 closed	pins 1 & 2 closed
80487SX	pins 1 & 2 closed	pins 2 & 3 closed
80486SX	pins 2 & 3 closed	pins 2 & 3 closed

CPU SPEED CONFIGURATION			
Speed	Jumper JP7A	Jumper JP7B	Jumper JP7C
66(internal)MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
50(internal)MHz	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed
33MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
25MHz	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed
20MHz	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed

SRAM JUMPER CONFIGURATION				
Size	Jumper JP8A	Jumper JP8B	Jumper JP8D	Jumper JP8E
64KB	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
128KB	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
256KB	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed

SRAM CONFIGURATION				
Size	Max. Cacheable Memory	Cache SRAM	Location	TAG
64KB	16MB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8
128KB	32MB	(4) 32K x 8	Bank 0	(1) 8K x 8
256KB	32MB	(8) 32K x 8	Banks 0 & 1	(1) 32K x 8