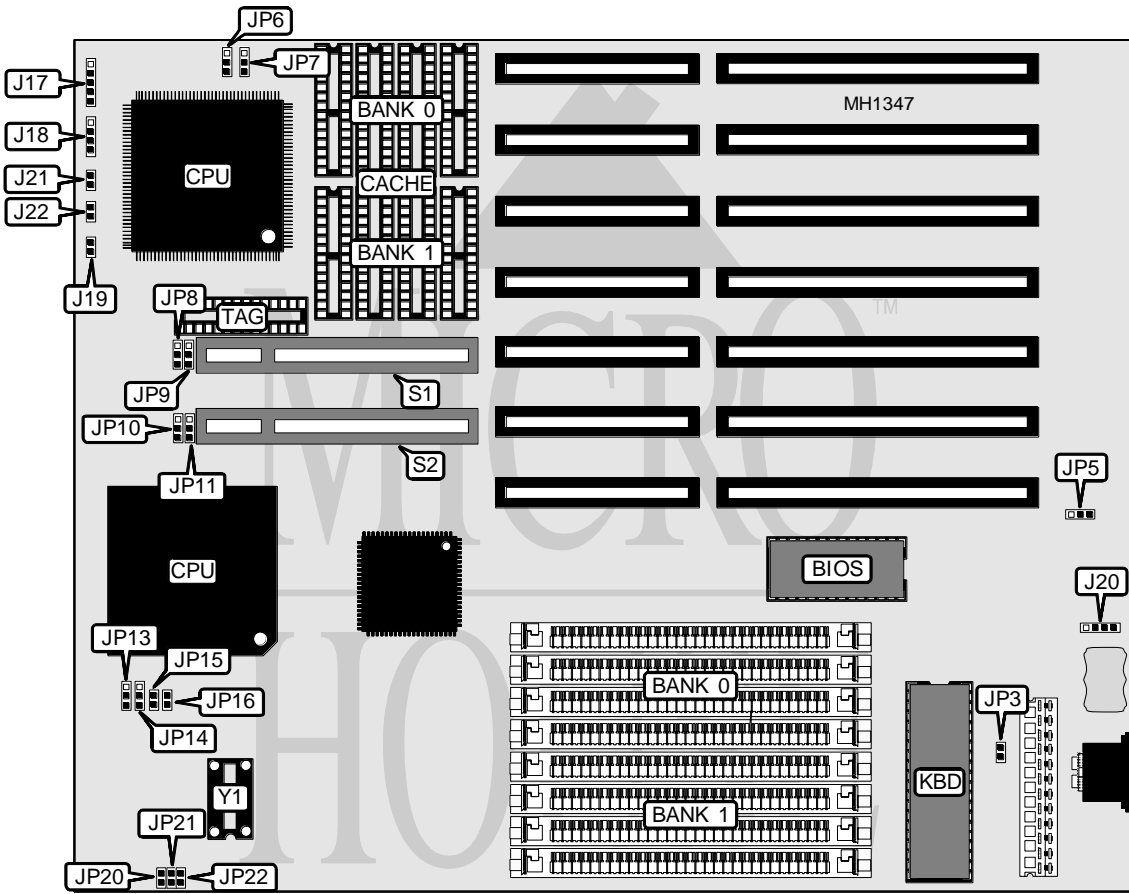


SOYO COMPUTER CO., LTD.
SY-025A2

Processor 80486SX/80487SX/80486DX/ODP486SX/80486DX2
Processor Speed 25/33/50(internal)/50/66(internal)MHz
Chip Set SIS
Max. Onboard DRAM 32MB
Cache 64/128/256KB
BIOS AMI
Dimensions 220mm x 254mm
I/O Options 32-bit VESA local bus slots (2)
NPU Options None



CONNECTIONS			
Purpose	Location	Purpose	Location
Keylock	J17	Turbo switch	J21
Speaker	J18	Turbo LED	J22
Reset	J19	32-bit VESA local bus slots (2)	S1 & S2
External battery	J20		

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SY-025A2

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Monitor type select color	JP3	Closed
Monitor type select monochrome	JP3	Open
í CMOS memory normal operation	JP5	pins 1 & 2 closed
CMOS memory clear	JP5	pins 2 & 3 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION		
Size	JP6	JP7
64KB	pins 1 & 2 closed	open
128KB	pins 2 & 3 closed	pins 1 & 2 closed
256KB	pins 2 & 3 closed	pins 2 & 3 closed

CPU TYPE CONFIGURATION				
Type	JP13	JP14	JP15	JP16
80486SX (PQFP)	Open	pins 2 & 3 closed	Open	Open
80486SX (PGA)	Open	pins 2 & 3 closed	Open	Closed
80487SX	pins 2 & 3 closed	pins 1 & 2 closed	Closed	Closed
80486DX	pins 1 & 2 closed	pins 1 & 2 closed	Closed	Closed
80486DX2	pins 1 & 2 closed	pins 1 & 2 closed	Closed	Closed

CPU SPEED CONFIGURATION					
Speed	OSC at Y1	JP8 - JP11	JP20	JP21	JP22
25MHZ	25MHz	pins 1 & 2 closed	Closed	Open	Closed
33MHZ	33MHz	pins 1 & 2 closed	Open	Closed	Closed
50iMHZ	25MHz	pins 1 & 2 closed	Closed	Open	Closed
50MHZ	50MHz	pins 2 & 3 closed	Open	Closed	Open
66iMHZ	33MHz	pins 1 & 2 closed	Open	Closed	Closed

Notes: The board may come with a clock generator at Y1.
 JP8 controls VESA bus slot S1's speed, JP9 Controls VESA bus slot S1's wait states.
 JP10 controls VESA bus slot S2's speed, JP11 Controls VESA bus slot S2's wait states.