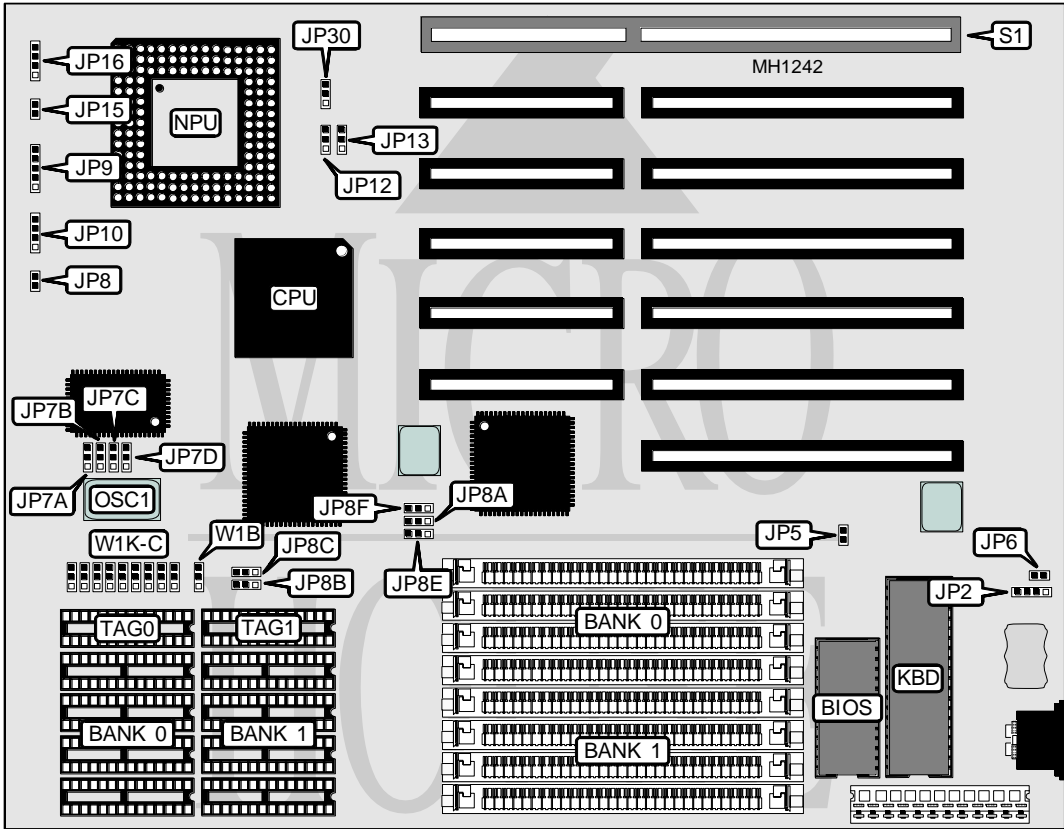


NEWTON NET TECHNOLOGY, INC.
N E 3 4 6 8 B

Processor	80386DX/CX486DLC/80486SX/80487SX/80486DX/80486DX2
Processor Speed	20/25/33/40/50(internal)/50/66(internal)
Chip Set	FOREX
Max. Onboard DRAM	32MB
SRAM Cache	64/128/256KB
BIOS	AMI
Dimensions	220.2mm x 250.2mm
I/O Options	32-bit local bus card slot
NPU Options	80387



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	JP2	Turbo switch	JP15
Reset switch	JP8	Turbo LED	JP16
Power LED & keylock	JP9	32-bit local bus card	S1
Speaker	JP10		

Continued on next page . . .

NEWTON NET TECHNOLOGY, INC. N E 3 4 6 8 B

... continued from previous page

USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	JP5	closed
í Factory configured - do not alter	JP6	open

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CPU SPEED CONFIGURATION				
Speed	JP7A	JP7B	JP7C	JP7D
20MHz	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
25MHz	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed
33MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
40MHz	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed
50MHz	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
66MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed
80MHz	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed

CPU TYPE CONFIGURATION					
CPU	JP12	JP13	JP30	W1B	W1K-C
80486DX2	pins 1 & 2	pins 1 & 2	pins 1 & 2	pins 1 & 2	pins 1 & 2
80486DX	pins 1 & 2	pins 1 & 2	pins 1 & 2	pins 1 & 2	pins 1 & 2
80487SX	pins 1 & 2	pins 1 & 2	pins 2 & 3	pins 1 & 2	pins 1 & 2
80486SX	pins 2 & 3	pins 2 & 3	pins 2 & 3	pins 1 & 2	pins 1 & 2
CX486DLC	N/A	N/A	N/A	pins 1 & 2	pins 2 & 3
80386DX	N/A	N/A	N/A	pins 2 & 3	pins 2 & 3
Note: Pins designated should be in the closed position.					

SRAM CONFIGURATION					
Size	Cache SRAM	Location	TAG0	TAG1	JP8A,B,C, E & F
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8	NONE	pins 1 & 2 closed
128KB	(4) 32K x 8	Bank 0	(1) 8K x 8	NONE	pins 1 & 2 closed
256KB	(8) 32K x 8	Banks 0 & 1	(1) 8K x 8	(1) 8K x 8	pins 2 & 3 closed