J-MARK COMPUTER CORPORATION 486WB CACHE

Processor 80386DX/CX486DLC

Processor Speed 33/40MHz **Chip Set** OPTI Max. Onboard DRAM 32MB

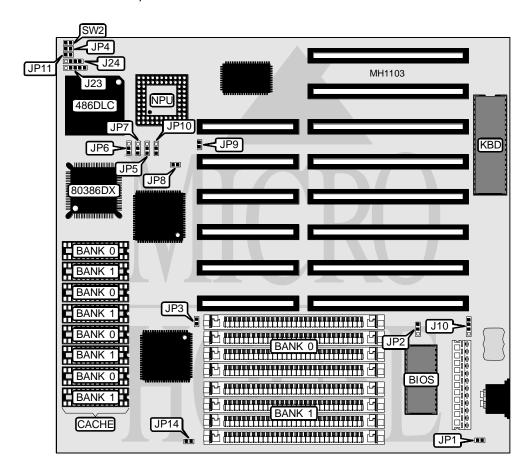
Cache 32/64/128/256KB

BIOS AMI

240mm x 220mm **Dimensions**

I/O Options None

NPU Options 80387/CX83D87



CONNECTIONS				
Purpose	urpose Location		Location	
External battery	J10	Turbo LED	JP4	
Power LED & keylock	J23	Reset switch	JP11	
Speaker	J24	Turbo switch	SW2	

Continued on next page . . .

J-MARK COMPUTER CORPORATION 486WB CACHE

. . . continued from previous page

USER CONFIGURABLE SETTINGS				
Function	Jumper	Position		
í Monitor type select color	JP1	Closed		
Monitor type select monochrome	JP1	Open		
í CMOS memory normal operation	JP2	pins 2 & 3 closed		
CMOS memory clear	JP2	pins 1 & 2 closed		
í Factory configured - do not alter	JP3	Closed		
í Factory configured - do not alter	JP14	Closed		

DRAM CONFIGURATION				
Size	Bank 0	Bank 1		
1MB	(4) 256K x 9	NONE		
2MB	(4) 256K x 9	(4) 256K x 9		
4MB	(4) 1M x 9	NONE		
8MB	(4) 1M x 9	(4) 1M x 9		
16MB	(4) 4M x 9	NONE		
32MB	(4) 4M x 9	(4) 4M x 9		

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	
32KB	(4) 8K x 8	NONE	
64KB	(4) 8K x 8	(4) 8K x 8	
128KB	(4) 32K x 8	NONE	
256KB	(4) 32K x 8	(4) 32K x 8	

CACHE JUMPER CONFIGURATION						
Size	JP5	JP6	JP7	JP8	JP9	JP10
32KB	1 & 2	2 & 3	1 & 2	Open	Open	2 & 3
64KB	2 & 3	2 & 3	1 & 2	Open	Open	1 & 2
128KB	2 & 3	2 & 3	2 & 3	Closed	Open	1 & 2
256KB	2 & 3	1 & 2	2 & 3	Closed	Closed	1 & 2
Note: Pins designated should be in the closed position.						