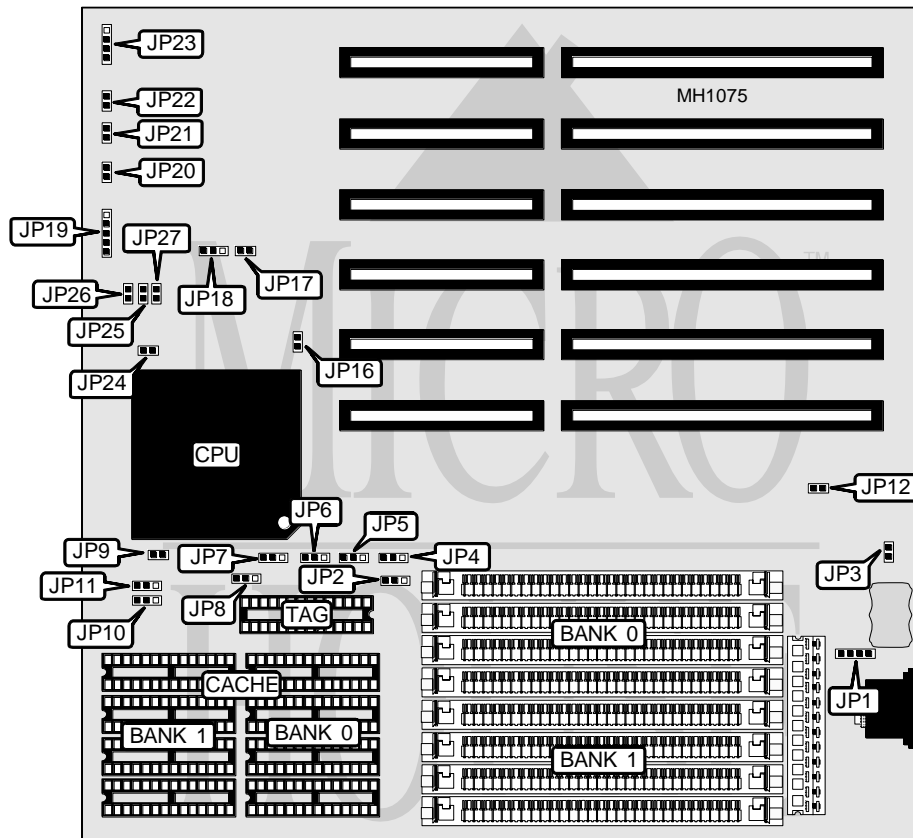


CHICONY, INC.

CH-486DLC-33/40H(L)

Processor	80486DX
Processor Speed	33/40MHz
Chip Set	OPTI
Max. Onboard DRAM	32MB
Cache	None
BIOS	AMI
Dimensions	220mm x 220mm
I/O Options	None
NPU Options	None



CONNECTIONS

Purpose	Location	Purpose	Location
External battery	JP1	Reset switch	JP21
Power LED & keylock	JP19	Turbo switch	JP22
Turbo LED	JP20	Speaker	JP23

Continued on next page . . .

CHICONY, INC.

CH-486DLC-33/40H(L)

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Battery type select internal	JP1	pins 2 & 3 closed
Battery type select external	JP1	Closed
í CMOS memory normal operation	JP3	pins 2 & 3 closed
CMOS memory clear	JP3	pins 2 & 3 closed
í Factory configured - do not alter	JP9	Open
í Monitor type select color	JP12	Closed
Monitor type select monochrome	JP12	Open
í Factory configured - do not alter	JP16	Open
í Factory configured - do not alter	JP17	Open
í Factory configured - do not alter	JP18	Open
í CPU speed select 33MHz	JP24	Closed
CPU speed select 40MHz	JP24	Open

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
32KB	(4) 8K x 8	NONE	(1) 8K x 8
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION								
Size	JP2	JP4	JP5	JP6	JP7	JP8	JP10	JP11
32KB	1 & 2	1 & 2	1 & 2	1 & 2	1 & 2	1 & 2	Open	2 & 3
64KB	1 & 2	2 & 3	1 & 2	2 & 3	1 & 2	1 & 2	Open	1 & 2
128KB	2 & 3	2 & 3	1 & 2	2 & 3	2 & 3	1 & 2	1 & 2	2 & 3
256KB	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3	1 & 2

Note: Pins designated should be in the closed position.

CPU CLOCK SOURCE CONFIGURATION			
Type	JP25	JP26	JP27
AV9107	Open	Open	Open
OSC	Closed	Closed	Closed