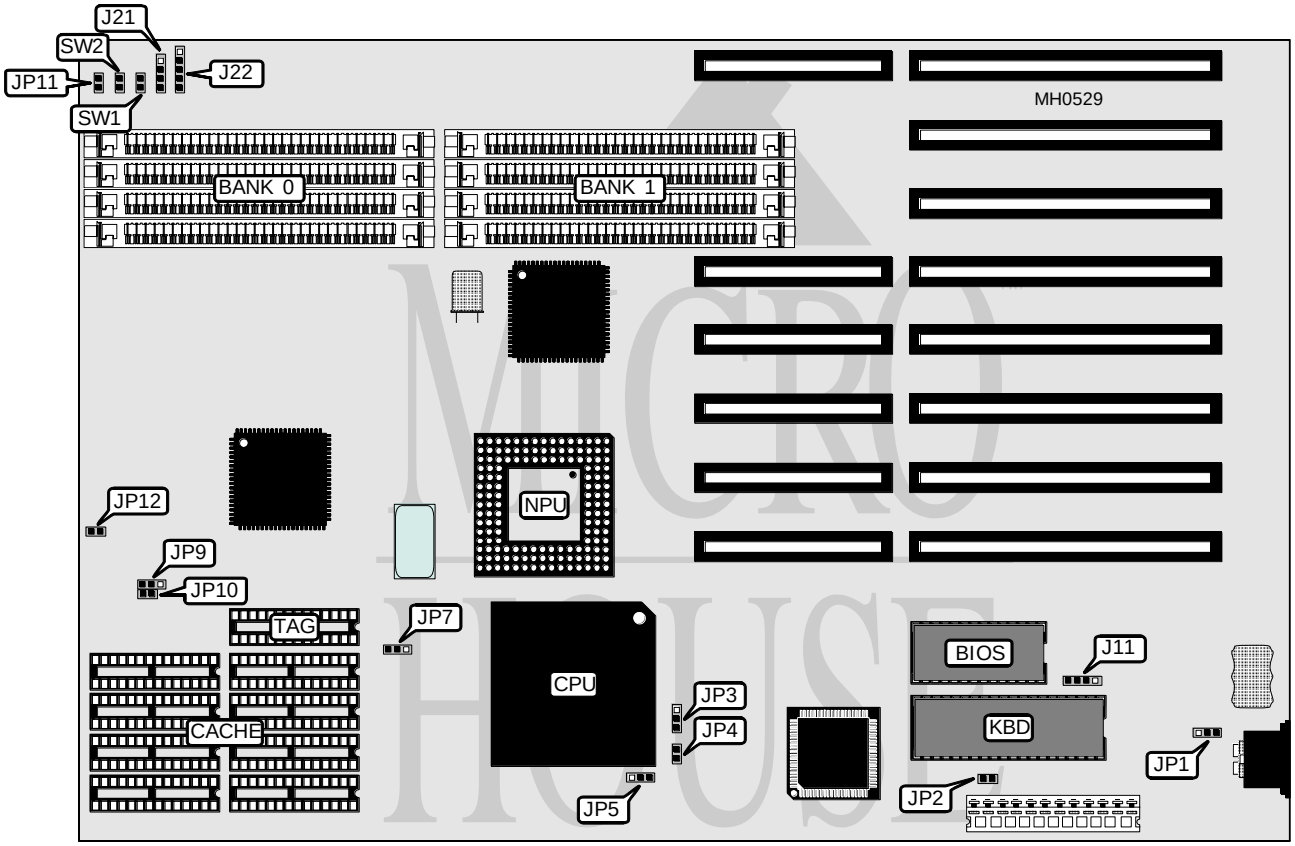
CHICONY, INC.
CH-486S-20B/25, CH-486-33G, CH-486-50G

Processor	80486SX/80487SX/80486DX
Processor Speed	20/25/33/50MHz
Chip Set	OPTI
Max. Onboard DRAM	32MB
Cache	64/256KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	None
NPU Options	4167



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J11	Turbo LED	JP11
Speaker	J21	Reset switch	SW1
Power LED & keylock	J22	Turbo switch	SW2

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í CMOS memory normal operation	JP1	pins 2 & 3 closed
CMOS memory clear	JP1	pins 1 & 2 closed
í Monitor type select color	JP2	Closed
Monitor type select monochrome	JP2	Open
í Factory configured - do not alter	JP7	pins 2 & 3 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 4M x 9	(4) 1M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0-	TAG (U33)	TAG (U34)
64KB	(8) 8K x 8	(1) 64K x 1	(1) 8K x 8
256KB	(8) 32K x 8	(1) 64K x 1	(1) 32K x 8

CACHE JUMPER CONFIGURATION			
Size	JP9	JP10	JP12
64KB	pins 2 & 3 closed	Open	Open
256KB	pins 1 & 2 closed	Closed	Closed

CPU TYPE CONFIGURATION			
Type	JP3	JP4	JP5
80486SX	pins 1 & 2 closed	Closed	pins 1 & 2 closed
80487SX	Open	Open	pins 2 & 3 closed
80486DX	pins 2 & 3 closed	Closed	pins 1 & 2 closed