UNIDENTIFIED
Y L - A 0 9

Processor	80286
Processor Speed	16MHz
Chip Set	C & T Neat
Max. Onboard DRAM	8MB
Cache	None
BIOS	AMI
Dimensions	330mm x 259mm
I/O Options	None
NPU Options	80287
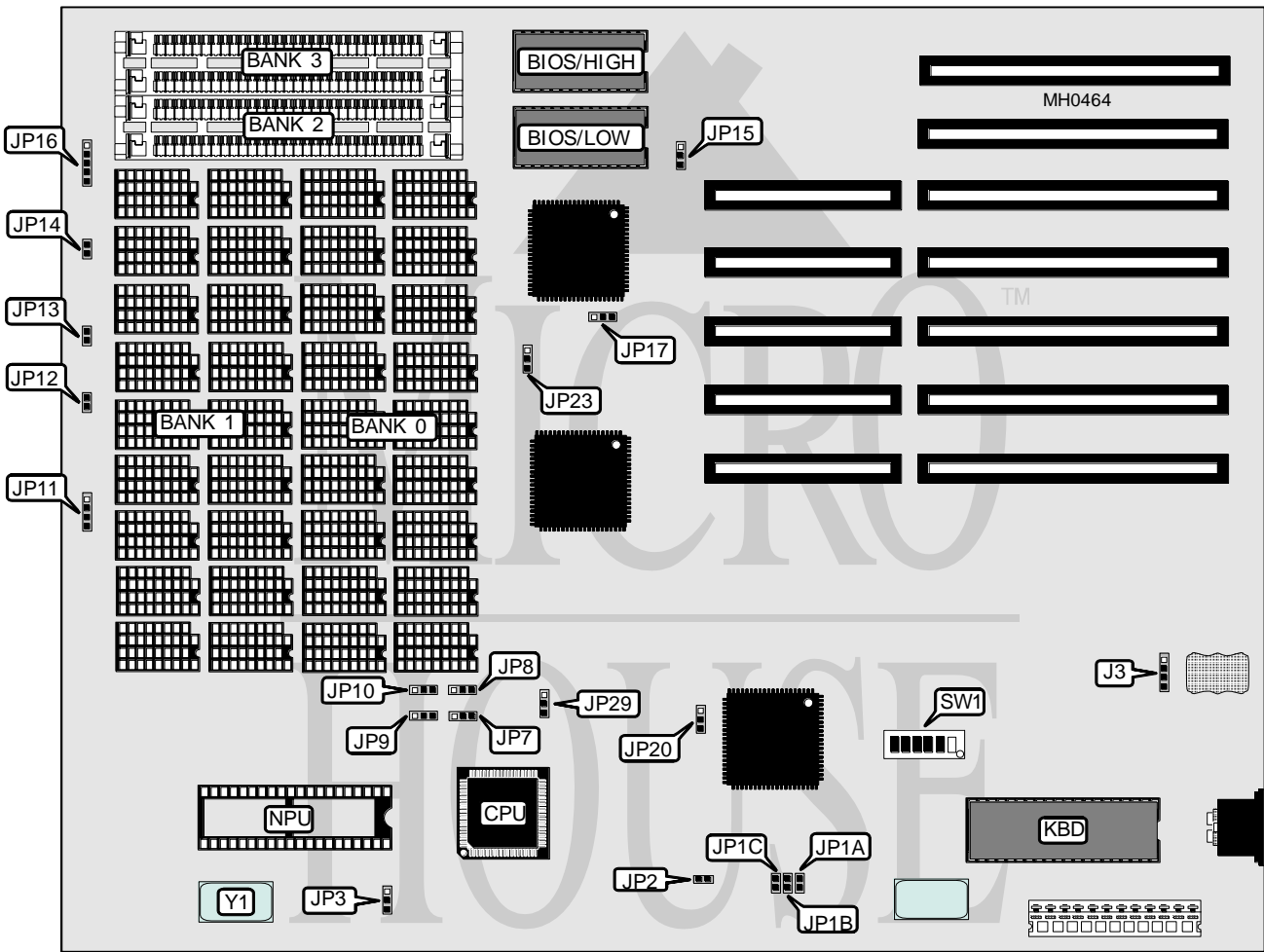
CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J3	Turbo LED	JP13
Speaker	JP11	Turbo Switch	JP14
Reset switch	JP12	Power LED & keylock	JP16

Continued on next page . . .

UNIDENTIFIED
Y L - A 0 9

USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	JP2	closed
í NPU mode select synchronous with CPU	JP3	pins 1 & 2 closed
NPU mode select synchronous with oscillator installed at Y1	JP3	pins 2 & 3 closed
í CPU speed select fast	JP14	closed
CPU speed select slow	JP14	open
í BIOS type select 27256	JP15	pins 2 & 3 closed
BIOS type select 27128	JP15	pins 1 & 2 closed
í Parity check enabled	JP17	pins 1 & 2 closed
Parity check disabled	JP17	pins 2 & 3 closed
í Quiet bus enabled	JP20	pins 1 & 2 closed
Quiet bus disabled (Use for high speed I/O cards)	JP20	pins 2 & 3 closed
í Same type of memory is used in all four banks	JP23	pins 1 & 2 closed
First two banks are different than last two banks of memory	JP23	pins 2 & 3 closed

DRAM CONFIGURATION				
Size	Bank 0	Bank 1	Bank 2	Bank 3
512KB	(18) 41256	NONE	NONE	NONE
1MB	(18) 41256	(18) 41256	NONE	NONE
1.5MB	(18) 41256	(18) 41256	(2) 256K x 9	NONE
2MB	(18) 41256	(18) 41256	(2) 256K x 9	(2) 256K x 9
2MB	(18) 411000	NONE	NONE	NONE
4MB	(18) 411000	(18) 411000	NONE	NONE
6MB	(18) 411000	(18) 411000	(2) 1M x 9	NONE
8MB	(18) 411000	(18) 411000	(2) 1M x 9	(2) 1M x 9

DRAM JUMPER CONFIGURATION						
Size	JP7	JP8	JP9	JP10	JP17	JP23
512KB	Open	2 & 3	Open	Open	1 & 2	1 & 2
1MB	Open	2 & 3	Open	2-3	1 & 2	1 & 2
1.5MB	1 & 2	2 & 3	Open	2-3	1 & 2	1 & 2
2MB	1 & 2	2 & 3	1 & 2	2-3	1 & 2	1 & 2
2MB	Open	2 & 3	Open	Open	1 & 2	1 & 2
4MB	Open	2 & 3	Open	2-3	1 & 2	1 & 2
6MB	1 & 2	2 & 3	Open	2-3	1 & 2	1 & 2
8MB	1 & 2	2 & 3	1 & 2	2-3	1 & 2	1 & 2
Note: Pins designated should be in the closed position.						

UNIDENTIFIED
YL-A09

DRAM SWITCH CONFIGURATION			
Size	SW1/3	SW1/4	SW1/5
512KB	Off	Off	Off
1MB	On	Off	Off
1.5MB	Off	On	Off
2MB	On	On	Off
2MB	Off	Off	On
4MB	On	Off	On
6MB	Off	On	On
8MB	On	On	On

I/O CONFIGURATION			
Setting	JP1A	JP1B	JP1C
I/O at full speed during memory refresh cycle	Open	Closed	Open
I/O at full speed during memory refresh cycle and DMA	Closed	Open	Open
I/O at full speed	Closed	Closed	Closed