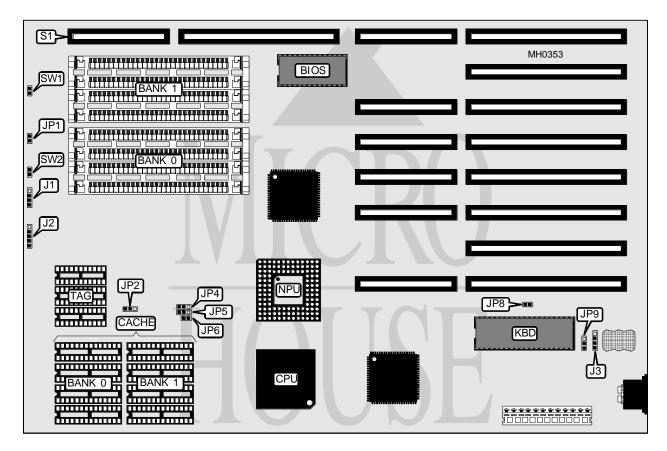
GIGA-BYTE TECHNOLOGY CO., LTD G A - 3 8 6 T S

- Processor Processor Speed Chip Set Max. Onboard DRAM SRAM Cache BIOS Dimensions I/O Options NPU Options
- 80386DX 33/40MHz OPTI 32MB 64/128/256KB AMI/MR 330mm x 218mm 32-bit external memory card slot 80387/3167



CONNECTIONS				
Purpose	Location	Purpose	Location	
Speaker	J1	32-bit external memory card	S1	
Power LED & Keylock	J2	Turbo switch	SW1	
External battery	J3	Reset switch	SW2	
Turbo LED	JP1			

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USER CONFIGURABLE SETTINGS				
Function	Jumper	Position		
í Monitor type select color	JP8	closed		
Monitor type select monochrome	JP8	open		
í CMOS memory normal operation	JP9	pins 1 & 2 closed		
CMOS memory clear	JP9	pins 2 & 3 closed		
Note: The location of JP9 may differ depending on the bo	ard revision.			

DRAM CONFIGURATION				
Size	Bank 0	Bank 1		
1MB	(4) 256K x 9	NONE		
2MB	(4) 256K x 9	(4) 256K x 9		
4MB	(4) 1M x 9	NONE		
8MB	(4) 1M x 9	(4) 1M x 9		
16MB	(4) 4M x 9	NONE		
32MB	(4) 4M x 9	(4) 4M x 9		

CACHE CONFIGURATION				
Size	Bank 0	Bank 1	TAG	
64KB	(4) 8K x 8	(4) 8K x 8	(3) 4K x 4	
128KB	(4) 32K x 8	NONE	(3) 16K x 4	
256KB	(4) 32K x 8	(4) 32K x 8	(3) 16K x 4	
Note: Pins designated sho	uld be in the closed position.			

CACHE JUMPER CONFIGURATION				
Size	JP2	JP4	JP5	JP6
64KB	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed	Open
128KB	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed	Closed
256KB	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed	Closed