RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- * Reorient the receiving antenna.
- * Relocate the computer away from the receiver.
- * Move the computer away from the receiver.
- * Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
- * Ensure that card slot covers are in place when no card is installed.
- * Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
- * If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in- line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

NOTE

- 1. When you see an error message appear on the screen after turning the power on, leave the system switched on for one or two hours to recharge the battery. You can then enter the system configuration.
- 2. Leave your system switched on for 10 to 15 hours to completely recharge the battery.
- 3. If you had left the system switched off for more than one month, follow step 2, above.

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SECTION 0 GENERAL FEATURES

The OCTEK 286EMS system board is a high performance system board that represents a significant technological advance over the conventional 80286 designs. It offers an increased power and flexibility architecture by supporting 80286 processor speeds up to 16 MHz. The design utilizes advanced main frame techniques such as two or four way interleaving along with high speed page mode capability. It is also optimized to allow mixing of DRAM types to give end user the maximum flexibility in choosing the correct DRAM capacity for their application.

This manual covers the necessary information to operate the OCTEK 286EMS system board. It will assist you in the installation and configuration of the system. By familiarizing the features of the board and where things are, user should be able to operate the system smoothly.

The OCTEK 286EMS system board is designed for the most advanced computer-based applications for today and in the future. The OCTEK 286EMS system provides a highly integrated approach to implement a very flexible system based on the PC/AT and the 80286 CPU. Key features of the board are summarized as follows:

0.1 PROCESSOR AND SYSTEM

- * 80286-16 CPU
- * Optional 80287 numeric coprocessor
- * 8/16 MHz system speed hardware/software switchable
- * Optimized for OS/2 operation
- * Real time clock and calendar circuit
- * Onboard battery backup for CMOS configuration table and real-time clock
- * On board power good test circuit

0.2 MEMORY SUBSYSTEM

* Memory Capacity:

2MB using 256Kx4 DRAM chips or 256K SIMMs 8MB using 1M SIMMs Support mix memory of 256K DRAM and 1M SIMMs

Page/Interleave memory supported:

- Page mode memory
- 2-way and 4-way page/interleave mode Hardware LIM/EMS 4.0 implementation

Shadow RAM support for System and Video BIOS Parity bit can either be enabled or disabled

Available Memory Configuration

- 512 KB
- -*640 KB
- 1 MB
- 1.5 MB
- 2 MB
- 3 MB
- 4 MB
- 4.5 MB
- 5 MB
- 6 MB
- 8 MB

(640 KB memory configuration is available only if SIMM type memory is used)

* ROM Capacity:

256K or 128K EPROM BIOS space for custom BIOS applications **0.3 I/O SUBSYSTEM**

- * Bus I/O Speed
 - Equal to Processor Clock Speed
 - Half of Processor Clock Speed
- * Eight expansion slots
 - 6 with a 36- and a 62-pin card-edge socket
 - 2 with only the 62-pin card-edge socket

Additional Features

- * Hardware control support
 - Keylock
 - Reset
 - Turbo LED
 - Power LED
 - Speaker
 - External Battery

- System support function:
 - 7-Channel Direct Memory Access16-level interruptThree programmable timersSystem clock

SECTION 1 INTRODUCTION

The design of cost effective IBM PC/AT compatible microcomputer requires taking advantage of every possible advanced technology. The OCTEK 286EMS is designed with top performance and flexibility in mind, it is a fully PC/AT compatible system board implemented with the high integration G2 AT chip set which supports the 80286 CPU at clock speeds up to 16 MHz zero wait state performance.

A distinguishing feature of this design includes the dual clock system. This innovation make it possible for your computer to operate at either of two clock speeds: 8 MHz or 16 MHz. In the 16 MHz mode, your computer will operate much faster than a conventional 80286-based computer.

Another significant advance feature of the OCTEK 286EMS is its memory subsystem. The system board utilizes advanced main frame techniques such as two or four way interleaving along with high speed page mode capability. It supports up to eight MByte of DRAMs on the system board, with hardware implementation of EMS 4.0. The hardware has been optimized to allow mixing of DRAM types to give the end user the maximum flexibility in choosing the correct DRAM capacity for your application. It supports both 256K and 1M DRAMs in a configuration of up to eight megabytes of on-board memory. This flexibility in configuration allows you to select an ideal cost/performance combination.

The OCTEK286EMS architecture features OS/2 optimization. OS/2 makes frequent DOS calls while operating in protected mode of 80286 CPU. In order to service these DOS calls, the 80286 CPU has to switch from protected to real mode quickly. OCTEK286EMS provides an unique method to handle the mode switching for OS/2 operation optimization. In an OS/2 environment, where frequent DOS calls are made, this feature provides significant performance improvement.

The OCTEK286EMS provides Shadow RAM for BIOS and Video ROM, these can be enabled or disabled in the SETUP program (See Section 5). When enabled the execution speed of the BIOS and/or the Video ROM program will be faster.

In addition, memory interleave is supported which will improve the system speed.

It also provides on-board power good source. The on- board power good generator provides a 'power-good' signal to indicate proper operation of the power supply. It allows you to used XT grade power supply which does not provide the circuitry to generate the power good signal.

The OCTEK 286EMS system is hardware and software compatible with associated PC-AT products. This means that virtually all the hardware and software that is available for the PC/AT can also be run on a system you build around the OCTEK 286EMS system board.

The OCTEK 286EMS is fully software compatible with the IBM PC-AT design. The OCTEK 286EMS is designed such that software is completely portable between the PC-AT to the OCTEK 286EMS. Note that "real-time" types of software programs could be the exception, as the higher operating speed of the OCTEK 286EMS could cause execution or human interface

problems.

The OCTEK 286EMS supports MS-DOS Version 2.0 and above, Xenix and all PC/AT application programs. Users can run applications designed for the PC/AT on the OCTEK 286EMS without any modification. Multi- tasking and multi-user capabilities are fully functional on the OCTEK 286EMS system board.

In addition, the OCTEK 286EMS provides standard expansion bus connectors so that add-on cards developed for the PC-AT will interface correctly.

The OCTEK 286EMS features high performance, low power consumption, low board space requirements, reliability and low cost.

For these reasons, the OCTEK 286EMS is the ideal choice for a person seeking affordable, well designed AT-style power.

SECTION 2 SYSTEM BOARD SWITCH SETTING

The switches on the system board are shown in the figure below and on the following pages. These settings are used to specify the system board memory type and memory size. If you change the memory size of the mainboard, you have to reset them accordingly.

Warning: Before you change any switch settings, make a note of how the switches are originally set.

Switch	Function	
1-4	RAM size & RAM type Selection	
5	ON for 640KB total memory OFF for all other memory configurations	
6 2.1 System	Reserved	
2.1 System board switch block location		

The following figure shows where the switch block is on the system board.

Note: *The switch settings below are for example only.*

The switch settings may be changed by using the tip of a pen to gently push the switches into the correct position.

2.2 RAM Configuration and Installation

The OCTEK286EMS supports the following memory components:

- a) 44256K DIPs
- b) 41256 DIPs (parity RAM)
- c) 64KB SIMM
- d) 256KB SIMM
- e) 1MB SIMM

The above memory components may be combined in such a way to obtain total memory of 512KB, 640KB, 1MB, 1.5MB, 2MB, 3MB, 4MB, 4.5MB, 5MB, 6MB and 8MB.

The OCTEK 286EMS system board provides sixteen 20- pins DIP sockets (for 44256 DRAMs) and eight 18-pins DIP sockets (for 41256 parity DRAMs). In addition, 8 SIMM sockets are provided for installation of 64KB, 256KB or 1MB SIMMs.

The DIPs DRAMs and the SIMMs are organized in 4 banks as shown below:

Bank 0 : U1,U2,U3,U4

: U5,U6 (Parity)

or

: SIMM at Bank 0 - low byte : SIMM at Bank 0 - high byte

Bank 1 : U7,U8,U9,U10

: U11,U12 (Parity)

or

: SIMM at Bank 1 - low byte : SIMM at Bank 1 - high byte

Bank 2 : U13,U14,U15,U16

: U17,U18 (Parity)

or

: SIMM at Bank 2 - low byte : SIMM at Bank 2 - high byte

Bank 3 : U19,U20,U21,U22

: U23,U24 (Parity)

or

: SIMM at Bank 3 - low byte : SIMM at Bank 3 - high byte

(U5,U6, U11,U12, U17,U18, U23,U24 are parity bits used for data checking. In normal situations, those bits are not needed. Hence, the user can left those sockets blank and thus allowing you to minimize the system cost. Also see Jumper setting JP1.) You may install in each **Bank** either using DIP DRAMs or SIMMs. But do not install DIP DRAMs and SIMMs on the same Bank.

The switch setting SW1-SW4 for different memory configurations are listed below:

SUMMARY OF SYSTEM BOARD SETTINGS

DIP S	WITC	H SET	TING	TYP	ES OF RA	AMS INS	TALLEI	O INTERLEAVE MEMORY
1	2 3	3 4	BAI	NK0 I	BANK1	BANK2	BANK	3 FACTOR TOTAL
OFF	OFF	OFF	OFF	256K	. -	-	-	- 512KB
OFF	OFF	OFF	ON	256K	256K	-	-	2-WAY 1 MB
OFF	OFF	ON	OFF	256K	256K	256K	-	- 1.5MB
OFF	OFF	ON	ON	256K	256K	256K	256K	4-WAY 2 MB
OFF	ON	OFF	OFF^*	256K	64K	-	-	- 640KB
OFF	ON	OFF	ON	256K	256K	_	-	2-WAY 1 MB
OFF	ON	ON	OFF	256K	256K	1M	-	- 3 MB
OFF	ON	ON	ON	256K	256K	1M	1M	2-WAY 5 MB
ON	OFF	OFF	OFF	1M	-	-	-	- 2 MB
ON	OFF	OFF	ON	1M	1M	-	-	2-WAY 4 MB
ON	OFF	ON	OFF	1M	1M	1M	-	- 6 MB
ON	OFF	ON	ON	1M	1M	1M	1M	4-WAY 8 MB
ON	ON	OFF	OFF	1M	-	-	-	- 2 MB
ON	ON	OFF	ON	1M	1M	-	-	2-WAY 4 MB
ON	ON	ON	OFF	1M	1M	256K	-	- 4.5MB
ON	ON	ON	ON	1M	1M	256K	256K	2-WAY 5 MB

^{*} DIP SWITCH-5 should be OFF for all memory configuration except for 640KB memory configuration DIP SWITCH-6 - Reserved

Page/Interleave Memory

Memory access for OCTEK 286EMS is based on what is called a page/interleave arrangement. This means information stored in the memory subsystem is divided up, some of it going to one bank and some to another. This allows faster memory access but requires that banks operate in pairs, hence the physical organization of the memory system. In order to use the interleave option, banks on the memory cards must be filled in pairs. Any configuration of the memory system which results in less than 2 MB total memory will not take adavantage of the page/interleave function. Use of the Interleave feature will maximize the performance of the OCTEK 286EMS.

Interleave will enable a faster execution speed for the programs. There are two types of interleave - 2way interleave & 4way interleave.

2way interleave refers to interleave at Bank0 & Bank1 or at Bank2 & Bank3. But note that interleave is supported in Bank0 & Bank1 when the same type of memory (either 256K or 1M) is installed in the 2 Banks. Similarily, interleave is supported in Bank2 & Bank3 when the same type of memory is installed in the 2 Banks.

4way interleave refers to interleave at the 4 Banks. This is supported only when the 4 Banks are installed of the same type of memory (either 256K or 1M). Shadow RAM

If you have 1MB or more of memory installed it is possible to use a feature of the OCTEK 286EMS's chip set called "Shadow RAM". This feature allows the relocation of the contents of the ROM BIOS to a memory location in RAM above 640K. This feature increases overall system speed. Use of the Shadow Ram feature is optional if only 1MB of memory is installed. It must be used if more memory is present. Turning on the Shadow RAM feature is done by using a section of the extended setup program described in Software Setup.

2.3 Examples

Example 1:

Installation of 640KB memory using DIP DRAMs and SIMMs:

Switch Setting:

Bank 0 : 44256 x 4 pcs

: 41256 x 2 pcs

Bank 1 : SIMM 64KB x 2 pcs

Example 2:

Installation of 1MB memory using DIP DRAMs:

Switch Setting:

Bank 0 : 44256 x 4 pcs

: 41256 x 2 pcs

Bank 1 : 44256 x 4 pcs

: 41256 x 2 pcs

Example 3:

Upgrading the installation of Example 2 to 3MB memory using SIMMs:

Switch Setting:

Bank 0 : 44256 x 4 pcs

: 41256 x 2 pcs

Bank 1 : 44256 x 4 pcs

: 41256 x 2 pcs

Bank 2 : SIMM 1MB x 2 pcs

Example 4:

Installation of 640KB memory using SIMMs:

Switch Setting:

Bank 0 : SIMM 256KB x 2 pcs Bank 1 : SIMM 64KB x 2 pcs

Example 5:

Installation of 4MB memory using SIMMs:

Switch Setting:

Bank 0 : SIMM 1MB x 2 pcs Bank 1 : SIMM 1MB x 2 pcs

Example 6:

Upgrading the installation of Example 5 to 5MB memory using DIP DRAMs :

Switch Setting:

Bank 0 : SIMM 1MB x 2 pcs Bank 1 : SIMM 1MB x 2 pcs

Bank 2 : 44256 x 4 pcs

: 41256 x 2 pcs

Bank 3 : 44256 x 4 pcs

: 41256 x 2 pcs

Example 7:

Upgrading the installation of Example 5 to 8MB memory using 1MB SIMMs :

Switch Setting:

Bank 0 : SIMM 1MB x 2 pcs
Bank 1 : SIMM 1MB x 2 pcs
Bank 2 : SIMM 1MB x 2 pcs
Bank 3 : SIMM 1MB x 2 pcs

SECTION 3 SYSTEM BOARD JUMPER SELECTION

The mainboard jumpers allow the user to select the desired system configuration. The tables below shows the function and the default settings of these jumpers. Details of these jumpers will be discussed in the following sections. (There are also other jumpers in the mainboard, do not alter these jumper settings as this may affect the normal operation of the system.)

Jumper	Function
JP1	Parity enable/disable
JP3	BIOS ROM chip size selection
JP7	80287 co-processor clock rate selector
JP8	Display adapter selection

Default Settings

3.1 Parity Enable/Disable			
JP8	Open	(Monochrome)	
JP7	Pin 1,2 short	(80287 clock at 10MHz)	
JP3	Pin 1,2 short	(256K ROM BIOS)	
JP1	Pin 2,3 short	(Parity check enable)	

What is Parity?

Parity is a method for detecting errors in data communications. The parity bit is added at the end of data word. The value of this bit is a function of the rest of the data word. There are several ways that the parity bit can be calculated.

"Even parity" means that the parity bit is set so that the sum of all the bits in the data word (including the parity bit) is even.

"Odd parity" similarly means that the parity bit is set so that the sum of all the data bits in a word (including the parity bit) is odd.

"No parity" means that no parity bit is added to the end of a data word. For the OCTEK-286EMS System board, Memory Data Parity Check can either be enabled or disabled by altering the setting of jumper JP1.

When installing *DIP* type RAM chips; *U*5, *U*6, *U*11, *U*12, *U*17, *U*18, *U*23 and *U*24 are the DRAM chips for the parity bit. If data parity check is not desired, these sockets can be left blank; thus enabling the user to minimize the number of RAM chips installed for the system.

41256 DRAM chips are used for parity bits.

JP1 Setting	Parity Check
1-2	Disable
2-3	Enable

Refer to the following figure for the location of jumper JP1 and the appropriate setting:

3.2 ROM Configuration and Installation

The OCTEK 286EMS contains sockets for two BIOS EPROMs that can either be 27128 or 27256. Setting of jumper JP3 determines the ROM size and the type of ROM being used in the system board. Installation of the chips is explained in the table below. No matter what BIOS is used, the low-byte chip should be inserted in socket U27 and the high-byte chip in socket U28.

JP3	Type of	ROM chip installation		
Setting	BIOS	U27	U28	
J				
1-2	64KB size	27256	27256	
2-3	32KB size	27128	27128	

Refer to the following figure for the location of jumper JP3 and the appropriate setting: 3.3 80287 Numeric Processor Installation

If you use certain applications or programming languages, you may want to install a math co-processor to enhance the performance of you system. Be ware, however, that your application program must be specifically designed to take advantage of the math co-processor to benefit from its presence in the system.

The 80287 Numeric Processor operates in conjunction with the 80286 CPU and will enhance the system's math capabilities. To install the 80287, simply insert the LSI chip into the empty socket below the power connector.

Important

Each pin on this LSI has a unique function. The 80287 should therefore be inserted into the socket in the correct direction. If it is inserted incorrectly, the LSI or the computer may be damaged. Install the LSI correctly by referring to the illustration. Care should be taken not to bend and damage any of the pins. When inserting the LSI into the socket, apply force evenly over the LSI body.

3.4 80287 Co-processor Clock Rate Selector

The operating clock rate of the co-processor depends on the clock rating of the 80287 chip used. The co-processor's clock rate should match the clock rating of the 80287 chip to guarantee proper and stable operation. Jumper JP7 is used to select the desire clock source for the 80287 co-processor.

In order to ensure maximum flexibility in choosing 80287 chip, there is a oscillator socket (Y4) provided so that an external clock source for the co-processor is possible. If external clock source is desired, JP7 should be set to position 2-3, and an oscillator should be installed on the socket located at "Y4". Note that the oscillator's frequency should match that of the 80287 chip. In this way, the user can readily make use of 80287 chip of any clock rate. (Please refer to the following table for details.)

If on the other hand, the user wishes to used on-board clock source so that no external oscillator is needed (socket "Y4" could left blank), then jumper JP7 should be set to position 1-2. This setting would meant that a 80287-10 is required.

Setting	JP7 clock sour	80287 ce (external)	Oscillator required	(Y4)	Co-processor
	1-2	On-board	None 80287	-10	
	2-3 External	External 24 MHz	18 MHz 80287-8	80287-6	6

External 30 MHz 80287-10 Refer to the following figure for the location of jumper JP7 and the appropriate setting: 3.5 Display Adapter Settings

The OCTEK-286EMS system can work with various display monitors if provided with a suitable display adapter. Jumper JP8 is used to signal the system what type of display adapter is installed. If you want to use two monitors (a color monitor and a high-resolution monochrome monitor, for example), set the adapter type to the monitor you want to use when the system boots. Refer to the figure below for the location of JP8 and the appropriate setting:

JP8 Setting	Adapter Type
ON	Color Graphics Adapter or
	Enhanced Graphics Adapter
OFF	Monochrome Adapter
Refer to the foll	owing figure for the location of jumper JP8 and the appropriate setting :

SECTION 4 SYSTEM BOARD CONNECTOR

This section describes with details of the hardware features in the system board. You may find the information in this section useful. Under typical conditions, these connectors will have to connected to the indicators and switches of the system unit.

Connector	Function
P1	Hardware reset connector
P2	Speaker connector
Р3	Turbo switch connector
P4	Turbo LED connector
P5	Power LED and Ext-Lock connector
P6-P7	Power supply connector
P8	External battery connector
KB1 Pin assignments are as fol	Keyboard connector llows :

4.1 P1 - Hardware reset connector

A reset will restarts the computer from the RAM test stage. If this has been connected to the front panel of your system case, the button can be used to restart your computer without turning the power off. If you encounter any problems while using unfamiliar software, you can always restart from the beginning by pushing the restart button.

Pin	Assignments
1	Selection pin

4.2 P2 - Speaker connector

The speaker connector is a 4-pin, keyed, Berg strip.

Pin	Assignments
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

4.3 P3 - Turbo switch connector

The operating speed of the system board can be selected by the turbo switch setting. A speed switchover circuit ensures a smooth switchover between operating speeds, even during system operation. Also software selection via keyboard is also allowed if appropriate BIOS is used.

Hardware Select Mode:

The turbo switch changes operation mode between 16MHz and 8MHz. This setting determines the speed at which the processor runs after booting. If you have a hardware switch on your case panel, connect it to jumper P3. You then can push the hardware switch to enter either Normal mode or Turbo mode. (When the 2 pins are shorted, the system will operate at lower speed at boot up.)

The pin assignments are as follows:

Pin	Assignments
1	Select pin
2	Ground

Software Select Mode:

In addition to setting the processor clock speed by front-panel switch (Turbo switch), you can also change processor speed 'on-the-fly' via keyboard command. The OCTEK286EMS has speed switching circuitry allowing it to change speed during operation, even while you are running a program.

The system is default to run in high speed, but the operating mode can also be changed. You can toggle the operating speed between turbo mode and normal mode by pressing the following keys simultaneously:

The turbo LED light will light up to show whether your computer is now running in turbo mode or normal mode. When the Turbo LED is turned on, the system is in Turbo mode (16 MHz). If the Turbo LED is off, the system is in Normal mode (8 MHz).

4.4 P4 - Turbo LED connector

The turbo LED indicates operation in Turbo mode (16MHz). This is a 2-pin keyed, Berg strip (0.1") male pin connector.

Pin	Assignments
1	+5Vdc
2	LED signal

4.5 P5 - Power LED and Ext-Lock connector

The power LED indicates whether the power is on. The keylock is used to enable or disable the keyboard. By disabling the keyboard, the user ensures that anyone who does not have the key will be unable to use the computer. Unlocking the keylock enables the normal operation of the keyboard. If this is connected to the front panel of your case, a key provided with the case can be used to disable the keyboard.

The power LED and keylock connector is a 5-pin Berg strip. Its pin assignments are as follow:

Pin	Assignments
1	LED Power
2	Key

- Ground 3 Keyboard inhibit 4 Ground 4.6 P6, P7 - Power supply connector

	Pin	Assignments
P6:	1	Ground
	2	Ground
	3	-5 Vdc
	4	+5 Vdc
	5	+5 Vdc
	6	+5 Vdc
P7:	1	Power good
	2	+5 Vdc
	3	+12 Vdc
	4	-12 Vdc
	5	Ground
4 7 P8 - I	6 External b	Ground

4.7 P8 - External battery connector

This is for connecting four "AA" size batteries instead of using the on-board battery for the CMOS RAM. This batteries provides the same function as the on- board batteries.

Assignments Pin

4.8 KB1 (DIN con	nnector) - Keyboard connector
4	Ground
3	Ground
2	N/C
1	6 Vdc

The keyboard connector is a five-pin DIN 90-degree printed circuit board (PCB) mounting. The pin assignments are as follows:

Pin	Assignments			
1	Keyboard clock			
2	Keyboard data			
3	Spare			
4	Ground			
5	+5 Vdc			

5.1 System BIOS

All microcomputer systems use a Basic Input Output System. This is software that has been permanently recorded in a ROM (Read Only Memory) chip and functions as the basic point of communication between the system board and the rest of the computer.

The BIOS provides an operational interface to the system and relieve the programmer from worrying about the characteristics of hardware devices. Thus, hardware modifications and enhancements become transparent to user's programs, access to BIOS is through the program interrupts of the 80286 microprocessor. Each BIOS entry point is available through its own interrupt.

5.2 Power Up

Upon your turning on the power of your OCTEK286EMS system, the system will go through a self-test routine which checks all of its internal devices. Complete testings will be carried out on the CPU, base 640K RAM, extended RAM, ROM, system board, CMOS memory, video controllers, parallel and serial subsystems, floppy and fixed disk subsystems and the keyboard.

When the self-test is completed, the system will search for the DOS (disk operating system) system file in drive A. If no system diskette is put in drive A, it will check the fixed disk (if installed).

5.3 First Time Startup

If it is the first time that the computer is started up, you will need to configure the system by telling the SETUP program what hardware configuration your system contains.

5.4 Configuring your System

The AMI BIOS, in addition to the BIOS program itself, contains a setup program that is called up everytime the system boots up. This is called the SETUP. The SETUP program lets you specify your system's configuration of diskette drives, hard disk drives, video display, memory, and date and time. The AMI BIOS provides a one-screen interactive equipment and machine configuration setup. The SETUP can be run after the system has been turned on and the memory test is finished or has been escaped. The SETUP program is built-in, you do not need a diskette to use it.

If your OCTEK286EMS is already installed in a working system, you will not need to use the SETUP program unless the configuration already recorded in the on-board CMOS RAM is lost or a change is made in your system hardware configuration. If the information is lost due to loss of battery power, you will need to reenter the configuration. If the configuration is altered,

the changes must be recorded.

5.4.1 Memory Test Bypass

After the system is powered on or after a reset, the BIOS performs diagnostics of the system and displays the size of the memory being tested.

Note that you can bypass the memory test by pressing the **<ESC>** key. This option would be useful when the memory on the system is quite large. You may hit the **<ESC>** key when the message following message appears on the screen:

Press <ESC> Key to bypass MEMORY test

5.4.2 Running Setup

Follow the instructions as they come up on the screen to complete the procedure. The initial prompt on the screen tells you to press the **** key if you want to use the setup program. It is displayed briefly just after the RAM test is run when you first turn on the system. If it disappears before you have a chance to respond turn the system off and on again or reset the system and the message will reappear. The initial screen prompt will be similar to:

Press key if you want to run SETUP or DIAGS.

Hit **PEL**> key to get into the Setup Mode. (Note that **PEL**> key will get you into the setup mode, only when the above message is displayed on the screen.)

Upon your pressing of the **** key, the following message will appear on the screen:

EXIT FOR BOOT RUN CMOS SETUP RUN DIAGNOSTICS

Use <Up> and **<Down>** keys to highlight the selected item. Highlight **RUNCMOSSETUP** for the SETUP program and press the **<Return>** key to enter this option.

In a moment, the following SETUP menu will appear:

Once you have entered the SETUP menu, enter the date, time, the primary display type, the floppy drive installed and the hard disk drive type (if installed). See **Appendix1** for a printed list of hard disk drive types. The SETUP program will automatically determines your computer's memory configuration and displays it on the SETUP menu.

Use the **<Up>, <Down> , <Left>, <Right>,** and **Return** keys to move between options. The field shown in reverse video is the current field, which is the one the user may changes. Then use **<PgUp>** and **<PgDn>** keys to select the correct values.

After you have entered the correct values to all of the SETUP options, you may now exit the SETUP program. To do so, press **<ESC>** key to exit. The following message will then appear:

Write data into CMOS and exit (Y/N)?

Press **Y** to update the data and exit the SETUP program.

The computer now performs a cold boot (equivalent to turning the power off and back on again), performs the memory test, and then tries to boot from the disk drive. If your hard disk has not yet been initialized, be sure that you have a bootable DOS diskette in the A drive.

5.5 Running AMI BIOS Diagnostics

Following the above procedures until the following display is shown on the screen:

EXIT FOR BOOT RUN CMOS SETUP RUN DIAGNOSTICS

Use the <**Up>** & **<Down>** to move the highlight bar to select "**RUN DIAGNOSTICS**" and then press **<Enter>**. The following screen will then appear :

The AMI Utilities includes services for the hard disk, floppy, keyboard, video and miscellaneous. It provides an easy to operate screen-menu allowing inexperienced users to operate the program. Simply press

<Left> or <Right> and <Up> or <Down> keys to move the highlight bar the option desired.

SECTION 6 TECHNICAL INFORMATION

This section provides the technical materials about the OCTEK 286EMS system board. The information in this section is for reference, and is intended for advanced readers who needs to understand the basic design and operation of the OCTEK 286EMS system.

6.1 GC101/GC102/GC113 AT Chip Set

The GC101 Peripheral Controller is the heart of the three chip system and forms most of the control circuits and "glue" logic of the AT architecture in a single CMOS VLSI chip.

The GC101 performs CPU and peripheral support functions including the following:

- * All Peripheral Devices and Refresh Counters
- * All mega functions
 - -82284 Clock Generator
 - -82288 Bus Controller
 - -8254 Timer
 - -8259 Interrupt Controller (2)
 - -8237 DMA Controller

The GC102 may be configured as either an Address Buffer of Data Buffer by strapping one pin high or low. This chip replaces address buffer, data transceivers, memory drivers, parity generators and supporting circuitry. The chip is now used as a Data Buffer in the system.

GC102 Data Buffer provides:

- * Buffers and latches data for the CPU expansion bus and memory
- * Parity bit generation and checking
- * Slew rate controlled outputs

GC113 Advanced Memory Manager provides:

- * Page Mode and 2 or 4-Way Interleave support
- * Hardware support for EMS4.0
- * Support Shadow RAM for Video and System BIOS
- * Supports 256K or 1M DRAMs
- * Supports up to 8MB of on-board system memory

6.2 OCTEK 286EMS SYSTEM BLOCK DIAGRAM

6.3 Microprocessor

The 80286 is a high-performance microprocessor with a 16-bit external data path, up to 16 megabytes of directly addressable physical memory and up to one gigabyte of virtual memory space. The operating speed of the 80286 chip is 8 MHz in Normal mode and 16 MHz in Turbo mode.

The 80286 operates in two modes: protected virtual address and real address.

Virtual address mode

The virtual address mode provides a 1-gigabyte virtual address space mapped onto a 16 megabyte physical address space. Virtual address space is larger than physical address space, and the use of a virtual address that does not map to a physical address location will cause a restartable interrupt.

This mode uses 32-bit pointers that consist of a 16-bit selector and offset components. The selector specifies an index into a memory-resident table, and the 24 bit base address of the desired segment is obtained from the memory table. A 16-bit offset is added to the segment base address to form the physical address. The microprocessor automatically references the tables whenever a segment register is loaded with a selector. Instructions that load a segment register will refer to the memory-based tables without additional program support. The memory-based tables contain 8-byte values called descriptors.

Real address mode

In this mode, physical memory is a contiguous array of up to 1 megabyte. The selector portion of the pointer is interpreted as the upper 16 bits of a 20-bit address, and the remaining 4 bits are set to zero. This mode of operation is compatible with the 8088 and 8086.

Segments in this mode are 64KB in size and may be read, written or executed. An interrupt may occur if data operands or instructions attempt to wrap around the end of a segment. In this mode, the information contained in the segment does not use the full 64KB, and the unused end of the segment may be overlay by another segment to reduce physical memory requirements.

6.4 System Memory Map

6.5 I/O Address Map

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O. I/O Address Map on the I/O slots

I/O address hex 100 to 3FF are available on the I/O channel.

6.6 System Timers

The system has three programmable timer/ counters controlled by the timer/counter from the GC101 chip set and are defined as channels 0 through 2:

Note: Channel 1 is programmed to generate a 15-micro- second period signal.

The 8254 Timer/Counter is treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters, the fourth is a control register for mode programming.

6.7 System Interrupts

Sixteen levels of system interrupts are provided by the 80286 NMI and two 8259 Interrupt Controller within the GC101 chip set. The following shows the interrupt- level assignments in decreasing priority.

6.8 Direct Memory Access (DMA)

The system supports seven DMA channels. Two DMA Controller are included in the GC101, with four channels for each chip. The DMA channels are assigned as follows: The following shows the addresses for the page register.

6.9 Real Time Clock and CMOS RAM

The CMOS RAM Chip (146818) contains the real-time clock and 64 bytes of CMOS RAM, it keeps configuration information when power is off. Upon you turn the system power on, CMOS will load the recorded configuration into the system so that the system can function in the right track with the equipped components. However, if you haven't configured the CMOS, or the battery which supports the power to the CMOS is weaken, you need to redefine the necessary parameters whenever the system is booting up.

The program of the CMOS setting will be loaded into the system automatically from the subsystem named BIOS. The following table shows the CMOS RAM addresses. CMOS RAM Address Map



Note: The setup program initializes registers A, B, C, and D when the time and date are set. Also Interrupt 1A is the BIOS's interface to read/set the time and date. It initializes the status bytes the same as the setup program.

6.10 Math Coprocessor

The 80287 Math Coprocessor enables the Micro-286 system to perform high-speed arithmetic, logarithmic functions, and trigonometric operations with extreme accuracy.

The coprocessor works in parallel with the microprocessor. The parallel operation decrease operating time by allowing the coprocessor to do mathematical calculations while the microprocessor continues to do other functions.

The Mathematics Coprocessor, 80287 is treated as an I/O device through I/O port address hex 0F8, 0FA and 0FC. The microprocessor sends OP codes and operands through these I/O ports. The microprocessor also receives and stores results through the same I/O ports. The "BUSY" signal generated by the coprocessor signifies to the microprocessor to wait until the coprocessor has finished executing.

The following describe the mathematics coprocessor control ports:

0F0 The latched Mathematics Coprocessor busy signal can be cleared with an 8- bit, Out command, to port F0. The coprocessor will latch "BUSY", if it asserts its error signal. Data output should be zero.

0F1 The Mathematics Coprocessor will reset to real address mode which is in the 8087 compatible if an 8- bit Out command is sent to port F1. Again, the data output should be zero. **6.11 System Expansion Bus**

The Micro-286 provides drive for up to eight XT- compatible cards (six of which can be AT-compatible with the second connector)

The I/O channel supports:

- * I/O address space from hex 100 to hex 3FF
- * Selection of data access (either 8 or 16 bit)

- * 24 bit memory addresses (16MB)
- * Interrupts
- * DMA channels
- * Refresh of system memory from channel microprocessors

There are eight 62-pin (JA1-JA8) and six 36-pin (JB1- JB6) edge connector sockets for I/O channel adapter cards. In two positions, the 36-pin connector is not present. These positions can support only 62-pin I/O bus adapters.

The following figure shows the pin numbering for I/O channel connectors JA1 to JA8. The following figure shows the pin numbering for I/O channel connectors JB1-JB6.

The following table summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side, JA1-JA8)

I/O Channel (B-Side, JA1-JA8)

I/O Channel (C-Side JB1-JB6)

I/O Channel (D-Side JB1-JB6)

APPENDIX **Hard Disk Drives supported by AMI BIOS**

			Write	Landing	1		
	Type				Cylinde	ers Head Precomp Zone	Capacity
	1	306	4	128	305	10MB	
	2	615	4	300	615	21MB	
	3	615	6	300	615	31MB	
	4	940	8	512	940	64MB	
	5	940	6	512	940	48MB	
	6	615	4	None	615	21MB	
	7	462	8	256	511	31MB	
	8	733	5	None	733	31MB	
	9	900	15	None	901	115MB	
	10	820	3	None	820	21MB	
	11	855	5	None	855	36MB	
	12	855	7	None	855	51MB	
	13	306	8	128	319	21MB	
	14	733	7	None	733	44MB	
15	Reserv	ed					
	16	612	4	All	663	21MB	
	17	997	5	300	997	42MB	
	18	997	7	None	997	58MB	
	19	1024	7	512	1023	61MB	
	20	733	5	300	977	31MB	
	21	733	7	300	732	42MB	
	22	733	5	300	733	31MB	
	23	306	4	All	336	10MB	
	24	925	7	All	925	56MB	
	25	925	9	None	925	72MB	
	26	754	7	754	754	46MB	
	27	754	11	None	754	72MB	
	28	699	7	256	699	46MB	
	29	923	10	None	823	71MB	
	30	918	7	918	918	55MB	
	31	1024	111	None	1024	98MB	
	32	1024	15	None	1024	133MB	
	33	1024	5	1024	1024	44MB	
	34	612	2	128	612	10MB	
	35	1024	9	None	1024	80MB	
	36	1024	8	512	1024	71MB	
	37	615	8	128	615	42MB	
	38	987	3	987	987	25MB	
	39	987	7	987	987	60MB	

40	820	6	820	820	42MB
41	977	5	977	977	42MB
42	981	5	981	981	42MB
43	830	7	512	830	50MB
44	830	10	None	830	72MB
45	917	15	None	918	115MB
46	1224	15	None	1223	152MB

47 USER TYPE

SUMMARY OF SYSTEM BOARD SETTINGS

סום	WITC	H SFT	TING	TVDF	SOFR	AMS INS	TAIIFI	D INTE	RIFA	VE MEMORY
1	2 3			NK0 BA						TOTAL
•			<i>D</i> ₁ 1	11110 131	11 11 11	D1111112	<i>D</i> ₁ 11 (1)	111010	51 0	101111
OFF	OFF	OFF	OFF	256K	-	-	-	- 512	2KB	
OFF	OFF	OFF	ON	256K	256K	-	-	2-WAY	1 N	1 B
OFF	OFF	ON	OFF	256K	256K	256K	-	-	1.5M	В
OFF	OFF	ON	ON	256K	256K	256K	256K	4-WAY	2	MB
OFF	ON	OFF	OFF*	256K	64K	-	-	- 64	40KB	
OFF	ON	OFF	ON	256K	256K	-	-	2-WAY	1 N	
OFF	ON	ON	OFF	256K	256K	1M	-		3 M	
OFF	ON	ON	ON	256K	256K	1M	1M	2-WAY	5	MB
								_		
ON	OFF	OFF	OFF	1M	-	-	-		MB	
ON	OFF	OFF	ON	1M	1M	-	-	2-WAY	4 N	
ON	OFF	ON	OFF	1M	1M	1M	-		6 M	
ON	OFF	ON	ON	1M	1M	1M	1M	4-WAY	8	MB
	_									
ON	ON	OFF	OFF	1M	-	-	-		MB	
ON	ON	OFF	ON	1M	1M	-	-	2-WAY	4 N	
ON	ON	ON	OFF	1M	1M	256K		-	4.5M	
ON	ON	ON	ON	1M	1 M	256K	256K	2-WAY	5	MB
****	DED	D'		.						
JUM	PEK	Pin		Funct	10 n					
JP1	1 7	Dari	ty chocl	z dicable						
JPI	1,2									

2,3 Parity check enable JP3 1,2 256K ROM BIOS 2,3 128K ROM BIOS JP7 1,2 Fixed 80287 clock rate; use 80287-10 2,3 User defined 80287 clock rate (Oscillator required at location "Y4")

JP8 short CGA, EGA or VGA mode open Monochrome mode

Connector	Function
P1	Hardware reset connector
P2	Speaker connector
P3	Turbo switch connector
P4	Turbo LED connector
P5	Power LED and Ext-Lock connector
P6-P7	Power supply connector
P8	External battery connector
KB1	Keyboard connector

^{*} DIP SWITCH-5 should be OFF for all memory configuration except for 640KB memory configuration DIP SWITCH-6 - Reserved

OCTEK 286EMS SYSTEM BOARD LAYOUT EMS Driver Version 4.00 Description

There is an EMS Driver Diskette that came with the motherboard. This EMS Memory Manager will conform to version 4.00 of the Lotus/Intel/Microsoft (LIM) expanded memory specification. Version 4.00 of the LIM specification is upward compatible with version 3.20 and will run programs written for that version of the memory manager.

This version of the Memory Manager supports both standard EMS and the Enhanced EMS (EEMS) types of expanded memory to allow multi-tasking.

<u>The memory manager should be installed in the CONFIG.SYS file as the first driver</u>. This allows other device dirvers, such as the ramdisk, to make use of the memory manager's services. After being loaded, the memory manager will determine the amount of expanded memory in the system and perform any required initialization. The syntax for installation of the memory manager is shown below.

device = MM.SYS [/Handles=nnn] [/Contexts=nnn] [/Depth=nn] [/Start=xxxx] [/Xclude=xxxx-xxxx] [/L=xxxx-xxxx] [/Address=xxx] [/M=nnnn] [/Test]

The numeric parameters for the memory manager should be specified in decimal except where specically noted otherwise. Memory sizes should be specified in K (1024) bytes without the K on the end of the number. 32,767 bytes would be specified as 32. Only the first character of the parameter is significant. For example "/D=" may be substituted for "/Depth=".

All of the parameters noted above are optional. Default values for each will be selected if the parameter is not specified. Below is a description of each of the memory manager's parameters.

OPTION PARAMETERS FOR THE LIM MEMORY MANAGER

This document provides information on the option parameters for the LIM memory manager by Quadtel. The format of this document is as follows:

- 1) General information
- 2) Individual discussion of the different option parameters

GENERAL INFORMATION:

HARDWARE OPTION PARAMETERS AND MEMORY MANAGER OPTION PARAMETERS:

There are two different types of option parameters: the hardware option parameters and the memory manager option parameters. The format for the two types is identical so the user does not usually need to be concerned with this distinction. However, there is one important item to note: if a hardware option parameter and a memory manager option parameter have the same name, the HARDWARE interpretation wins out. Hence any naming conflicts cause the memory manager to effectively lose an option.

SPECIFICATION OF NUMBERS:

In the next section on the discussion of the option parameters, the following formats will be used for representing numbers:

Symbol Meaning

dd a single byte decimal value:[0-255]
dddd a single word decimal value:[0-65535]
xx a single byte hex value: [00-FF]
xxxx a single word hex value: [0000-FFFF]

OPTION PRAMETERS:

HARDWARE OPTION PARAMETERS:

/A = xxxx

Sets the base I/O address of the EMS controller (GC103 only) e.g. /A=02E8 the base I/O address is at 02E8

Note: No test is done at the time this option is entered to verify the a controller chip does indeed exist at this I/O address. However, the initialization routines performed later will fail if this is not a controller address.

/M = dddd

Tells the memory manager how many kilobytes of extended memory can be used for EMS

memory. This value is rounded UP to the next multiple of 16. If /M is not used, or /M=0 is entered, then NO extended memory is allocated as EMS memory. This parameter overrides the amount of EMS memory specified by setup.

e.g. /M=384 EMS can use 384K of available memory

/M=120 EMS can use 128K of available memory

Note: No test is done at the time this option is entered to verify that EMS has at least the amount of memory specified.

MEMORY MANAGER OPTION PARAMETERS:

/C=dddd

Sets the number of contexts that EMS can save. The number of contexts must lie in the range [3,255].

e.g. /C=8 8 contexts can be saved simultaneously

D=dd

Sets the depth of a context (number of registers) that can be saved. The context depth must lie in the range [1,32].

e.g. /D=12 Each stack frame can hold 12 registers.

/H=dddd

Sets the maximum number of handles the manager will have open at any time. This number must lie in the range [3,255].

e.g. /H=128 128 handles can be open at one time.

/I = xxxx - xxxx

Excludes the specified I/O range from the scan. The start address range must be less than the end address range or an error will be generated.

e.g. /I=03D0-03D9 I/O 3D0-3D9 is excluded.

/X = xxxx - xxxx

Sets an address range which should be EXCLUDED from EMS paging. The exclusion option can be used to prevent special RAM sections from being banked out. The memory manager will automatically exclude address ranges for ROM and standard video cards; these do not need to be specified. Both of the addresses entered are considered to be paragraph addresses. The addresses will be rounded UP to the next multiple of 1K, unless they are already a multiple of 1K. The second value must be larger than the first or an error will occur.

e.g. /X=A000-A800 Excludes A0000-A8000 from paging

e.g. /X=4015-5000 Excludes 44000-50000 from paging

/L = xxxx - xxxx

Sets an address range which should be INCLUDED in EMS paging. The addresses are interpreted exactly as in the $\!\!/\!X$ exclude option parameter.

e.g. /L=3800-4200 Includes 38000-42000 in paging

/S = xxxx

Sets the start of page frame address. This is the address at which EMS pages will appear as they are mapped in. It is often referred to as the EMS window. The address is interpreted exactly as in the /X exclude option parameter and it must be less than E000.

e.g. /S=9000 Sets the page frame address to 90000

/F

Full display option. This option causes the status of the memory manager to be displayed. e.g. $\slash\!F$

/N

Specifies that non-volatile and display memory can be used by the EMS memory manager. e.g. $\ensuremath{/N}$

/V

Specifies that only volatile memory is to be used by the EMS memory manager.

e.g./V

T

Enables a pattern test and two different types of address tests to be performed on the memory during the memory manager initialization.

e.g./T

/Z

Disables memory testing during initialization.

e.g./Z

CHKMEM

A utility called CHKMEM is provided which will display the amount of allocated system and expanded memory. Simply type CHKMEM from the DOS prompt and then press ENTER. If the "/A" optional parameter is used, all of the allocated handles will be displayed with their respective names and sizes.