Advanced/ML Motherboard Specification Update

Release Date: August 1997

Order Number: 281814-014

The Advanced/ML motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Advanced/ML motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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REVISION HISTORY

Date of Revision	Version	Description
May 1996	-001	This document is the first Specification Update for the Intel Advanced/ML motherboard.
June 1996	-002	Added Errata 2-5 and Documentation Changes 1-2.
July 1996	-003	Added Documentation Changes 3-4.
September 1996	-004	Added Documentation Changes 5-7.
October 1996	-005	Added Documentation Change 8.
November 1996	-006	Added Errata 6-7 and Updated Erratum 4.
December 1996	-007	Added Errata 8-9.
January 1997	-008	Added Specification Change 1, Erratum 10 and PBA/BIOS Table.
February 1997	-009	Added Documentation Change 9.
March 1997	-010	Added AA Revision to Motherboard Identification table. Revised format of PBA/BIOS revision table. Added Erratum 11 and Documentation Change 10. Updated Errata 1 and 2. Updated Documentation Change 2 and 8.
April 1997	-011	Added Documentation Change 11.
June 1997	-012	Updated Errata 7 and 11. Added Specification Clarification 1.
July 1997	-013	Added Specification Clarification 2 and Documentation Changes 12-14.
August 1997	-014	Added Specification Clarification 3 and Documentation Change 15.

PREFACE

This document is an update to the specifications contained in the *Advanced/ML Motherboard Technical Product Specification* (Order Number 281806). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium processor. Items contained in the *Pentium Processor Specification Update* that either do not apply to the Advanced/ML motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430HX PCIset Specification Update* (Order Number 297652) for specification updates concerning the 82430HX PCIset. Items contained in the *82430HX PCIset Specification Update* that either do not apply to the Advanced/ML motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82371SB PIIX3 Specification Update* (Order Number 297658) for specification updates concerning the 82371SB PIIX3. Items contained in the *82371SB PIIX3 Specification Update* that either do not apply to the Advanced/ML motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the Advanced/ML motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for Advanced/ML Motherboards

GENERAL INFORMATION

Basic Advanced/ML Motherboard Identification Information

AA Revision	PBA Revision	82430HX PCIset Stepping	BIOS Revision	Notes
654950-202	654951-202	A1	1.00.01.DB0	1, 2 ,3, 4, 11
654950-203	654951-203	A1	1.00.03.DB0	1, 2, 3, 4, 11
654950-204	654951-204	A1	1.00.03.DB0	1, 5, 6, 7, 11
654950-205	654951-205	A1	1.00.05.DB0	1, 5, 6 ,7, 11
654950-206	654951-206	A3	1.00.06.DB0	1, 8, 9, 10, 11
654950-207	654951-207	A3	1.00.07.DB0	1, 8, 9, 10, 11
654850-202	655038-202	A1	1.00.01.DB0	1, 2, 3, 4, 11
654850-203	655038-203	A1	1.00.03.DB0	1, 2, 3, 4, 11
654850-204	655038-204	A1	1.00.03.DB0	1, 5, 6, 7, 11
654850-205	655038-205	A1	1.00.05.DB0	1, 5, 6, 7, 11
654850-206	655038-206	A3	1.00.06.DB0	1, 8, 9, 10, 11
654850-207	655038-207	A3	1.00.07.DB0	1, 8, 9, 10, 11

NOTES:

1. The PBA number is found on a small label on the component side of the board.
2. The 82430HX PCIset kit used on this PBA revision consists of two different components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A1	SU087
82371SB	A1	SU052

3. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
4. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision: 2-12. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.

5. The 82430HX PCIset kit used on this PBA revision consists of two different components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A1	SU087
82371SB	B0	SU093

6. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
7. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision: 1-7. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
8. The 82430HX PCIset kit used on this PBA revision consists of two different components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A3	SU115
82371SB	B0	SU093

9. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
10. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision: 1-7. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
11. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the Advanced/ML motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71-79, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update.*

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Advanced/ML motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Only 256 KB pipeline burst SRAM cache supported
NO.	**PLANS**	**ERRATA**
1	Fixed	ECC non-detection of single/double bit errors on partial memory writes
2	Fixed	BIOS SETUP does not recognize February 29, 2000 as a valid date
3	Fixed	System BIOS does not recognize certain dates as valid
4	Fixed	PCI Delayed Transactions are not supported
5	Fixed	System BIOS may detect memory in unpopulated SIMM* rows
6	Fixed	BIOS Setup reports incorrect OverDrive® processor speed
7	Fixed	BIOS does not support no-emulation mode for CD-ROM boot
8	Fixed	DMA channel will be unavailable in Enhanced Parallel Port (EPP) Mode
9	Fixed	CMOS checksum may be lost if power is cycled during boot
10	NoFix	Video capture card may hang system due to improper TRST# signal
11	NoFix	Slave on secondary IDE channel is not disabled
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	PCI 2.1 Specification optional features
2	Doc	Administrator and user passwords
3	Doc	Power supply considerations
NO.	**PLANS**	**DOCUMENTATION CHANGES**
1	Doc	Remove repeated phrase
2	Doc	Addition of “VESA* Video Power Down” section
3	Doc	Change missing form factor dimension shown in section 1.3, Figure 2 as “?.?” to “3.100”
4	Doc	Add power consumption table to section 1.13
5	Doc	In Section 1.1, “Overview”, 200 MHz will be added to the list of processor speeds supported

NO.	PLANS	DOCUMENTATION CHANGES
6	Doc	In Section 1.4, “Microprocessors”, 200 MHz will be added to the list of processor speeds supported
7	Doc	Addition of jumper settings for 200 MHz processors
8	Doc	Revision of Motherboard Configuration jumper settings
9	Doc	Revision of Section 3.12.8.6, “Memory Error Correction”
10	Doc	Revision of Section 1.8, “Motherboard Connectors”
11	Doc	Revision of Section 1.5.1, “Second Level Cache”
12	Doc	Revision of Section 1.10.3, “Clear CMOS (J7K1-A, Pins 4,5,6)”
13	Doc	Revision of Section 1.6.1, “82439HX Xcelerated Controller (TXC)”
14	Doc	Revision of Section 1.9, “Add-In Board Expansion Connectors”
15	Doc	Addition of “Power Supply Considerations” section

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
654951-202	1.00.01.DB0	1-6, 8-11
	1.00.02.DB0	1, 4-6, 8-11
	1.00.03.DB0	1, 4, 6, 8-11
	1.00.04.DB0	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11
654951-203	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0	1, 4, 6, 8-11
	1.00.04.DB0	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11

PBA Revision	BIOS Revision	Errata That Apply
654951-204	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0	1, 4, 6, 8-11
	1.00.04.DB0	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11
654951-205	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0‡	1, 4, 6, 8-11
	1.00.04.DB0‡	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11
654951-206	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0‡	1, 4, 6, 8-11
	1.00.04.DB0‡	1, 4, 8-11
	1.00.05.DB0‡	1, 4, 8-11
	1.00.06.DB0	1, 8-11
	1.00.07.DB0	10-11
	1.00.08.DB0	10-11
654951-207	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0‡	1, 4, 6, 8-11
	1.00.04.DB0‡	1, 4, 8-11
	1.00.05.DB0‡	1, 4, 8-11
	1.00.06.DB0‡	1, 8-11
	1.00.07.DB0	10-11
	1.00.08.DB0	10-11

PBA Revision	BIOS Revision	Errata That Apply
655038-202	1.00.01.DB0	1-6, 8-11
	1.00.02.DB0	1, 4-6, 8-11
	1.00.03.DB0	1, 4, 6, 8-11
	1.00.04.DB0	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11
655038-203	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0	1, 4, 6, 8-11
	1.00.04.DB0	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11
655038-204	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0	1, 4, 6, 8-11
	1.00.04.DB0	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11
655038-205	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 8-11
	1.00.03.DB0‡	1, 4, 6, 8-11
	1.00.04.DB0‡	1, 4, 8-11
	1.00.05.DB0	1, 4, 8-11
	1.00.06.DB0	1, 4, 8-11
	1.00.07.DB0	1, 4, 10-11
	1.00.08.DB0	1, 4, 10-11

PBA Revision	BIOS Revision	Errata That Apply
655038-206	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 811
	1.00.03.DB0‡	1, 4, 6, 8-11
	1.00.04.DB0‡	1, 4, 8-11
	1.00.05.DB0‡	1, 4, 8-11
	1.00.06.DB0	1, 8-11
	1.00.07.DB0	10-11
	1.00.08.DB0	10-11
655038-207	1.00.01.DB0‡	1-6, 8-11
	1.00.02.DB0‡	1, 4-6, 811
	1.00.03.DB0‡	1, 4, 6, 8-11
	1.00.04.DB0‡	1, 4, 8-11
	1.00.05.DB0‡	1, 4, 8-11
	1.00.06.DB0‡	1, 8-11
	1.00.07.DB0	10-11
	1.00.08.DB0	10-11

NOTE:

‡ This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Advanced/ML Motherboard Technical Product Specification* (Order Number 281806). All Specification Changes will be incorporated into a future version of that specification.

1. Only 256 KB Pipeline Burst SRAM Cache Supported

The motherboard will only support 256 KB of pipeline burst SRAM as a second level cache. References to 512 KB of pipeline burst SRAM will be removed from Section 1.2, Motherboard Manufacturing Options and Section 1.6.1, 82439HX Xcelerated Controller (TXC).

ERRATA

1. ECC Non-detection of Single/Double Bit Errors on Partial Memory Writes

PROBLEM: When the 82439HX TXC performs a partial write to main memory (data less than a 64-bit quadword) in ECC mode, single bit errors are corrected but not logged. Double bit errors are not detected or logged.

IMPLICATION: Normally, the controller is able to buffer writes and group them into quadwords. In all these cases where 64 bits are written to memory at a time, both single and double bit errors will be signaled to the operating system. Single bit errors will be corrected using the information contained in the checkbits that are stored with the data in memory. Double bit errors cannot be corrected by the memory controller, but the operating system can warn the user that the error has occurred.

If the controller must perform a partial write, a read-merge-write cycle will occur so that the proper checkbits can be regenerated across the entire 64 bits to be written into DRAM. If erroneous data is read during this cycle, the following will occur:

For single bit errors, the error will be corrected based on the memory checkbits. The corrected data will be written back to memory, but the error will not be flagged to the system, so the user will not receive information from the error log that could be useful in isolating a failing memory module.

For double-bit errors, no error will be detected or signaled to the operating system. The erroneous data will be rewritten to memory and a set of regenerated checkbits will be rewritten at the same time, marking the erroneous data as correct.

WORKAROUND: None. However, for ECC systems that require only single bit error protection, the A1 stepping of the 430HX PCIset does provide this level of reliability.

STATUS: This erratum was fixed in PBA revision 654951-206 and 655038-206 when used with BIOS revision 1.00.07.DB0.

2. BIOS SETUP Does Not Recognize February 29, 2000 As a Valid Date

PROBLEM: The BIOS Setup program will not allow the system date to be set to Feb 29, 2000.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: If the system BIOS has not been upgraded, the system date will have to be reset to the correct date on March 1, 2000.

STATUS: This erratum was fixed in BIOS revision 1.00.02.DB0.

3. System BIOS Does not Recognize Certain Dates As Valid

PROBLEM: If the motherboard is powered on or reset with the system date set to October 20-31 or December 20-31, the system BIOS will report “CMOS Time and Date Not Set” and the system date will be reset to Jan 01, 1990 during Power On Self Test (POST). If the user resets the system to the correct date and reboots, the system BIOS reports the same error message and again resets the date to Jan 01, 1990.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.02.DB0.

4. PCI Delayed Transactions Are Not Supported

PROBLEM: An erratum to the A1 stepping of the 82371SB PCI ISA IDE Xcelerator (PIIX3) requires that the option for Delayed Transactions be turned off by the BIOS.

IMPLICATION: System level performance and compatibility are not affected by turning off delayed transactions. The system will be PCI 2.1 compatible and will support all PCI 2.1 compliant cards.

WORKAROUND: None.

STATUS: This erratum was fixed in PBA revision 654951-206 and 655038-206 when used with BIOS revision 1.00.06.DB0.

5. System BIOS May Detect Memory In Unpopulated SIMM Rows*

PROBLEM: During Power-On Self Test (POST), the system BIOS may improperly determine that memory is present in an unpopulated SIMM* bank. Subsequently, the BIOS memory sizing algorithm may fail to reflect the correct total memory configuration.

IMPLICATION: If memory is falsely detected in the first SIMM bank (Bank 0), a POST error (code E8h) will be generated and the system will not boot. No sizing problems have been observed in cases where memory is falsely detected in a higher numbered SIMM bank and the lowest numbered bank is populated.

WORKAROUND: Install SIMMs in consecutive banks beginning with Bank 0.

STATUS: This erratum was fixed in BIOS revision 1.00.03.DB0.

6. BIOS Setup Reports Incorrect OverDrive® Processor Speed

PROBLEM: The BIOS Setup program reports the speed of a 166 MHz OverDrive® processor as 200 MHz.

IMPLICATION: The BIOS Setup program display is incorrect. The OverDrive processor on the motherboard operates at 166 MHz.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.04.DB0

7. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an “El Torito” bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum was fixed in a BIOS revision 1.00.08.DB0.

8. DMA Channel Will Be Unavailable in Enhanced Parallel Port (EPP) Mode

PROBLEM: When Enhanced Parallel Port (EPP) is selected as the parallel port type in the BIOS Setup program, a DMA channel resource is allocated to the parallel port even though none is required.

IMPLICATION: The DMA channel used by the parallel port will not be available for use by other devices.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.07.DB0.

9. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte is not updated. The next time the computer is turned on, the message “CMOS Checksum Invalid” will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

Date and Time Not Set
Press <F1> for Setup, <Esc> to Boot

is displayed, the user must reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.07.DB0.

10. Video Capture Card May Hang System Due to Improper TRST# Signal

PROBLEM: If a PCI add-in card that implements boundary scan is installed, the computer may not boot. In accordance with the PCI 2.1 specification, the add-in card expects the TRST# signal to be pulled down if JTAG is not supported by the motherboard. The motherboard does not implement JTAG boundary scan and does not pull the TRST# signal down.

IMPLICATION: The computer may not boot if a PCI card that implements JTAG boundary scan is inserted.

WORKAROUND: None. PCI add-in cards that implement JTAG boundary scan are not compatible with this motherboard.

STATUS: This erratum will not be fixed.

11. Slave on Secondary IDE Channel Is Not Disabled

PROBLEM: If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.
- ATAPI device attached as slave to the secondary IDE connector.

IMPLICATION: In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Advanced/ML Motherboard Technical Product Specification* (Order Number 281806). All Specification Clarifications will be incorporated into a future version of that specification.

1. PCI 2.1 Specification Optional Features

The following will be added to section 1.9, Add-in Board Expansion Connectors:

The following optional features in the PCI 2.1 Specification are not implemented on the Advanced/ML motherboard:

- Cache Support Pins **SBO#** and **SDONE** (Section 2.2.7)
- **PRSNTx#** (Section 2.2.8)
- **CLKRUN#** (Section 2.2.8)
- 64 Bit Bus Extension Pins (Section 2.2.9)
- 66 MHz support (Section 2.2.8)
- JTAG/Boundary scan (Section 2.2.10)

2. Administrator and User Passwords

The following will be added to Section 3.12.12, Security Screen Options:

If an administrator password has been set, but no user password has been set, a user can create a password by entering BIOS Setup at boot by pressing the <F1> key and pressing enter at the administrator password prompt. Once in BIOS Setup, a user will be able to create a new user password.

Once defined, a user password can be cleared by either defining a new user password in Setup, or by moving the Password Clear jumper (J7K1-A) on the motherboard. See Section 1.10.4, Password Clear Jumper for more information on how to use this jumper.

3. Power Supply Considerations

The Advanced/ML motherboard has been designed to be configured in a system that uses a power supply that complies with the recommendations of ATX Specification Version 2.01. See Documentation Change 15 for the specific recommendations that must be met by a power supply for the motherboard.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Advanced/ML Motherboard Technical Product Specification* (Order Number 281806). All Documentation Changes will be incorporated into a future version of the appropriate Advanced/ML motherboard documentation.

1. Remove Repeated Phrase

IDE support section 1.6.3 which reads “PIO Mode 4 PIO Mode 4” should be changed to read “PIO Mode 4”.

2. Addition of VESA Video Power Down Section*

The following text will be added between sections 3.12.9.2 and 3.12.9.3. All corresponding sections will be renumbered as appropriate.

VESA VIDEO POWER DOWN

Sets the command issued to the video system when the computer goes into power management mode. The options are:

- Disabled
- Standby
- Suspend
- Sleep (**default**)

3. Refer to Summary Table of Changes

4. Power Consumption

The system configuration listed in section 1.13 should be listed as follows: a 133 MHz Pentium® Processor, 16 MB EDO RAM, 256 KB PBSRAM cache, 3.5-inch floppy drive, 1.6 GB IDE hard drive, 6X IDE CD-ROM, and S3* Trio64* V+ PCI graphics card running at the DOS prompt.

Table 5 in section 1.13 should be replaced with the following:

Table 5. Power Usage

		DC (amps)			
	AC (watts)	**+5 V**	**-5 V**	**+12 V**	**-12 V**
No APM enabled					
Windows* 95	43	3.27	0	.01	.01
APM Enabled					
Windows 95	28.2	1.32	0	.01	.01

5-6. Refer to Summary Table of Changes

7. Addition of Jumper Settings for 200 MHz Processors

Table 2, CPU/SYSTEM Speed Settings, will be replaced in its entirety as follows:

Table 2. CPU/SYSTEM Speed Settings

CPU Freq. (MHz)	Host Bus Freq. (MHz)	J7K1-C	K7K1-D	CPU Clock Multiplier
200	66	1-2,5-6	1-2,5-6	3
166	66	1-2,5-6	2-3,5-6	2.5
150	60	2-3,4-5	2-3,5-6	2.5
133	66	1-2,5-6	2-3,4-5	2
120	60	2-3,4-5	2-3,4-5	2
100	66	1-2,5-6	1-2,4-5	1.5
90	60	2-3,4-5	1-2,4-5	1.5
75	50	2-3,5-6	1-2,4-5	1.5
reserved	-	2-3,5-6	1-2,5-6	-
reserved	-	2-3,4-5	1-2,5-6	-

8. Revision of Motherboard Configuration Jumper Settings

Section 1.10.1, Table 1, Configuration Jumper Settings will be replaced in its entirety as follows:

Table 1. Configuration Jumper Settings

Function	Jumper	Configuration
CMOS Clear	J7K1-A	4-5 Keep (**Default**) 5-6 Clear
Password Clear	J7K1-A	1-2 Password Enabled (**Default**) 2-3 Password Clear/Disabled
CMOS Setup Access	J7K1-B	* 1-2 Access Allowed (**Default**) 2-3 Access Denied
VRE/OVD	J7K1-B	4-5 OVD/Standard [3.3-3.465 V] (**Default**) 5-6 VRE [3.4-3.6 V] **CAUTION: This jumper should not be changed unless changing to a new processor type.**

9. Revision of Section 3.12.8.6, Memory Error Correction

The section title will be changed and the section will be replaced in its entirety as follows:

MEMORY ERROR DETECTION

Sets the type of error detection or correction. This field appears if either ECC or Parity system memory is detected. Parity and ECC memory may be configured to run either as Parity or ECC (parity memory may be configured to run in ECC mode). The options are:

- Disabled **(default)**
- ECC
- Parity

10. Revision of Section 1.8, Motherboard Connectors

The PCI IDE connectors shown in figure 3, Motherboard Connector Locations will be re-labeled as follows.

- The PCI IDE connector on the outside edge of the board will be renamed from “Secondary” to “Primary”.
- The PCI IDE connector on the inside of the board near the SIMM* connectors will be renamed from “Primary” to “Secondary”.

11. Revision of Section 1.5.1, Second Level Cache

This section will be replaced in its entirety as follows:

Manufacturing options for second-level (L2) cache are no cache, 256 KB, or 512 KB direct-mapped, write-back cache. The L2 cache is contained in two global write enable (GWE) pipeline burst SRAM (PBSRAM) devices soldered to the motherboard. An 8 Kbit x 8 external Tag SRAM provides caching support for the first 64 MB of main memory. There are no upgrade options.

12. Revision of Section 1.10.3, Clear CMOS (J7K1-A, Pins 4,5,6)

This section will be replaced in its entirety as follows:

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the system on. When the system reports that “NVRAM cleared by jumper”, the system can be turned off, and the jumper should be returned to the 4-5 position to restore normal operation. Default is for this jumper to be on pins 4-5.

Caution: This procedure should only be done if, after a BIOS update, the system does not boot to a point where BIOS Setup can be entered or if, after CMOS default settings have been restored from within the Setup program, the system does not boot to the operating system.

13. Revision of Section 1.6.1, 82439HX Xcelerated Controller (TXC)

The fourth bullet in this section will be replaced in its entirety as follows:

- Fully synchronous PCI bus interface
  - — 25/30/33 MHz
  - — PCI to DRAM data transfers up to or greater than 100 MB/sec
  - — Up to 4 PCI masters in addition to the PIIX3

14. Revision of Section 1.9, Add-In Board Expansion Connectors

The text in the first paragraph of this section will be replaced in its entirety as follows:

The motherboard Expansion Slots support up to four bus mastering PCI and up to three ISA add-in boards. One of the PCI slots may be shared with an ISA slot.

15. Addition of Power Supply Considerations Section

The following section will be added between 1.13 and 1.15. All corresponding sections will be renumbered as appropriate.

For typical configurations, the motherboard is designed to operate with at least a 200 W power supply that complies with version 2.01 of the ATX Specification. A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must comply with the following recommendations found in the indicated sections of that specification:

- The potential relation between 3.3VDC and +5VDC power rails (Section 4.2)
- The current capability of the +5VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)