Intel Embedded Processor Module

EMBMOD133 and EMBMOD166

Preliminary Datasheet

Product Features

- Intel Pentium® Processor with Voltage Reduction Technology with internal/bus frequency of 133/66 MHz (EMBMOD133)
- Intel Mobile Pentium® Processor with MMX™ Technology with internal/bus frequency of 166/66 MHz (EMBMOD166)
- Processor (host) reference and PCI clock generation
- Voltage regulation supports processor core input voltage of 2.9 V (EMBMOD133) or 2.45 V (EMBMOD166)
- Passive heat sink and Tape Carrier Package (TCP) lead cover attached
- Integrates Intel 82439HX System Controller (TXC)
  - PCI 2.1 compliant
  - Integrated second-level cache controller
  - Integrated DRAM controller
  - Optional parity
  - Optional error checking and correction

The Intel Embedded Processor Module is a fundamental building block for the embedded system designer. The Intel Embedded Processor Module incorporates an Intel Pentium® processor, a 256-Kbyte (EMBMOD133) or 512-Kbyte (EMBMOD166) second-level cache, an Intel 430HX PCIset 82439HX System Controller (TXC), a clock generator and a voltage regulator on a single printed circuit board.

Notice: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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Preliminary Datasheet

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1.0 Introduction

The Intel Embedded Processor Module is a fundamental building block for the embedded system designer. The Intel Embedded Processor Module incorporates an Intel Pentium® processor, a 256-Kbyte or 512-Kbyte second level cache, an Intel 430HX PCIset 82439HX System Controller (TXC), a clock generator and a voltage regulator on a single printed circuit board.

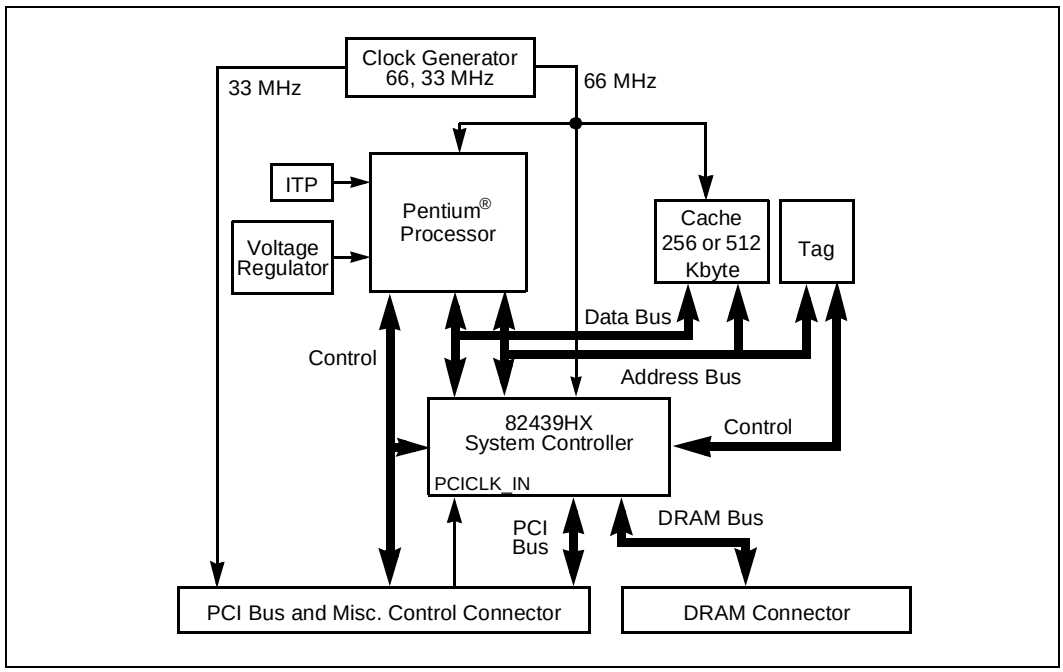
Intel's PCIset architecture allows for physical partitioning at both the PCI and DRAM interface. Therefore the electrical interconnect defined for the Intel Embedded Processor Module includes the PCI bus, DRAM memory bus and some additional PCI sideband signals. An on-board voltage regulator provides the DC conversion from the system DC voltage to the processor's core voltage.

Building around the modular design gives the embedded system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards
- No requirement for manufacturing capabilities on the Tape Carrier Package (TCP) processors
- Faster Time to Market
- Future modules provide an upgrade path using a standard interface

The 430HX PCIset consists of two VLSI devices: the 82439HX System Controller (TXC), and the 82371SB PCI ISA IDE Xcelerator (PIIX3). The system manufacturer's motherboard which connects to the module must include the PIIX3 device.

Figure 1. Intel Embedded Processor Module Block Diagram



1.1 Related Documents

Table 1. Related Documents

Document Name	Order Number
Intel Packaging Handbook	240800
AP-757, Embedded Processor Module Design Guide	273120
AP-759, Embedded Processor Module Thermal Design Guide	273143
Pentium® Processor with Voltage Reduction Technology at 75/100/120/133/150 MHz datasheet (EMBMOD133)	242557
Mobile Pentium® Processor with MMX™ Technology datasheet (EMBMOD166)	243292
Pentium® Processor Family Developer's Manual	241428
Intel Architecture Software Developer's Manual Vols. 1 and 2	243190 and 243191
Intel 430HX PCIset 82439HX System Controller (TXC) datasheet	290551
Intel 430HX PCIset 82439HX System Controller (TXC) Timing Specification	272945

2.0 Module Connector Interface

2.1 Signal Description

Table 2 provides a list of Intel Embedded Processor Module signals by category and the corresponding number of signals in each category.

Table 2. Module Connector Signal Summary

Signal Group	Number
Memory	103
PCI Bus	56
Processor/PIIX3 sideband	10
Clocks	10
Voltage: 3.3 V	27
Voltage: 5.0 V	9
ITP/JTAG	1
Ground	30
Reserved/NC	14
Total	260

Table 3 describes the nomenclature used in the connector signal description tables in this section.

Table 3. Signal Description Nomenclature

Type	Description
#	The signal is active low
I	Standard input signal
O	Standard output signal
I/O	Input and output signal
5V	5 V signal
3V	3 V signal
3V/5V	3 V signal/5 V tolerant
TTL	Supports TTL levels

2.2 J1 Connector Signal Description (120-Pin)

Table 4 lists the Intel Embedded Processor Module J1 interface signals. The 120-pin J1 connector contains the PCI, processor/PIIX3 sideband, Power, Ground, and Clock signals.

Table 4. J1 Connector Signal Description (Sheet 1 of 3)

Signal[1]	Type	Description
COREV_SENSE	O	Power Good on processor core.
3.3V	I	3.3 Volt supply voltage.
12MHZ	O	**12 MHz Clock Signal:** Keyboard Clock.
14.318MHZ	O	**14.318 MHz Reference Clock.**
24MHZ	O	**24 MHz Clock Signal:** I/O Clock.
A20M#	I	**Address Bit 20 Mask:** When enabled, this causes the processor to emulate the address wraparound at 1 Mbyte, which occurs on the Intel 8086 processor.
AD[31:0]	I/O 5V	**Address/Data** is the standard PCI address and data lines. An address is driven with FRAME# assertion. Data is driven or received in following clocks.
C/BE[3:0]#	I/O 5V	**Command/Byte Enable:** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
CPURST	I^2	**CPU Reset:** The PIIX3 asserts CPURST to reset the CPU. The PIIX3 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven synchronously to the rising edge of PCICLK. When a hard reset is initiated through the RC register, the PIIX3 resets its internal registers to the default state.
DBRST	O	**Debugger Reset Output:** A debugger may assert DBRESET (high) while performing a “Reset All” or “Reset Target” debugger commands. Connect DBRESET to the system reset circuitry such that the system and processor are reset when DBRESET is asserted. This signal is asynchronous.
DEVSEL#	I/O 5V	**Device Select:** This signal is driven by the TXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.

NOTES:
1. All signals in the PCI interface conform to the PCI Revision 2.1 specification.
2. Signals are open drain on the 82371SB and require an external pull-up resistor on the system manufacturer’s motherboard which connects to the module.

Table 4. J1 Connector Signal Description (Sheet 2 of 3)

Signal[1]	Type	Description
FERR#	O	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the CPU. IGNNE# is only used when the PIIX3 coprocessor error reporting function is enabled in the XBCSA Register. When FERR# is asserted, the PIIX3 generates an internal IRQ13 to its interrupt controller unit. The PIIX3 then asserts the INTR output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active. FERR# has a weak internal pull-up used to ensure a high level when the coprocessor error function is disabled.
FRAME#	I/O 5V	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GND	I	**Signal Ground.**
GNT[3:0]#	O 5V	**PCI Grant:** Permission is given to the master to use PCI. Weak external pull-up resistors are required on these signals.
IGNNE#	I^2	**Ignore Error:** This signal is connected to the ignore error pin on the CPU. IGNNE# is only used when the PIIX3 coprocessor error reporting function is enabled in the XBCSA Register. When FERR# is asserted, indicating a coprocessor error, a write to the Coprocessor Error Register (F0H) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. When FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted.
INIT	I^2	**Initialization:** The PIIX3 asserts INIT when it detects a shutdown special cycle on the PCI Bus or when a soft reset is initiated via the RC Register.
INTR	I^2	**CPU Interrupt:** INTR is driven by the PIIX3 to signal the CPU that an interrupt request is pending and needs to be serviced. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state.
IRDY#	I/O 5V	**Initiator Ready** is asserted when the initiator is ready for a data transfer.
LOCK#	I/O 5V	**Lock** is used to establish, maintain, and release resource locks on PCI.
N/C	—	No Connect.
NMI	I^2	**Non-maskable Interrupt:** NMI is used to force a non-maskable interrupt to the CPU. The PIIX3 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed.
PAR	I/O 5V	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0].
PCI_CLK[0:5]	O	**33 MHz PCI Clock Outputs.**
PCICLK_IN	I	**Input 82439HX PCI Clock.**
PCIRST#	I	**PCI Reset:** This signal has two functions, depending on the programming of the APIC Chip Select bit (XBCS Register). See the APIC Signal Description for the APICACK# function. The PIIX3 asserts PCIRST# to reset devices that reside on the PCI Bus. The PIIX3 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven active for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK.

NOTES:
1. All signals in the PCI interface conform to the PCI Revision 2.1 specification.
2. Signals are open drain on the 82371SB and require an external pull-up resistor on the system manufacturer's motherboard which connects to the module.

Table 4. J1 Connector Signal Description (Sheet 3 of 3)

Signal[1]	Type	Description
PHLD#	I 5V	**PCI Hold:** This signal comes from the expansion bridge. It is the bridge request for PCI. The PHLD# protocol supports passive release. A weak external pull-up resistor is required on this signal.
PHLDA#	O 5V	**PCI Hold Acknowledge:** This signal is driven by the TXC to grant PCI to the expansion bridge. The PHLDA# protocol supports passive release. A weak external pull-up resistor is required on this signal.
REQ[3:0]#	I 5V	**PCI Request:** PCI master requests for PCI. Weak external pull-up resistors are required on these signals.
SERR#	O 5V	**System Error:** The TXC asserts SERR# to signal a system error. A system error can be generated for either single bit error (correctable) events or any ECC bit error (correctable or uncorrectable), or for parity error.
SMI#	I^2	**System Management Interrupt:** SMI# is an active low synchronous output that is asserted by the PIIX3 in response to one of many enabled hardware or software events.
STOP#	I/O 5V	**Stop** is asserted by the target to request the master to stop the current transaction.
STPCLK#	I^2	**Stop Clock:** STPCLK# is an active low synchronous output that is asserted by the PIIX3 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK.
TRDY#	I/O 5V	**Target Ready** is asserted when the target is ready for a data transfer.

NOTES:
1. All signals in the PCI interface conform to the PCI Revision 2.1 specification.
2. Signals are open drain on the 82371SB and require an external pull-up resistor on the system manufacturer's motherboard which connects to the module.

2.3 J2 Connector Signal Description (140-Pin)

Table 5 lists the Intel Embedded Processor Module J2 interface signals. The 140-pin J2 connector contains the DRAM, power, and ground signals.

Table 5. J2 Connector Signal Description

Signal	Type	Description
3.3V	I	3.3 Volt supply voltage.
5.0V	I	5 Volt supply voltage.
CAS[7:0]#	O 3V	**Column Address Strobe:** These pins select the DRAM column.
GND	I	Signal Ground.
MA[11:2]	O 3V	**Memory Address:** This is the row and column address for DRAM. These buffers include programmable size selection.
MAA[1:0]	O 3V	**Memory Address Copy A:** One copy of the memory addresses (MA[11:2]) that change during a burst read or write of DRAM. Size selection of the I/O buffers on these pins on the 82439HX is programmable.
MAB[1:0]	O 3V	**Memory Address Copy B:** A second copy of the memory addresses (MA[11:2]) that change during a burst read or write of DRAM. Size selection of the I/O buffers on these pins on the 82439HX is programmable.
MD[63:0]	I/O 3V/5V TTL	**Memory Data:** These signals are connected to the DRAM data bus.
MPD[7:0]	I/O 3V/5V TTL	**Memory Parity Data:** These signals connect to the DRAM parity or ECC bits. The MPD pins have similar timing and drive capability to the MD pins. ECC versus parity operation is determined by the PCI Control Register (PCON[DDIM] field) in the 82439HX. These signals have internal weak pull-down resistors, the same as the MD signals. These signals are always driven during write cycles, regardless of the existence of parity memory.
MWE#	O 3V	**Memory Write Enable:** Use MWE# as the write enable for the memory data bus. This signal has a programmable size selection, which is selected through the DRAM Extended Control Register (DRAMEC[MAD] field) in the 82439HX.
N/C	—	No Connect.
RAS[7:0]#	O 3V	**Row Address Strobe:** These pins select the DRAM row.

NOTE: All 3 V output signals can drive 5 V TTL inputs.

2.4 ITP/JTAG Connector Signal Description

Table 6 lists the Intel Embedded Processor Module Intel Test Port (ITP) interface signals. The 20-pin connector will *not* be populated on production modules. The ITP connector can be attached by the system integrator to gain access to the debug capabilities within the processor.

Table 6. Intel Test Port (ITP) Interface Signal Description

Signal Name	Dir	Description
DBRESET	I	**Debugger Reset Output:** A debugger may assert DBRESET (high) while performing “Reset All” or “Reset Target” debugger commands. DBRESET should be connected to the system reset circuitry so that the system and processor are reset when DBRESET is asserted. This signal is asynchronous.
GND		Signal Ground.
INIT	O	**Processor Initialization:** (Pentium processor signal) A debugger may use INIT to support emulating through the CPU INIT sequence while maintaining breakpoints or breaking on INIT.
N/C		**No Connect.** Leave this pin unconnected.
PRDY	O	**Probe Ready:** From the PRDY pin on the Pentium processor.
RESET	O	**Reset Signal:** (Pentium processor signal) A debugger may use RESET to support emulating through the reset while maintaining breaking on RESET.
R/S#	I	**Run/Stop:** Connect to the R/S# pin on the Pentium processor.
TCK	I	Boundary scan clock. (Pentium processor signal)
TDI	I	**Boundary scan data input:** (Pentium processor signal) This signal connects to TDI of the Pentium Processor.
TDO	O	**Boundary scan data output:** (Pentium processor signal) This signal connects to the TDO from the Pentium processor.
TMS	I	**Boundary scan mode select** (Pentium processor signal).
TRST#	I	Boundary Scan Reset (Pentium processor signal).
V_{CC}		**V_{CC}** from the Pentium processor system. A debugger uses this signal to sense that system power is on. Connect this signal to V_{CC} through a 1 KΩ (or smaller) resistor.

2.5 J1 Connector Pin Assignment (120-Pin)

Table 7 lists the signals for each pin of the 120-pin J1 connector. See Figure 6 for connector orientation.

Table 7. PCI Connector Pin Assignment (J1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	INIT	A31	GND	B01	3.3V	B31	AD22
A02	CPURST	A32	PHLDA#	B02	STPCLK#	B32	3.3V
A03	3.3V	A33	AD21	B03	SMI#	B33	LOCK#
A04	A20M#	A34	AD19	B04	GND	B34	AD20
A05	INTR	A35	3.3V	B05	NMI	B35	AD24
A06	IGNNE#	A36	FRAME#	B06	FERR#	B36	GND
A07	GND	A37	AD17	B07	N/C	B37	AD18
A08	24MHZ	A38	REQ0#	B08	3.3V	B38	AD16
A09	N/C	A39	GND	B09	COREV_SENSE	B39	IRDY#
A10	12MHZ	A40	CBE2#	B10	N/C	B40	3.3V
A11	3.3V	A41	AD15	B11	14.318MHZ	B41	CBE1#
A12	N/C	A42	TRDY#	B12	GND	B42	GNT0#
A13	PCICLK_1	A43	3.3V	B13	N/C	B43	AD14
A14	N/C	A44	AD13	B14	PCICLK_2	B44	GND
A15	GND	A45	REQ1#	B15	N/C	B45	AD12
A16	PCICLK_3	A46	AD11	B16	3.3V	B46	DEVSEL#
A17	N/C	A47	GND	B17	PCICLK_4	B47	AD10
A18	PCICLK_5	A48	AD9	B18	N/C	B48	3.3V
A19	3.3V	A49	AD8	B19	PCICLK_0	B49	GNT1#
A20	DBRST	A50	AD7	B20	GND	B50	CBE0#
A21	N/C	A51	3.3V	B21	PCICLK_IN	B51	REQ2#
A22	N/C	A52	STOP#	B22	N/C	B52	GND
A23	GND	A53	AD5	B23	PCIRST#	B53	AD6
A24	N/C	A54	GNT2#	B24	3.3V	B54	AD4
A25	AD30	A55	GND	B25	AD31	B55	PAR
A26	AD28	A56	AD3	B26	AD29	B56	3.3V
A27	3.3V	A57	REQ3#	B27	AD27	B57	AD2
A28	AD26	A58	AD1	B28	GND	B58	SERR#
A29	PHLD#	A59	3.3V	B29	AD25	B59	GNT3#
A30	AD23	A60	AD0	B30	CBE3#	B60	GND

2.6 J2 Connector Pin Assignment (140-Pin)

Table 8 lists the signals for each pin of the 140-pin J2 connector. See Figure 6 for connector orientation.

Table 8. DRAM Connector Pin Assignment (J2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	GND	A36	CAS5#	B01	MWE#	B36	CAS0#
A02	MAA1	A37	GND	B02	MAB1	B37	MPD2
A03	MAA0	A38	MD55	B03	5.0V	B38	MD23
A04	MAB0	A39	CAS4#	B04	MA6	B39	GND
A05	5.0V	A40	CAS2#	B05	MA5	B40	MPD4
A06	MA4	A41	3.3V	B06	MA3	B41	MPD0
A07	MA2	A42	MPD6	B07	5.0V	B42	CAS6#
A08	MA8	A43	RAS0#	B08	MA11	B43	3.3V
A09	GND	A44	MPD7	B09	MA7	B44	MPD1
A10	MA10	A45	GND	B10	MA9	B45	MPD5
A11	MD0	A46	RAS2#	B11	5.0V	B46	RAS1#
A12	MD32	A47	MD08	B12	MD48	B47	GND
A13	5.0V	A48	MD40	B13	MD16	B48	MPD3
A14	MD33	A49	3.3V	B14	MD17	B49	RAS3#
A15	MD01	A50	MD25	B15	GND	B50	MD41
A16	MD49	A51	MD24	B16	MD02	B51	3.3V
A17	5.0V	A52	MD56	B17	MD34	B52	MD30
A18	MD35	A53	GND	B18	MD18	B53	MD44
A19	MD50	A54	MD26	B19	5.0V	B54	MD57
A20	MD03	A55	MD09	B20	MD19	B55	GND
A21	GND	A56	MD46	B21	MD36	B56	MD11
A22	MD04	A57	3.3V	B22	MD51	B57	MD10
A23	RAS7#	A58	MD42	B23	5.0V	B58	MD12
A24	RAS5#	A59	MD59	B24	MD05	B59	3.3V
A25	5.0V	A60	MD58	B25	MD52	B60	MD60
A26	MD20	A61	GND	B26	RAS6#	B61	MD27
A27	RAS4#	A62	MD43	B27	3.3V	B62	MD28
A28	MD53	A63	MD61	B28	MD21	B63	GND
A29	GND	A64	MD29	B29	MD37	B64	MD45
A30	CAS7#	A65	3.3V	B30	CAS3#	B65	MD13
A31	MD22	A66	MD62	B31	GND	B66	MD63
A32	MD38	A67	MD14	B32	MD06	B67	3.3V
A33	3.3V	A68	MD47	B33	CAS1#	B68	MD31
A34	MD39	A69	GND	B34	MD07	B69	MD15
A35	MD54	A70	N/C	B35	3.3V	B70	GND

2.7 ITP/JTAG Connector Pin Assignment

Table 9 lists the signals for each pin of the 20-pin ITP/JTAG connector. For connector orientation, refer to the ITP connector manufacturer's documentation.

Table 9. ITP Connector Pin Assignment (J3)

Pin	Signal	Pin	Signal
1	INIT	11	PRDY
2	DBRESET	12	TDI
3	RESET	13	TDO
4	GND	14	TMS
5	N/C	15	GND
6	3.3V	16	TCLK
7	R/S#	17	GND
8	GND	18	TRST#
9	N/C	19	N/C
10	GND	20	N/C

3.0 Functional Description

3.1 Embedded Processor Module

The Intel Embedded Processor Module uses the Pentium® Processor with Voltage Reduction Technology (EMBMOD133) or the Mobile Pentium® Processor with MMX™ Technology (EMBMOD166) with an internal frequency of 133 or 166 MHz (respectively) and a bus frequency of 66 MHz.

3.2 L2 Cache

The Pentium processor's internal cache is complemented by a second-level cache using 256 Kbytes (EMBMOD133) or 512 Kbytes (EMBMOD166) of high speed synchronous pipelined burst SRAM. The L2 cache can support up to 64 Mbytes of system memory. The L2 cache has a 3.3 V interface to the host system bus and the 82439HX System Controller (TXC). The L2 cache subsystem includes a 32 K x 8 cache tag RAM (provided on module). The upper address bits of the tag chip are disabled.

3.3 System Controller

Intel's 82439HX system controller is a highly integrated device that combines the Pentium processor bus controller, the DRAM controller, second-level cache controller and the PCI bus controller into one component. The 82439HX is PCI 2.1 compliant. The PCI bus for the Intel Embedded Processor Module operates at 33 MHz (one-half the host frequency) and is provided by the system baseboard. The system designer must take one of the six PCI clocks generated on the

processor module, deskew the signal and route it back to the processor module. This ensures that the Host-to-PCI clock skew specification is met. Refer to Intel's latest revision of the 430HX PCIset datasheets for complete details.

3.4 Clock Generation

A clock synthesizer circuit is provided on the Intel Embedded Processor Module. The clock generator accepts a 14.318 MHz input signal from a crystal oscillator. The clock generator provides the 66 MHz clock needed for the Pentium processor and the 82439HX, and the 33 MHz clocks needed for the 82439HX and the PCI interface. Additional outputs from the clock circuit are buffered 14.318 MHz, 24 MHz, and 12 MHz signals. Six buffered copies of the 33 MHz PCI clock signal are available.

3.5 Voltage Regulation

The Pentium processor with Voltage Reduction Technology requires 2.9 V for the core and 3.3 V for the I/O interface. The Pentium processor with MMX™ technology requires 2.45 V for the core and 3.3 V for the I/O interface.The Intel Embedded Processor Module has an integrated voltage regulation circuit on-board to provide the 2.9 V or 2.45 V processor core requirement. The input to the voltage regulation circuit is 5.0 V and is provided by the system baseboard. The voltage regulator can supply a minimum of 3.0 A (on the 133 MHz module) or 4.1 A (on the 166 MHz module) to the Pentium processor. The voltage regulator is a switching regulator which increases the efficiency of the circuit as compared to a linear regulator.

3.6 Connectors

The Intel Embedded Processor Module interfaces to the I/O subsystem via two high-density connectors. The 140-pin connector (J2) contains the DRAM interface, power and ground connections. The 120-pin connector (J1) contains the PCI interface, processor/PIIX3 sideband signals, clocks, power and ground connections. The connectors are low profile, with a 5 mm stacking height, and high density (0.8 mm pitch). The connectors minimize baseboard-to-module spacing.

All pins labeled N/C are "no connect" pins and are reserved for future use.

The connectors should not be used as the only mechanical connection to the system baseboard. Use the four mounting holes provided on the module as the mechanical interface to the system baseboard. The four mounting holes are electrically connected to ground.

The module also provides the ability to add an ITP connector to facilitate debug and software development. The ITP connector is not installed on production modules. The following components must be installed for the ITP to function correctly:

Table 10. Additional Components for ITP

Location	Component
U8	74LVQ04 Hex Inverter
R41	1.0 KΩ Resistor
R42	0Ω Resistor

3.7 Thermal Considerations

The Intel Embedded Processor Module (EMBMOD133) uses a passive heat sink as the thermal solution. The heat sink is mechanically attached to the topside of the module and uses an electrically and thermally conductive compound for the module-to-heat sink interface.

Figure 2 shows the orientation of the module in the 0 and 180 degree airflow rotation. Figure 3, Figure 4 and Table 11 contain the thermal characterization data showing the relationship between θ_{CA} and the airflow required to ensure that the maximum case temperature is not exceeded. The maximum case temperature is 95° C for the Pentium processor and 85° C for the 82439HX System Controller and SRAM.

Figure 2. Airflow Direction

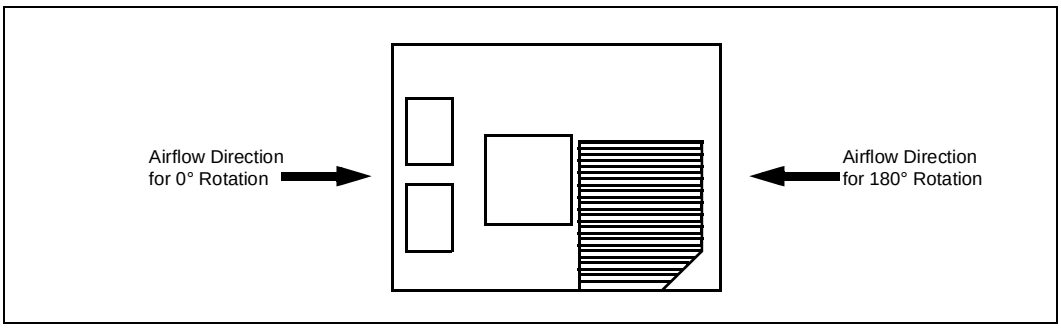


Figure 3. Thermal Resistance vs. Airflow, 0° Rotation

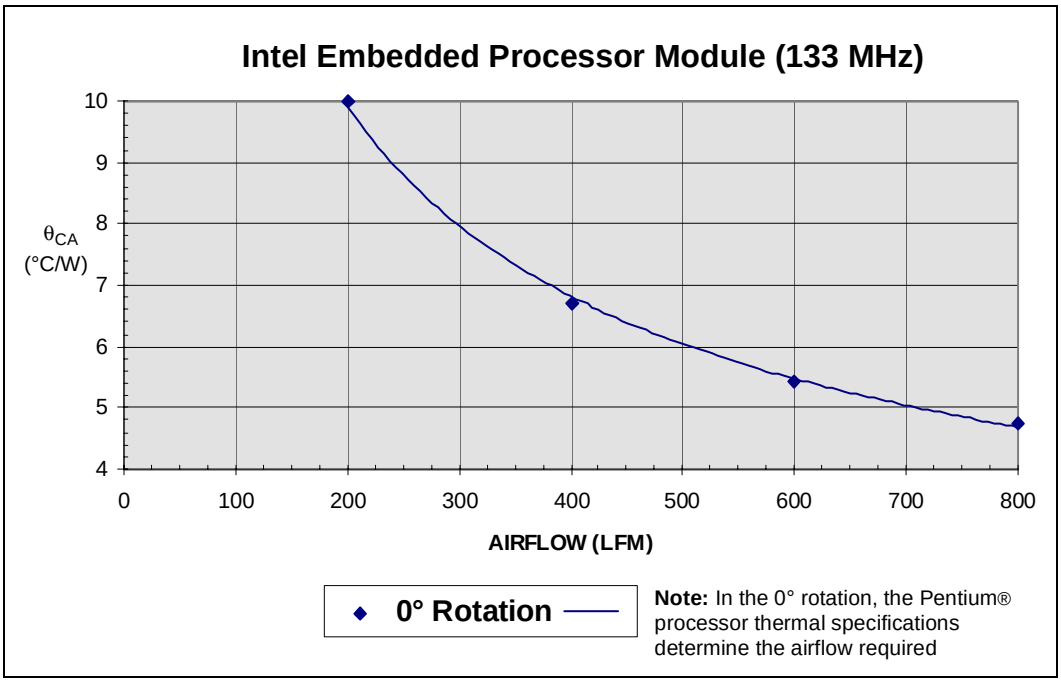


Figure 4. Thermal Resistance vs. Airflow, 180° Rotation

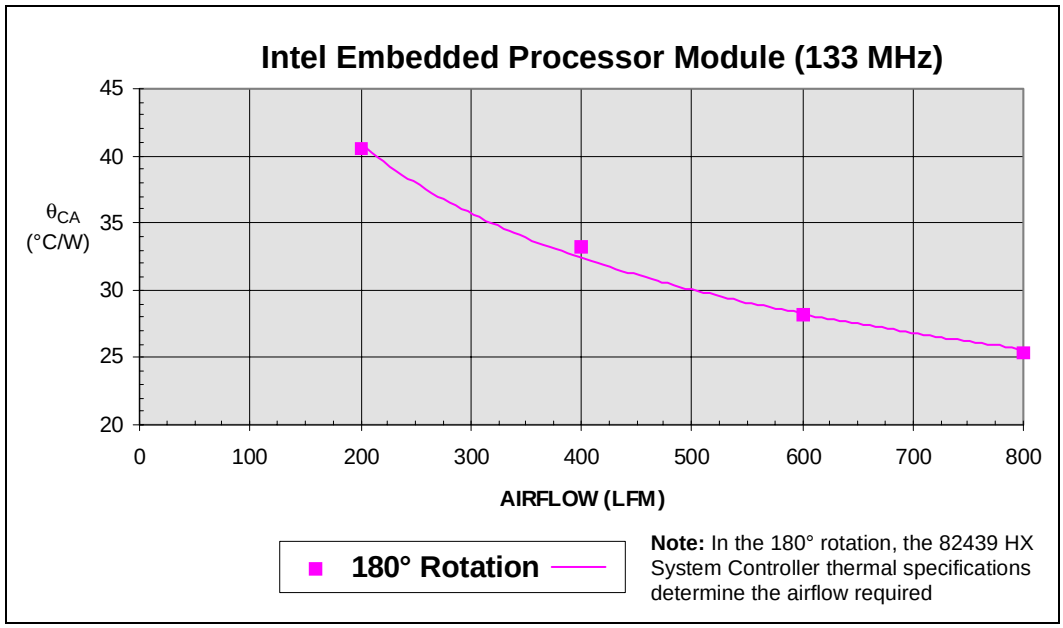


Table 11. Tested Airflows and Rotation

Airflow	θ_{CA} (0° Rotation)	θ_{CA} (180° Rotation)
800	4.8	25.4
600	5.4	28.2
400	6.7	33.2
200	10.0	40.5

The test conditions were:

- All measurements were taken in an “open air” environment (no enclosure around the module)
- **0° rotation:** Airflow direction is from the 82439HX System Controller (BGA) to the Pentium processor (TCP); T_C = 95° C
- **180° rotation:** Airflow direction is from the Pentium processor (TCP) to the 82439HX System Controller (BGA); T_C = 85° C

The equation used to calculate θ_{CA} is:

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

Where:

θ_{CA} = Case-to-Ambient Thermal Resistance (°C/ W)

T_C = Case Temperature

T_A = Ambient Temperature

P= Power in Watts

When considering the thermal requirements for the Embedded Processor Module in a specific application, always ensure that the maximum case temperature is not exceeded for any component on the module, regardless of the orientation of the module. Refer to the *Intel Embedded Processor Module Thermal Design Guide* (order number 273143).

The thermal solution for the EMBMOD166 is under development. The thermal characterization data for the EMBMOD166 will be published when it becomes available.

3.7.1 Maximum and Typical Power Design Examples

Below is an example of determining the airflow required during maximum power consumption:

T_C (TCP) = 95° C; T_C (BGA) = 85° C
T_A = 50° C
P_{TCP} = 7.9 W, P_{BGA} = 1.2 W
θ_{CA} (TCP, 0° rotation) = 5.7 °C/W
θ_{CA} (BGA, 180° rotation) = 29.1 °C/W

Figure 3 and Figure 4 indicate that this example would require about 550 LFM in the 0° rotation, and about 550 LFM in the 180° rotation.

The next example shows the same calculation for typical power consumption:

T_C (TCP) = 95° C; T_C (BGA) = 85° C
T_A = 50° C
P_{TCP} = 3.5 W, P_{BGA} = 1.0 W
θ_{CA} (TCP, 0° rotation) = 12.9 °C/W
θ_{CA} (BGA, 180° rotation) = 35.0 °C/W

Figure 3 and Figure 4 indicate that this example would require about 100 LFM in the 0° rotation, and about 325 LFM in the 180° rotation.

3.8 Custom Heat Sink Designs

Intel does *not* recommend removing the heat sink from the Embedded Processor Module. But if you must remove the heat sink for a custom thermal solution, care must be taken not to damage the module or any components on the module. Custom thermal solutions must also ensure that maximum case temperatures for all components on the Embedded Processor Module are not exceeded.

Warning: Damage to the board or components voids the warranty of the module.

3.8.1 Removing the Heat Sink

The following procedure *must* be followed when removing the heat sink:

Caution: Allow the heat sink to cool to room temperature before removing the heat sink from the module.

1. Wear a grounding strap at all times when handling the modules to protect against electrostatic discharge.
2. Use needle-nose pliers to gently squeeze the nose of each push pin together and push the pins through the module.

3.8.2 Installing the Heat Sink

The following procedure *must* be followed when installing the heat sink:

1. Remove any existing thermally conductive grease with a clean cloth.
2. Add approximately 1/8 gram of thermally conductive grease evenly onto the pedestal of the heat sink.
3. Align the heat sink holes with the plated holes on the module.
4. Press push pins through the holes with approximately 6 lb. force until the nose of the pin latches onto the module.

Note: See the *Intel Embedded Processor Module Thermal Design Guide* (order number 273143) for a list of vendors of thermally conductive grease.

3.9 Electrical Design

Clock signals generated on the module are routed on impedance-controlled signal layers. To minimize clock skew, the 66 MHz clock lines are matched and have a length of 9.3 inches. Extra space was added between the clock lines and other signals to minimize signal crosstalk. The lengths of the 33 MHz clock lines are also matched. The 33 MHz clock input on the 82439HX comes from the external connector. Series termination resistors are provided on the Intel Embedded Processor Module, but provisions should be made on the baseboard for AC termination at the signal destination. The memory CAS and RAS signals are terminated on the module with series resistors.

Power filtering is performed on the module for the 2.9/2.45 V, 3.3 V, and 5 V supplies. A separate analog ground plane for the clock generator is provided. All power and ground leads are as short as possible and are wider than signal traces in order to minimize IR and L-di/dt losses.

The design rules for the 430HX PCIset were followed on the module. Pentium processor signals that must be tied off are terminated on the module. PCI signals REQ[3:0]# and GNT[3:0]# are pulled up on the module. All other PCI signals must be terminated on the baseboard. The following signals have space for termination resistors on the module. These resistors are *not* populated on the production modules and must be provided by the host system.

INIT, RESET, A20M#, IGNNE#, SMI#, NMI, INTR, FERR#

A COREV_SENSE signal is provided to the baseboard for power-good sensing. The DBRESET signal from the ITP is provided on the PCI connector for baseboard use (with PWRGOOD). Power-good sensing is done on the baseboard. The baseboard must supply 2.0 A of 3.3 V and 3.5 A (EMBMOD133) or 4.1 A (EMBMOD166) of 5.0 V.

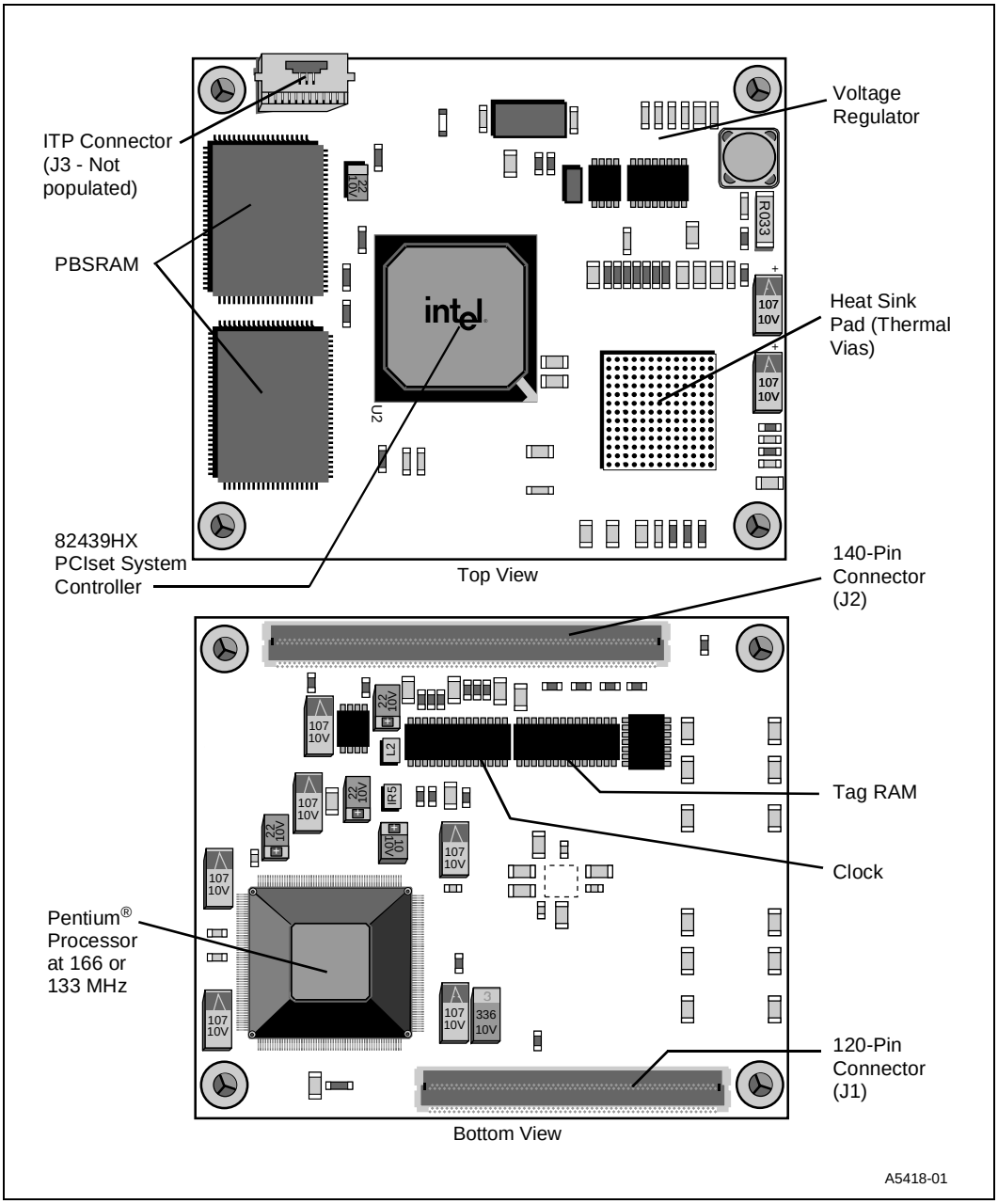
4.0 Mechanical Data

4.1 Module Dimensions

This section provides the physical dimensions for the Intel Embedded Processor Module.

Figure 5 shows top and bottom views of the Intel Embedded Processor Module.

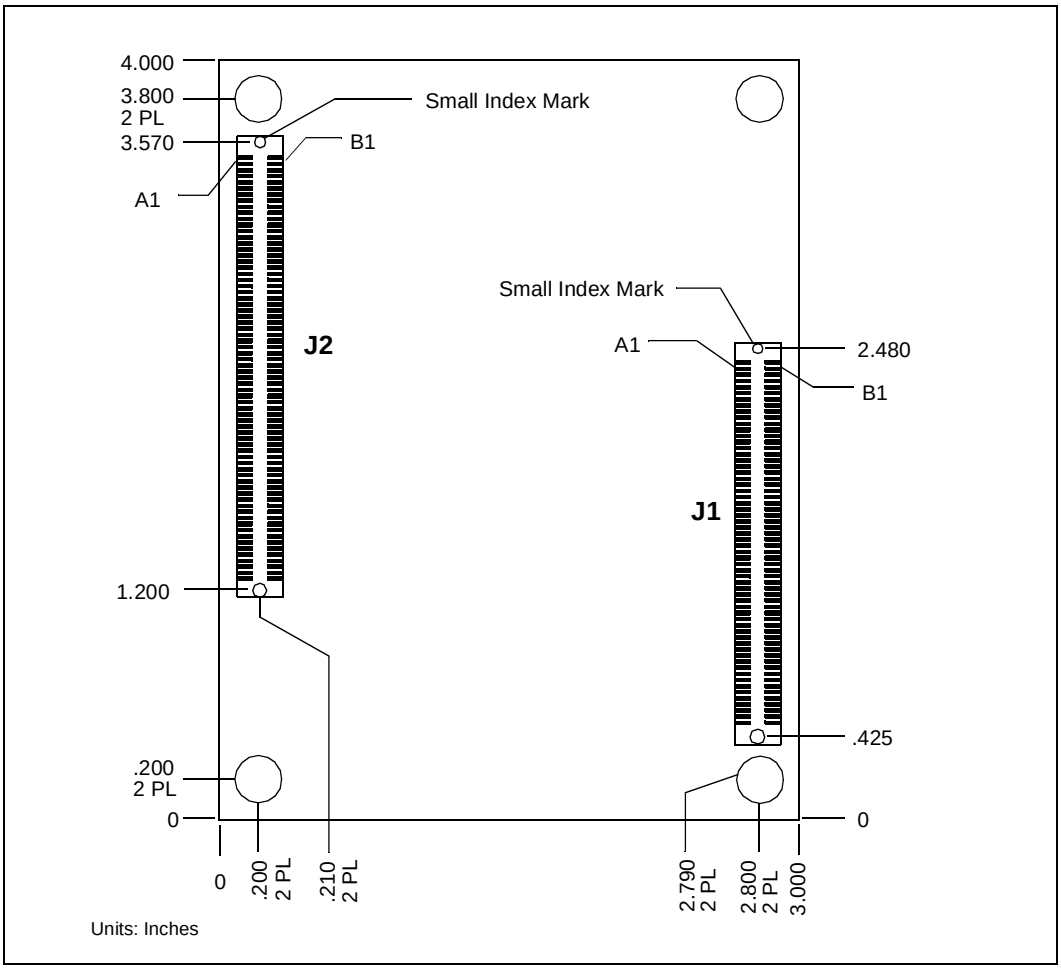
Figure 5. Intel Embedded Processor Module — Top and Bottom View



4.1.1 Dimensions and Connector Orientation

Figure 6 shows the board dimensions and the connector orientation for the Intel Embedded Processor Module.

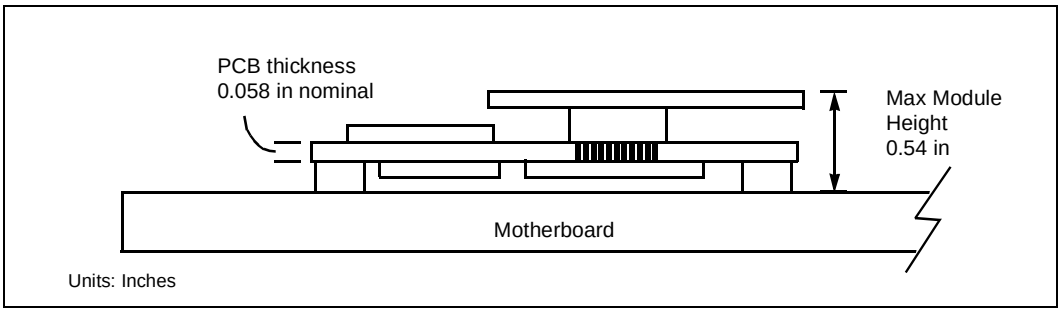
Figure 6. Board Dimensions and Connector Placement



4.1.2 Printed Circuit Board Thickness and Clearance

Figure 7 is a profile view of the Intel Embedded Processor Module showing the nominal thickness of the printed circuit board (0.058 inches) and the maximum module height (0.54 inches). The clearance from the motherboard to the underside of the Embedded Processor Module printed circuit board is fixed by the connector stacking height of 5 mm. Actual clearance varies depending on component thickness and location.

Figure 7. Profile of the Intel Embedded Processor Module



4.2 Connector Specifications

The Intel Embedded Processor Module connectors are surface mount, 0.8 mm pitch, 140-pin and 120-pin connectors. Table 12 summarizes some of the critical specifications for the connectors.

Table 12. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Beryllium Copper
	Housing	Thermoplastic Molded Compound LCP
Electrical	Current	0.5 A
	Voltage	100 VAC
	Termination Resistance	20 mΩ max. @20 mV open circuit with 10 mA
	Insulation Resistance	500 MΩ min. @ 500 VDC
Mechanical	Mating Cycles	100 cycles
	Connector Mating Force	0.9 N (90 gf) max. per contact
	Connector Un-mating Force	0.1 N (10 gf) min. per contact

5.0 Environmental Standards

The environmental standards for this product are being developed. Table 13 provides the parameter list to which specifications will be defined.

Table 13. Environmental Standards

Parameter	Condition	Specification
Temperature	Non-operating Operating	-25 ° C to 65° C 0 ° C to 50 ° C
Shock	Unpackaged Packaged	Trapezoidal, 30 G, 11 ms Half Sine, 2 ms at 36” Simulated Free Fall
Vibration	Unpackaged Packaged Packaged	5 Hz to 500 Hz, 2.2 gRMS 10 Hz to 500 Hz, 1.0 gRMS 11,800 impacts, 2 Hz to 5 Hz (low frequency)
ESD	Air Discharge	0 to 2 kV (no detectable error)