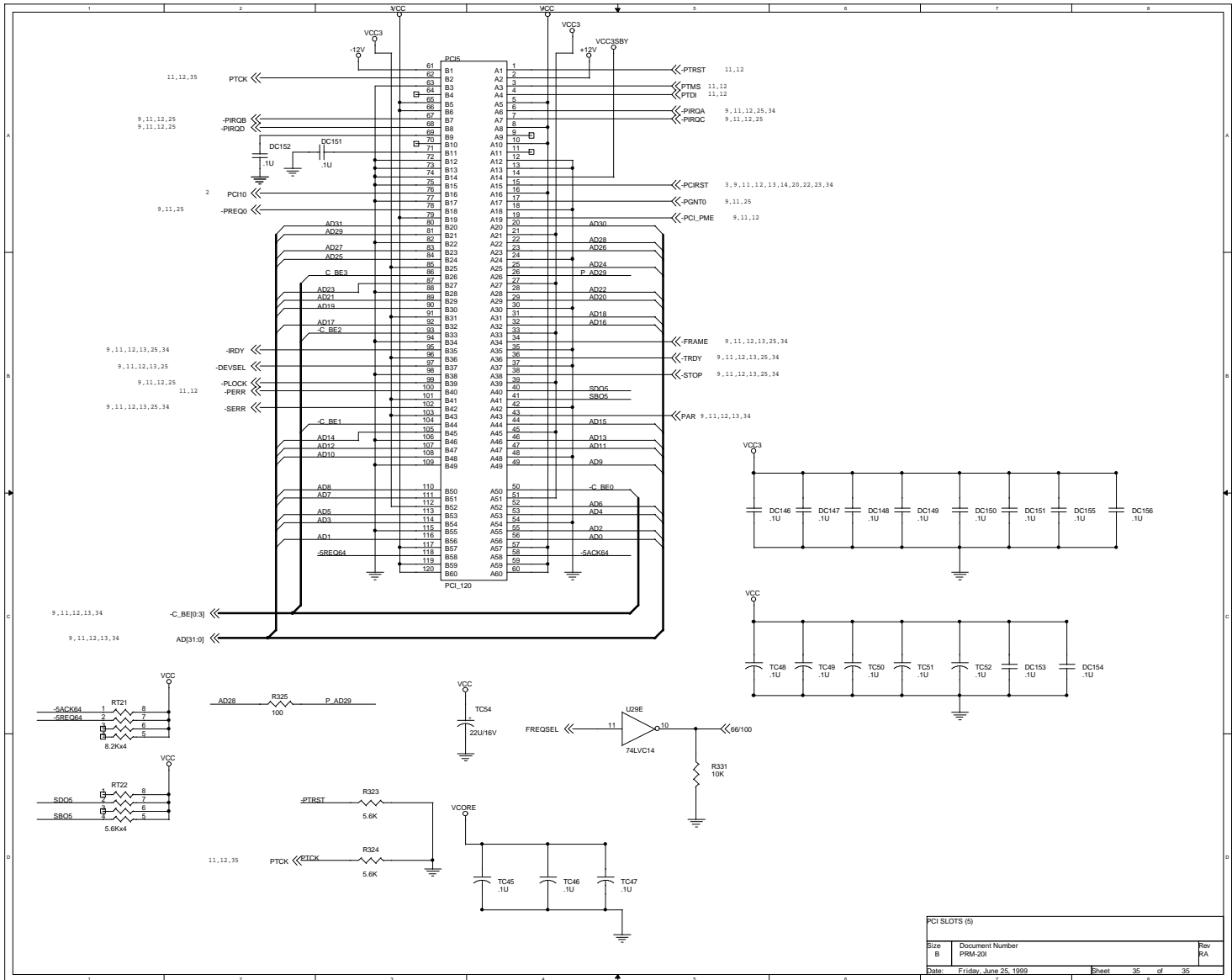
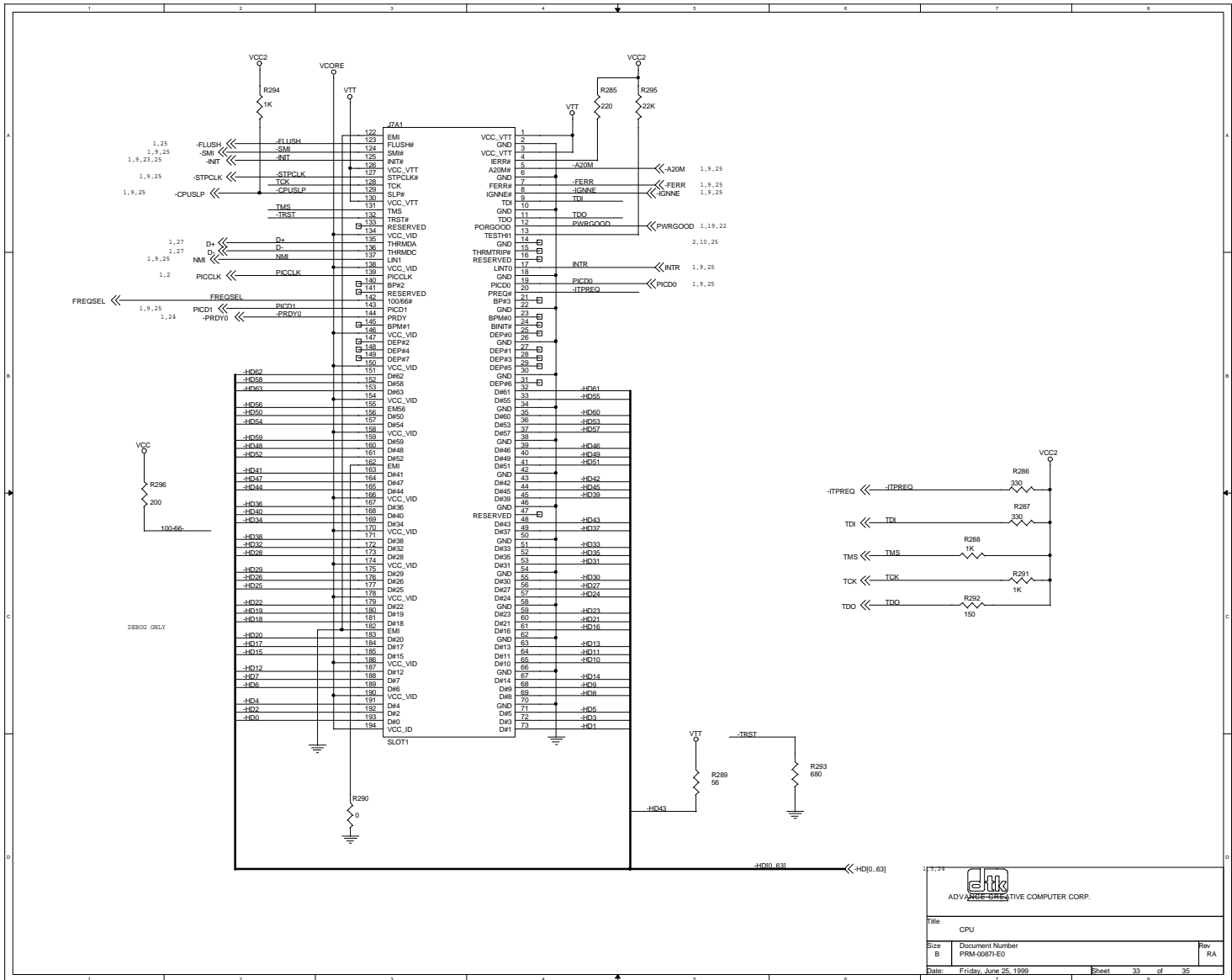



- LINE
- 1, 8CH
- 2, 8CH
- 3, 8CH
- 4, 8CH
- 5, 8CH
- 6, 8CH
- 7, 8CH
- 8, 8CH
- 9, 8CH
- 10, 8CH
- 11, 8CH
- 12, 8CH
- 13, 8CH
- 14, 8CH
- 15, 8CH
- 16, 8CH
- 17, 8CH
- 18, 8CH
- 19, 8CH
- 20, 8CH
- 21, 8CH
- 22, 8CH
- 23, 8CH
- 24, 8CH
- 25, 8CH
- 26, 8CH
- 27, 8CH
- 28, 8CH
- 29, 8CH
- 30, 8CH
- 31, 8CH
- 32, 8CH
- 33, 8CH
- 34, 8CH
- 35, 8CH



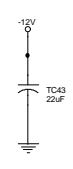
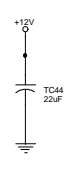
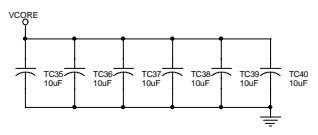
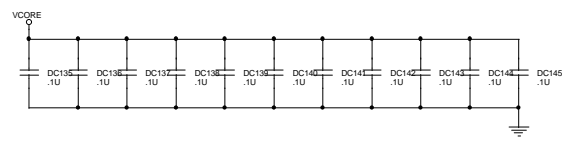
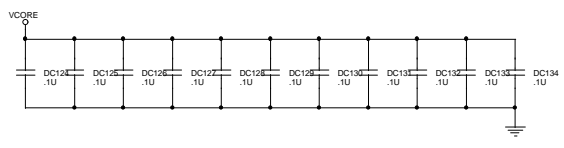
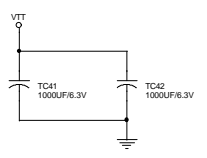
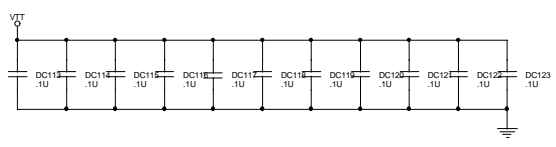
PCI SLOTS (9)		
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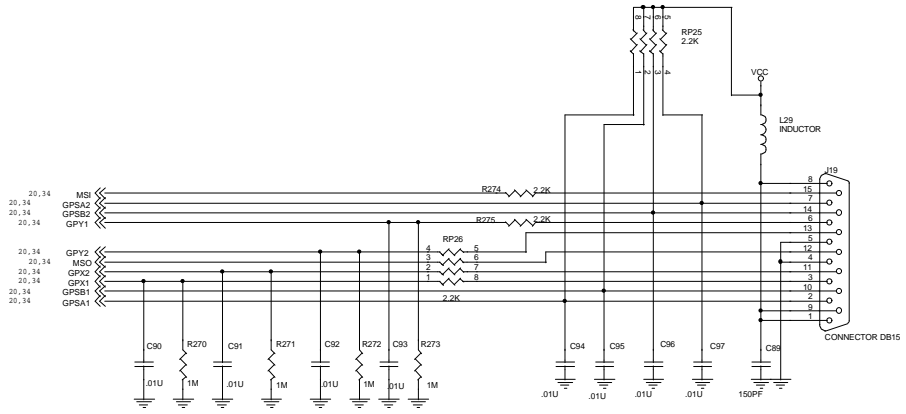
 ADVANCED MICRO DEVICES INTEL CORPORATION	
Title: CPU	
Size: B	Document Number: PRM-00871-EO
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L1085		
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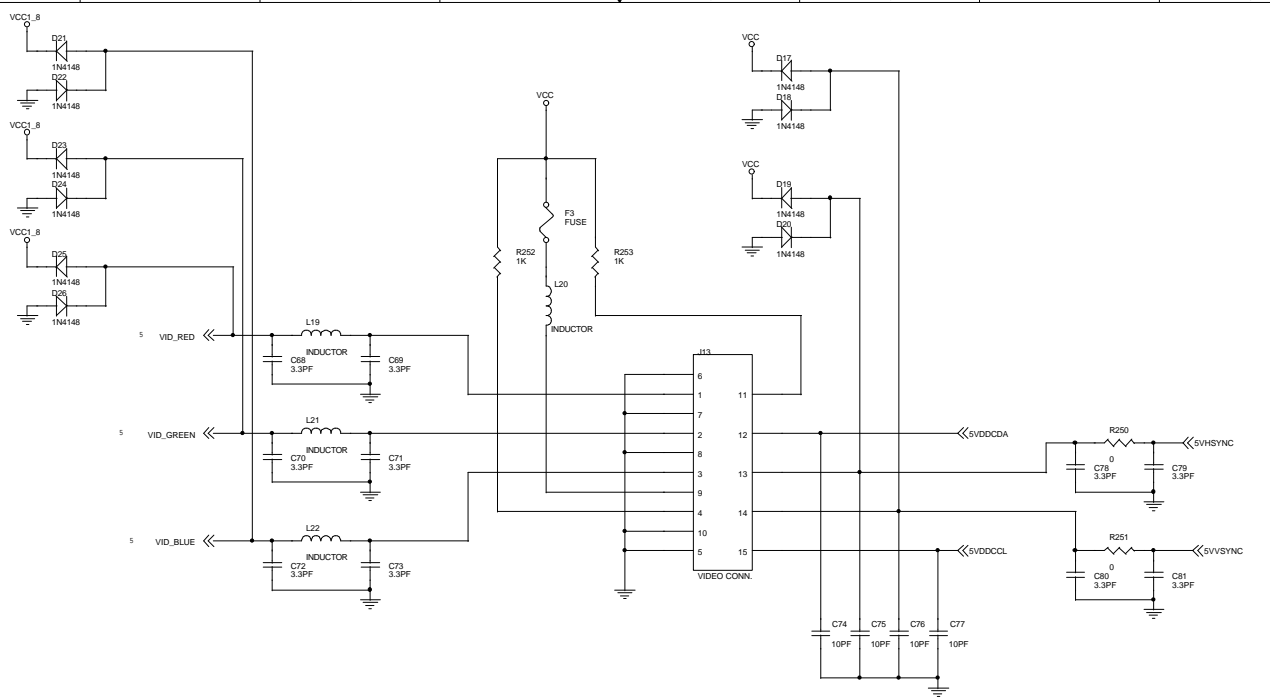
GAME & MIDI PORT CIRCUIT



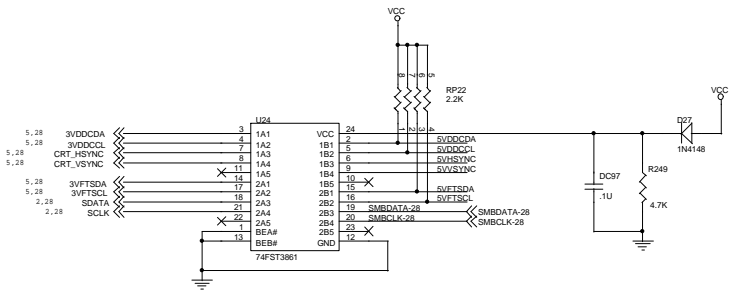
V83627HF CIRCUIT (LPC I/O CIRCUIT)		
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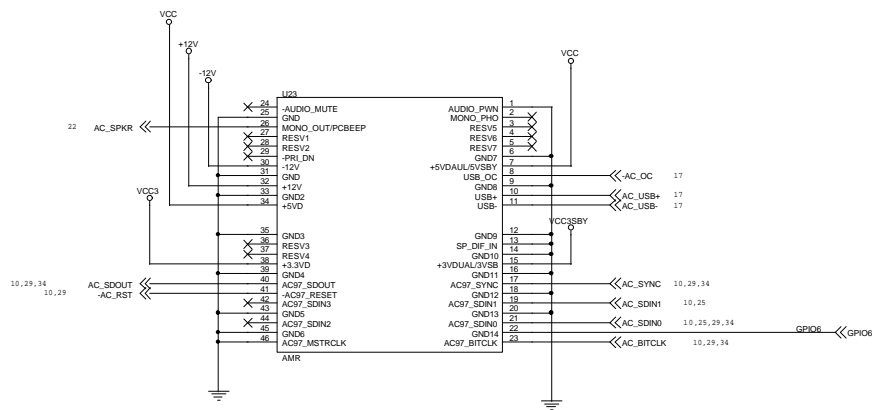


5, 28	3VDDCCDA	1	8	5VDDCCDA
5, 28	3VDDCCL	2	7	5VDDCCL
5, 28	CRT_HSYNC	3	6	5VHSYNC
5, 28	CRT_VSYNC	4	5	5VVSNC
		0		



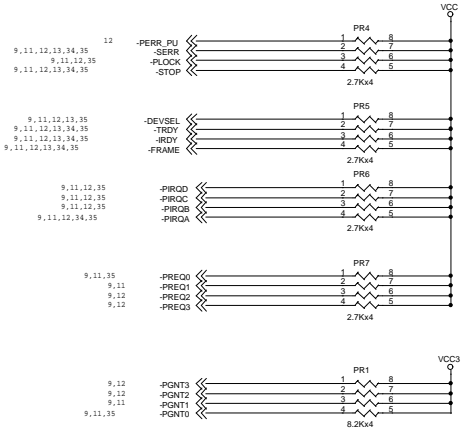
5, 28	3VFTSDA	1	8	5VFTSDA
5, 28	3VFTSCL	2	7	5VFTSCL
2, 28	SDATA	3	6	SMDATA-28
2, 28	SCLK	4	5	SMBCLK-28
		0		



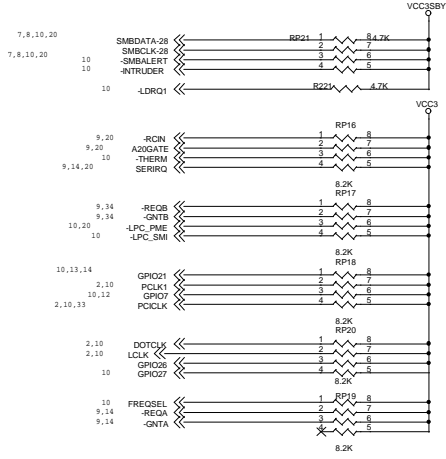


MMR_CONN		
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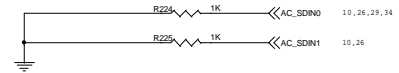
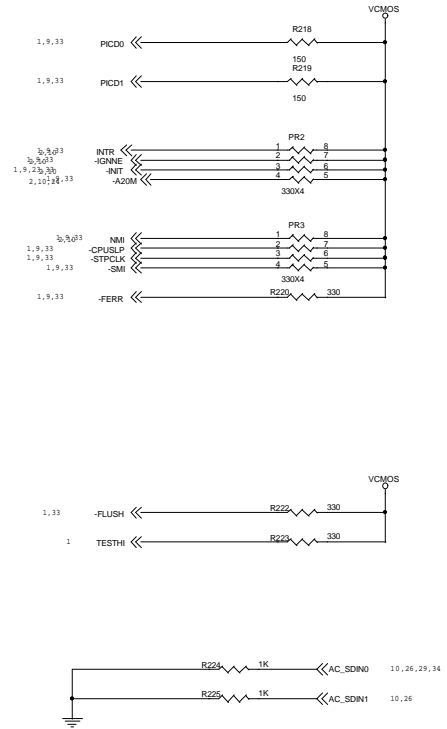
### PCI BUS



### I<sup>2</sup>C



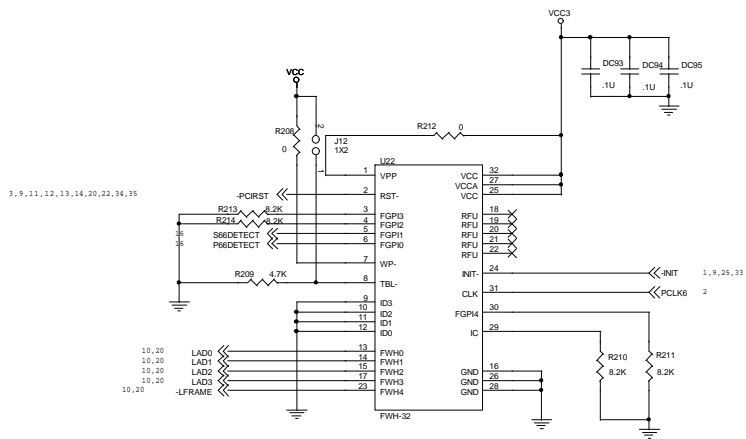
### CPU



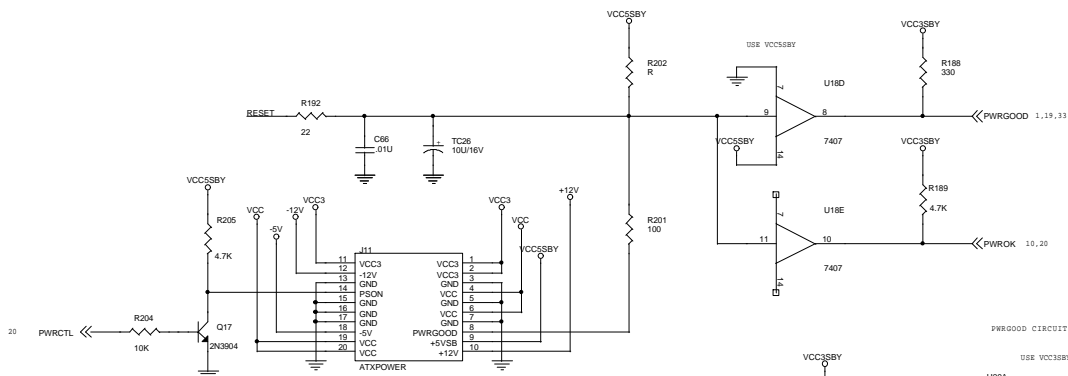
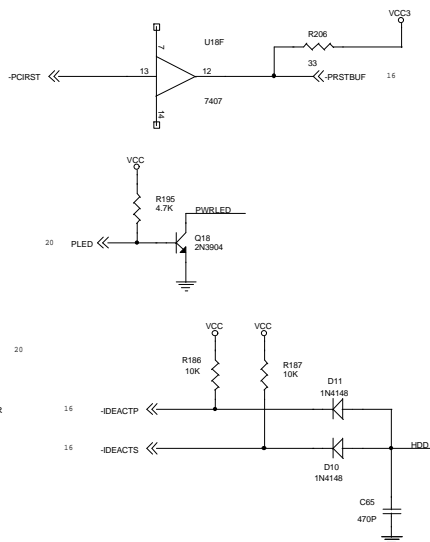
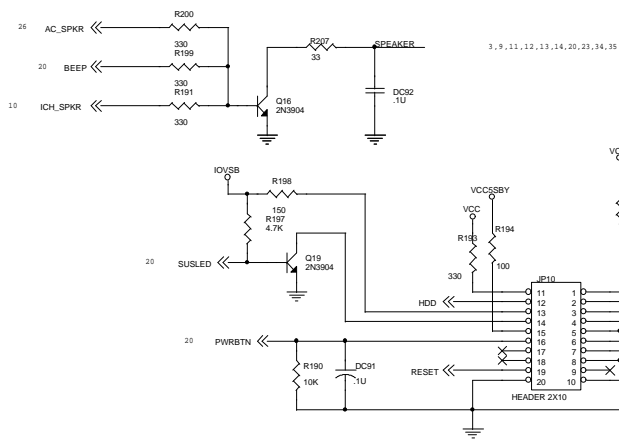
#### BUS RESISTORS

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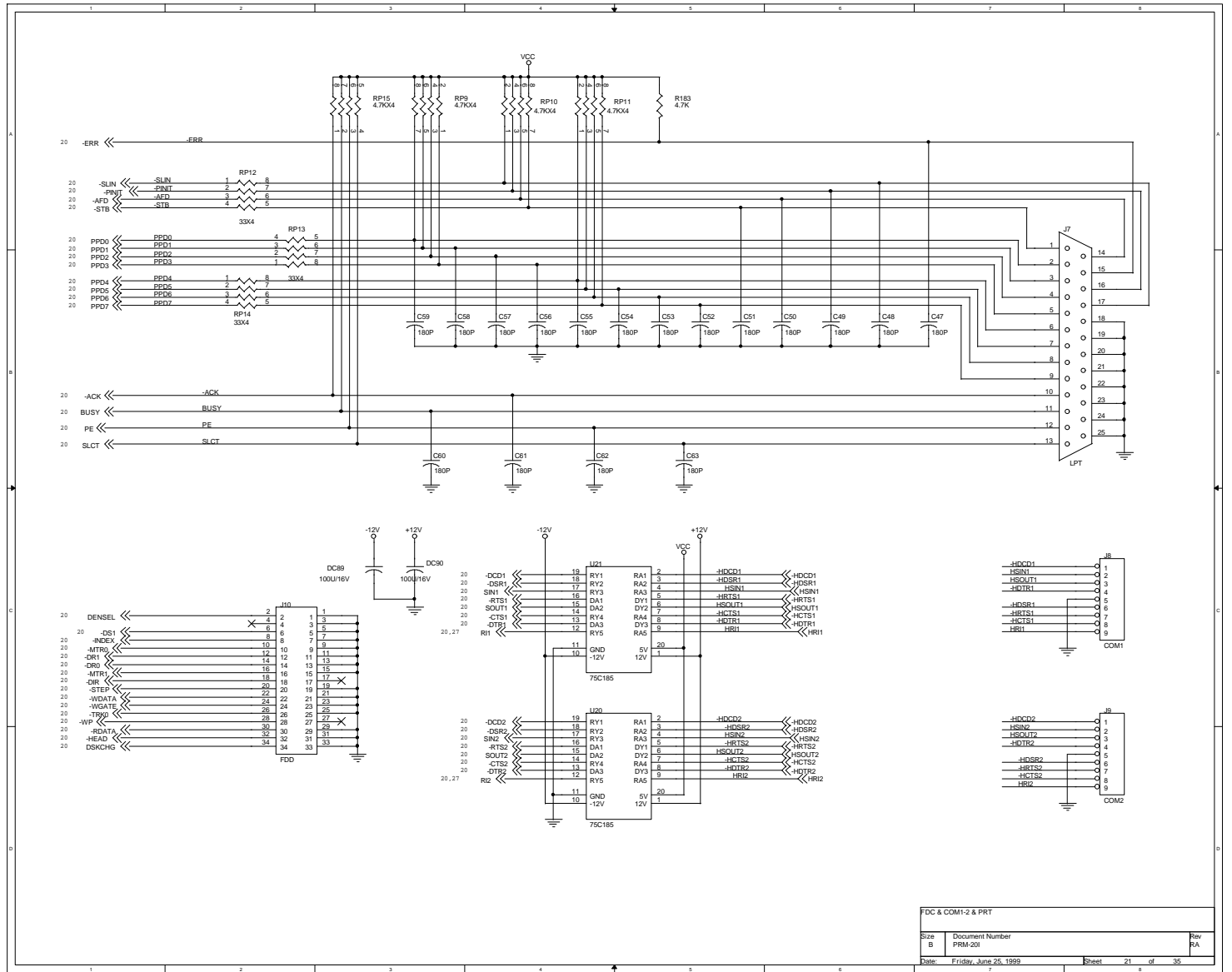


FWH		Rev
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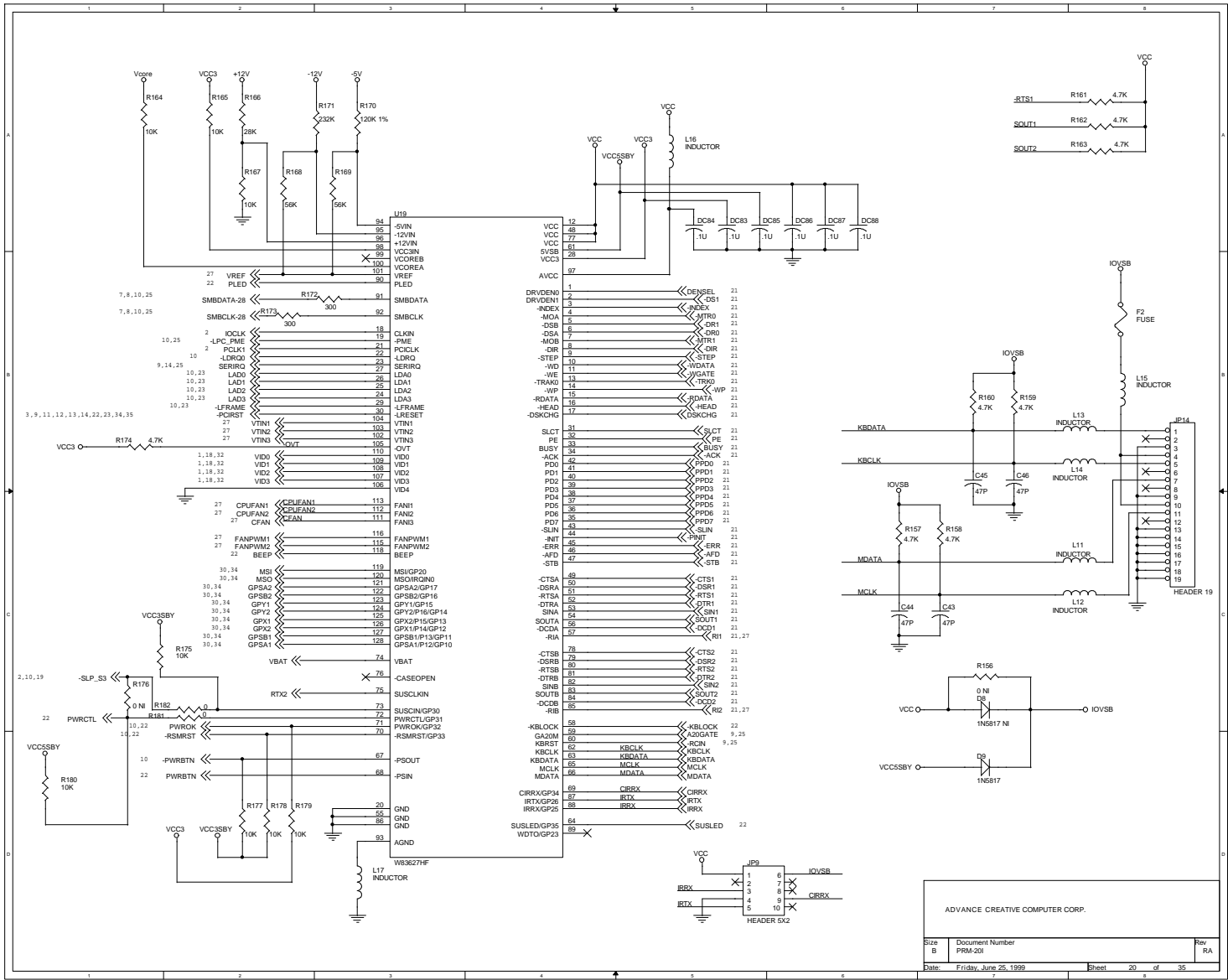
Resume Reset circuitry using a 1 msec delay and Schmitt trigger logic

RTX_PWR	
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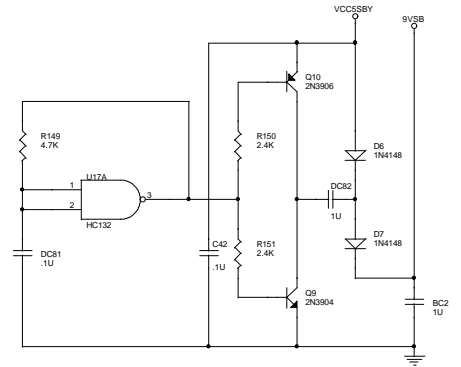
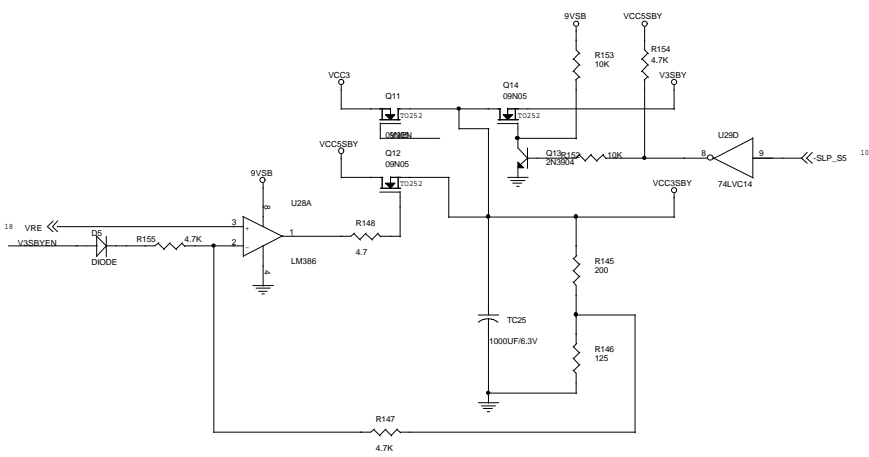
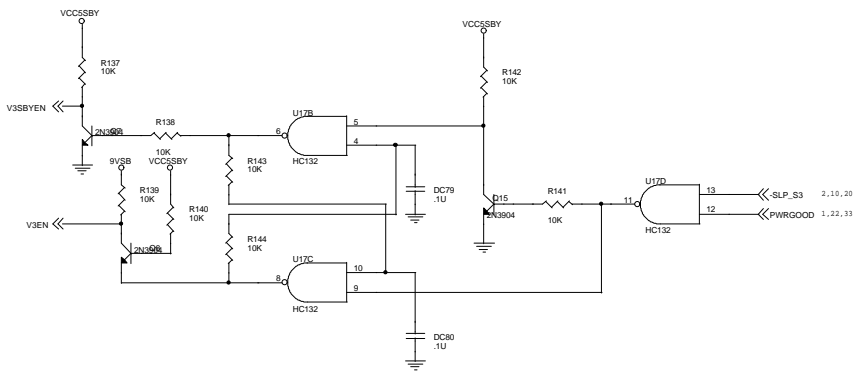


FDC & COM1-2 & PRT		
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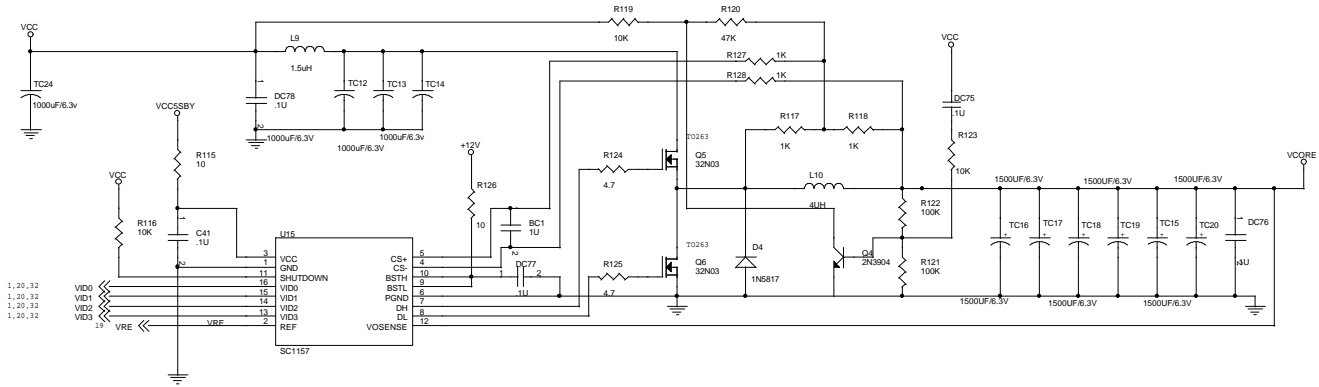




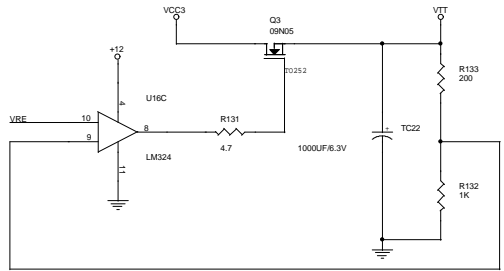
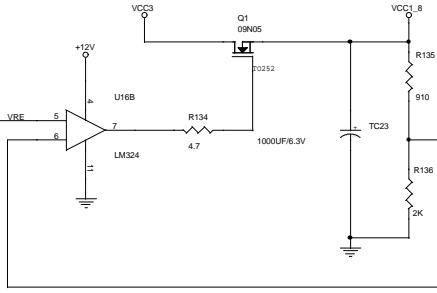
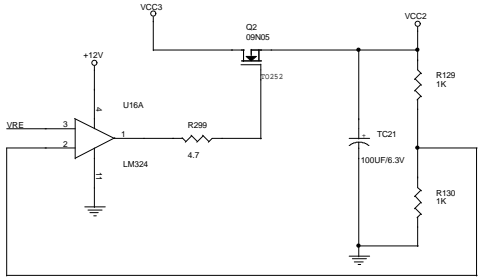
ADVANCE CREATIVE COMPUTER CORP.		
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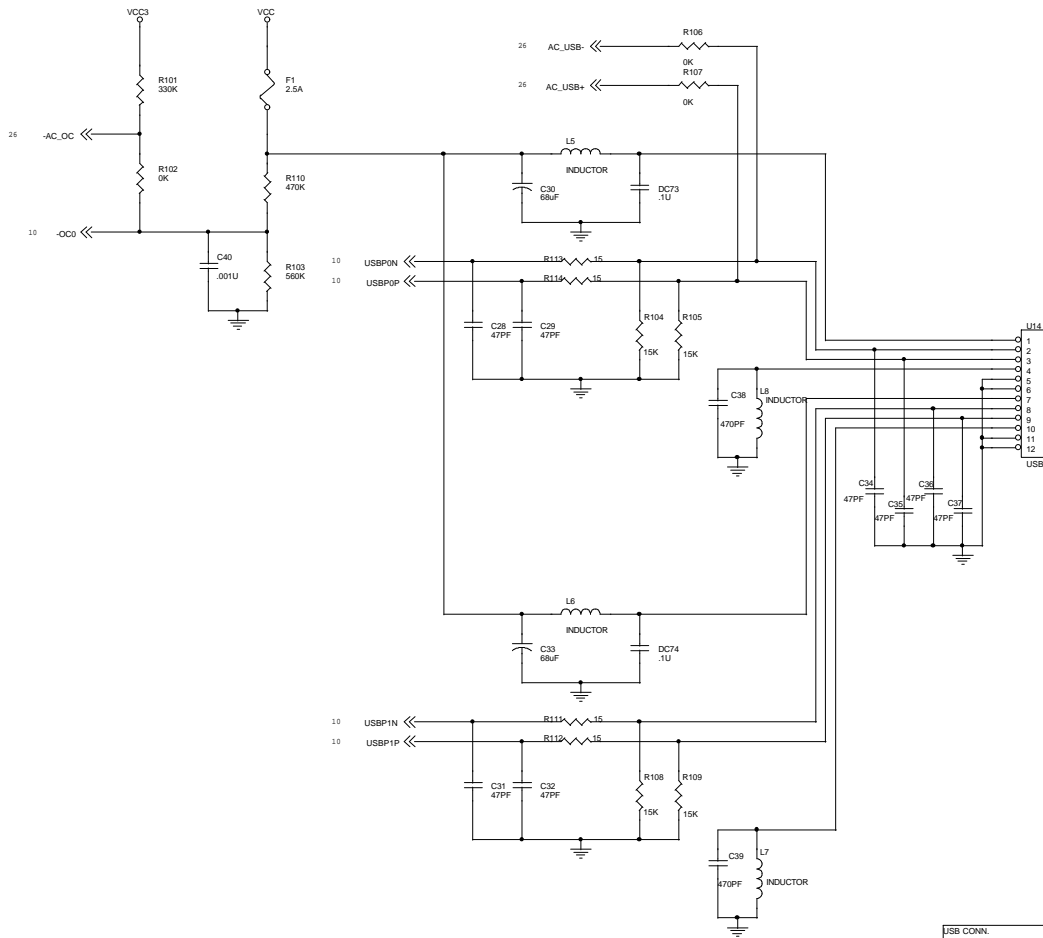
PAC CONTROL SECTION		
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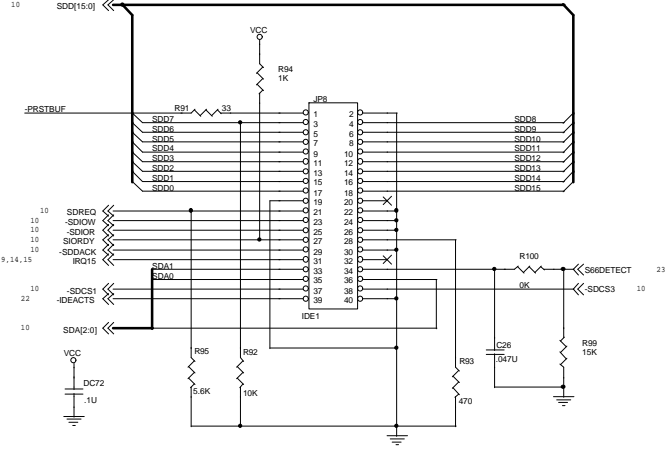
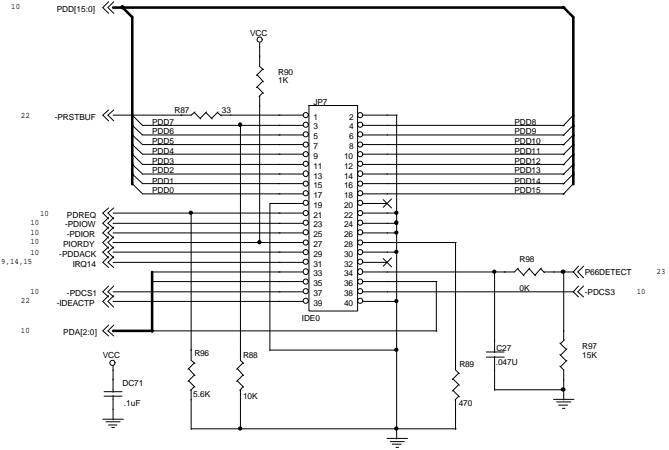
1, 20, 32  
1, 20, 32  
1, 20, 32  
1, 20, 32



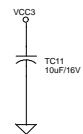
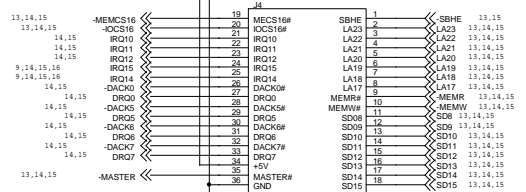
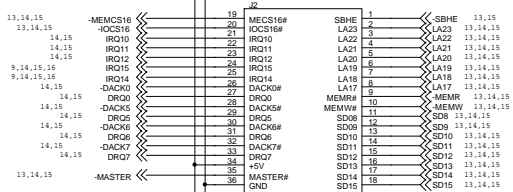
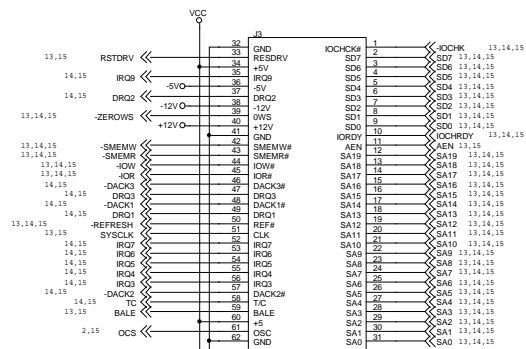
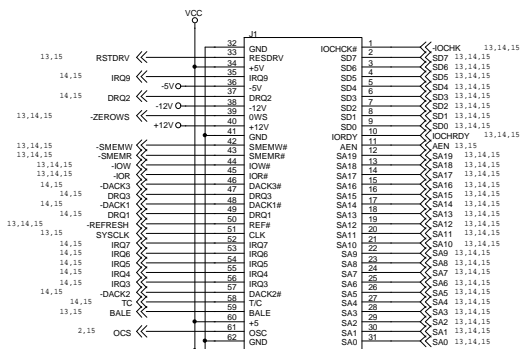
SC1157 POWER CIRCUIT		
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USB CONN.		
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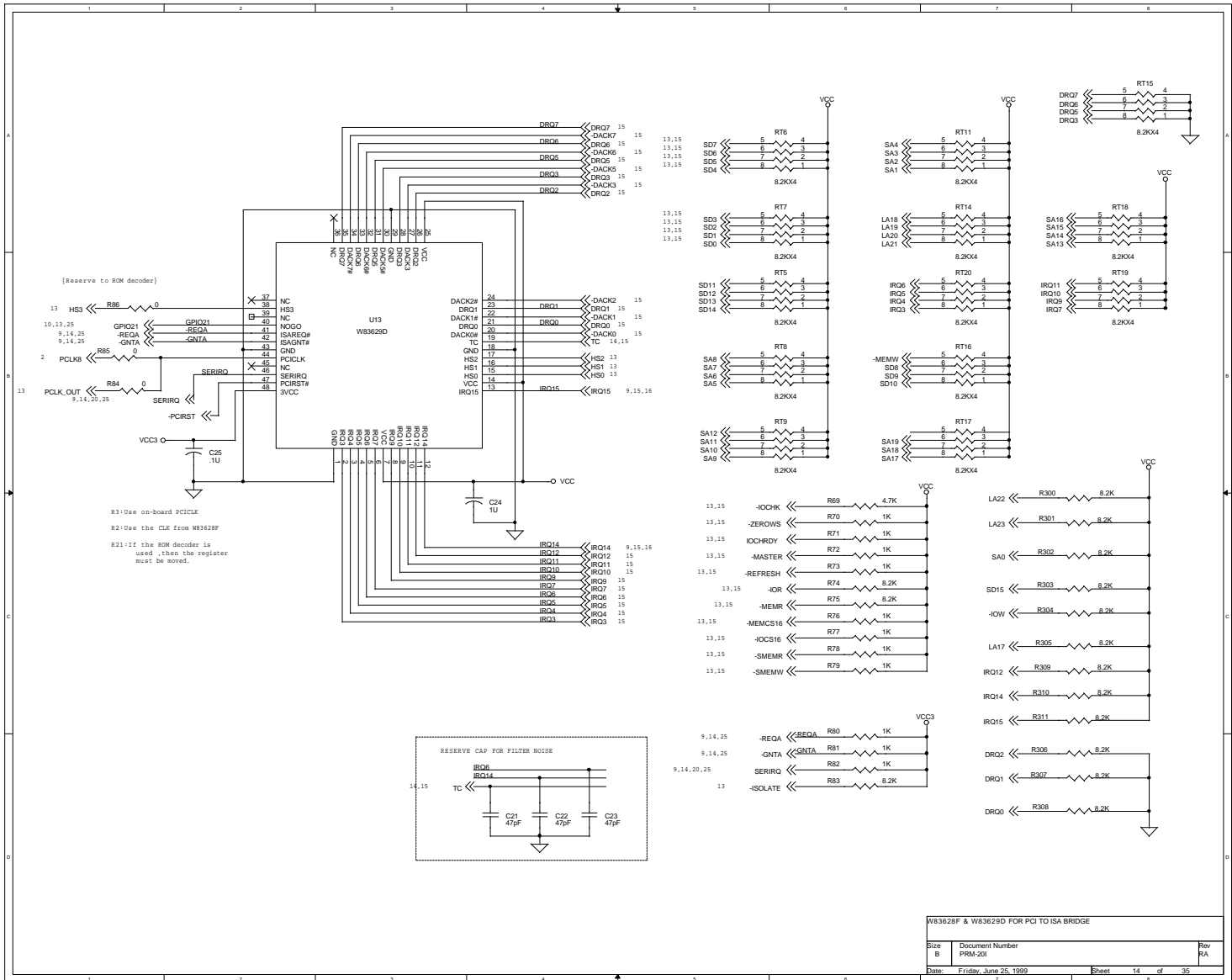


DE CONNECTORS		
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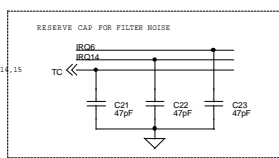


W83628F & W83629D FOR PCI TO ISA BRIDGE

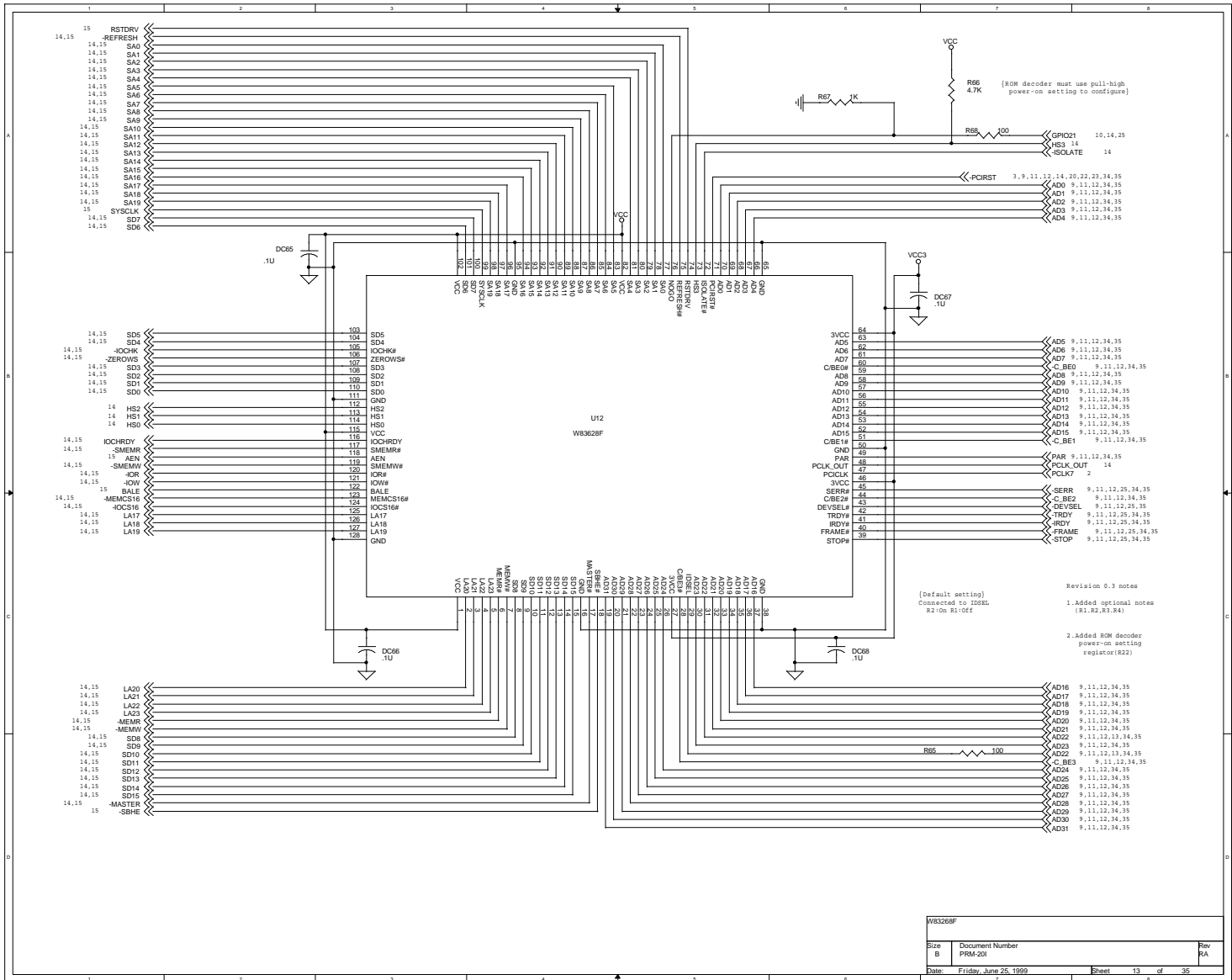
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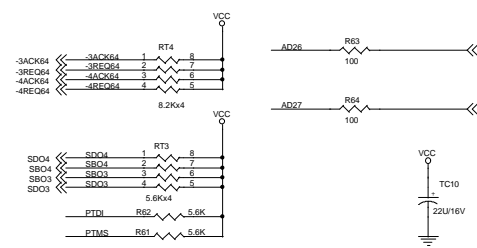
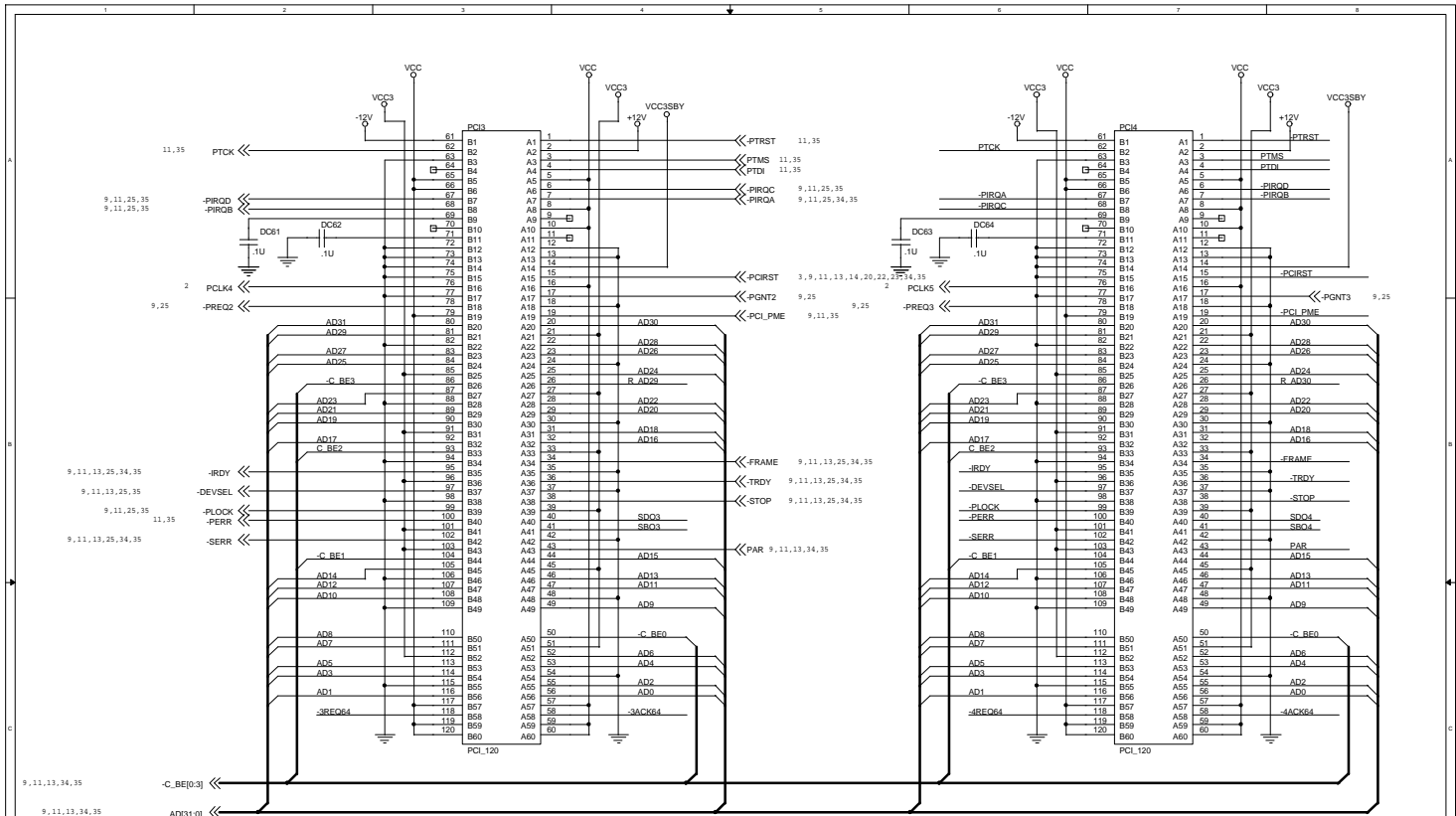
R3: Use on-board PCICLK  
 R2: Use the CLK from W83628F  
 R1: If the ROM decoder is used, then the register must be moved.



W83628F & W83629D FOR PCI TO ISA BRIDGE		
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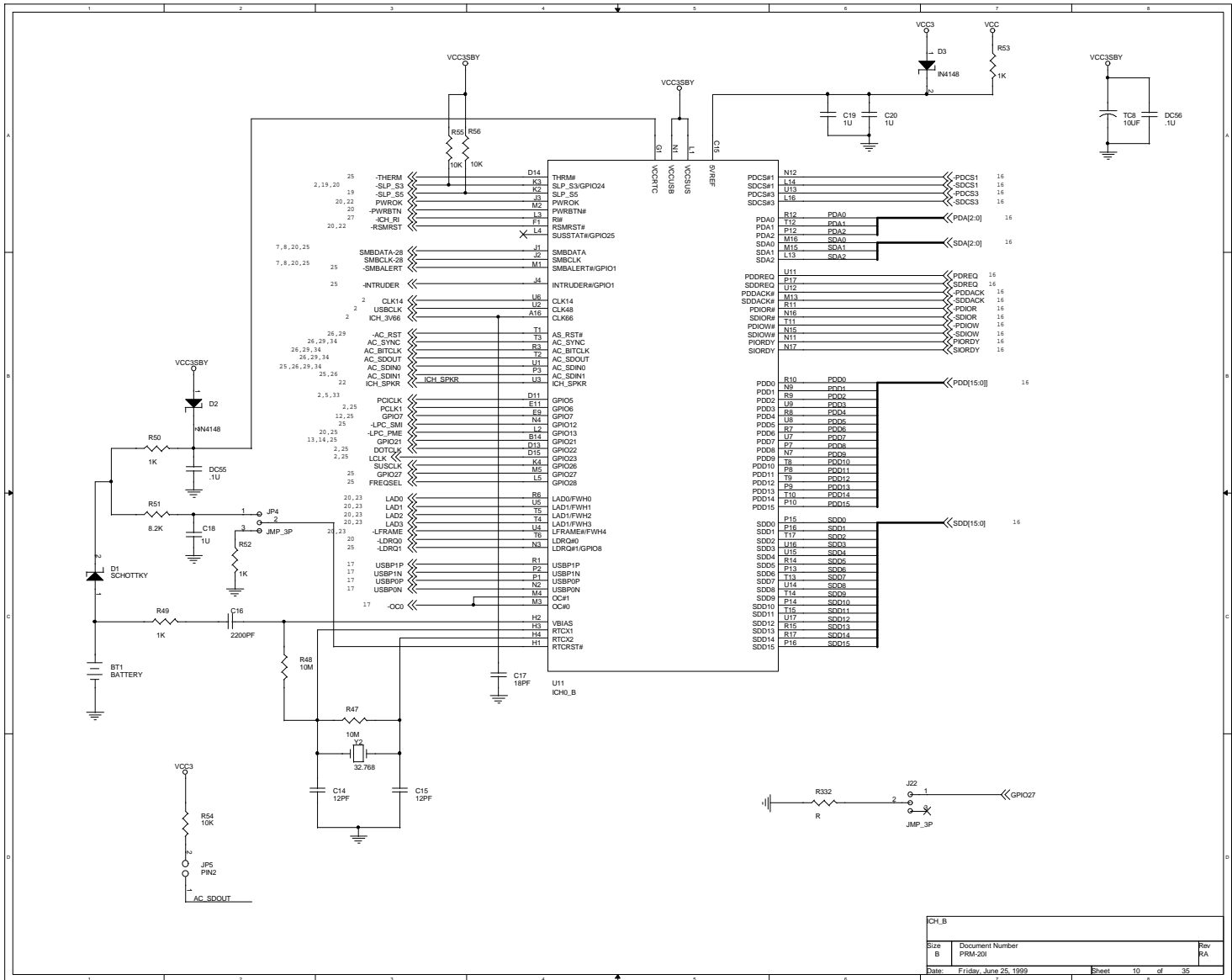




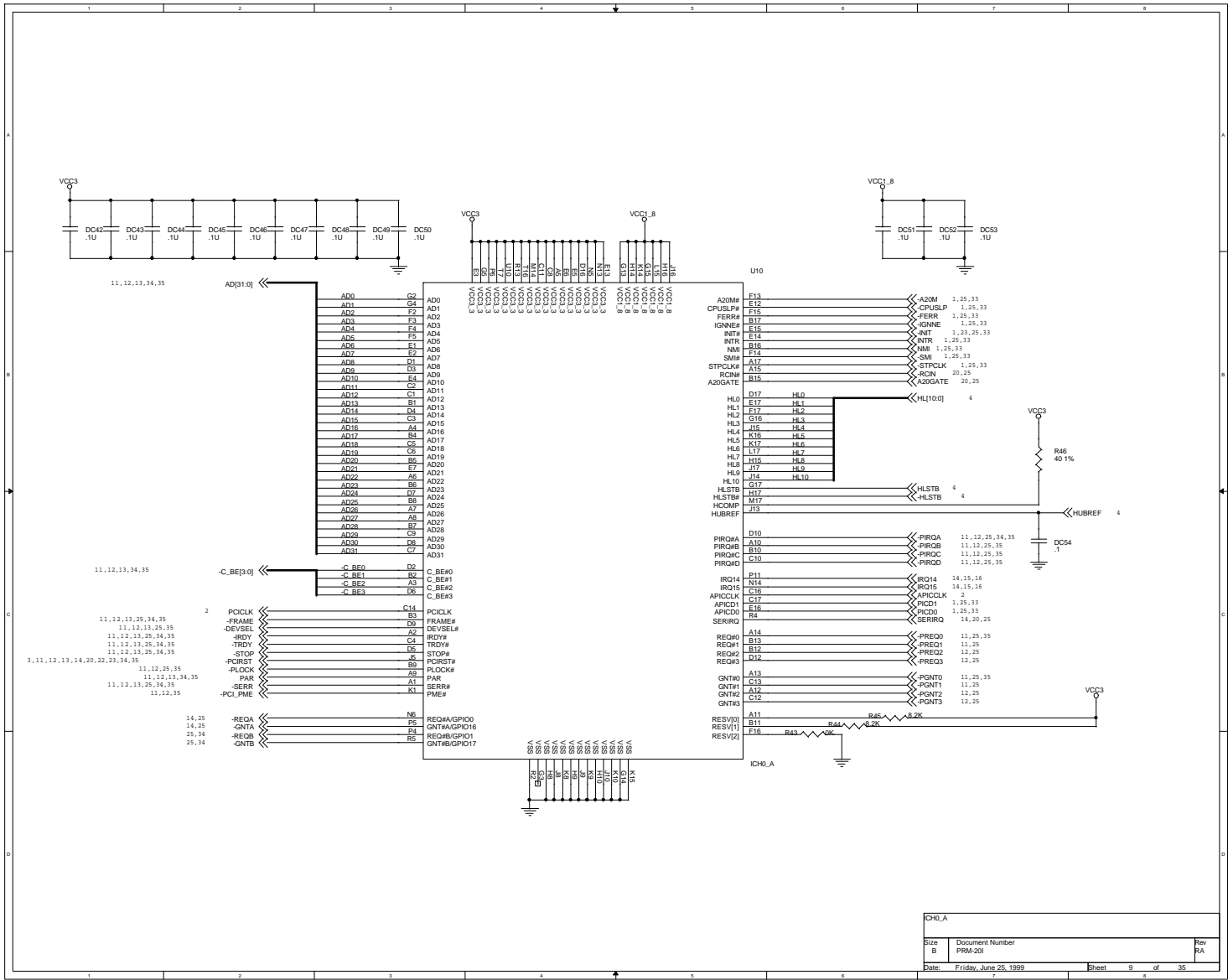


PCI SLOTS (3 & 4)		Rev
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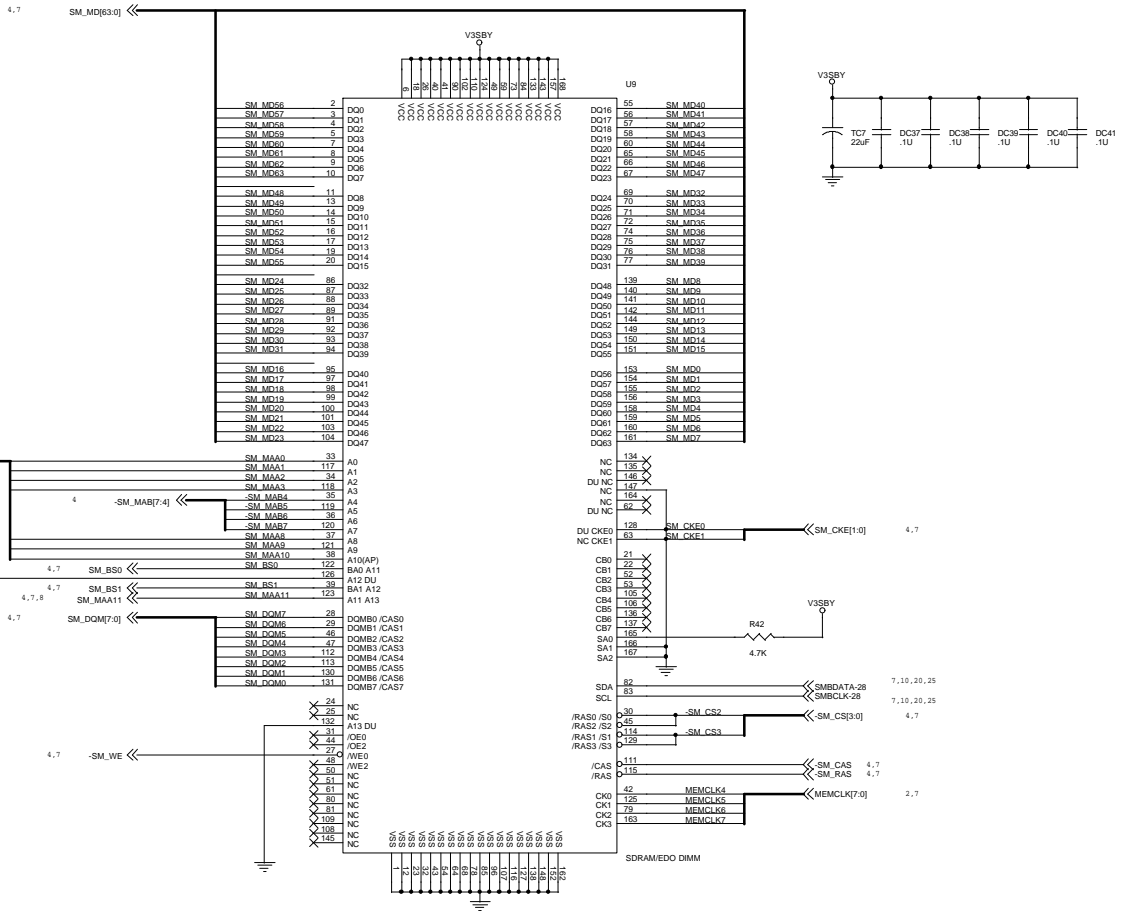


CH. B		Rev
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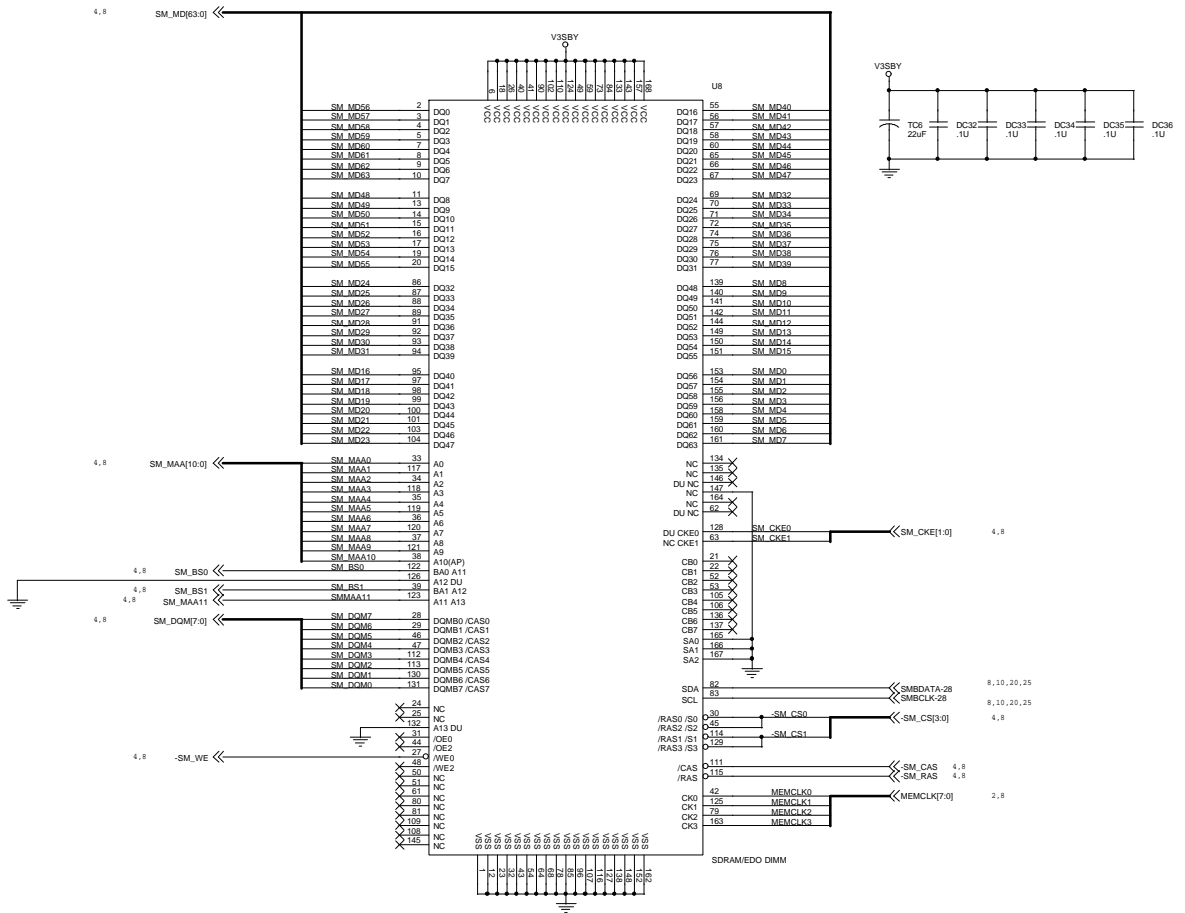
ICH0_A		Rev
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# DIMM CONNECTOR 1

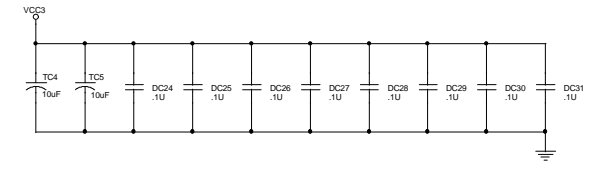
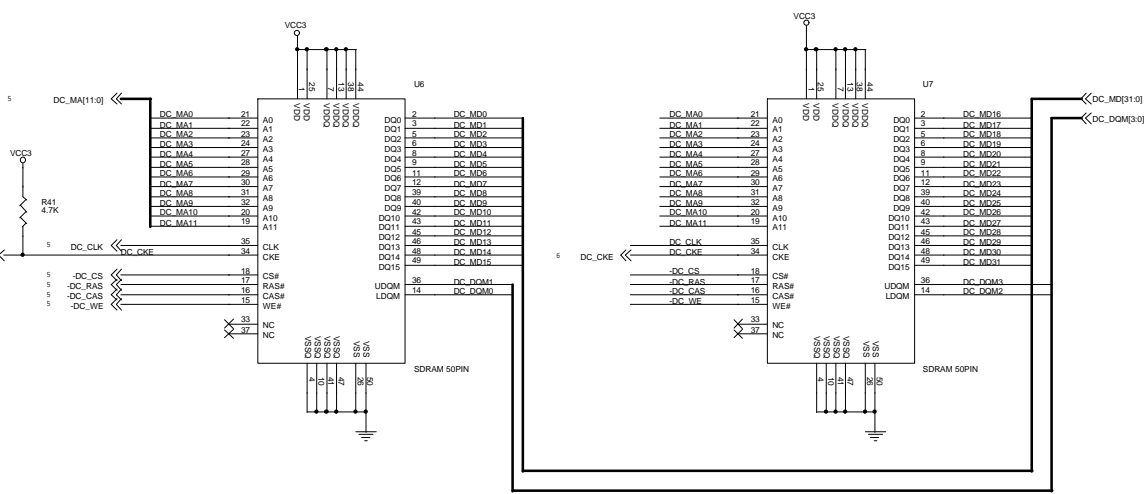


DIMM SOCKET(1)		
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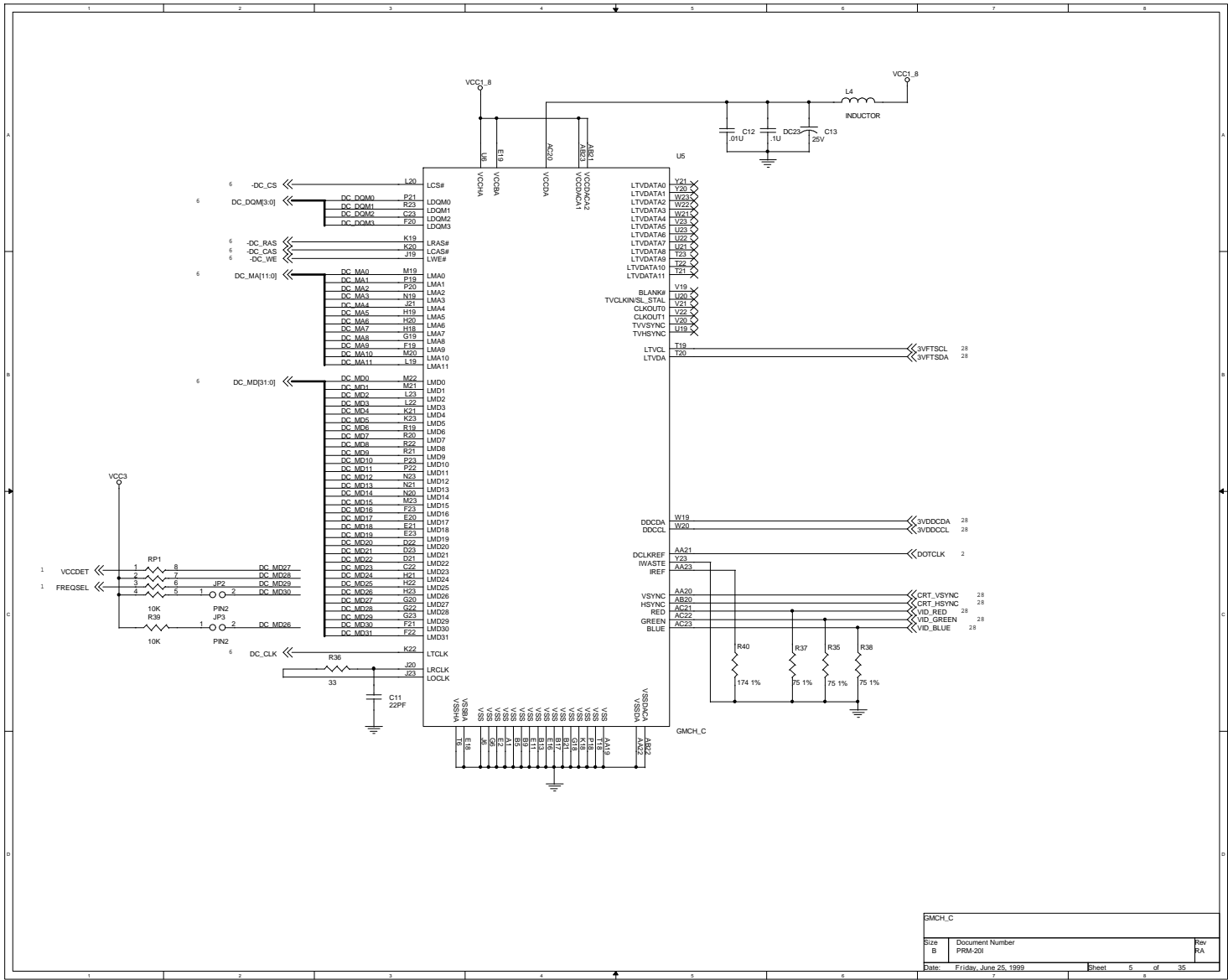
# DIMM CONNECTOR 0



DIMM SOCKET(2)		
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SDRAM 50PIN		Rev
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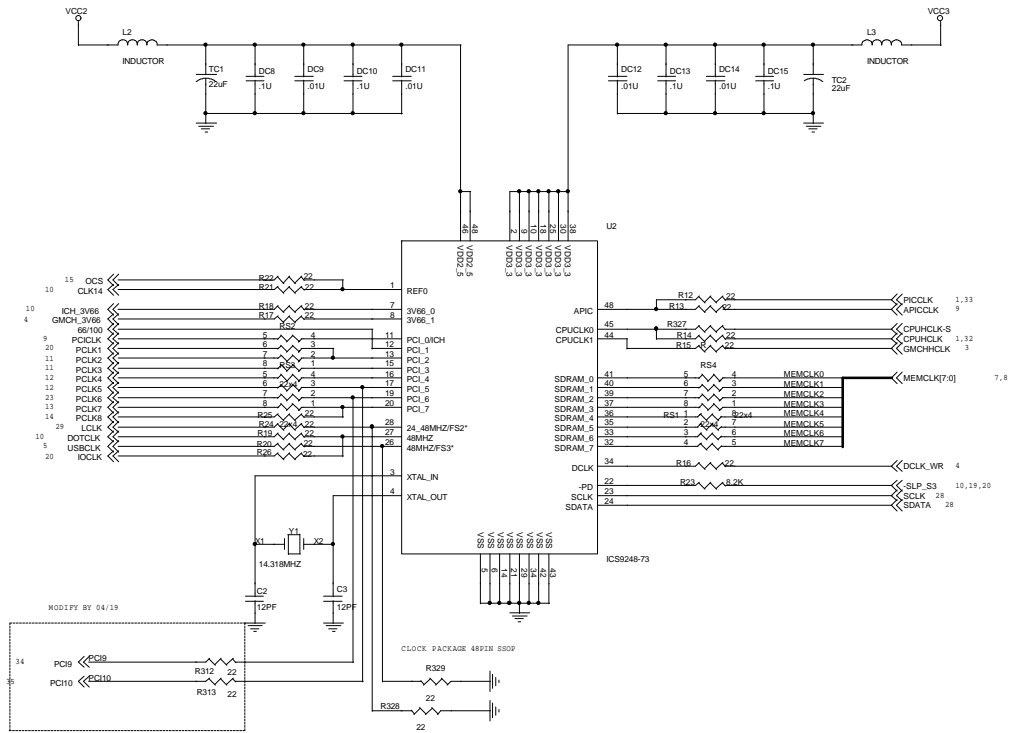


SMCH_C		
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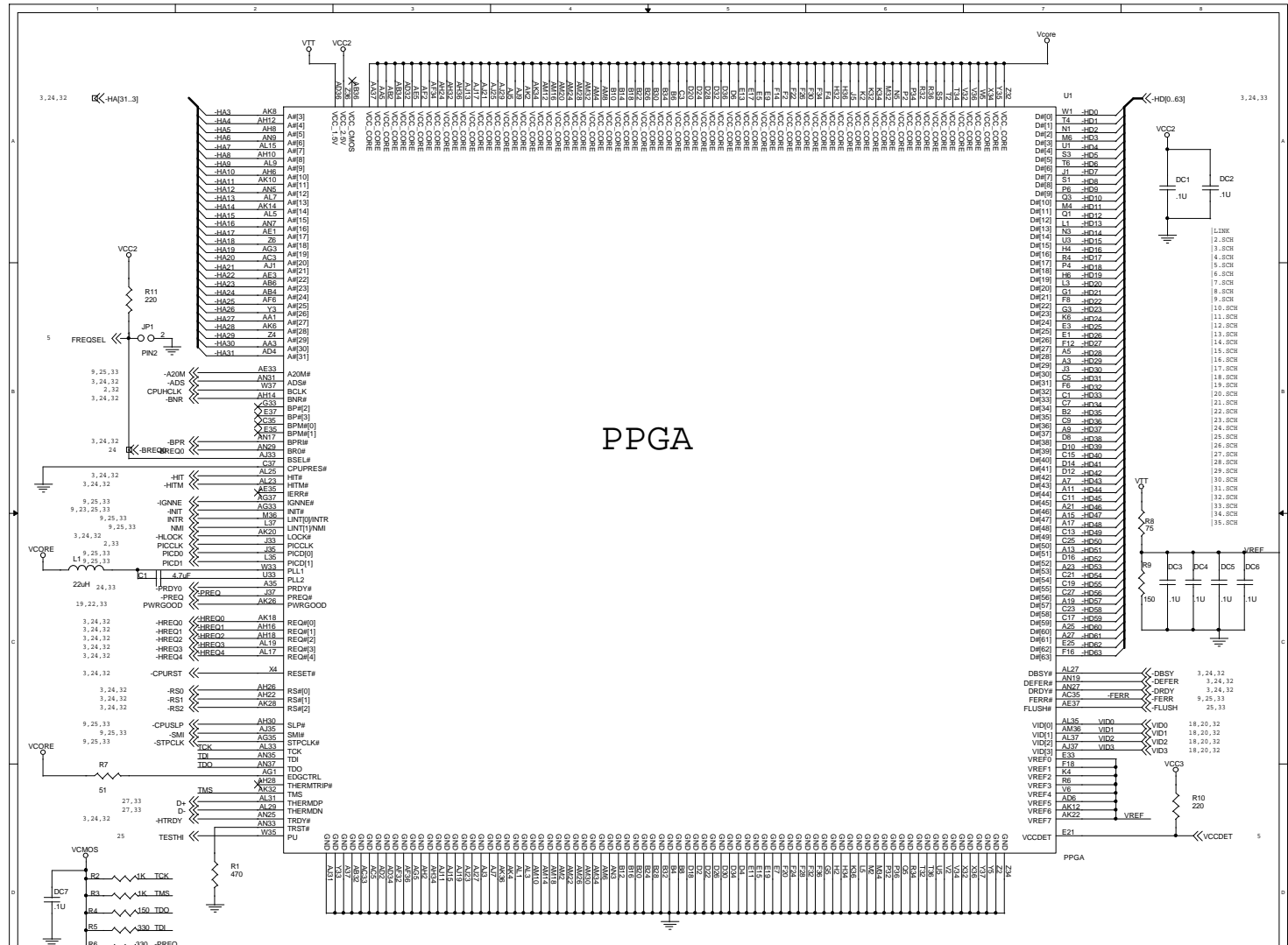








CLOCK		
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# PPGA

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