

AR-B1670
Half Size Celeron/Pentium III
CPU BOARD with LAN, VGA, and LCD
User' s Guide

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PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B1670 CPU BOARD

This guide introduces the Acrosser AR-B1670 CPU board.

The information provided in this manual describes about the card functions and features. It also helps you to start, set up and operate your AR-B1670. General system information can also be found in this publication.

0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 3, "Setting Up The System" in this guide, if you have not already installed AR-B1670. Check the packing list before you install and make sure the accessories are completely included.

The AR-B1670 CD provides the newest information regarding the CPU card. **Please refer to the files of the enclosed utility CD.** It contains the modification, hardware & software information. And it also has updated the product functions that may not be mentioned here.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original packaging for this purpose.

You can assure efficient servicing for your product by following these guidelines:

1. Include your name, address, daytime telephone and facsimile numbers and E-mail.
2. A description of the system configuration and/or software at the time is malfunction,
3. A brief description of the problem occurred.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the quality of our products and the readability of our publications. They create a very important part of input used for product enhancement and revision. In any case, we believe that the information that you provide in anyway appropriate for us to use and distribute it without incurring any obligation. You may, of course, continue to use the information you provide.

If you have any suggestions for improving particular sections of this publication or if you find any errors on it, please send your comments to Acrosser Technology Co., Ltd. or your local sales representative and indicate the manual title and book number.

Internet electronic mail to: webmaster@acrosser.com

0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller", describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumpers and the connector settings.
- Chapter 4, "CRT/LCD Flat Panel Display", describes the configuration and installation procedure for using LCD and CRT displays.
- Chapter 5, "Installation", describes setup procedures and information on the utility diskette.
- Chapter 6, "BIOS Console", provides the BIOS settings options.
- Chapter 7, Specifications
- Chapter 8, Placement & Dimensions
- Chapter 9, Programming RS-485 & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

1. Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
2. When unpacking and handling the board or other system components, place all materials on an antic static surface.
3. Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

0. OVERVIEW

This chapter provides an overview of your system's features and capabilities. The topics are covered as follow:

- Introduction
- Packing List
- Features

0.1 INTRODUCTION

The AR-B1670 makes 550MHz, industrial computing a reality. Developed for small size, high-speed system, this half-size PCI card is excellent for embedded applications due to its stand-alone operation, especially because the AR-B1670 provides an on-board LCD controller.

Great speeds are attained through the PCI-driven IDE controllers. By providing a PCI interface to these one controllers, the AR-B1670 offers an exciting option for engineers involved in high performance projects. Also, the BIOS is available for the interface with peripherals quickly and easily. The AR-B1670 comes with 2MB V-RAM onboard, one RS-232C and one RS-232C/RS-485 serial port, and one-168PIN DIMM connectors, which can support up to 256MB of SDRAM.

The AR-B1670 is perfect for medical and telecommunications applications, factory floor networks. It uses as a MMI for high-speed processes, or as a controller for graphics intensive systems.

0.2 PACKING LIST

These accessories are included with the system. Before you begin installing your AR-B1670 board, please make sure that the following items have been included inside the AR-B1670 package.

- The quick setup manual
- 1 AR-B1670 CPU board
- 1 Hard disk drive adapter cable
- 1 Floppy disk drive adapter cable
- 1 Parallel port adapter cable mounted on one bracket.
- 1 RS-232 & PS/2 Mouse interface cable mounted on one bracket.
- 1 Software utility CD

0.3 FEATURES

The AR-B1670's features are summarized as follow:

Form Factor

- Half size PCI slot card (122 mm by 185 mm)

Processor

- 370-contact processor pin grid array PGA370S socket
- Support for the Intel® Celeron™ processor on the 66-MHz host bus
- PIII™ and Cyrix III processor on the 100-MHz host bus

Chipset Intel® 82440BX AGPset, consisting of:

- Intel® 82443BX PCI/AGP controller (PAC)
- Intel® 82371EB PCI/ISA IDE Xcelerator (PIIX4E)

Memory

- One 168-contact DIMM sockets
- Support for up to 256 MB of 66-MHz and 100MHz, synchronous DRAM (SDRAM)

I/O Control

- SMSC FDC37C672 I/O controller

Peripheral Interfaces

- One IDE interface
- One floppy interface
- Two serial ports
- One touch screen serial port
- One USB ports
- One parallel port
- PS/2 keyboard
- PS/2 mouse

LAN Subsystem

- Real tech 8139C 10/100 Mbps PCI LAN controller
- RJ-45 LAN connector

Graphics Subsystem

- Integrated Chips 69000 HiQVideo™ Accelerator with Integrated 2MB video memory
- Support either CRT or flap panel display
- High-Performance Flat Panel Display resolutions and color depth at 3.3V
 - 640x480 x 24bpp
 - 800x600 x 24bpp
 - 1024x768 x 16bpp
 - 1280x1024 x 8bpp

BIOS

- AMI BIOS stored in 39SF020 2 Mb flash memory

1. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1670 CPU boards. The topics are covered as follow:

- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port

1.1 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented on the AR-B9625 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high-speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The Following is the system information for the DMA channels:

Slave with four 8-bit chnls	Master with three 16-bit chnls
DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4(0): Cascade for controller 1
Channel 1: IBM SDLC	Channel 5(1): Spare
Channel 2: Diskette adapter	Channel 6(2): Spare
Channel 3: Spare	Channel 7(3): Spare

Table 1-1 DMA Channel Controller

1.2 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the output buffer of the keyboard controller. Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send and receive routines.

1.3 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B9625 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute. These two controllers are cascaded with the second controller representing IRQ8 to IRQ15, which is rerouted through IRQ2 on the first controller.

The following is the system information of interruption levels:

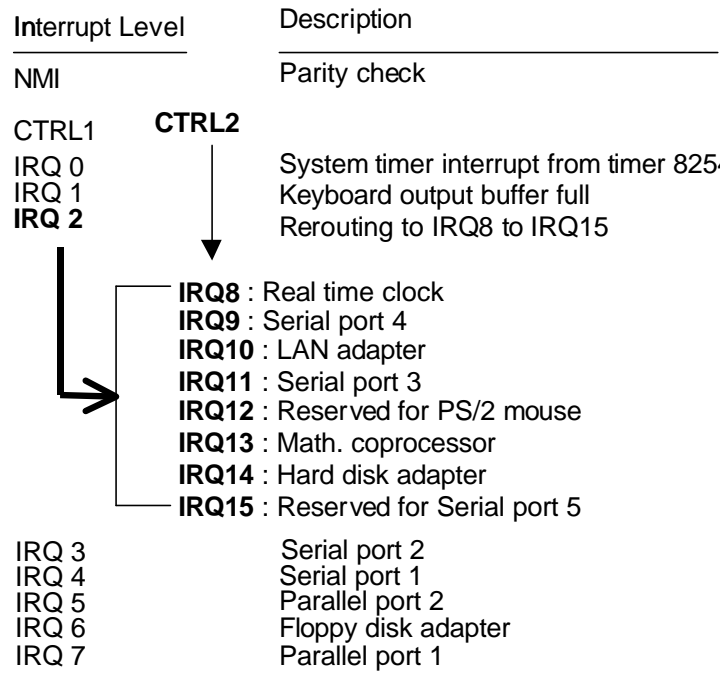


Figure 1-1 Interrupt Controller

1.3.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	AR-B1670 :Intel 440BX Chipset Address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
076-077	Watchdog
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 3 (LPT 3)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/Streaming Type Adapter
378-37F	Parallel printer port 2 (LPT 2)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 1 (LPT 1)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/Graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 1-2 I/O Port Address Map

1.3.2 PCI Bus Assignments (Bus1)

Pin	Signal Name	Pin	Signal Name
A1	-TRST	B1	-12V
A2	+12V	B2	TCK
A3	TMS	B3	GND
A4	TDI	B4	TD0
A5	+5V	B5	+5V
A6	-INTA	B6	+5V
A7	-OMTC	B7	-INTB
A8	+5V	B8	-INTD
A9	NC	B9	-PRST 1
A10	+5V	B10	NC
A11	NC	B11	-PRST 2
A12	GND	B12	GND
A13	GND	B13	GND
A14	NC	B14	NC
A15	-RST	B15	GND
A16	+5V	B16	CLK
A17	-GNT	B17	GND

Pin	Signal Name	Pin	Signal Name
A18	GND	B18	-REQ
A19	NC	B19	+5V
A20	AD30	B20	AD31
A21	+3.3V	B21	AD29
A22	AD28	B22	GND
A23	AD26	B23	AD27
A24	GND	B24	AD25
A25	AD24	B25	+3.3V
A26	IDSEL	B26	C/BE3
A27	+3.3V	B27	AD23
A28	AD22	B28	GND
A29	AD20	B29	AD21
A30	GND	B30	AD19
A31	AD18	B31	+3.3V
A32	AD16	B32	AD17
A33	+3.3V	B33	C/BE2
A34	-FRAME	B34	GND
A35	GND	B35	-IRDY
A36	-TRDY	B36	+3.3V
A37	GND	B37	-DEVSEL
A38	-STOP	B38	GND
A39	+3.3V	B39	-LOCK
A40	SDONE	B40	-PERR
A41	-SB0	B41	+3.3V
A42	GND	B42	-SERR
A43	PAR	B43	+3.3V
A44	AD15	B44	C/BE1
A45	+3.3V	B45	AD14
A46	AD13	B46	GND
A47	AD11	B47	AD12
A48	GND	B48	AD10
A49	AD9	B49	GND

Table 1-3 PCI Bus Assignments

Pin	Signal Name	Pin	Signal Name
C1	C/BE0	D1	AD8
C2	+3.3V	D2	AD7
C3	AD6	D3	+3.3V
C4	AD4	D4	AD5
C5	GND	D5	AD3
C6	AD2	D6	GND
C7	AD0	D7	AD1
C8	+5V	D8	+5V
C9	-REQ64	D9	-ACK64
C10	+5V	D10	+5V
C11	+5V	D11	+5V

Table 1-4 PCI Bus Assignments

1.3.3 Real-Time Clock and Non-Volatile RAM

The AR-B1670 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because it uses CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 1-5 Real-Time Clock & Non-Volatile RAM

1.3.4 Timer

The AR-B1670 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

1.4 SERIAL PORTS

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) not only used to convert parallel data to a serial format on the transmit side but also used to convert serial data to parallel on the receiver side. The serial format is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, 1.5 (in a five-bit format only) or two stop bits (in a 6,7, or 8-bit format) in order to transmission and reception. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are not only included the use of this 16x clock to drive the receiver logic but also included in the ACE is as a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table gives a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

Table 1-6 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 1-7 Serial Port Divisor Latch

1.5 PARALLEL PORT**(1) Register Address**

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 1-8 Registers' Address

(2) Printer Interface Logic

The parallel portion of the SMC37C672 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level possible.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

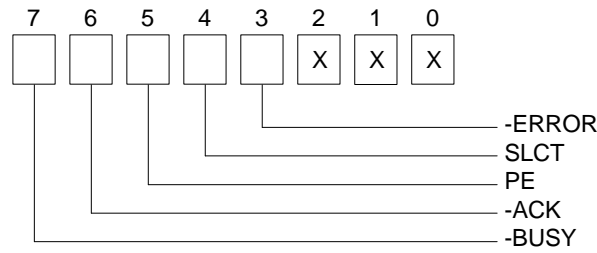


Figure 1-2 Printer Status Buffer

NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

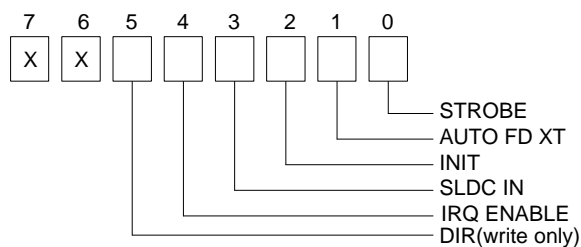


Figure 1-3 Bit's Definition

NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is writing only.

Bit 4: A 1 in this position allows an interruption to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

2. SETTING UP THE SYSTEM

This chapter describes the pin assignments for the system's external connectors and jumper settings.

- Overview
- System Settings

2.1 OVERVIEW

The AR-B1670 is a Pentium II/III grade single CPU boards. This section provides hardware and jumper settings, connector locations, and pin assignments.

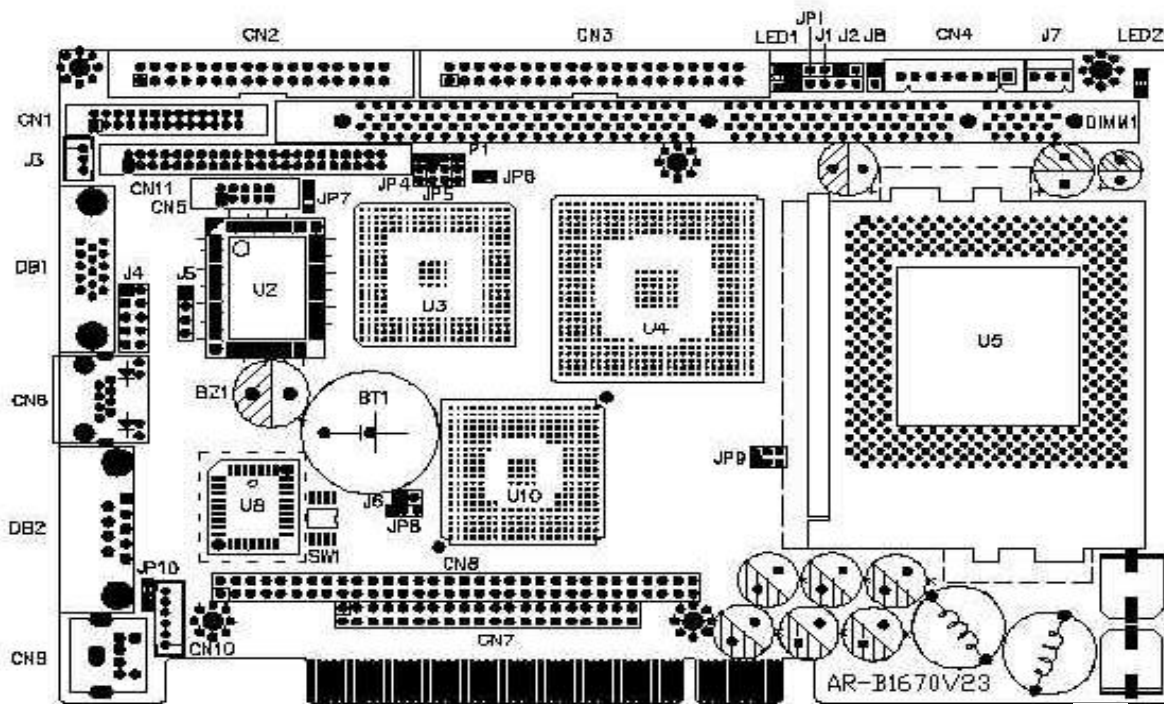


Figure 2-1 External System Location

2.2 SYSTEM SETTINGS

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of the jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1670 jumper pins, and the factory-default settings.

CAUTION: Do not touch any electronic components unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

2.2.1 Hard Disk (IDE) Connector (CN3)

A 40-pin header type connector (CN3) is provided to interface with up to two embedded hard disk drives (IDE PCI bus). This interface, through a 40-pin cable, allows the user to connect up to two drives in a “daisy chain” fashion. To enable or disable the hard disk controller, please use the BIOS Setup program. The following table illustrates the pin assignments of the hard disk drive's 40-pin connector.

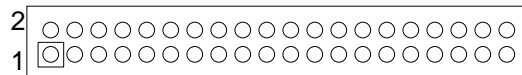


Figure 2-2 CN3: Hard Disk (IDE) Connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	DRQ A	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	-CHRDY A	28	NOT USED
29	DACK A	30	GROUND
31	-IRQ A	32	NOT USED
33	SA 1	34	NOT USED
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND

Table 2-1 HDD Pin Assignment

2.2.2 PC/104 Connector

(1) 64-Pin PC/104 Connector Bus A & B (CN8)

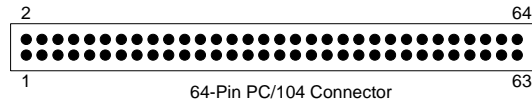


Figure 2-3 CN8: 64-Pin PC/104 Connector Bus A & B

		CN8			
		1	2		
-IOCHCK ---	A1	●	●	B1	--- GND
SD7 ---	A2	●	●	B2	--- RSTDRV
SD6 ---	A3	●	●	B3	--- +5 VDC
SD5 ---	A4	●	●	B4	--- IRQ9
SD4 ---	A5	●	●	B5	--- -5 VDC
SD3 ---	A6	●	●	B6	--- DRQ2
SD2 ---	A7	●	●	B7	--- -12 VDC
SD1 ---	A8	●	●	B8	--- ZWS
SD0 ---	A9	●	●	B9	--- +12 VDC
IOCHRDY ---	A10	●	●	B10	--- GND
AEN ---	A11	●	●	B11	--- -SMEMW
SA19 ---	A12	●	●	B12	--- -SMEMR
SA18 ---	A13	●	●	B13	--- -IOW
SA17 ---	A14	●	●	B14	--- -IOR
SA16 ---	A15	●	●	B15	--- -DACK3
SA15 ---	A16	●	●	B16	--- DRQ3
SA14 ---	A17	●	●	B17	--- -DACK1
SA13 ---	A18	●	●	B18	--- DRQ1
SA12 ---	A19	●	●	B19	--- -REFRESH
SA11 ---	A20	●	●	B20	--- BUSCLK
SA10 ---	A21	●	●	B21	--- IRQ7
SA9 ---	A22	●	●	B22	--- IRQ6
SA8 ---	A23	●	●	B23	--- IRQ5
SA7 ---	A24	●	●	B24	--- IRQ4
SA6 ---	A25	●	●	B25	--- IRQ3
SA5 ---	A26	●	●	B26	--- -DACK2
SA4 ---	A27	●	●	B27	--- TC
SA3 ---	A28	●	●	B28	--- BALE
SA2 ---	A29	●	●	B29	--- +5 VDC
SA1 ---	A30	●	●	B30	--- OSC
SA0 ---	A31	●	●	B31	--- GND
GND ---	A32	●	●	B32	--- GND

Figure 2-4 CN8: 64-Pin PC/104 Connector Bus A & B

(2) 40-Pin PC/104 Connector Bus C & D (CN7)

		CN7			
		1	2		
GND ---	C1	●	●	D1	--- GND
-BHE ---	C2	●	●	D2	--- -MEM16
LA23 ---	C3	●	●	D3	--- -IOCS16
LA22 ---	C4	●	●	D4	--- IRQ10
LA21 ---	C5	●	●	D5	--- IRQ11
LA20 ---	C6	●	●	D6	--- IRQ12
LA19 ---	C7	●	●	D7	--- IDEIRQA
LA18 ---	C8	●	●	D8	--- IDEIRQB
LA17 ---	C9	●	●	D9	--- -DACK0
-MEMR ---	C10	●	●	D10	--- DRQ0
-MEMW ---	C11	●	●	D11	--- -DACK5
SD8 ---	C12	●	●	D12	--- DRQ5
SD9 ---	C13	●	●	D13	--- -DACK6
SD10 ---	C14	●	●	D14	--- DRQ6
SD11 ---	C15	●	●	D15	--- -DACK7
SD12 ---	C16	●	●	D16	--- DRQ7
SD13 ---	C17	●	●	D17	--- +5 VDC
SD14 ---	C18	●	●	D18	--- -MASTER
SD15 ---	C19	●	●	D19	--- GND
Not Used ---	C20	●	●	D20	--- GND

Figure 2-5 CN7: 40-Pin PC/104 Connector Bus C & D

(3) PC/104 Bus Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 – SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence: (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 2-2 PC/104 Bus Signal Description

2.2.3 Keyboard and PS2 Mouse Connector

(1) 6-Pin Mini DIN Keyboard Connector (CN9)

The CN9 is a Mini-DIN 6-pin connector. This keyboard connector is PS/2 type keyboard connector. This connector is also for a standard IBM-compatible keyboard when used with the included keyboard adapter cable.

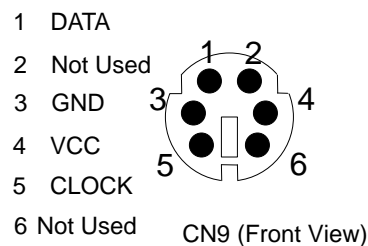
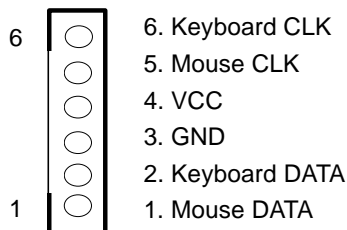


Figure 2-6 CN9: 6-Pin Mini DIN Keyboard Connector

(2) PS2 Mouse and Keyboard connector (CN10)

CN10 provides connection of PS2 mouse and Keyboard. Those pins for keyboard are parallel with CN9, which provides another selection of connecting with keyboard.



2.2.4 FDD Port Connector (CN2)

The AR-B1670 provides a 34-pin header type connector for supporting up to two floppy disk drives. To enable or disable the floppy disk controller, please use the BIOS Setup program.

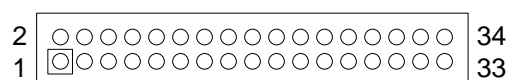


Figure 2-7 CN2: FDD Port connector

Pin	Signal	Pin	Signal
1-33(odd)	GROUND	18	-DIRECTION
2	DRVEN 0	20	-STEP OUTPUT PULSE
4	NOT USED	22	-WRITE DATA
6	DRVEN 1	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE 0	28	-WRITE PROTECT
12	-DRIVE SELECT 1	30	-READ DATA
14	-DRIVE SELECT 0	32	-SIDE 1 SELECT
16	-MOTOR ENABLE 1	34	DISK CHANGE

Table 2-3 FDD Pin Assignments

2.2.5 Parallel Port Connector (CN1)

To use the parallel port, an adapter cable has to be connected to the CN1 (26-pin header type) connector. The connector for the parallel port is a 25-pin D-type female connector.

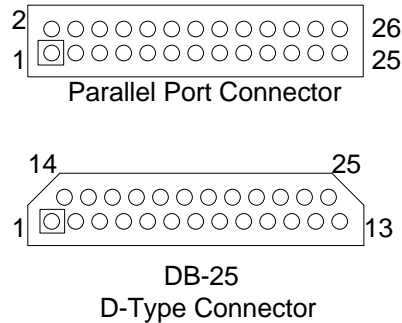


Figure 2-8 CN1: Parallel Port Connector

CN1	DB-25	Signal	CN1	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	No Used

Table 2-4 Parallel Port Pin Assignments

2.2.6 Serial Port

AR-B1670 is equipped with two serial ports. COM-A is a standard RS-232 interface. It uses DB2 to connect with other equipments. If you want to connect COM-A to a RS-485 network, you should connect an external RS-485 adaptor to DB2 and adjust jumper position of JP10. AR-M9912 RS-485 converter is a good solution to convert RS-232 to isolated RS-485 interface. COM-B uses CN5 and an adaptor cable to interface with external equipment. It can be configured as a RS-485 or RS-232 port. Configuring JP5 can configure COM-B as an RS-232 or RS-485. You can also use AR-M9912 to converter COM-B as an isolated RS-485 port.

(1) RS-232/RS-485 Select (JP5, JP7 & JP10)

(A) COM-A RS-485 Adapter Select (JP10)

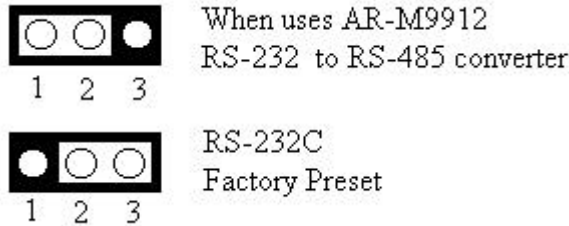


Figure 2-9 JP10: COM-A RS-485 Adapter Select

(B) COM-B RS-485 Adapter Select (JP7)

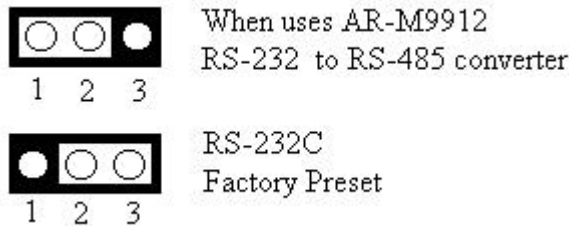


Figure 2-10 JP7: COM-B RS-485 Adapter Select

(C) COM-B RS-232C/RS-485 Select (JP5)

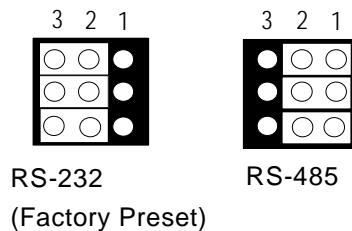
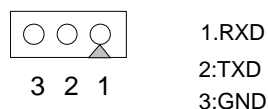


Figure 2-11 JP5: COM-B RS-232C/RS-485 Select

(D) Touch Screen Connector (J3)

J3 is a serial port, which is parallel with COM-B. It provides another choice when user needs a serial port but need to connect from board directly without connecting through a D-type connector. The typical application is a touch screen panel.



(2) RS-485 Terminator Select (JP6)

Install a 2-pin jumper cap on JP6 will cross a 150 Ohms resistor over the COM2 when it is configured as RS-485 interface.

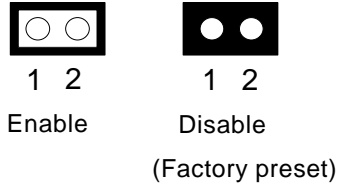


Figure 2-12 JP6: RS-485 Terminator Select

(3) RS-232 Connector (CN5 & DB2)

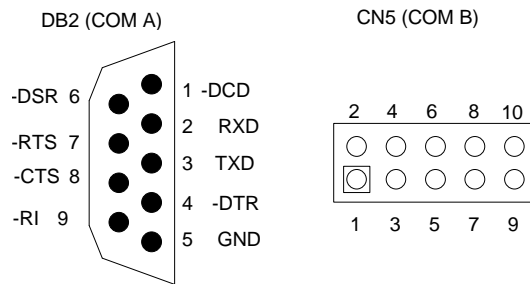


Figure 2-13 DB2 & CN5: RS-232 Connector

DB2	Signal	DB2	Signal
1	-DCD	6	-DSR
2	RXD	7	-RTS
3	TXD	8	-CTS
4	-DTR	9	-RI
5	GND	--	Not Used

Table 2-5 Serial Port RS-232 Connector Pin Assignments

CN5	Signal	CN5	Signal
1	-DCD	2	-DSR
3	RXD	4	-RTS/485+
5	TXD	6	-CTS
7	-DTR/485-	8	-RI
9	GND	10	Case GND

2.2.7 CN6: Ethernet RJ-45 Header

The system supports onboard network connectivity. To utilize this function, install the network driver from the utility diskette, and connect the cable to the following RJ-45 header.

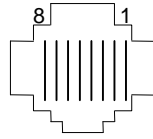


Figure 2-14 CN6: RJ-45 Header

J9:RJ45 HEADER	Signal	J9:RJ45 HEADER	Signal
1	TPTX+	8	No connection
2	TPTX-	9	No connection
3	TPRX+	10	No connection
4	No connection	11	LED -
5	No connection	12	LED +
6	TPRX-	13	LAN CG
7	No connection	14	LAN CG

Table 2-6 RJ-45 Pin Assignments

2.2.8 USB Connector (J4)

USB is the abbreviation of Universal Serial Bus. The Universal Serial Bus (USB) standard is a low-to-medium speed interface for the connection of PC peripherals.

The USB standard simplifies the connection of peripherals to PCs with a uniform hardware and software interface. Personal computers equipped with USB allow computer peripherals to be automatically configured as soon as they are physically attached - without the need to reboot or run setup.

USB is a leading edge technology that allows the user to quickly and easily add a wide range of peripheral devices from printers to keyboards and telephony devices to fax/modems. Universal Host Controller Interface (UHCI) and future support for the Open Host Controller Interface (OHCI) ensure USB compatibility and usability well into the future.

The connector on the CPU board supports two Universal Serial Bus ports. An optional external port bracket attaches to the onboard connector via an attached cable. With the optional port bracket installed you can attach USB devices to the external ports. If the USB ports are installed, the USB Controller line in the Integrated Peripherals section of the CMOS Setup utility must be set to "Enabled". USB ports may also require Operating System support for USB devices.

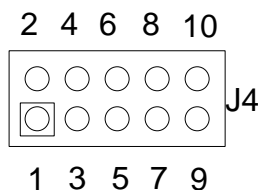


Figure 2-14 J4: USB Connector

Pin	Description	Pin	Description
1	VCC	2	VCC
3	-DATA0	4	-DATA1
5	+DATA0	6	+DATA1
7	GND0	8	GND1
9	CASE0	10	CASE1

Table 2-6 J4: USB Connector Pin Assignments

2.2.9 External Speaker Header (J5)

Besides the onboard buzzer, you can use an external speaker by connecting it to the J5 header.

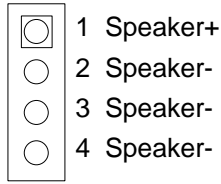


Figure 2-15 J5: External Speaker Header

2.2.10 Reset Header (J8)

The J8 jack is used to connect to an external reset switch. Shorting these two pins will reset the system.

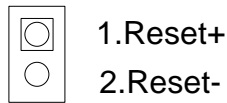


Figure 2-16 J8: Reset Header

2.2.11 LED Header

(1) HDD LED Header (J2)

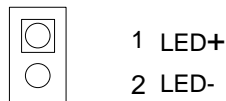


Figure 2-17 J2: HDD LED Header

2.2.12 Power Connector (CN4)

The CN4 is an 8-pin power connector. You can directly connect the power supply to the onboard power connector for stand-alone applications.

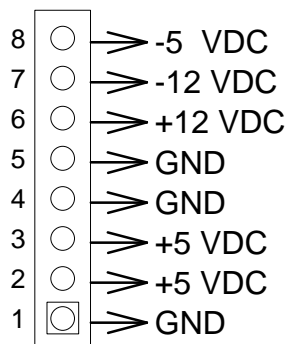


Figure 2-18 CN4: 8-Pin Power Connector

2.2.13 CPU Setting

For different CPUs, please set proper FSB clock on JP9 as described below. No other setting is required.

Supported Processors

Types	Designation	System bus frequency	L2 Cache Size
Pentium III processor in an FC-PGA package	500E, 550E, 600E, 650, 700, 750, 800, 850 and 900	100 MHz	256KB
Celeron processor in an FC-PGA package	533A, 566, 600, 633, 667, 700, 533A, 566, 600, 633, 667, 700	66 MHz	128KB
Celeron processor in a PPGA package	300A, 333, 366, 400, 433, 466, 500, 533	66 MHz	128KB
Cyrix III processor	500MHz, and 600MHz	100 MHz	128KB (L1)

The processor fan header (J7) on the board is intended to drive a processor-mounted fan either full-speed or off, depending on the operating state of the system. The fan speed is monitored by the hardware monitor subsystem.

CPU Cooling Fan Power Connector (J7)

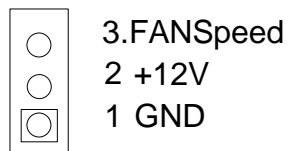


Figure 2-19 J7: CPU Cooling Fan Power Connector

System Bus Clock (JP9)

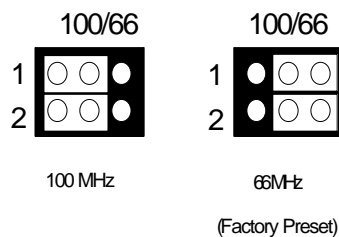


Figure 2-20 JP9: System Bus Clock

2.2.14 External Battery Connector

J6 is a 2-pin connector and provides the connection of an external battery. When using an external connector, mini jumper on JP8 should set to the position 2 and 3.



2.2.15 DRAM Configuration

It can assemble 16/32/64/128/256MB 168 pin DIMM Module Memory. When you set up 168-pin DIMM Module Memory, AR-B1670 will auto-detect DRAM, and adopt correct save in order to make memory work till the best situation.

Caution: Set up 168-pin DIMM Module Memory, please insert into slot vertical, if the direction is wrong and it leads to failure, please confirm the direction is right.

3. CRT/LCD FLAT PANEL DISPLAY

This chapter describes the configuration and installation procedures for LCD & CRT displays. The following topics are covered:

- CRT Connector
- LCD Flat Panel Displays

DON T SUPPORT EXTERNAL VGA CARD

3.1 CRT CONNECTOR (DB1)

The AR-B1670 supports CRT color monitors. It uses an onboard VGA chipset and you can use the VGA RAM 2MB. For different VGA display modes, your monitor must possess certain characteristics (the right drivers) to display the mode you want.

To connect to a CRT monitor, an adapter cable has to be connected to the DB1 connector. DB1 is used to connect with a VGA monitor when you are using the on-board VGA controller as a display adapter. Pin assignments for the DB1 connector are as follows:

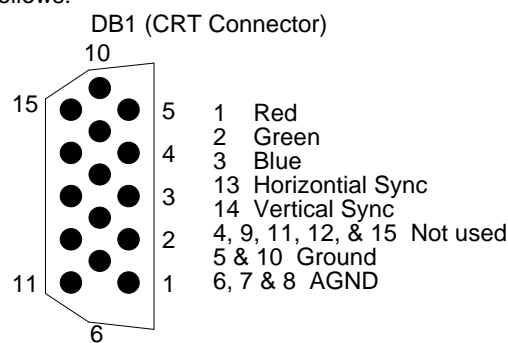


Figure 3-1 DB1: CRT Connector

3.2 LCD FLAT PANEL DISPLAYS

Figure 4-2 shows the connection between AR-B1670 and LCD panel.

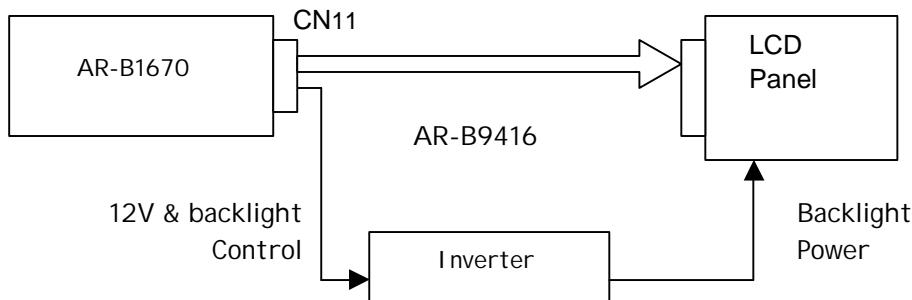


Figure 3-2 LCD Panel Block Diagram

The VGA BIOS of AR-B167 support 640X480 resolution TFT display. Connecting AR-B1670 to other LCD needs different LCD BIOS. Please visit our web site (www.acrosser.com) or contact with our technical support department (csd@acrosser.com.tw) for supports of LCD connecting.

3.2.1 Inverter Board

Acrosser provide a series of optional kit to simplify the connection of CPU card with LCD panels.

Products	LCD types
AR-K0001	Single-tube backlight TFT LCD
AR-K0002	DSTN LCD
AR-K0003	MONO LCD
AR-K0005	LVDS TFT LCD
AR-K0009	Dual-tube backlight TFT LCD

3.2.2 LCD Connector

LCD Panel Display Connector (CN11)

CN11 is a 44-pin connector, which is used for the interface of flat panel display. The pin descriptions are listed in Table 4-1.

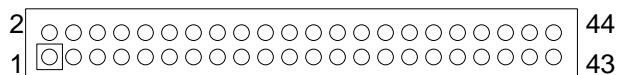


Figure 3-3 CN11: LCD Display Connector

Pin Number	Signal Name	Description
1	GND	Ground
2	SHFCLK	Shift Clock. Pixel clock for flat panel data.
3	GND	Ground
4	LP	Latch Pulse. Flat Panel equivalent of HSYNC. Some panels use the signal name of CL1.
5	FLM	First Line Marker. Flat Panel equivalent of VSYNC.
6	GND	Ground
7	P0(B0)	Flap panel data bus (P0 to P23) of up to 24-bits.
8	P1(B1)	
9	P2(B2)	
10	P3(B3)	
11	P4(B4)	
12	P5(B5)	
13	GND	Ground
14	P6(B6)	
15	P7(B7)	
16	P8(G0)	
17	P9(G1)	
18	P10(G2)	
19	P11(G3)	
20	GND	Ground
21	P12(G4)	
22	P13(G5)	
23	P14(G6)	
24	P15(G7)	
25	P16(R0)	

26	P17(R1)	
27	GND	Ground
28	P18(R2)	
29	P19(R3)	
30	P20(R4)	
31	P21(R5)	
32	P22(R6)	
33	P23(R7)	
34	GND	Ground
35	VCC	+5V
36	VCC	+5V
37	+12V	+12V
38	+12V	+12V
39	GND	Ground
40	GND	Ground
41	DE	Display Enable (DE) for TFT Panels
42	ENBLK	Power sequencing control for enabling the backlight.
43	GND	Ground
44	NC	No Connection

Table 3-1 LCD Display Assignments

Note:

1. To make the connecting cable for flat panel, please refer to the data sheet of flat panel.
2. The Display Enable (DE) control signal of TFT display on pin-41 is factory pre-set by the BIOS. Please stay the jumper of JP4 on DE/M position as Figure 4-4.

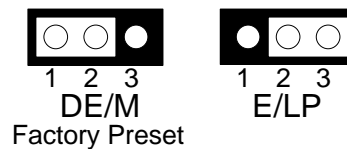


Figure 3-4 JP4: DE/E Signal from M or LP

4. INSTALLATION

This chapter describes the utility diskette installation procedure. The following topics are covered:

- Overview
- Utility Diskette – for AR-B1670
- Watchdog Timer

4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1670 CPU cards. Please carefully read the CPU card's hardware descriptions before installation, especially jumper settings, switch settings and cable connections.

Follow steps listed below for proper installation:

- Step 1 :** Read the CPU card's hardware description in this manual.
- Step 2 :** Install any SDRAM DIMM modules onto the CPU card.
- Step 3 :** Set the jumpers.
- Step 4 :** Make sure that the power supply connected to your passive back plane is turned off.
- Step 5 :** Plug the CPU card into a free PICMG slot on the back plane and secure it in place with a screw to the system chassis.
- Step 6 :** Connect all necessary cables. Make sure that the FDC, HDC; serial and parallel cables are connected to pin 1 of the related connector.
- Step 7 :** Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.
- Step 8 :** Plug the keyboard into the keyboard connector.
- Step 9 :** Turn on the power.
- Step 10:** Configure your system with the BIOS Setup program then re-boot your system.
- Step 11:** If the CPU card does not work, turn off the power and carefully read the hardware description again.
- Step 12:** If the CPU card still does not perform properly, return the card to your dealer for immediate service.

4.2 UTILITY DISKETTE – FOR AR-B1670

AR-B1670 provides six driver diskettes containing drivers VGA for WIN3.1, WIN95/98, and WINNT4.0 and LAN chip. The contents of these diskettes are: disk#1 is WIN3.1&WINNT4.0 drivers, disk#2 is WIN95 driver; disk#3 is WIN98 driver, disk#4 is LAN chip drivers, disk#5 is BIOS update utility and disk#6 is users manual. After extracting the compressed files, please refer to the README.TXT file in the decompressed sub-directories for any troubleshooting before driver installation.

4.2.1 WIN 3.1 Driver

For the WIN31 operating system, the user must be in DOS mode to decompress the compressed file. And then follow these steps:

- Step 1:** Make a new directory for the VGA drivers.
C: \>**MD VAW31**
- Step 2:** Insert Utility Disk #1 into the floppy disk drive, and then copy the compressed file—WIN31DRV.EXE, which is a self-extraction program. You can copy the file and execute the file in DOS mode.
C: \>**COPY A: \WIN31DRV. EXE C: \VAW31**
- Step 3:** Change directory to the newly created directory, and extract the compressed file. You can find that there are there are many files and one <windows> directory generated.

C: \>**CD VAW31**
C: \VAW31>**WIN31DRV**
- Step 4:** In WIN31 mode execute the SETUP.BAT file. It will generate the SETUP MENU.
C: \VAW31>**SETUP**
- Step 5:** The screen shows the chip type and presses any key to enter the main menu.
- Step 6:** Please choose the <Windows Version 3.1 (6555X accelerated drivers)>, press [ENTER] to select <All Resolutions>. When this line appears [*], that means this item is selected. Press [End] to install.
- Step 7:** The screen will show the dialog box to prompt the user for the WIN31 path. The default is C:\WINDOWS.
- Step 8:** Follow the setup steps' messages. When completed the setup procedure will generate the following message.

The Installation is done!

Change to your Windows directory and type SETUP to run the Windows Setup program. Choose one of the new drivers marked by an *. Please refer to the User's Guide to complete the installation.

- Step 9:** Press [Esc] to return the main menu, and press [Esc] to return to the DOS mode.
- Step 10:** In WIN31, you can find the <Chips CPL> icon located in the {CONTROL PANEL} group.
- Step 11:** Adjust the <Refresh Rate>, <Cursor Animation>, , <Resolution>, and <Big Cursor>.

4.2.2 WIN 95 Driver

For the WIN95 operating system, the user must be in DOS mode to decompress the compressed file.

- Step 1:** Enter into WIN95 Operating System and Insert Utility Disk #2 (WIN 95 DRV).
- Step 2:** Click<START> items and choose <RUN...>.
- Step 3:** In the <Open> item, you key in A: \w95500, in the same time, you start setting up Driver. When the process is done, you re-start setting up the computer.
- Step 4:** Enter into the WIN95 operating system; the picture is 640*480 256 colors form. Click <Settings> and enter into " Control Panel " " Display", you may alter resolution pixels according to what you need.

CAUTION: If you decompress the files in the newly created directory, you can find the README file, it gives detailed installation information.

4.2.3 WIN 98 Driver

For the WIN98 operating system, the user must be in DOS mode to decompress the compressed file.

- Step 1:** Enter into WIN98 Operating System and Insert Utility Disk #3 (WIN 98 DRV).
- Step 2:** Click<Start> items and choose <RUN...>.
- Step 3:** In the <Open> item, you key in A:\ w98600, in the same time, you start setting up Driver. When the process is done, you re-start setting up the computer.
- Step 4:** Enter into the WIN98 operating system, the picture is 640*480 256 colors form. Click <Settings> and enter into " Control Panel " " Display", you may alter resolution pixels according to what you need.

CAUTION: If you decompress the files in the newly created directory, you can find the README file, it gives detailed installation information.

4.2.4 WINNT4.0 Driver

For the WINNT4.0 operating system, the user must decompress the compressed files in DOS mode. And then follow these steps:

- Step 1:** Make a new directory to contain the VGA drivers.
C: \>MD VGANT40
- Step 2:** Insert Utility Disk into the floppy disk drive, and then copy the compressed file—NT40DRV.EXE in the newly created directory.
C: \>COPY A: \NT40DRV. EXE C: \VGANT40
- Step 3:** Change directory to the new directory, and then extract the compressed file.
C: \>CD VGANT40
C: \VGANT40>NT40DRV
- Step 4:** Enter the WINNT4.0 operating system; choose the <SETTING> item from the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files ' path.
C: \VGANT40
- Step 5:** Find the <Chips Video Accelerator (65545 / 48 / 50 / 54 / 55 68554 69000)> item, select it and click the <OK> button.
- Step 6:** Find the <Chips> item in the <DISPLAY> icon. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, ...and other functions. Please refer to the messages posted during installation.

4.2.5 LAN DRIVER UTILITES

Introduction

When the AR-B1670 is embedded with the LAN function, it can support various network adapters. Installation programs for LAN drivers are provided in Disk#4. The user must be in DOS mode to decompress the compressed file.

Installing Driver Procedure on Microsoft Windows 95/98

Executing Windows 95/98, it will auto-detect your system configuration and find the adapter hardware.

- Step 1:** Specify the path, which the files decompress to.
- Step 2** Windows 95 will appear some messages to insert Windows 95 system disk to complete setup
- Step3** Windows 95 will finish the other installation procedure automatically, and then restart the system.

Installing Driver Procedure on Microsoft Windows NT

- Step1** In the Main group of NT, select the "Control Panel" icon.
In the Control Panel window, choose the " Network" icon.

- In the Main group of NT, select the "Control Panel" icon.
- The user must be in DOS mode to decompress the compressed file the user must be in DOS mode to decompress the compressed file Windows 95 will appear some messages to insert Windows 95 system disk to complete setup Windows 95 will finish the other installation procedure automatically, then restart the system. In the Control Panel window, choose the " Network" icon. In the Network settings dialog box, choose the "Add adapter" button.
- In the list of network cards, select "<other> requires disk from manufacturer", and press the <Enter> button.
- Specify the path, which the files decompress to.
- The screen will show the "select Line Speed" dialog box, which is provided by the RTL8139.SYS driver. The default value " auto" so that the line speed can be auto detected as 10Mb or100Mb, while the RTL8139.SYS is loading.
- The screen will show the "Input Ethernet ID" dialog box, which is provided by the RTL8139.SYS driver. The option is only required when you have more than one RTL8139 PCI Fast Ethernet adapter on this computer.
- Select "SKIP" if only one adapter is installed on this computer.
- "Bus Location" display in next screen. Your machine contains more than one hardware bus; please select the bus Type and Bus number on which your network adapter card is installed.
- NT will then perform the binding process. If there is any additional information for these packages.
- 10.Re-boot your system when installation is implemented.

Note: For Installing Multiple LAN Adapters:

Enter Windows NT and follow the above setup procedure step2 in the " Network Settings" dialog box, choose the configure..." button. The "input Ethernet ID" dialog box appears and input adapter's Ethernet ID. Last step is to select OK and close the NETWORK SETUP. Select SKIP if only one adapter is installed on this computer.

4.3 WATCHDOG TIMER

The AR-B1670 is equipped with a programmable time-out period watchdog timer. You can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out, because of system hang, the timer will generate a interrupt to execution your command or TSR. The time-out period can be programmed to be from 1 seconds to 255 minutes.

4.4 EXECUTION OF THE WATCHDOG

1. Execute TSR program., and indicate Hard Ware interrupt (IRQ 3,4,5,9,10,11,12,15).
(Ex: WD_tsr 15).
2. Execute WD_DEMO, Customers can refer to source and adjust the program you need.

5. BIOS CONSOLE

This chapter describes the BIOS menu displays and explains how to perform common tasks needed to get up and running. It also presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power Management
- PCI/Plug and Play
- Peripheral Setup
- Hardware Monitor Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit
- BIOS Update

5.1 BIOS SETUP OVERVIEW

The BIOS is a program used to initialize and set up the I/O system of the computer, which includes the PCI bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer is turned on, the BIOS will perform diagnostics on the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to select the option and configure the functions.

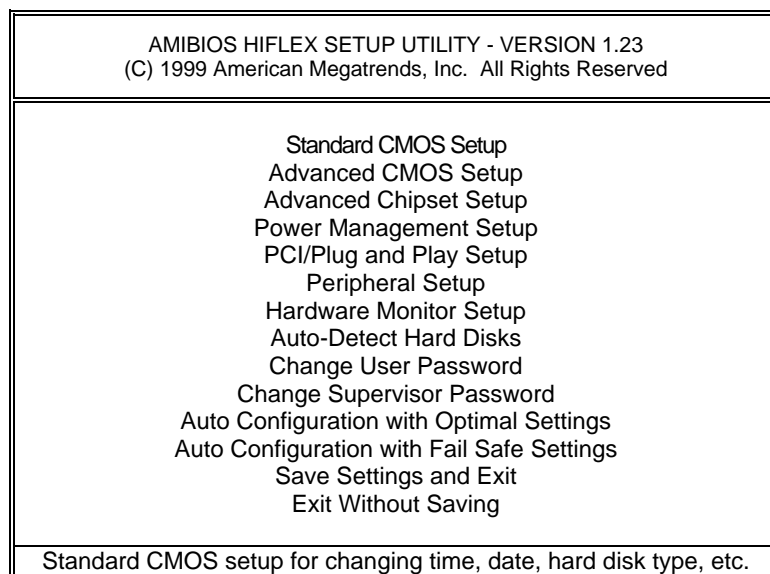


Figure 5-1 BIOS: Setup Main Menu

- CAUTION:** 1. In the AR-B1670 BIOS the factory-default setting is the <Auto Configuration with Optimal Settings>. Acrosser recommends using the BIOS default settings, unless you are very familiar with the settings function, or you can contact the technical support engineers (FAE).
2. If the BIOS loses the settings, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operating system. This option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Settings> in the main menu. This option gives best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

5.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configurations and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

AMBIOS SETUP - STANDARD CMOS SETUP									
(C) 1999 American Megatrends, Inc. All Rights Reserved									
Date (mm/dd/yyyy): Tue Jun 02, 1998					640KB				
Time (hh/mm/ss): 13:39:30					63MB				
Floppy Drive A: Not Installed									
Floppy Drive B: Not Installed									
	Type	Size	Cyln	Head	Wpcom	Sec	LBA Mode	Blk Mode	PIO 32Bit Mode
Pri Master	: Auto						Off	Off	Auto Off
Pri Slave	: Auto						Off	Off	Auto Off
Sec Master	Auto						Off	Off	Auto Off
Sec Slave	Auto						Off	Off	Auto Off
Boot Sector Virus Protection					Disabled				
Month: Jan - Dec					ESC:Exit :Sel				
Day: 01 - 31					PgUp/PgDn:Modify				
Year: 1901 - 2099					F2/F3:Color				

Figure 5-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <Disabled>. This setting is recommended because it conflicts with new operating systems. Installation of a new operating systems requires that you disable this to prevent write errors.

5.3 ADVANCED CMOS SETUP

The <Advanced CMOS Setup> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

AMIBIOS SETUP - ADVANCED CMOS SETUP (C) 1999 American Megatrends, Inc. All Rights Reserved		
Quick Boot	Enabled	Available Options : Disabled Enabled
1st Boot Device	IDE-0	
2nd Boot Device	Floppy	
3rd Boot Device	CDROM	
4th Boot Device	Disabled	
Try Other Boot Devices	Yes	
Floppy Access Control	Read-Write	
Hard Disk Access Control	Read-Write	
S.M.A.R.T. for Hard Disks	Disabled	
BootUp Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
PS/2 Mouse Support	Enabled	
Typemaice Rate	Fast	
System Keyboard	Absent	
Primary Display	Absent	
Password Check	Setup	
Boot to OS/2 > 64MB	No	
Wait For 'F1' If Error	Disabled	
Hit 'DEL' Message Display	Enabled	
Internal Cache	WriteBack	
External Cache	WriteBack	
C000, 16k Shadow	Cached	
C400, 16k Shadow	Cached	
C800, 16k Shadow	Disabled	
CC00, 16k Shadow	Disabled	
D000, 16k Shadow	Disabled	
D400, 16k Shadow	Disabled	ESC:Exit :Sel
D800, 16k Shadow	Disabled	PgUp/PgDn:Modify
DC00, 16k Shadow	Disabled	F2/F3:Color

Figure 5-3 BIOS: Advanced CMOS Setup

Quick Boot

This category speeds up the <Power On Self Test> (POST) after you power on the computer. If it is set to **Enabled**, the BIOS will shorten or skip some check items during POST.

1st Boot Device

2nd Boot Device

3rd Boot Device

4th Boot Device

These options determine where the system looks first for an operating system.

Try Other Boot Devices

If you have other boot up device other than the above mentioned devices, such as **IDE-0, IDE-1, IDE-3, IDE-4**, Floppy.

Floppy Access Control

This option determines the floppy access method, which can be either read only or normal (read/write). When set to read only, the data in the hard disk is being read instead of being written." Normal" allows the floppy to be read or written.

HDD Access Control

This option determines the floppy access method, which can be either read only or normal (read/write). When set to read only, the data in the hard disk is being read instead of being written." Normal" allows the floppy to be read or written.

Available options: Disabled, Enabled

S.M.A.R.T for hard Disks

S.M.A.R.T is abbreviation of Self-Monitoring Analysis and Reporting Technology. It is reliable and precautionous technology. When Hard Disk disorder, it prevents Hard Disk from the loss of data.

Boot Up Num-Lock

This item is used to activate the Num-Lock function upon system boot. If the setting is on, after a boot, the Num-Lock light is lit, and the user can automatically use the number keys.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the setting to **Disabled** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When **<Enabled>**, the BIOS swaps the floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is set to **Enabled**, the BIOS will seek the floppy <A> drive one time upon boot up.

PS/2 Mouse Support

The setting of **Enabled** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. **Disabled** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

System Keyboard

This function specifies that a keyboard is attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If **Always** is chosen, a user password prompt appears every time the computer is turned on. If **Setup** is chosen, the password prompt appears if the BIOS is executed.

Boot to OS/2 >64MB

When using the OS/2 operating system with DRAM of greater than 64MB installed, you need to **Enabled** this option; otherwise leave this on the setup default of **Disabled**.

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this option is set to **Disabled**, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to **Disabled** to prevent the following message:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Internal Cache

This option specifies the caching algorithm used for the L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 5-1 Internal Cache Setting

External Cache

This option specifies the caching algorithm used for the L2 secondary cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 5-2 External Cache Setting

Shadow

These options control the location of the contents of the 16KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 5-3 Shadow Setting

5.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C) 1999 American Megatrends, Inc. All Rights Reserved		
***** SDRAM Timing *****		Available Options :
Configure SDRAM Timing by SPD	Disabled	Disabled
SDRAM RAS# to CAS# delay	3 SCLKs	Enabled
RAS# Precharge	3 SCLKs	
CAS# Latency	3 SCLKs	
Loadoff Cmd Timing	Auto	
DRAM Refresh Rate	124.8us	
Memory Hole	Disabled	
Graphics Aperture Size	64MB	
8bit I/O Recovery Time	1 Sysclk	ESC:Exit :Sel
16bit I/O Recovery Time	1 Sysclk	PgUp/PgDn:Modify
USB Keyboard / Mouse Legacy Support	Disabled	F2/F3:Color

Figure 5-4 BIOS: Advanced Chipset Setup

Configure SDRAM Timing by SPD:

SPD is the abbreviation Serial Presence Detect. SPD takes accord the chip types, capacity, timing, voltage data. The system can auto adjust memory according to the data to reach the best situation.

SDRAM RAS# to CAS# delay:

When CPU saves data from memory, it has to deliver RAS single first, and then CAS single. The item is to set up the interval between two singles.

RAS# Precharge:

This item is the time when RAS has to be re-located.

CAS# Latency:

This item is to set up the time when memory receives one CAS single, after how much clock, the memory starts to write and read data.

Loadoff Cmd Timing:

It is the first read-write action under burst pattern

DRAM Refresh Rate:

The rate is the speed when updating DRAM Data.

Memory Hole:

This reserves the 15MB to 16MB memory address space for use of ISA expansion cards.

Graphics Aperture Size:

The item is to set up AGP display to use how much memory to save Texture Data.

8 bit I/O Recovery Time:

The item is to set up CPU to demand ISA Bus 8 bit how much it takes to recovery.

16 bit I/O Recovery Time:

The item is to set up CPU to demand ISA Bus 16 bit how much it takes to recovery.

Memory Hole at 15-16 MB

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

USB Keyboard/Mouse Legacy Support

These options are used to <Enabled> the USB function and it's only useful in the DOS mode.

5.5 POWER MANAGEMENT

This section is used to configure the power management features. This <Power management Setup> option allows you to reduce power consumption. This feature turns off the video display and shuts down the hard disk after a period of inactivity.

MIBIOS SETUP - Power Management Setup (C) 1998 American Megatrends, Inc. All Rights Reserved		
Power Management /APM	Disabled	Available Options : Disabled Enabled
Video Power Down Mode	Disabled	
Hard Disk Power Down Mode	Disabled	
Standby Time Out (Minute)	Disabled	
Suspend Time Out (Minute)	Disabled	
Display Activity	Ignore	
Device 6 (Serial Port 1)	Monitor	
Device 7 (Serial Prot 2)	Monitor	
Device 8 (Parallel Port)	Ignore	
		ESC:Exit :Sel PgUp/PgDn:Modify F2/F3:Color

Figure 5-5 BIOS: Power Management Setup

Power Management /APM

Enabled this option is to enable the power management and APM (Advanced Power Management) features.

Video Power Down Mode

This option specifies the power management state that the video subsystem enters after specified period of display inactivity has expired.

Hard Disk Power Down Mode

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity have expired.

Standby Time Out**Suspend Time Out**

These options specify the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed on Suspend mode. In Suspend mode, nearly all power use is curtailed.

Device

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by BIOS. When any activity occurs, the computer enters Full On mode.

6.6 PCI/PLUG AND PLAY

This section is used to configure PCI / Plug and Play features. The <PCI & PNP Setup> option configures the PCI bus slots. All PCI bus slots on the system use INTA#, thus all installed PCI cards must be set to this value.

AMIBIOS SETUP - PCI/PLUG AND PLAY SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	Yes	Available Options : Yes No
Clear NVRAM	No	
PCI Latency Timer (PCI Clocks)	64	
PCI IDE BusMaster	Disabled	
DMA Channel 0	PnP	
DMA Channel 1	PnP	
DMA Channel 3	PnP	
DMA Channel 5	PnP	
DMA Channel 6	PnP	
DMA Channel 7	PnP	
IRQ 3	PCI /PnP	
IRQ 4	PCI /PnP	
IRQ 5	PCI /PnP	
IRQ 7	PCI /PnP	
IRQ 9	PCI /PnP	
IRQ 10	PCI /PnP	
IRQ 11	PCI /PnP	
IRQ 12	PCI /PnP	
IRQ 14	PCI /PnP	
IRQ 15	PCI /PnP	
Reserved Memory Size	Disabled	ESC:Exit :Sel
Reserved Memory Address	C800	PgUp/PgDn:Modify F2/F3:Color

Figure 5-6 BIOS: PCI / Plug and Play Setup

Plug and Play Aware O/S

Set this option to **Yes** if the operating system installed in the computer is Plug and Play-aware. The BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 (and above) operating system detects and enables all other PnP-aware adapter cards. Windows 95 (and above) is PnP-aware. Set this option to **<No>** if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

Clear NVRAM

This sets the operating mode of the boot block area of the BIOS FLASH ROM to allow programming in the **Yes** setting.

PCI Latency Timer (PCI Clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks.

PCI IDE Bus Master

When **Enabled** this option specifies that the IDE controller on the PCI local bus has bus mastering capability.

DMA & IRQ

These options specify the bus that the named IRQs/DMA lines are used on. These options allow you to specify IRQs/DMA for use by legacy ISA adapter cards. These options determine if the BIOS should remove an IRQ/DMA from the pool of availability of IRQs/DMA passed to the BIOS configurable devices. If more IRQs/DMA must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ/DMA by assigning the option to the ISA/EISA setting. The onboard I/O is configurable with BIOS.

Reserved memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards.

Reserved memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

5.7 PERIPHERAL SETUP

This section is used to configure the peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Auto	Available Options : Auto Disabled Enabled
OnBoard Serial Port1	Auto	
OnBoard Serial Port2	Auto	
OnBoard Parallel Port	Auto	
Parallel Port Mode	Normal	
Parallel Port IRQ	Auto	ESC:Exit :Sel PgUp/PgDn:Modify F2/F3:Color
Parallel Port DMA Channel	N/A	
OnBoard PCI IDE	Enabled	
Primary Master Prefetch	Enabled	
Primary Slave Prefetch	Enabled	

Figure 5-7 BIOS: Peripheral Setup

OnBoard FDC

This option enables the floppy drive controller on the AR-B1670.

OnBoard Serial Port

This option enables the serial port on the AR-B1670.

OnBoard Parallel Port

This option enables the parallel port on the AR-B1670.

Parallel Port Mode

This option specifies the parallel port mode, ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE1284 specifications.

Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

Onboard PCI MASTER/SLAVE Prefetch

This option specifies the onboard IDE controller channels that will be used.

5.8 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

5.9 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. The user can set either a Supervisor password or a User password.

5.10 SETTING THE PASSWORD

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after the BIOS is exited and saved. The next time the system boots, you are prompted for the password.

Enter new supervisor password:

5.11 PASSWORD CHECKING

The password check option is enabled in Advanced Setup by choosing either **Always** (the password prompt appears every time the system is powered on) or **Setup** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter a 1 to 6 characters password. The password does not appear on the screen when typed. Make sure you write it down.

5.12 LOAD DEFAULT SETTING

This section permits users to select a group of settings for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

5.12.1 Auto Configuration with Optimal Setting

The user can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

Load high performance setting (Y/N) ?

5.12.2 Auto Configuration with Fail Safe Setting

The user can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

Load failsafe settings (Y/N) ?

5.13 BIOS EXIT

This section is used to exit the BIOS main menu. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

5.13.1 Save Settings and Exit

This item is in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

When you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

Save current settings and exit (Y/N) ?

5.13.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to abandon all the modified data and Exit Setup.

Quit without saving (Y/N) ?

5.14 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1670 provides the FLASH BIOS update function for you to easily to update to a newer BIOS version. Please follow these operating steps to update to a new BIOS:

Step 1: Turn on your system and don't detect the CONFIG.SYS and AUTOEXEC.BAT files.

Step 2: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 3: In the MS-DOS mode, you can type the FLASH812 program.

```
A:\>FLASH812
```

Step 4: Press [ALT+F], The <File> box will show the following message, this message will be highlighted.

```
BIOS Filename Loading ... . After typing in the File name you must press<ENTER> or press <ESC> to exit.
```

Step 5: And then please enter the file name to the <Enter File Name> box. And the <Message> box will show the following notice.

```
Are you sure to write this BIOS into flash ROM?
```

Step 6: Press the <Enter> key to update the new BIOS.
Then the <Message> box will show the <Programming now ...>.

Step 7: When the BIOS update is successful, the message will show <Flash ROM Update Completed - Pass>.

NOTE: 1 The BIOS Flash disk is not a standard accessory. Now that the onboard BIOS is updated to the newest version, if you need to add some functions in the future please contact the technical support (FAE) engineers. They will provide the newest known BIOS for updating.

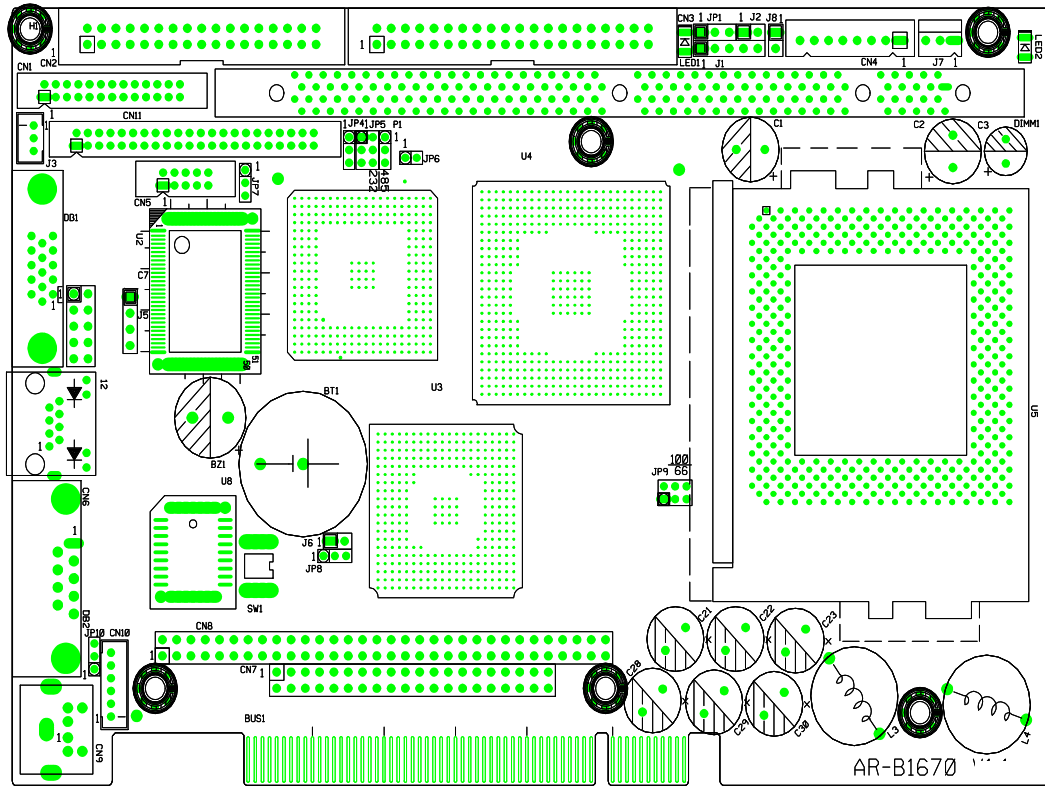
6. SPECIFICATIONS

AR-B1670 --- Socket 370 Pentium III PCI half-size CPU Card with LAN/VGA/LCD

- * **CPU:** Supports 66MHz system bus Celeron and 100MHz system bus Pentium III CPU (Socket 370).
- * **Chipset:** Intel 440BX, Supports ECC parity checking SDRAM.
- * **Bus Interface:** PICMG PCI and Non-stack through PC/104 bus.
- * **RAM Memory:** Supports one 168-pin DIMM (SDRAM) socket, 256MB maximum.
- * **Watchdog:** Software programmable.
- * **VGA/LCD Display:** C&T 69000 chipset with internal 2MB VRAM (PCI bus, 1024*768/64K colors).
CRT – with 15-pin HDB15 connector located at bracket.
LCD – with 2.0mm 44-pin connector
- * **Super I/O:** 1 PCI IDE – One 2.54mm 40-pin connector
1 FDC – with 2.54mm 34-pin connector
1 Parallel – Supports SPP/EPP/ECP mode with 2.0mm 26-pin connector
2 RS-232C – COM2 can be configured as RS-485 port.
1 IrDA port, IrDA 1.1 Compliant
Touch Screen uses 2.0mm 3-pin JST connector.
- * **Keyboard** PS2, 6-pin mini-DIN connector
- * **Mouse:** PS/2 compatible mouse port
- * **USB:** 2 USB ports with 2.54mm 10-pin header
- * **Ethernet:** 10/100Mbps with RJ-45 Connector (Located at Bracket)
- * **BIOS:** AMI flash BIOS (256KB, including VGA/LCD BIOS). Provides utility program to update new version of BIOS.
- * **RTC:** Supports ACPI function with on-board battery and optional external battery pack.
- * **Speaker:** On-board buzzer and external speaker (with 4-pin 2.54mm header).
- * **H/W Monitoring:** Hardware monitoring for CPU temperature, fan speed, and power voltage
- * **LED Indicators:** Power LED and hard disk LED.
- * **BUS Drive Cap.:** PCI – 6 TTL level loads maximum.
PC/104 – 8 TTL level loads maximum.
- * **Power Req.:** +5V – 4.0A maximum and +12V – 0.6A maximum (Based on 333 MHz CPU)
- * **CE Design-In:** Add EMI components to COM ports, Parallel port, CRT, USB, Keyboard, and PS/2 mouse.
- * **Dimensions:** Half size, 185 mm x 122 mm (7.28" x 4.80").

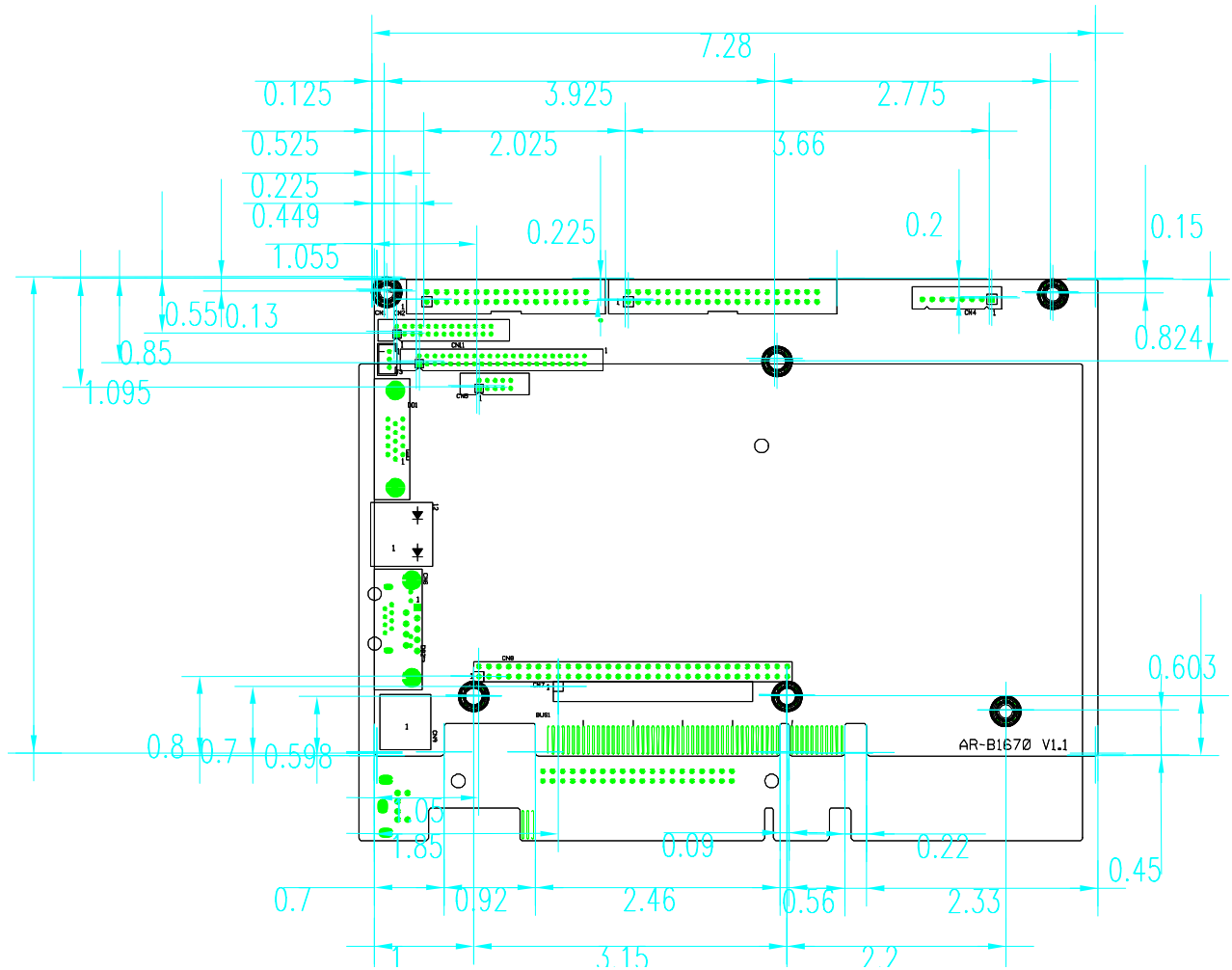
7. PLACEMENT & DIMENSIONS

7.1 PLACEMENT



Unit: mil (1 inch = 25.4 mm = 1000 mil)

8.DIMENSIONS



9. PROGRAMMING RS-485 & INDEX

9.1 PROGRAMMING RS-485

The majority of the communicative operations of the RS-485 are the same as the RS-232. When the RS-485 proceeds with the transmission, which needs to control the DTR (TXC) signal, the installation steps are as follows:

Step 1: Enable DTR (Data Terminal Relay)

Step 2: Send out data

Step 3: Wait for data to empty

Step 4: Disable DTR

(1) Initializing the COM port

Step 1: Initialize the COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are the same.)

Step 2: Disable DTR (Data Terminal Relay) the bit 0 of the address of offset+4 just sets to "0".

NOTE: Control the AR-B1670 CPU card's DTR signal to enable/disable the RS-485's TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable the DTR signal, and the bit 0 of the address of offset+4 just sets to "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) so that all sets are set to "0".

Step 4: Disable the DTR signal, and the bit 0 of the address of offset+4 sets to "0"

(3) Send out one block data (Transmit – the data can be more than two characters long)

Step 1: Enable the DTR signal, and the bit 0 of the address of offset+4 just sets to "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) so that all sets are set to "0".

Step 4: Disabled DTR signal, and the bit 0 of the address of offset+4 sets to "0"

(4) Receive data

The RS-485's operation of receiving data is the same as RS-232's.

(5) Basic Language Example**a.) Initial 86C450 UART**

```
10 OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20 REM Reset DTR
30 OUT &H3FC, (INP(%H3FC) AND &HFA)
40 RETURN
```

b.) Send out one character to COM1

```
10 REM Enable transmitters by setting DTR ON
20 OUT &H3FC, (INP (&H3FC) OR &H01)
30 REM Send out one character
40 PRINT #1, OUTCHR$
50 REM Check transmitter holding register and shift register
60 IF ((INP & H3FD) AND &H60) >0) THEN 60
70 REM Disable transmitters by resetting DTR
80 OUT &H3FC, (INP (&H3FC) AND &HEF)
90 RETURN
```

c.) Receive one character from COM1

```
10 REM Check COM1: receiver buffer
20 IF LOF (1)<256 THEN 70
30 REM Receiver buffer is empty
40 INPSTR$=""
50 RETURN
60 REM Read one character from COM1: buffer
70 INPSTR$=INPUT$(1, #1)
80 RETURN
```

11. CONNECTORS AND JUMPERS INDEX

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CN7	40 pin PC/104 connector bus C & D	2-3
CN8	64 pin PC/104 connector bus A & B	3-3
CN9	6 Pin mini keyboard connector	2-3
CN10	PS2 Mouse/Keyboard	3-5
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12.APPENDIX A. ADDRESS MAPPING

Memory Map:

MEMORY MAP	ASSIGNMENT
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	Intel 82443BX Pentium(r) II Processor to AGP Controller
0xA0000-0xBFFFF	Chips And Technologies 69000
0xCC000-0xEFFFF	PCI bus
0x8000000-0xFFFEFFFF	PCI bus
0xEDE00000-0xEFEFFFFF	Intel 82443BX Pentium(r) II Processor to AGP Controller
0xE5C00000-0xE5CFFFFF	Intel 82443BX Pentium(r) II Processor to AGP Controller
0xE8000000-0xEBFFFFF	Intel 82443BX Pentium(r) II Processor to AGP Controller
0xEE000000-0xEEFFFFF	Chips And Technologies 69000
0xEFFFFFF00-0xEFFFFFFF	Realtek RTL8139(A) PCI Fast Ethernet Adapter
0x0000-0x9FBFF	System board
0x9FC00-0x9FFFF	System board
0xF0000-0xFFFFF	System board
0x100000-0x7FFFFFFF	System board
0xFFFF0000-0xFFFFFFFF	System board

13.APPENDIX B. INTERRUPT REQUEST (IRQ)

SETTING	HARDWARE USING THE SETTING
01	PC/AT Enhanced PS/2 Keyboard (101/102-Key)
02	N/A
03	Communications Port (COM2)
04	Communications Port (COM1)
05	N/A
06	Standard floppy disk controller
07	
08	System CMOS/real time clock
09	N/A
10	Realtek RTL8139(A) PCI Fast Ethernet Adapter
11	Intel 82371AB/EB PCI to USB Universal Host Controller
12	Logitech PS/2 Port Mouse
13	Numeric data processor
14	Primary IDE Channel
15	N/A