AR-B1474
INDUSTRIAL GRADE
486DX/DX2/DX4 CPU CARD
User's Guide

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0.PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B1474 SERIAL CPU BOARD

This guide introduces the Acrosser AR-B1474 serial CPU board.

Use the information describes this card's functions, features, and how to start, set up and operate your AR-B1474 serial CPU board. You also could find general system information here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B1474, refer to the Chapter 3, "Setting Up the System" in this guide. Check the packing list, make sure the accessories in the package.

AR-B1474 diskette provides the newest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification and hardware & software information, and adding the description or modification of product function after manual published.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing of your product by following these guidelines:

1. Include your name, address, telephone and facsimile number where you may be reached during the day.
2. A description of the system configuration and/or software at the time is malfunction.
3. A brief description is in the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

Please send your comments to Acrosser Technology Co., Ltd. or your local sales representative.

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0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, “Overview”, provides an overview of the system features and packing list.
- Chapter 2, “System Controller” describes the major structure.
- Chapter 3, “Setting Up the System”, describes how to adjust the jumper, and the connectors setting.
- Chapter 4, “Installation”, describes setup procedures including information on the utility diskette.
- Chapter 5, “Solid State Disk,” describes the various type SSD’s installation steps.
- Chapter 6, “BIOS Console”, providing the BIOS options setting.
- Chapter 7, Specifications
- Chapter 8, Placement & Dimensions
- Chapter 9, Memory Banks & Programming RS-485
- Chapter 10, SSD Types Supported & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system component, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the “golden finger” connectors on the bottom of every board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B1474 is a half size industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. The total on-board memory for the AR-B1474 can be configured from 1MB to 32MB by using all 72-pin type DRAM devices.

The 8 layers PCB CPU card is equipped with a IDE HDD interface, a floppy disk drive adapter, 1 parallel port, 2 serial ports, a watchdog timer and a solid state disk. Its dimensions are as compact as 122mm x 185mm. It's highly condensed features make it an ideal cost/performance solution for high-end commercial and industrial applications where CPU speed and mean time between failure is critical.

The AR-B1474 provides 2 bus interfaces, ISA bus and PC/104 compatible expansion bus. Based on the PC/104 expansion bus, you could easy install thousands of PC/104 module from hundreds venders around the world. You could also directly connect the power supply to the AR-B1474 on-board power connector in stand alone applications.

A watchdog timer, which has a software programmable time-out interval, is also provided on this CPU card. It ensures that the system will not hang-up if a program can not execute normally.

For diskless application, the AR-B1474 provides up to 3MB of bootable ROM, FLASH, or SRAM disk space by using 64K x 8 to 1M x 8 memory chips.

The AR-B1474 is implemented with M1429 and M1431 chipset incorporate a memory controller, parity generation and checking, two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, an address buffer and a data buffer.

A super I/O chip (SMC37C669) is embedded in the AR-B1474 card. It combines functions of a floppy disk drive adapter, a hard disk drive (IDE) adapter, two serial (with 16C550 UART) adapters and 1 parallel adapter.

The I/O port configurations can be done by setting the BIOS setup program.

As an UART, the chip supports serial to parallel conversion on data characters received from a peripheral device or a MODEM , and parallel to serial conversion on data character received from the CPU. The UART includes a programmable baud rate generator, complete MODEM control capability and a processor interrupt system. As a parallel port, the SMC37C669 provides the user with a fully bi-directional parallel centronics-type printer interface.

This manual has been written to assist you in installing, configuring and running the AR-B1474 CPU card. Each section is intended to guide you through it's procedures clearly and concisely, allowing you to continue to the next chapters without any difficulty.

1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B1474 card, take a moment to make sure that the following items have been included inside the AR-B1474 package.

- The quick setup manual
- 1 AR-B1474 all-in-one CPU card
- 1 Keyboard adapter cable
- 1 Parallel port interface cable
- 1 Hard disk drive interface cable
- 1 Floppy disk drive interface cable
- 1 40-pin header for PC/104 adapter
- 1 64-pin header for PC/104 adapter
- 1 Software utility diskettes

NOTE: If there are any discrepancies, please contact your Acrosser distributor immediately.

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- All-in-one designed 486DX/DX2/DX4 CPU card
- Support 3.3V/5V CPU with voltage regulator
- Support ISA bus and PC/104 bus
- Support 128KB to 512KB second level cache on-board
- Support up to 32MB DRAM on-board
- Support shadow memory and EMS
- Legal AMI BIOS
- IDE hard disk drive interface
- Floppy disk drive interface
- Bi-direction parallel interface
- 2 serial ports with 16C550 UART
- DS12887 or compatible RTC
- Programmable watchdog timer
- Up to 3MB solid state disk (SSD)
- On-board build-in buzzer
- 8 layers PCB

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1474 serial CPU board. The following topics are covered:

- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port

2.1 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B1474 card. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high-speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

Following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.2 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the serial keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interrupt may be used for both send and receive routines.

2.3 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1474 card. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

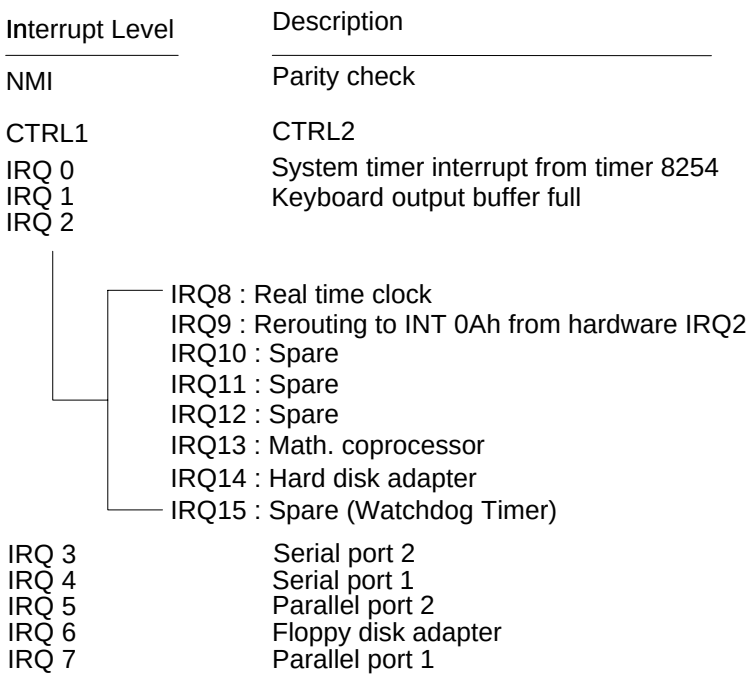


Figure 2-1 Interrupt Controller

2.3.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	M1429 chipset address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
210-213	SSD
214-215	Watchdog
218-21A	EMS register 1
278-27F	Parallel printer port 3 (LPT 3)
290-293	SSD
294-295	Watchdog
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
310-313	SSD
314-315	Watchdog
378-37F	Parallel printer port 2 (LPT 2)
380-38F	SDLC, bisynchronous 2
390-393	SSD
394-395	Watchdog
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display and printer port 1 (LPT 1)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-2 I/O Port Address Map

2.3.2 Real-Time Clock and Non-Volatile RAM

The AR-B1474 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-3 Real-Time Clock & Non-Volatile RAM

2.3.3 Timer

The AR-B1474 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.3.4 ISA Bus Pin Assignment

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
A1	-IOCHCK	Input	B1	GND	Ground
A2	SD7	Input/Output	B2	RSTDRV	Output
A3	SD6	Input/Output	B3	+5V	Power
A4	SD5	Input/Output	B4	IRQ9	Input
A5	SD4	Input/Output	B5	-5V	Power
A6	SD3	Input/Output	B6	DRQ2	Input
A7	SD2	Input/Output	B7	-12V	Power
A8	SD1	Input/Output	B8	-ZWS	Input
A9	SD0	Input/Output	B9	+12V	Power
A10	IOCHRDY	Input	B10	GND	Ground
A11	AEN	Output	B11	-SMEMW	Output
A12	SA19	Input/Output	B12	-SMEMR	Output
A13	SA18	Input/Output	B13	-IOW	Input/Output
A14	SA17	Input/Output	B14	-IOR	Input/Output
A15	SA16	Input/Output	B15	-DACK3	Output
A16	SA15	Input/Output	B16	DRQ3	Input
A17	SA14	Input/Output	B17	-DACK1	Output
A18	SA13	Input/Output	B18	DRQ1	Input
A19	SA12	Input/Output	B19	-REFRESH	Input/Output
A20	SA11	Input/Output	B20	BUSCLK	Output
A21	SA10	Input/Output	B21	IRQ7	Input
A22	SA9	Input/Output	B22	IRQ6	Input
A23	SA8	Input/Output	B23	IRQ5	Input
A24	SA7	Input/Output	B24	IRQ4	Input
A25	SA6	Input/Output	B25	IRQ3	Input
A26	SA5	Input/Output	B26	-DACK2	Output
A27	SA4	Input/Output	B27	TC	Output
A28	SA3	Input/Output	B28	BALE	Output
A29	SA2	Input/Output	B29	+5V	Power
A30	SA1	Input/Output	B30	OSC	Output
A31	SA0	Input/Output	B31	GND	Ground

Table 2-4 ISA Bus Pin Assignment

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
C1	SBHE	Input/Output	D1	-MEMCS16	Input
C2	LA23	Input/Output	D2	-IOCS16	Input
C3	LA22	Input/Output	D3	IRQ10	Input
C4	LA21	Input/Output	D4	IRQ11	Input
C5	LA20	Input/Output	D5	IRQ12	Input
C6	LA19	Input/Output	D6	IRQ15	Input
C7	LA18	Input/Output	D7	IRQ14	Input
C8	LA17	Input/Output	D8	-DACK0	Output
C9	-MEMR	Input/Output	D9	DRQ0	Input
C10	-MEMW	Input/Output	D10	-DACK5	Output
C11	SD8	Input/Output	D11	DRQ5	Input
C12	SD9	Input/Output	D12	-DACK6	Output
C13	SD10	Input/Output	D13	DRQ6	Input
C14	SD11	Input/Output	D14	-DACK7	Output
C15	SD12	Input/Output	D15	DRQ7	Input
C16	SD13	Input/Output	D16	+5V	Power
C17	SD14	Input/Output	D17	-MASTER	Input
C18	SD15	Input/Output	D18	GND	Ground

Table 2-5 ISA Bus Pin Assignment

2.3.5 ISA Bus Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMW [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 2-6 ISA Bus Signal Description

2.4 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE2) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required handle the communications link.

The following table is summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-7 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: “0” if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-8 Serial Port Divisor Latch

2.5 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-9 Registers' Address

(2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer’s Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

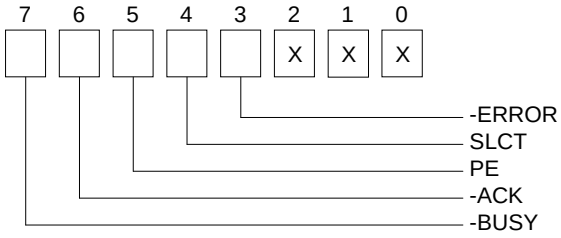


Figure 2-2 Printer Status Buffer

NOTE: X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer’s ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

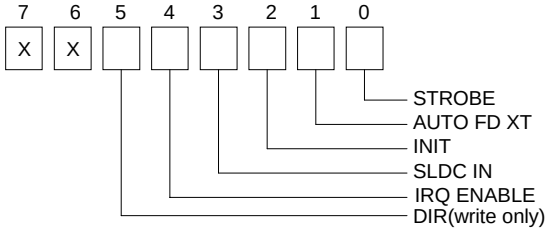


Figure 2-3 Bit’s Definition

NOTE: X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING UP THE SYSTEM

This section describes pin assignments for system’s external connectors and the jumpers setting.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B1474 is a half size industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. The total on-board memory for the AR-B1474 can be configured from 1MB to 32MB by using all 72-pin type DRAM devices.

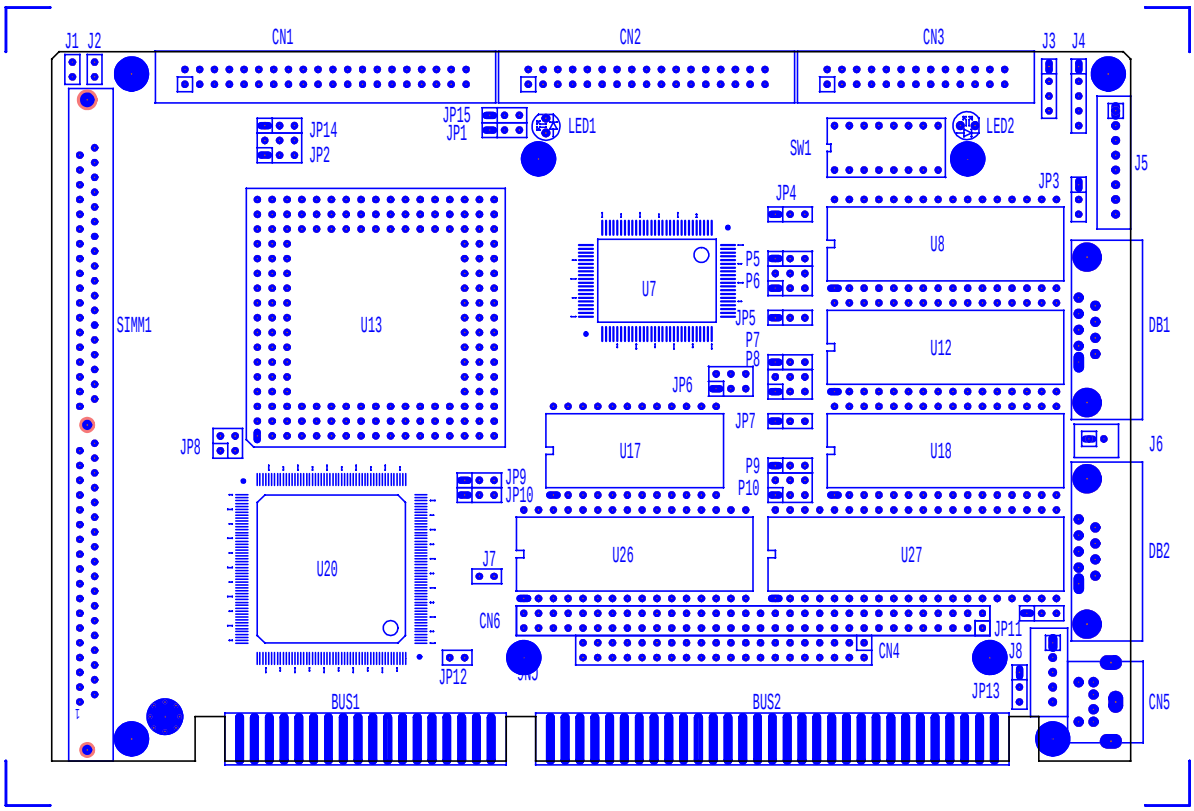


Figure 3-1 AR-B1474 Placement

3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1474 jumper pins, and the factory-default setting.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.2.1 Serial Port

(1) RS-485 Adapter Select (JP3 & JP11)

JP3 and JP11 can be set independently. JP3 selects COM-A port and JP11 selects COM-B port.

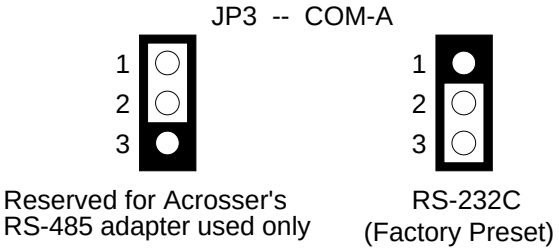


Figure 3-2 JP3: RS-485 Adapter Select for COM-A

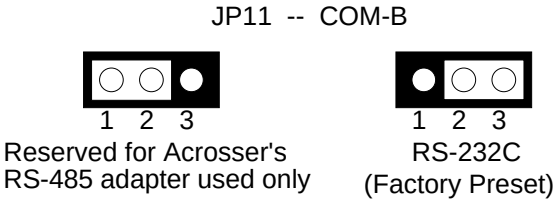


Figure 3-3 JP11: RS-485 Adapter Select—COM-B

(2) RS-232 Connector (DB1 & DB2)

There are two serial ports with EIA RS-232C interface on the AR-B1474. COM-A and COM-B use two on-board D-type 9-pin male connectors (DB1 & DB2). If you want to configure the serial port, please refer to the BIOS configuration.

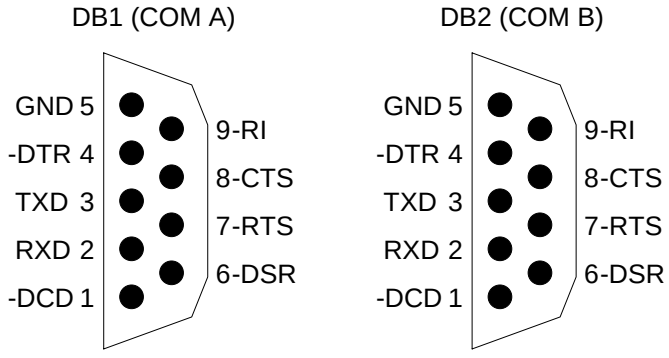


Figure 3-4 DB1 & DB2: RS-232 Connector

3.2.2 Hard Disk (IDE) Connector (CN1)

A 40-pin header type connector (CN1) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 40-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use BIOS Setup program to select. The following table illustrates the pin assignments of the hard disk drive's 40-pin connector.

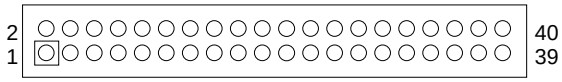


Figure 3-5 CN1: Hard Disk (IDE) connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	Not used
21	Not Used	22	GROUND
23	-IOW	24	GROUND
25	-IOR	26	GROUND
27	Not Used	28	BALE
29	Not Used	30	GROUND
31	IRQ14	32	-IOCS16
33	SA 1	34	Not used
35	SA 0	36	SA 2
37	-CS 0	38	-CS 1
39	HD LED A	40	GROUND

Table 3-1 HDD Pin Assignment

3.2.3 Power Connector (J5)

J5 is 8-pin power connector. Using the J5, you can connect the power supply to the on board power connector for stand alone applications directly.

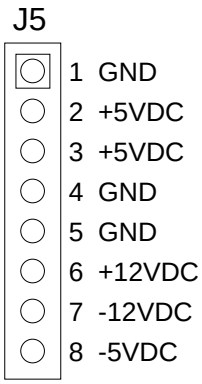


Figure 3-6 J5: Power Connector

3.2.4 FDD Port Connector (CN2)

The AR-B1474 provides a 34-pin header type connector for supporting up to two floppy disk drives.

To enable or disable the floppy disk controller, please use BIOS Setup program to select.

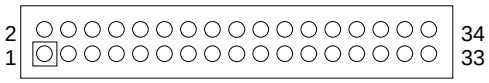


Figure 3-7 CN2: FDD Port connector

Pin	Signal	Pin	Signal
1-33(odd)	GROUND	18	-DIRECTION
2	-Reduce Write Current	20	-STEP OUTPUT PULSE
4	Not used	22	-WRITE DATA
6	Not used	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE A	28	-WRITE PROTECT
12	-DRIVE SELECT B	30	-READ DATA
14	-DRIVE SELECT A	32	-SIDE 1 SELECT
16	-MOTOR ENABLE B	34	-DISK CHANGE

Table 3-2 FDD Pin Assignment

3.2.5 Parallel Port Connector (CN3)

To use the parallel port, an adapter cable has been connected to the CN3 (26-pin header type) connector. This adapter cable is included in your AR-B1474 package. The connector for the parallel port is a 25-pin D-type female connector.

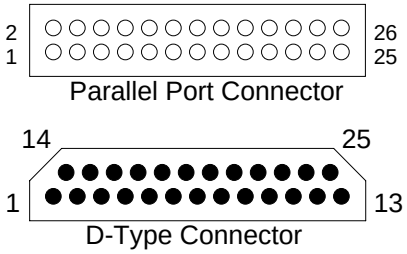


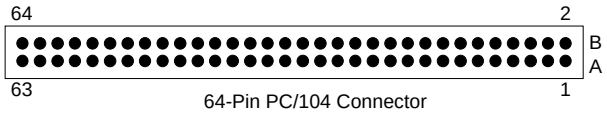
Figure 3-8 CN3: Parallel Port Connector

CN3	DB-25	Signal	CN3	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper Empty	24	25	Ground
25	13	Printer Select	26	--	No Connect

Table 3-3 Parallel Port Pin Assignments

3.2.6 PC/104 Connector

(1) 64-Pin PC/104 Connector Bus A & B (CN6)

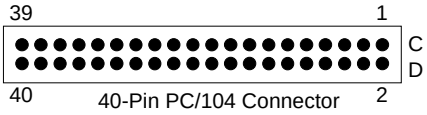


CN6

	1	2	
-IOCHCK ---	A1	B1	--- GND
SD7 ---	A2	B2	--- RSTDRV
SD6 ---	A3	B3	--- +5 VDC
SD5 ---	A4	B4	--- IRQ9
SD4 ---	A5	B5	--- -5 VDC
SD3 ---	A6	B6	--- DRQ2
SD2 ---	A7	B7	--- -12 VDC
SD1 ---	A8	B8	--- -ZWS
SD0 ---	A9	B9	--- +12 VDC
IOCHRDY---	A10	B10	--- KEY
AEN ---	A11	B11	--- -SMEMW
SA19 ---	A12	B12	--- -SMEMR
SA18 ---	A13	B13	--- -IOW
SA17 ---	A14	B14	--- -IOR
SA16 ---	A15	B15	--- -DACK3
SA15 ---	A16	B16	--- DRQ3
SA14 ---	A17	B17	--- -DACK1
SA13 ---	A18	B18	--- DRQ1
SA12 ---	A19	B19	--- -REFRESH
SA11 ---	A20	B20	--- BUSCLK
SA10 ---	A21	B21	--- IRQ7
SA9 ---	A22	B22	--- IRQ6
SA8 ---	A23	B23	--- IRQ5
SA7 ---	A24	B24	--- IRQ4
SA6 ---	A25	B25	--- IRQ3
SA5 ---	A26	B26	--- -DACK2
SA4 ---	A27	B27	--- TC
SA3 ---	A28	B28	--- BALE
SA2 ---	A29	B29	--- +5 VDC
SA1 ---	A30	B30	--- OSC
SA0 ---	A31	B31	--- GND
GND ---	A32	B32	--- GND

Figure 3-9 CN6: 64-Pin PC/104 Connector Bus A & B

(2) 40-Pin PC/104 Connector Bus C & D (CN4)



CN4

	1	2	
GND ---	C1	D1	--- GND
SBHE ---	C2	D2	--- -MEMCS16
LA23 ---	C3	D3	--- -IOCS16
LA22 ---	C4	D4	--- IRQ10
LA21 ---	C5	D5	--- IRQ11
LA20 ---	C6	D6	--- IRQ12
LA19 ---	C7	D7	--- IRQ15
LA18 ---	C8	D8	--- IRQ14
LA17 ---	C9	D9	--- -DACK0
-MEMR ---	C10	D10	--- DRQ0
-MEMW ---	C11	D11	--- -DACK5
SD8 ---	C12	D12	--- DRQ5
SD9 ---	C13	D13	--- -DACK6
SD10 ---	C14	D14	--- DRQ6
SD11 ---	C15	D15	--- -DACK7
SD12 ---	C16	D16	--- DRQ7
SD13 ---	C17	D17	--- +5 VDC
SD14 ---	C18	D18	--- -MASTER
SD15 ---	C19	D19	--- GND
KEY ---	C20	D20	--- GND

Figure 3-10 CN4: 40-Pin PC/104 Connector Bus C & D

(3) PC/104 ISA Bus Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 – SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-4 PC/104 ISA Bus Pin Assignment

3.2.7 CPU Setting

The AR-B1474 accepts many types of microprocessor, such as INTEL/AMD/CYRIX 486DX/DX2/DX4. All of these CPUs include an integer processing unit, floating-point processing unit, memory-management unit, and cache. They can give a two to ten-fold performance improvement in speed over the 386 processor, depending on the clock speeds used and specific application. Like the 386 processor, the 486 processor includes both segment-based and page-based memory protection schemes. Instruction processing time is reduced by on-chip instruction pipelining. By performing fast, on-chip memory management and caching, the 486 processor relaxes requirements for memory response for a given level of system performance.

(1) AMD DX2-80 CPU Select (JP1)

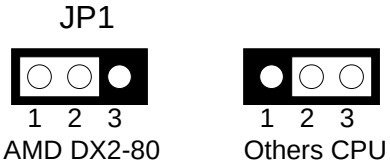


Figure 3-11 JP1: AMD DX2-80 CPU Select

(2) CPU Voltage Select (JP2)

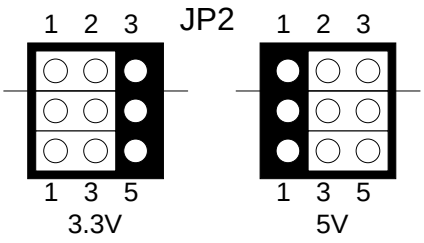


Figure 3-12 JP2: CPU Voltage Select

(3) AMD 4X CPU (5x86) Select (JP15)

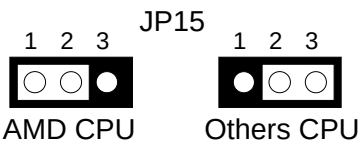


Figure 3-13 JP15: AMD 4X CPU (5x86) Select

(4) CPU Clock Select (JP6 & JP9)

For different type of CPUs, the clock generator and clock divisor need to be set by JP6 and JP9. The clock base is selected by JP6, JP9 is used to select single or half clock system. We recommend that you refer the following table for setting the CPU clock.

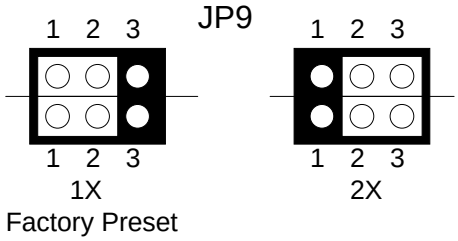


Figure 3-14 JP9: CPU System Clock Multiplier Select

Pin	Definition
1-2	A
3-4	B
5-6	C

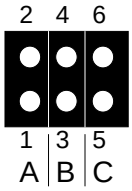


Table 3-5 JP6: CPU Base Clock

CPU Type	CPU Clock	Base Clock	JP9	JP6			Note
				A	B	C	
DX-25, DX2-50, DX4-75	25MHz	50MHz	1X	Close	Open	Open	
DX-33, DX2-66, DX4-100, 5X86-133	33.3MHz	33.3MHz	1X	Close	Open	Close	Factory Preset
DX-40, DX2-80, DX4-120	40MHz	40MHz	1X	Close	Close	Open	
DX-50	50MHZ	50MHz	1X	Close	Close	Close	

Table 3-6 CPU Clock Setting

3.2.8 Memory Setting

(1) Cache RAM Size Select (JP8)

The AR-B1474 can be configured to provide a write-back or write-through cache scheme and support 128KB to 512KB cache systems. A write-back cache system may provide better performance than a write-through cache system. The BIOS Setup program allows you to set the cache scheme either write-back or write-through, either the internal cache selection.

The AR-B1474 needs four 32Kx8 SRAM chips to construct 128KB cache. To construct 256KB cache, four 64Kx8 SRAM chips are needed. Four 128Kx8 SRAM chips will provide 512KB cache.

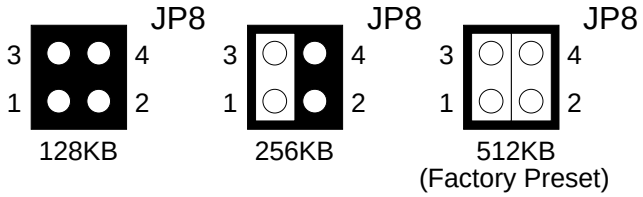


Figure 3-15 JP8: Cache RAM Size Select

(3) DRAM Configuration

There is one 32-bit memory bank on the AR-B1474 card. It can be one-side or double-side SIMM (Single-Line Memory Modules) which is designed to accommodate 256Kx36 bit to 8Mx36 bit SIMMs. This provides the user with up to 32MB of main memory. The 32-bit SIMM (without parity bit) also can be used on AR-B1474 card. There are six on-board memory configurations available. Please refer to the following table for details:

SIMM1	Total Memory
256KX32(X36)	1MB
512KX32(X36)	2MB
1MX32(X36)	4MB
2MX32(X36)	8MB
4MX32(X36)	16MB
8MX32(X36)	32MB

Table 3-7 DRAM Configuration

3.2.9 LED Header (J1, J2 & J4)

(1) External Power LED & Keyboard Lock Header (J4)

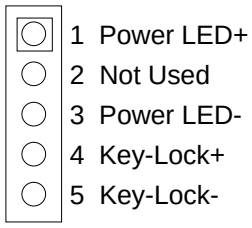


Figure 3-16 J4: Power LED & Key Lock Header

(2) HDD LED Header (J1)

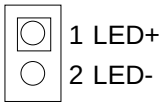


Figure 3-17 J1: HDD LED Header

(3) Watchdog LED Header (J2)

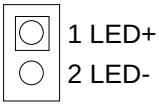


Figure 3-18 J2: Watchdog LED Header

3.2.10 Keyboard Connector

(1) 6-Pin Mini DIN Keyboard Connector (CN5)

CN5 is a 6-pin Mini-DIN connector. This keyboard connector is PS/2 type keyboard compatible. An PC/AT compatible keyboard can be used by connecting the provided adapter cable CN5 and keyboard.

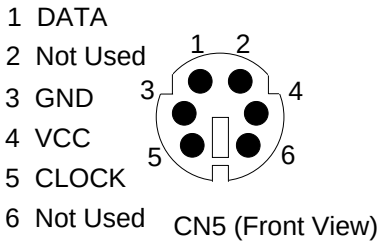


Figure 3-19 CN5: Keyboard Connector

(2) AUX. Keyboard Connector (J8)

A PC/AT compatible keyboard can be used by connected the provided adapter cable between J8 and the keyboard. The pin assignments of J8 connector are as follows:

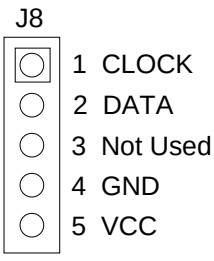


Figure 3-20 J8: AUX. Keyboard Connector

3.2.11 External Speaker Header (J3)

Besides the on board buzzer, you can use an external speaker by connecting J3 header directly.

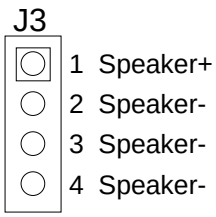


Figure 3-21 J3: External Speaker Header

3.2.12 Reset Header (J7)

J7 is used to connect to an external reset switch. Shorting these two pins will reset the system.

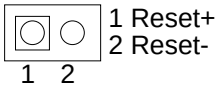


Figure 3-22 J7: Reset Header

3.2.13 Battery Setting

(1) Battery Charger Select (JP4)

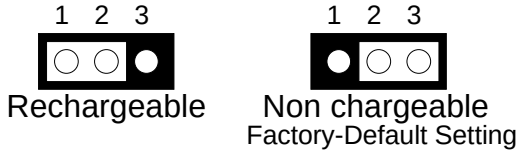


Figure 3-23 JP4: Battery Charger Select

(2) External Battery Connector (J6)

J6 allows users to connect an external 4.5 to 6 VDC battery to the AR-B1474 if the on-board battery is empty. Only the SRAM disk will sink the battery current. If no SRAM chip will be used, no battery is needed. The battery charger on AR-B1474 does not source charge current to the external battery which connects on J6.

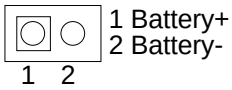


Figure 3-24 J6: External Battery Connector

3.2.14 CRT Display Type Select (JP13)

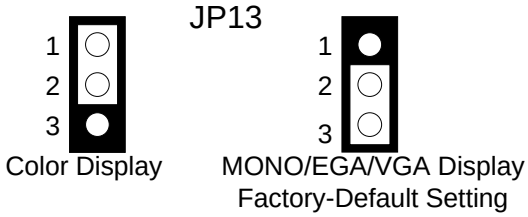


Figure 3-25 JP13: CRT Display Type Select

4. INSTALLATION

This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Utility Diskette
- Write Protect Function
- Watchdog Timer

4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1474 CPU card. Please read the details of the CPU card's hardware descriptions before installation carefully, especially jumpers setting, switch setting and cable connection.

Follow steps listed below for proper installation:

Step 1 : Read the CPU card's hardware description in this manual.

Step 2 : Install any DRAM SIMM onto the CPU card.

Step 3: Install the EPROMs, FLASHs ro SRAMs on the memory sockets.

Step 4 : Set jumpers and switch.

Step 5 : Make sure that the power supply connected to your passive CPU board is turned off.

Step 6 : Plug the CPU card into a free AT-bus slot or PICMG slot on the backplane and secure it in place with a screw to the system chassis.

Step 7 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

Step 8 : Connect the hard disk/floppy disk flat cables from the CPU board to the drives. Connect a power source to each drive.

Step 9 : Install a MDA, CGA, EGA or VGA display card in your system.

Step 10 : Plug the keyboard into the keyboard connector.

Step 11 : Turn on the power.

Step 12: Configure your system with the BIOS Setup program then re-boot your system.

Step 13: If the CPU card does not work, turn off the power and read the hardware description carefully again.

Step 14: If the CPU card still does not perform properly, return the card to your dealer for immediate service.

4.2 UTILITY DISKETTE

To support the AR-B1474 solid state disk's operations, the following programs or files has been provided on the accompanying utility diskette:

(1) PGM1474.EXE

PGM1474.EXE PGM1474.EXE is used to program the 12V FLASH EPROM after the ROM pattern files are generated by RFG.EXE The PGM1474.EXE can also program the correctness of the ROM pattern files onto 5V FLASH EPROM (start from MEM1) or SRAM for testing the ROM pattern files.

To execute PGM1474.EXE, the main menu will be displayed on your screen. There are 8 options on the main menu.

Quit to DOS
Quits and exits to the DOS.

OS Shell
Exits from PGM1474 temporarily to the DOS prompt. Type EXIT to return to PGM1474 main menu.

Load ROM File
If this option is used, the PGM1474 will prompt you for the ROM pattern file name. This option is useful if you have not previously entered a ROM pattern file name or if you wish to use a different ROM pattern file. The PGM1474 will check and display the ROM file name, ROM file size, (FLASH) memory capacity and the number of ROM pattern files that will be loaded and copied onto the (FLASH) memory chips.

Verify Memory
If ROM pattern files were loaded without error, this option instructs PGM1474 to verify the contents of (FLASH) memory chips with the current ROM pattern files.

Program Memory
If there are no mistakes in your ROM pattern file, then this menu option will erase (FLASH) memory, write the current ROM pattern files onto (FLASH) memory and verify data that was just written to (FLASH) memory, using the ROM pattern files.

Memory Type/Mfr.
Before you program the (FLASH) memory chips, make sure that the FLASH's type and manufactory match the one shown on the main menu. Otherwise, you can use this option to select the proper type and manufacture and instruct the program to use a right programming algorithm.

Select PGM Chips
Normally the PGM1474 will program all ROM pattern files onto the FLASH memories with the ROM pattern files just loaded. But you can use this option to select which memory chips that you want to program and which memory chips need to be skipped. The PGM1474 will only program the selected chips when writing data to the FLASH memory. This is very useful when some of the memory chip were verified and programmed previously.

Select FLASH PLSCNTs
If the 12V FLASHs have been programmed several times, please select the <Slowest> FLASH PLSCNT mode instead of <Standard> mode. In the <Slower> or <Slowest> mode, PGM1474.EXE will retry more times to program data onto the 12V FLASHs correctly.
The default setting is <Slowest> mode.

(2) WD1474.EXE

WD1474.EXE This program demonstrates how to enable and trigger the watchdog timer. It allows you to test the <TIMES-OUT & RESET> function when the watchdog timer is enabled.

(3) WP1474.EXE

WP1474.EXE This program demonstrates how to enable and disable software write protected function. It also shows the current protect mode of write or read only memory.

(4) BU1474.EXE

BU1474.EXE BU1474.EXE is used to update the SSD BIOS conveniently if the SSD BIOS need to be revised. This program will erase the BIOS ROM and reprogram with revised BIOS.

(5) RFG.EXE

RFG.EXE This program is used to generate ROM pattern files in a binary format. Each ROM pattern file has the same size as the FLASH or EPROM and can be easily programmed on to the FLASH with on-board programmer or on to EPROM with any EPROM programmer. If you have specified a DOS drive in the *.PGF file, RFG will generate bootable ROM pattern files for the EPROM or FLASH disk. The RFG supports the following DOS: MS-DOS, PC-DOS, DR-DOS, and X-DOS.

NOTE: If you want to use AR-B1474 with any DOS which is not supported by RFG, please send your requirement to Acrosser Technology Co., Ltd. or contract with your local sales representative.

The RFG.EXE provided in the utility diskette is a program that converts the files you list in the PGF and convert them into ROM pattern file. The RFG will determine how many EPROMs are needed and generate the same number of ROM pattern files. These ROM pattern files are named with the name assigned by the ROM_NAME in the PGF and the extension names are *.R01, *.R02….etc. To generate ROM pattern files.
The ROM File Generator main menu will be displayed on the screen. There are 7 options on the main menu. They serve the following functions:

Quit to DOS
Quits and exits to the DOS

OS Shell
Exits from the RFG temporarily to the DOS prompt. Type <EXIT> to return to the RFG main menu.

Load PFG File
If this option is used, the RFG will prompt you for the PGF file name. This option is useful if you have not previously entered a PGF name or you wish to use a different PGF file. The RFG will check and display the PGF filename, ROM pattern file name, EPROM capacity, DOS version and the number of ROM pattern files that will be generated.

Type Current PGF File
This option instructs the RFG to use the DOS type command to display the contents of the current PGF file.

Generate ROM File(s)
If there is no mistake in your *.PGF file, then this menu option will generate ROM pattern files. The number of ROM pattern file generated by the RFG will depend on the total capacity needed by your files. For instance, if 3 files are generated, then you will need to use 3 EPROMs (The size depends upon the number

stated in your PGF). The ROM pattern files will have the same file names, but will have different extension names. For example:

TEST.R01, TEST.R02, TEST.R03…etc.

Display Error in PGF File

This option displays errors that were detected in your PGF.

Help to PGF File

This option gives information on how to write a PGF file and how to generate ROM pattern files. An example PGF is also included.

Move the reverse video bar to <Generate ROM File(s)> then press [ENTER]. The ROM pattern file is a binary file. The file size will be the same size as the EPROM that you assigned in the PGF. For example, if you are using 128KX8 EPROM memory chips, then the size of ROM patterns file will be 131072 bytes. For other chips the file size will be:

64KX8 EPROM----65536 bytes
256KX8 EPROM—262144 bytes
512KX8 EPROM---524288 bytes
1MX8 EPROM -----1048576 bytes

(6) RFGDEMO.PGF

RFGDEMO.PGF This file provides a sample PROGRAM GROUP FILE which illustrates how to create ROM pattern files correctly.

The PGF is an ASCII text file that can be created by using any text editor, word processor or DOS <COPY CON> command. The PGF lists what files will be copied and if DOS is going to be copied. This file can have any DOS filename, but the extension name must be *.PGF. For example, followings are valid filenames.

RFGDEMO.PGF
MYRFG.PGF
MSDOS.PGF
….

An examples of the *.PGF file is as follow.

```
ROM_NAME=TEST1      ; ROM pattern file name is TEST1
                    ;The output file names will be TEST1.R01, TEST1.R02..etc.
DOS_DRIVE=C:        ; DOS system drive unit is drive C:
                    ;If user does not want to copy DOS
                    ;system files onto the ROM disk
                    ;write as DOS_DRIVE=NONE
ROM_SIZE=128        ;128 means 128KX8 (27C/29F010) EPROM size used
                    ;256 means 512KX8 (27C/29F020) EPROM size used
                    ;512 means 512KX8 (27C/29F040) EPROM size used
                    ;1024 means 1MX8 (27C080) EPROM size used
```

The following two files are options which depend on whether the ROM disk is to be bootable or not.

CONFIG.SYS
AUTOEXEC.BAT

```
;Below are user's files
A:\USER1.COM     ; File USER1.COM on root of drive A:
USER2.EXE        ; File USER2.EXE on current directory & drive
C:\TTT\USER3.TXT ; File USER3.TXT on sub-directory TTT of drive C:
```

4.3 WRITE PROTECT FUNCTION

The AR-B1474 provides hardware and software write protect functions for small page 5V FLASH disk and only software write protected function for SRAM disk. This is to prevent your data on 5V FLASH or SRAM disk from accidental deletion or overwrite. If your FLASH/SRAM disk is write protected, any write operation to the protected FLASH/SRAM disk will get a write protect error:

```
Write protect error writing drive A
About, Retry, Fail?
```

4.3.1 Hardware Write Protect

To enable the hardware protect function for small page 5V FLASH disk, please set the SW1-5 to "ON" and the SW1-6 to "OFF", please refer to the "Switch Setting".

4.3.2 Software Write Protect

If you need the write protect function and sometimes you have to write or update data on your FLASH/SRAM disk, you can use the software write protect instead of hardware write protect. The software write protect function is enabled or disabled by writing a data to an I/O port.

4.3.3 Enable the Software Write Protect

Writes data 08h to the base port+2 address

Example 1: (in assembly language)

```
MOV DX, 212H     ; If the AR-B1474's base I/O address is 210H
MOV AL, 08H      ; Enable byte = 08h
OUT DX, AL
```

Example 2: (in BASICA language)

```
OUT &H212, &H08; REM If the AR-B1474's base I/O address is 210h
```

Example 3: (in Turbo C language)

```
outportb(0x212,0x08);/*If the AR-B1474's base I/O address is 210h*/
```

4.3.4 Disable the Software Write Protect

Writes data 0 to the base port+2 address

Example 1: (in assembly language)

```
MOV DX, 212H     ; If the AR-B1474's base I/O address is 210h
MOV AL, 00H      ; Disable byte=00h
OUT DX, AL
```

Example 2: (in BASICA language)

```
OUT &H212, &H00      ; REM If the AR-B1474's base I/O address is 210h
```

Example 3: (in Turbo C language)

```
outportb(0x212,0x00);    /*If the AR-B1474's base I/O address is 210h*/
```

4.4 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The AR-B1474 is equipped with a programmable time-out period watchdog timer. This watchdog timer can be enabled by your program. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang-up, it will generate a reset signal to reset the system or generate the IRQ15 signal to tell your program that the watchdog is times out. The time-out period can be programmed to be 6 to 42 seconds.

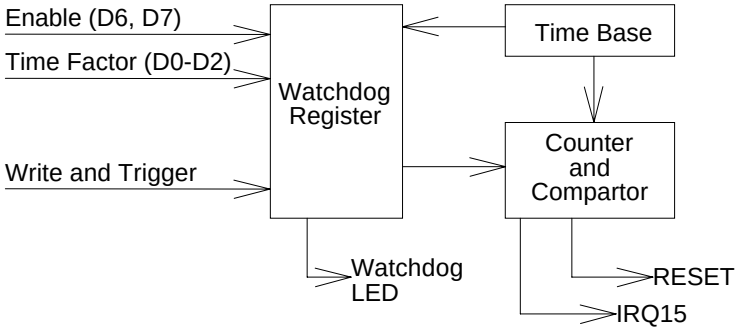


Figure 4-1 Watchdog Block Diagram

4.4.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog is times out.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out period.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 4-1 Time-Out Setting

If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period.

Time Factor	Time-Out Period (Seconds)
0C0H	3
0C1H	6
0C2H	12
0C3H	18
0C4H	24
0C5H	30
0C6H	36
0C7H	42

Table 4-2 Time-Out Setting

NOTE: 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.
2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

4.4.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is Base Port+4. The following is a BASICA program which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000        REM Points to command register
1010              WD_REG% = BASE_PORT% + 4
1020        REM Timer factor = 84H (or 0C4H)
1030              TIMER_FACTOR% = %H84
1040        REM Output factor to watchdog register
1050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

4.4.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010              WD_REG% = BASE_PORT% + 4
2020        REM Timer factor = 84H (or 0C4H)
2030              TIMER_FACTOR% = &H84
2040        REM Output factor to watchdog register
2050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

4.4.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010              WD_REG% = BASE_PORT% + 4
3020        REM Timer factor = 0
3030              TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050              OUT WD_REG%, TIMER_FACTOR%
      ., etc.
```

5.SOLID STATE DISK

The section describes the various type SSDs’ installation steps as follows. This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Switch Setting
- Jumper Setting
- ROM Disk Installation

5.1 OVERVIEW

The AR-B1474 provides three 32-pin JEDEC DIP sockets which may be populated with up to 3MB of EPROM or 1.5MB of FLASH or 1.5MB of SRAM disk. It is ideal for diskless system, high reliability and/or high-speed access applications, controller for industrial or line test instruments, etc.

FLASH disk function allows you to directly program the ROM disk without having to purchase any additional programming equipment. If small page (less or equal 512 bytes per page) 5V FLASHs were used, you could format FLASH disk and copy files onto FLASH disk just like using a normal floppy disk. You could use all of the related DOS command (such as COPY, DEL, …etc.) to update files on the 5V FLASH disk.

The write protect function allows you to prevent your data on small page 5V FLASH or SRAM disk from accidental deletion or overwrite.

Data retention of SRAM is ensured by an on-board Lithium battery or an external battery pack that could be connected to the AR-B1474.

5.2 SWITCH SETTING

We will show the locations of the AR-B1474 switch, and the factory-default setting.

CAUTION: The switch setting needs to adjust with the jumpers setting, make sure the jumper settings and the switch setting are correct.

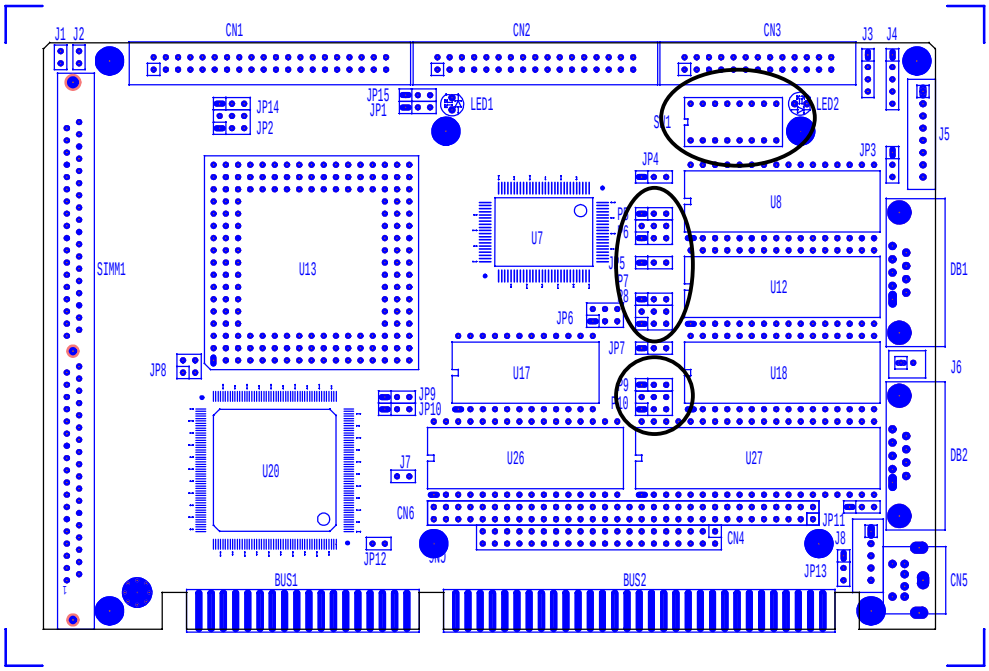


Figure 5-1 Switch & SSD Type Jumper Location

5.2.1 Overview

There is 1 DIP Switch located on the AR-B1474. It performs the following functions:

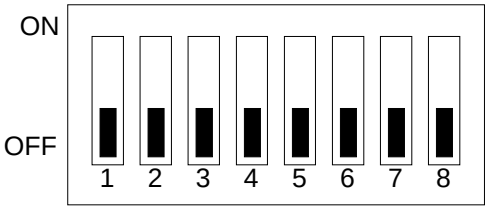


Figure 5-2 SW1: Switch Select

SW1-1 & SW1-2 Set the base I/O port address
SW1-3 & SW1-4 Set the starting memory address
SW1-5 & SW1-6 Set the drive number of solid state disk
SW1-7 & SW1-8 Set the used ROM memory chips

5.2.2 I/O Port Address Select (SW1-1 & SW1-2)

SW1-1 & SW1-2 are provided to select one of the four base port addresses for the watchdog timer and the solid state disk. The AR-B1474 occupies 6 I/O port addresses. Followings state selections of base port address.

SW1-1	SW1-2	Base Port	Solid State Disk	Watchdog
OFF (*)	OFF	210h	210h-213h	214h-215h
ON	OFF	290h	290h-293h	294h-295h
OFF	ON	310h	310h-313h	314h-315h
ON	ON	390h	390h-393h	394h-395h

Table 5-1 I/O Port Address Select

5.2.3 SSD Firmware Address Select (SW1-3 & SW1-4)

The AR-B1474's SSD firmware occupies 16KB of memory. SW1-3 & SW1-4 are used to select the memory base address. You must select an appropriate address so that the AR-B1474 will not conflict with memory installed on other add-on memory cards. Additionally, be sure not to use shadow RAM area or EMM driver's page frame in this area.

SW1-3	SW1-4	SSD BIOS Address	Bank Memory Address
OFF (*)	OFF	C800:0 (8KB)	CA00:0 (8KB)
ON	OFF	CC00:0 (8KB)	CE00:0 (8KB)
OFF	ON	D000:0 (8KB)	D200:0 (8KB)
ON	ON	DC00:0 (8KB)	DE00:0 (8KB)

Table 5-2 SSD Firmware Address Select

If you are not going to use the solid state disk (SSD), you could use JP7 to disable the SSD BIOS. The AR-B1474 will not occupy any memory address if the SSD BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page which is used by AR-B1474. For example, write a statement in the CONFIG.SYS file as follow: (If the memory configuration of AR-B1474 is C800:0)

DEVICE=C:\DOS\EMM386.EXE X=C800-CFFF

5.2.4 SSD Drive Number (SW1-5 & SW1-6)

The AR-B1474 SSD can simulate one or two disk drives. You can assign the drive letter of the AR-B1474 by configuring SW1-5 & SW1-6.

You can make the computer to boot from SSD by copying DOS into the SSD. If your SSD does not have DOS, the computer will boot from your hard disk or floppy disk. In this condition, the SSD BIOS of AR-B1474 will set the drive letter of the SSD to the desired drive letter automatically.

The AR-B1474 would simulate a single disk drive when only (FLASH) EPROM or SRAM (starting from MEM1 socket) is installed. The drive numbers with respect to the switch setting when the AR-B1474 simulates single disk drives.

SW1-5	SW1-6	Occupies floppy disk number (SSD)
OFF (*)	OFF	0 or 1 (Note 1)
ON	OFF	0 or 2 (Note 2)
OFF	ON	0
ON	ON	0

Table 5-3 SSD Drive Number

NOTE: 1. If there is no DOS on this SSD, the disk number will 1 (B:). If any DOS is found by the AR-B1474 SSD BIOS, the disk number will be 0 (A:) But, you can change the disk number from 0 to 1 by pressing the <ESC> key during system bootup.

2. If there is no DOS on this SSD, the disk number will be 2 (C: or D: or…). If any DOS is found by the AR-B1474 SSD BIOS, the disk number will be 0 (A:). But, you can change the disk number from 0 to 2 by pressing the <ESC> key during system bootup.

(1) Simulate 2 Disk Drive

When (FLASH) EPROM and SRAM are both used on the AR-B1474, or you only have installed SRAM that does not start from MEM1 socket, the AR-B1474 will simulate two disk drives. The drive numbers respect to those switch settings when AR-B1474 simulates two disk drives.

SW1-5	SW1-6	Occupies floppy disk number	
		FLASH (EPROM)	SRAM
OFF	OFF	0 or 1 (Note 1)	2
ON	OFF	0 or 2 (Note 2)	3
OFF	ON	0	1
ON	ON	0	2

Table 5-4 SSD Drive Number for Simulate 2 Disk Drive

NOTE: 1. If there is no DOS on this SSD, the disk number will be 1 (B:). If any DOS is found by the AR-B1474 SSD BIOS, the disk letter will be 0 (A:). But, you can change the disk number from 0 to 1 by pressing the <ESC> key during system bootup.

2. If there is no DOS on this SSD, the disk number will be 2 (C: or D: or….). If any DOS is found by the AR-B1474 SSD BIOS, the disk number will be 0 (A:). But, you can change the disk number from 0 to 2 by pressing the <ESC> key during system bootup.

(2) Disk Drive Name Arrangement

If any logical hard disk drives exist in your system, there will also be a different disk number depending on which version DOS you are using.

The solid state disk drive number with there respective DOS drive designation are listed in table as follows. The solid state disk drive number is changeable as the DOS version. The following table expresses the variety.

Condition	Floppy disk No.				Logical hard disk			
	0	1	2	3	1	2	3	4
No Logical hard disk	A:	B:	C:	D:	--	--	--	--
1 Logical hard disk	A:	B:	C:	D:	E:	--	--	--
2 Logical hard disk	A:	B:	C:	D:	E:	F:	--	--
3 Logical hard disk	A:	B:	C:	D:	E:	F:	G:	--
4 Logical hard disk	A:	B:	C:	D:	E:	F:	G:	H:

Table 5-5 SSD Drive Number for DOS Version before 5.0

Condition	Floppy disk No.				Logical hard disk			
	0	1	2	3	1	2	3	4
No Logical hard disk	A:	B:	C:	D:	--	--	--	--
1 Logical hard disk	A:	B:	D:	E:	C:	--	--	--
2 Logical hard disk	A:	B:	E:	F:	C:	D:	--	--
3 Logical hard disk	A:	B:	F:	G:	C:	D:	E:	--
4 Logical hard disk	A:	B:	G:	H:	C:	D:	E:	F:

Table 5-6 SSD Drive Number for DOS Version 5.0 and Newer

5.2.5 ROM Type Select (SW1-7 & SW1-8)

SW1-7 & SW1-8 are used to select the memory type of ROM disk section.

SW1-7	SW1-8	EPROM Type
OFF	OFF	UV EPROM (27Cxxx)
ON	OFF	5V FLASH 29Fxxx (*Note)
OFF	ON	5V FLASH (29Cxxx & 28EExxx)
ON	ON	12V FLASH (28Fxxx)

Table 5-7 ROM Type Select

NOTE: It is also used to perform the hardware write protection of small page 5V FLASH (29Cxxx or 28EExxx) disk.

5.3 JUMPER SETTING

Before installing the memory into memory sockets MEM1 through MEM3, you have to configure the memory type which will be used (ROM/RAM) on the AR-B1474. Each socket is equipped with a jumper to select the memory type.

You can configure the AR-B1474 as a (FLASH) EPROM disk (ROM only), a SRAM disk (SRAM only) or a combination of (FLASH) EPROM and SRAM disk.

It is not necessary to insert memory chips into all of the sockets. The number of SRAM chips required depends on your RAM disk capacity. The number of EPROM chips required depends on the total size of files that you plan to copy onto the ROM disk and whether or not it will be bootable.

Insert the first memory chip into MEM1 if you are going to configure it as a ROM or SRAM disk. If you use a combination of ROM and RAM, then insert the (FLASH) EPROM chip starting with the MEM1, and insert the SRAM chips starting from the first socket which is configured as SRAM.

- M1:is used to configure the memory type of MEM1
- M2:is used to configure the memory type of MEM2
- M3:is used to configure the memory type of MEM3

CAUTION: When the power is turned off, please note the following precautions.

1. If your data has been stored in the SRAM disk, do not change the jumper position or data will be lost.

2. Make sure jumpers are set properly. If you mistakenly set the jumpers for SRAM and you have EPROM or FLASH installed, the EPROM or FLASH will drain the battery's power.

5.3.1 SSD BIOS Select (JP7)

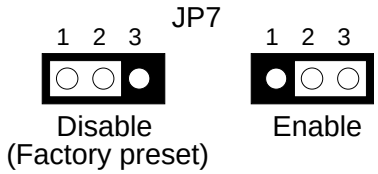


Figure 5-3 JP7: SSD BIOS Select

5.3.2 SSD Memory Type Setting (M1 ~ M3 & JP5)

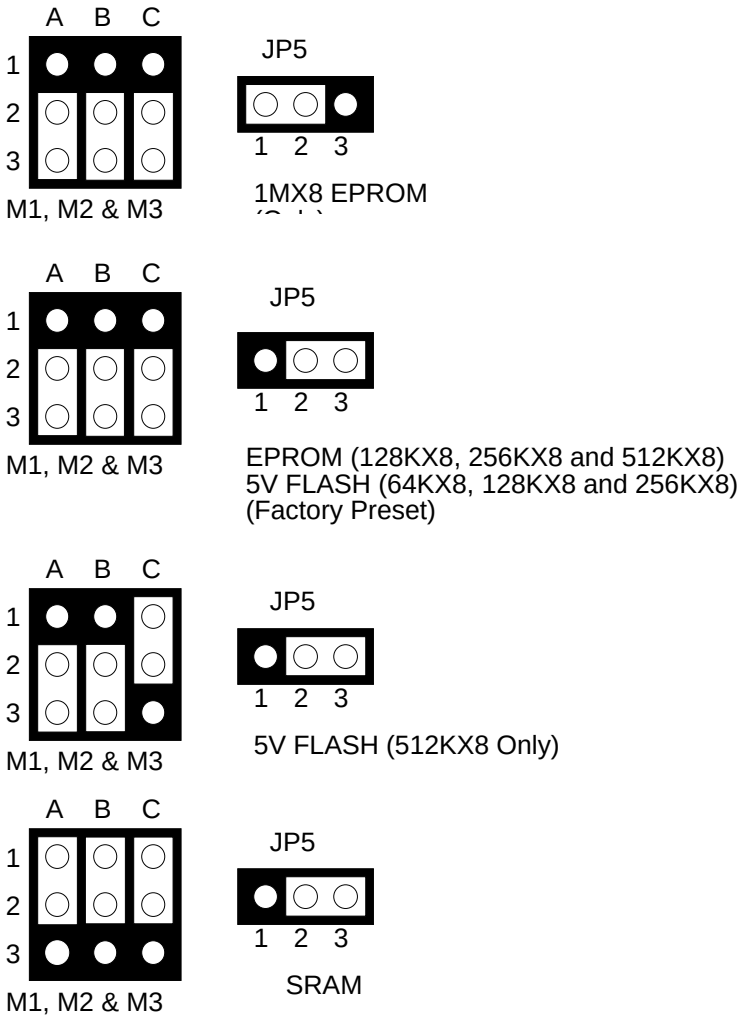


Figure 5-4 M1~M3 & JP5: Memory Type Setting

5.4 ROM DISK INSTALLATION

The section describes the various type SSDs’ installation steps as follows. The jumper and switch adjust as SSD’s different type to set.

5.4.1 UV EPROM (27Cxxx)

(2) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and EPROM type on SW1.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

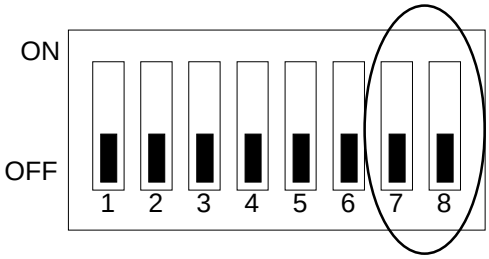


Figure 5-5 UV EPROM (27CXXX) Switch Setting

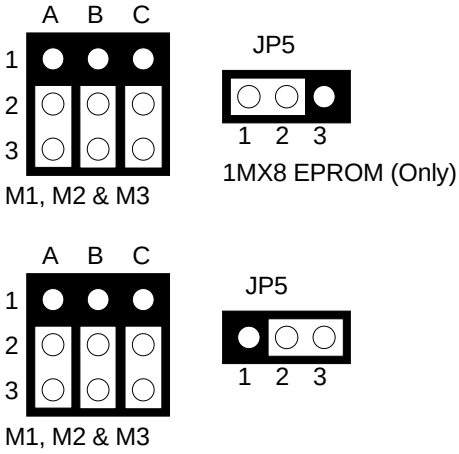


Figure 5-6 UV EPROM Jumper Setting

(2) Software Programming

Use the UV EPROM, please refer to the follow steps:

Step 1: Turn on the power and boot DOS from hard disk drive or floppy disk drive.

Step 2: Making a Program Group File (*.PGF file)

Step 3: Using the RFG.EXE to generate ROM pattern files, and counting the ROM numbers as the pattern files.

Step 4: In the DOS prompt type the command as follows.

```
C:\>RFG [file name of PGF]
```

Step 5: In the RFG.EXE main menu, choose the <Load PGF File> item, that is user editing *.PGF file.

Step 6: Choose the <Generate ROM File(s)>, the tools program will generate the ROM files, for programming the EPROMs.

Step 7: Program the EPROMs
Using the instruments of the EPROM writer to load and write the ROM pattern files into the EPROM chips. Make sure that the EPROMs are verified by the program without any error.

Step 8: Install EPROM chips
Be sure to place the programmed EPROMs (R01, R02….) into socket starting from MEM1 and ensure that the chips are installed in the sockets in the proper orientation.

5.4.2 Large Page 5V FLASH Disk

If you are using large page 5V FLASH as ROM disk, it is the same procedure as step 1 to step 4 of using the UV EPROM.

(2) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and large page 5V FLASH type on SW1.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

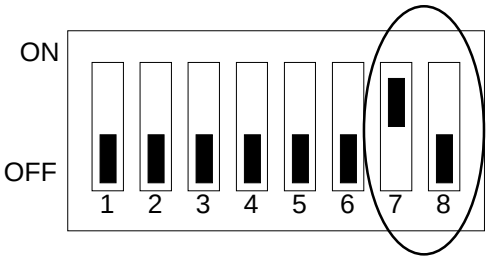
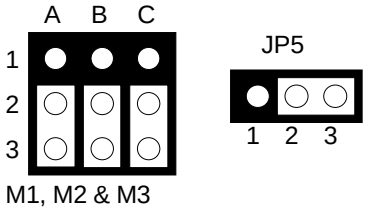
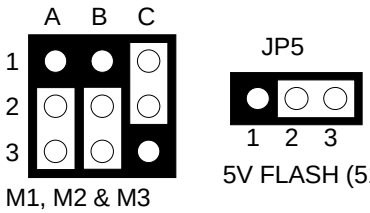


Figure 5-7 5V Large FLASH (29FXXX) Switch Setting



M1, M2 & M3

5V FLASH (64KX8, 128KX8 and 256KX8)
(Factory Preset)



M1, M2 & M3

5V FLASH (512KX8 Only)

Figure 5-8 Large Page 5V FLASH Jumper Setting

(2) Software Programming

And then, you should create a PGF and generate ROM pattern files by using the RFG.EXE.

Step 1: Making a Program Group File (*.PGF file)

Step 2: Generate ROM pattern files

Step 3: Turn off your system, and then install FLASH EPROMs into the sockets.

NOTE: Place the appropriate number of FLASH EPROM chips (the numbers depends on the ROM pattern files generated by RFG.EXE) into the socket starting from MEM1 and ensure that the chips are installed in the sockets in the proper orientation. Line up and insert the AR-B1474 board into any free slot of your computer.

Step 4: Turn on your system, and Program FLASH EPROMs.

NOTE: The FLASH EPROM program is built-in the AR-B1474 board. The FLASH EPROMs can be programmed on the AR-B1474. Before programming the FLASH EPROMs, please insert at least the same number of FLASH EPROMs, please insert at least the same number of FLASH EPROMs, please insert at least the same number of FLASH chips as the ROM pattern files generated.

Step 5: The PGM1474.EXE file is a program that loads and writes the ROM pattern files onto the (FLASH) memory chips. To program the FLASH EPROM.

Step 6: In the DOS prompt type the command as follows.

```
C:\>PGM1474 [ROM pattern file name]
```

Step 7: In the main menu, choose the <Load ROM File> item, that is the ROM_NAME=[file name] in the *.PGF file.

Step 8: Choose the <Program Memory> item, this item program will program the EPROMs.

NOTE: Move the reverse video bar to the <Program memory> option then press <ENTER>. PGM1474 will write the ROM pattern files onto the (FLASH) memories. Ensure that data is verified by the PGM1474 correctly.

Step 9: Reboot the system

NOTE: Reboot your computer by making a software or hardware reset.

5.4.3 Small Page 5V FLASH ROM Disk

(1) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and EPROM type on SW1.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

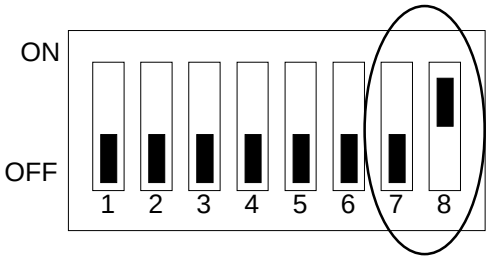


Figure 5-9 5V FLASH (29CXXX & 28EEXXX) Switch Setting

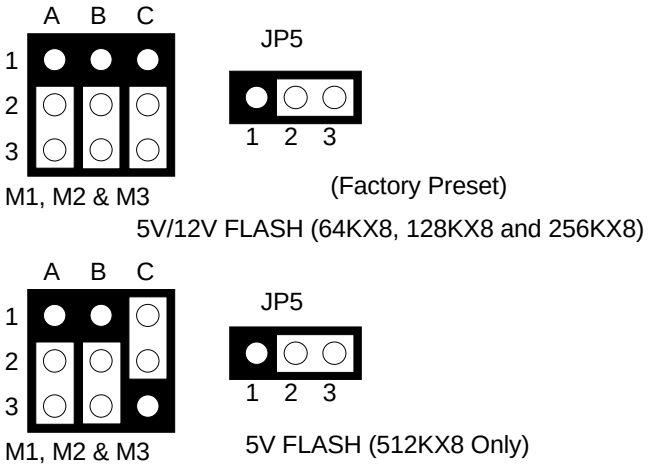


Figure 5-10 5V FLASH (29CXXX & 28EEXXX) Jumper Setting

(2) Using Tool Program

If small page 5V FLASH EPROMs are used, you can use the same method as step 1 to step 4 of using the UV EPROM:

Step 1: Making a Program Group File (*.PGF file)

Step 2: Generating ROM pattern files

Step 3: Installing FLASH EPROMs

Step 4: Programming FLASH EPROMs

Step 5: Reboot system

(3) Typing DOS Command

You can use another way to format and copy files to the 5V FLASH EPROM. This method provides the convenience of using a RAM disk. You can use the DOS <FORMAT> and <COPY> command to format and copy files. Follow the following steps to format and copy files to the FLASH disk. it is the same procedure as step 1 to step 4 of using the UV EPROM.

Step 1: Turn on your computer, when the screen shows the SSD BIOS menu, please hit the [F1] key during the system boot-up, this enables you to enter the FLASH setup program. If the program does not show up, check the switch setting of SW1.

Step 2: Use <Page-Up>, <Page-Down>, <Right>, and <Left> arrow keys to select the correct FLASH memory type and how many memory chips are going to be used.

Step 3: Press the [F4] key to save the current settings.

Step 4: After the DOS is loaded, use the DOS [FORMAT] command to format the FLASH disk.

To format the disk and copy DOS system files to the disk.

C:\>FORMAT [ROM disk letter] /S /U

To format the disk without copying DOS system files.

C:\>FORMAT [ROM disk letter] /U

Step 5: Copy your program or files to the FLASH disk by using DOS [COPY] command.

CAUTION: It is not recommended that the user formatted the disk and copy files to the FLASH disk very often. Since the FLASH EPROM's write cycle life time is about 10,000 or 100,000 times, writing data to the FLASH too often will reduce the life time of the FLASH EPROM chips, especially the FLASH EPROM chip in the MEM1 socket.

5.4.4 RAM Disk

(1) Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number on SW1.

Step 3: Insert programmed SRAM chips into sockets starting at MEM1.

NOTE: If you use the SRAM, please skip the SW1-7 & SW1-8 setting.

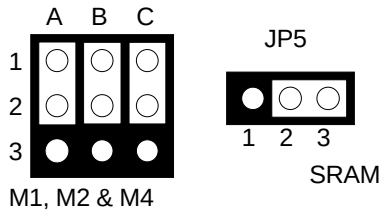


Figure 5-11 SRAM Jumper Setting

(2) Software Programming

It is very easy to use the RAM disk. The RAM disk operates just like a normal floppy disk. A newly installed RAM disk needs to be formatted before files can be copied to it. Use the DOS command [FORMAT] to format the RAM disk.

Step 1: Use jumper block to select the memory type as SRAM refer.

Step 2: Select the proper I/O base port, firmware address and disk drive number on SW1.

Step 3: Insert SRAM chips into sockets starting from MEM1

Step 4: Turn on power and boot DOS from hard disk drive or floppy disk drive.

Step 5: Use the DOS command [FORMAT] to format the RAM disk. If you are installing SRAM for the first time.
To format the RAM disk and copy DOS system files onto the RAM disk.

```
C:\>FORMAT [RAM disk letter] /S /U
```

To format the RAM disk without copying DOS system files into the RAM disk.

```
C:\>FORMAT [RAM disk letter] /U
```

Step 6: Use the DOS command [COPY] to copy files onto the RAM disk. For example, if you want to copy file <EDIT.EXE> to the RAM disk from drive C: and the RAM disk is assigned as drive A:.

```
COPY C:EDIT.EXE A:
```

NOTE: In addition, you can use any other DOS command to operate the RAM disk.

5.4.5 Combination of ROM and RAM Disk

The AR-B1474 can be configured as a combination of one ROM disk and one RAM disk. Each disk occupies a drive unit.

Step 1: Use jumper block to select the proper ROM/RAM configuration you are going to use.

Step 2: Insert the first programmed EPROM into the socket mem1, the second into the socket MEM2, etc.

Step 3: Insert the SRAM chips starting from the first socket assigned as SRAM.

Step 4: Select the proper I/O base port, firmware address and disk drive number on SW1.

Step 5: Turn on power and boot DOS from hard disk drive or floppy disk drive.

Step 6: Use the DOS command [FORMAT] to format the RAM disk.

```
C:\>FORMAT [RAM disk letter] /U
```

Step 7: If 5V FLASH (small page) is being used for the first time.
And then use the DOS command [FORMAT] to format the FLASH disk.

Step 8: If large page 5V FLASH is being installed for the first time, please use the FLASH programming utility PGM1474.EXE to program ROM pattern files, which have been generated by RFG.EXE onto the FLASH chips.

NOTE: Users can only boot DOS from the ROM disk drive if the AR-B1474 is configured as a ROM and a RAM disk. You don't need to copy DOS onto the RAM disk.

5.5 INSTALLATION D.O.C.

5.5.1 Hardware Setting

(1) SSD BIOS Setting (JP7)

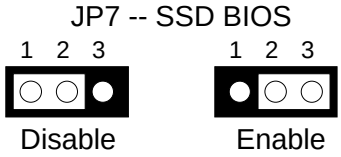


Figure 5-12 JP7: SSD BIOS Setting

(2) D.O.C. Socket Select (M1)

DiskOnChip only use MEM1 socket, so user must set the M1 for adjusting the DiskOnChip's type.

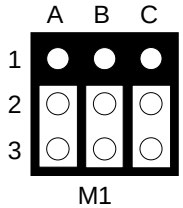


Figure 5-13 M1: D.O.C. Socket Select

(3) D.O.C. Setting (SW1-8)

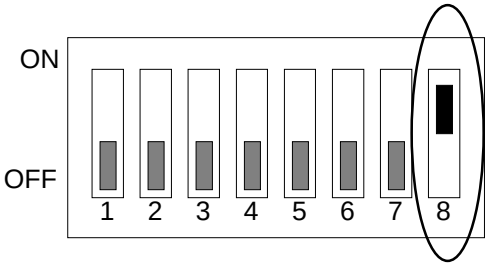


Figure 5-14 SW1-8: D.O.C. Setting

Note: There is 1 DIP switch located on the AR-B1474. It performs the followings:

SW1-1 & SW1-2	Set the base I/O port address
SW1-3 & SW1-4	Set the starting memory address
SW1-5, SW1-6 & SW1-7	The function now is unavailable
SW1-8	Set the DiskOnChip only

5.5.2 Software Setting

We will attach the BU1474.EXE and 1474DOC.INI these two files, BU1474.EXE is the utility program, and the 1474DOC.INI is for D.O.C. BIOS. When user execute the two files for updating will show the message on the screen as follows:

AR-B1474 Special SSD BIOS for DiskOnChip Version 1.5M (C) 1998 Acrosser
DOC Socket Service – Version 0.2
(C) Copyright 1992 – 1996, M-Systems Ltd.

TrueFFS – BIOS – Version 3.3.5 for DiskOnChip 2000 (V1.05)
Copyright (C) M – Systems, 1992 – 1997

Note: If you want to use the D.O.C., and please contact technical engineer for the utility programs.

6. BIOS CONSOLE

This chapter describes the AR-B1474 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power Management
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit
- BIOS Update

6.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

CAUTION: 1. AR-B1474 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

6.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk’s installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

6.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference.

System BootUp Sequence

The option determines where the system looks first for an operating system.

System BootUp Num-Lock

This item is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Floppy Drive Seek At Boot

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon bootup.

System BootUp CPU Speed

The option set the speed of the CPU at system boot time.

Typematic Rate (Chars/Sec)

Typematic Rate sets the rate at which characters on the screen repeat when a key is pressed and held down.

Above 1MB Memory Test

When this option is enabled, the BIOS memory test will be performed on all system memory. When this option is disabled, the memory test will be done only for the first 1MB of system memory.

Memory Test Tick Sound

The option enables or disabled the ticking sound during the memory test.

Password Checking Option

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Hard Disk Type 47 RAM Area

Specify in this option if the top 1KB of the system programming area beginning at 639K or 0:300 in the system BIOS area in low memory will be used to store hard disk information.

Wait for 'F1' If Error

BIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Internal Cache Memory

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 6-1 Internal Cache Setting

External Cache Memory

This option specifies the caching algorithm used for L2 secondary (external) cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 6-2 External Cache Setting

BootSector Virus Protection

When enabled, BIOS warns the user when any program attempts to write to or format the boot sector and allows the user to intervene.

Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 6-3 Shadow Setting

Video ROM Shadow C000, 32K

When this option is set to ***Enabled***, the video ROM area from C000h-C7FFh is copied (shadowed) to RAM for faster execution.

IDE Block Mode Transfer

If your hard disk supports multi-sector transfer, you can enable this option to speed the IDE transfer rate. When ***Enabled***, the Read/Write and From/To operations between BIOS and hard disk will be done block by block.

IDE LBA Mode

The maximum capacity of a standard IDE disk drive without LBA mode was 528MB. The LBA mode enables IDE drive to have more than 528MB in one disk drive.

OnBoard FDC

This option enables the floppy drive controller on the AR-B1474.

OnBoard IDE

This option ***Enabled/Disabled*** the use of the IDE controller on the AR-B1474.

Parallel Port Address

This option is used to select the port address and the IRQ of the on-board parallel port. The addresses are 378H, 278H, 3BCH, and Disable. The IRQs are IRQ5 & IRQ7 for selecting.

Parallel Port Mode

This option is specifies the parallel port mode. The settings are Printer or Extended (Bi-direction). The system support four mode: SPP, EPP & SPP, ECP, ECP & EPP for selecting.

Serial Port 1

This option is used to select the port address and the IRQs of the on-board serial port A. The options are 3F8H, 2F8H, 3E8H, 2E8H, and Disable. The system support IRQ3, IRQ4, IRQ5, and IRQ9 for selecting.

Serial Port 2

This option is used to select the port address and the IRQs of the on-board serial port B. The options are 3F8H, 2F8H, 3E8H, 2E8H, and Disable. The system support IRQ3, IRQ4, IRQ5, and IRQ9 for selecting.

6.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

Automatic Configuration

If selecting a certain setting for one BIOS Setup option determines the settings for one or more other BIOS Setup options, BIOS automatically assigns the dependent settings and does not permit the end user to modify these settings unless the setting for the parent option is changed. Invalid options are grayed and cannot be selected. There is two department: DRAM Setting and ISA Bus Clock & Timing Setting

AR Bus Clock Select
DRAM Read Wait State
DRAM Write Wait State
CACHE Read Wait State
CACHE Write Wait State
Cycle Check Point

These options set the DRAM and Cache RAM access speed. If AUTO Config Function option is enabled, the other options will return to the default settings.

I/O Recovery Feature
I/O Recovery Period

If I/O Recovery Feature option is enabled, the BIOS inserts a delay time between two I/O commands. The delay time is defined in I/O Recovery Period option.

Memory Remapping

If this option is enabled, the un-shadowed RAM area will be remapped to 1MB area above.

Parity Check

This option enables or disables parity error checking for all system RAM. This option must be ***Disabled*** if the used DRAM SIMMs are 32-bit but not 36-bit devices.

Slow Refresh

This options sets the DRAM refresh cycle time. The settings are 15us, 30us, 60us, and 120us.

Hidden Refresh

Hidden refresh separates refreshing of AT-bus memory and local DRAM. The AT-bus controller arbitrates between CPU accesses to the AT bus, DMA, and AT refresh, while the DRAM controller arbitrates between CPU DRAM accesses and DRAM refresh cycle.

Ext. Cache WB/WT Feature

This option selects the type of caching algorithm of secondary cache memory. The settings are Wr-Thru or Wr-Back.

Int. Cache WB/WT Feature

This option selects the type of caching algorithm of CPU internal cache memory. The settings are Wr-Thru or Wr-Back.

ISA Write Cycle Insert WS

When ***Enabled***, the wait state is added in both I/O and memory write cycle.

16-Bit ISA I/O Command WS

This option sets the wait state of 16-bit I/O cycle. The settings are 0WS, 1WS, 2WS, and 3WS.

16-Bit ISA Mem. Command WS

This option sets the wait state of 16-bit memory cycle. The settings are 0WS, 1WS, 2WS, and 3WS.

Polling Clock Select

This option sets the polling clock of IRQ and DRQ signals. The settings are CLK2, CLK2/2, CLK2/3, CLK2/4, 28.6MHz, and 14.3MHz.

6.5 POWER MANAGEMENT

This section is used to configure Power management setup for configuring power management features.

IDE Standby Mode (Min.)

This option specifies the length of time of hard disk drive inactivity that must expire before the IDE hard disk drive is placed in IDE Standby Power Down Mode.

6.6 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

6.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

6.7.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

6.7.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

6.8 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

6.8.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

6.8.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

6.9 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

6.9.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

6.9.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

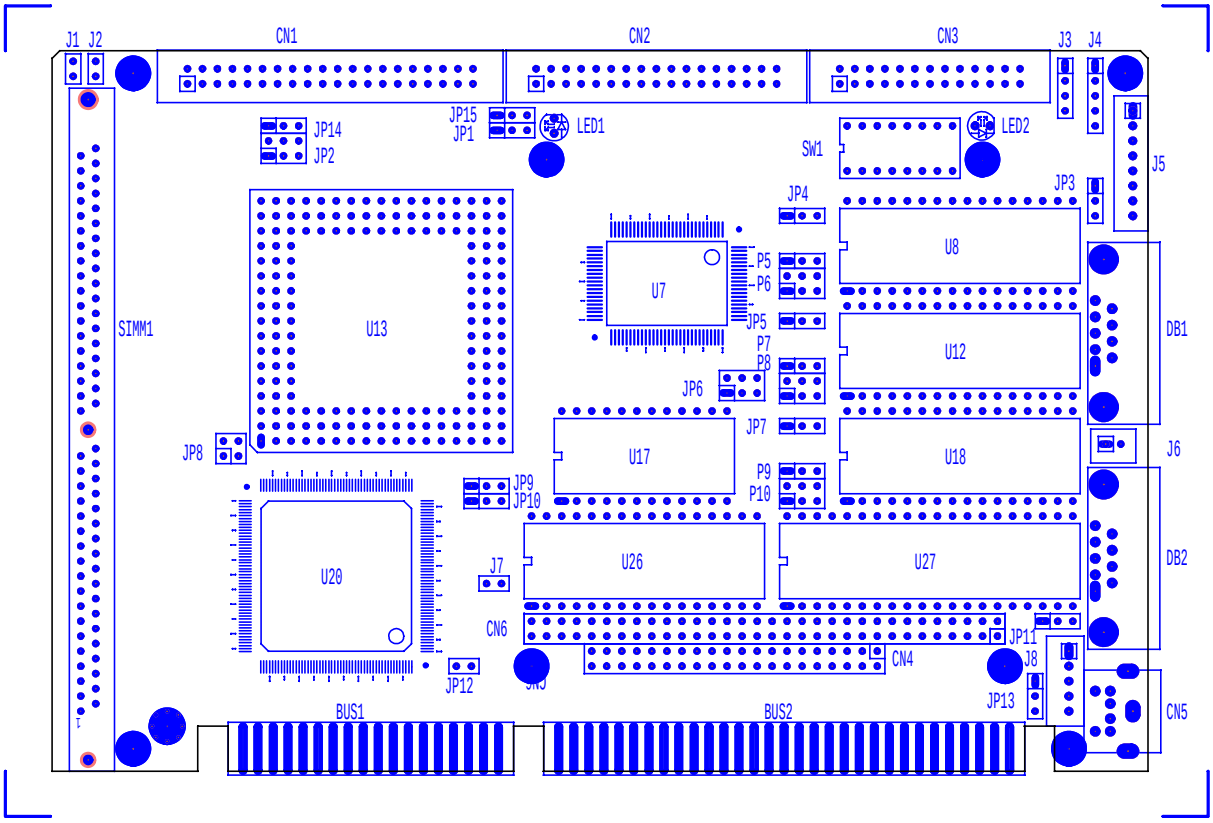
```
Quit without saving (Y/N) ?
```

7. SPECIFICATIONS

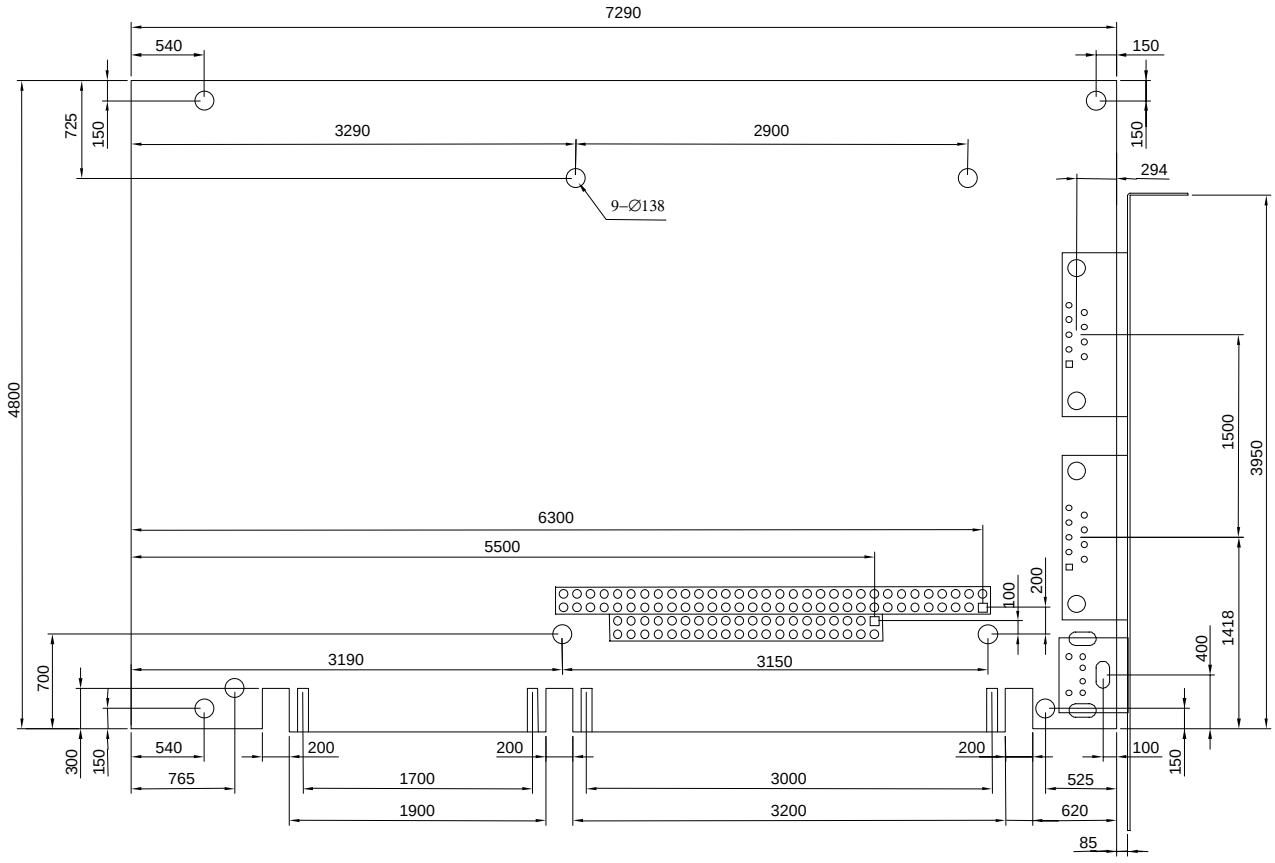
CPU:	25-100 MHz INTEL/AMD/CYRIX 80486DX/DX2/DX4
Bus Interface:	ISA (PC-AT) Bus and PC/104 Bus
Chipset:	ALI M1429 and M1431
RAM Memory:	1MB to 32MB using 32-bit or 36-bit 72-pin SIMMs with access time of 70ns or less
Shadow RAM:	Up to 256KB in 32 KB blocks supports system and video BIOS
Extended Memory Mapping:	Fully supports the LIM EMS 4.0 and 3.2 specifications
Co-Processor:	Supported by all CPUs
BIOS:	Legal AMI system BIOS
IDE HDD Interface:	Supports up to two IDE type hard disk drives (software enable/disable)
Floppy Disk Drive:	Supports up to two 5.25 (360KB & 1.2MB) or 3.5 (720KB & 1.44MB) floppy disk drives (software enable/disable)
Parallel Port:	One Centronic parallel port configurable to LPT1, LPT2, LPT3, or disable.
Serial Port:	Two RS-232C serial port (with 16byte FIFOs, 16C550 compatible) configures as COM1, COM2, COM3, COM4 or disable
Real-Time Clock/Calendar:	DS12887 or compatible chip
Watchdog Timer:	Programmable time-out interval from 6 to 42 seconds. The activity can be Reset System or Generate IRQ 15 Signal
Solid State Disk:	Up to 3MB bootable solid state disk, it accepts 128Kx8 to 1Mx8 EPROM, 128Kx8 to 512Kx8 SRAM, and 64Kx8 to 512Kx8 5V FLASH
Speaker:	Build-in buzzer
DMA Channels:	7 DMA channels
Interrupt Levels:	15 vectored interrupt levels
Keyboard Port:	PS/2 compatible 6-pin mini DIN connector, adapter cable for PC/AT is included
Bus Speed:	Programmable 1/4, 1/5, 1/6, 1/8, 1/10, or 1/12 input clock and 7.159MHz
PCB:	8 layers for noise reduction
System Performance:	Landmark speed V2.0: 359MHz (INTEL 80486DX4-100)
Power Supply:	Only +5V DC +/-% Power requirements: +5V@ 1.5A maximum
Stand Alone Operation:	Provides external power connector and 4 fixed holes for stand-alone operation
Operating Temperature:	0 to 60 degree C (140 degree F)
Storage Temperature:	-25 to 85 degree C
Humidity:	0 to 95% (non-condensing)
Dimensions:	Half size, 12.2cm x 18.5cm (4.80" x 7.29")
Weight:	280g (without CPU, DRAM SIMM, ROM and RAM chips)

8. PLACEMENT & DIMENSIONS

8.1 PLACEMENT



8.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

9.MEMORY BANKS & PROGRAMMING RS-485

9.1 USING MEMORY BANK

This section provides the information about how to access the memory on the AR-B1474 without using the AR-B1474 SSD BIOS. The AR-B1474 hardware divides every 8K bytes of memory into a memory bank. To access the data in the memory, you have to assign the chip number and the bank number. On every chip, the memory bank number starts from zero. The last memory bank number depends on the size of the memory chip used on the AR-B1474. For example, if you use the 256K bytes memory chip, the bank number on every chip would be in the range of 0 to 31. The chip numbers and the bank numbers are determined by the bank select register on the AR-B1474.

The I/O addresses of these registers are determined by SW1-1and SW1-2. The memory address of the memory bank is located on the range selected by SW1-3 and SW1-4.

The I/O port address of the bank select register is base port+0. The following is the format of the bank select register and bank enable register.

BASE+0

D7	D6	D5	D4	D3	D2	D1	D0
CS1	CS0	K5	K4	K3	K2	K1	K0

Where:
CS1-CS0 : Chip select

CS1	CS0	Socket
0	0	Disable
0	1	MEM1
1	0	MEM2
1	1	MEM3

For different types of memory, K0 to K5 have different explanations. These bits are used to select the bank number of specific memory located in CS0 and CS1.

Memory	K5	K4	K3	K2	K1	K0
64KB EPROM (FLASH)	0	1	0	BS2	BS1	BS0
128KB EPROM (FLASH)	0	1	BS3	BS2	BS1	BS0
256KB EPROM (FLASH)	BS4	1	BS3	BS2	BS1	BS0
512KB EPROM (FLASH)	BS4	BS5	BS3	BS2	BS1	BS0
128KB SRAM	1	0	BS3	BS2	BS1	BS0
512KB SRAM	BS5	BS4	BS3	BS2	BS1	BS0

NOTE: BS0 to BS5 are the memory bank select bits. For example, 128KB memory has sixteen 8K-byte banks, so 4 bits (BS0 to BS3) are needed, and 512KB memory needs 6 bits (BS0 to BS5), etc.

Example 1: Select the 10th bank of the MEM1 on the AR-B1474. The AR-B1474 is using 27C020 (256K*8), and the base port is &H210.

```
100 base_port=&H210
110 OUT base_port+0,&H59
```

Example 2: Select the 40th bank of MEM3 on the AR-B1474. The AR-B1474 is using 27C040 (512K*8), and the base port is &H390.

```
200 base_port=&H390
210 OUT base_port+0,&HD7
```

9.2 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 proceeds the transmission which needs control the TXC signal, and the installing steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: Please refer to the section of the “Serial Port” in the chapter “System Control” for the detail description of the COM port’s register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets “0”.

NOTE: Control the AR-B1474 CPU card’s DTR signal to the RS-485’s TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets “1”.

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer’s data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be “0”.

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets “0”

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets “1”.

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer’s data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be “0”.

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets “0”

(4) Receive data

The RS-485’s operation of receiving data is in the same of the RS-232’s.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10    OPEN “COM1:9600,m,8,1”AS #1 LEN=1
20    REM Reset DTR
30    OUT &H3FC, (INP(%H3FC) AND &HFA)
40    RETURN
```

b.) Send out one character to COM1

```
10    REM Enable transmitter by setting DTR ON
20    OUT &H3FC, (INP(&H3FC) OR &H01)
30    REM Send out one character
40    PRINT #1, OUTCHR$
50    REM Check transmitter holding register and shift register
60    IF ((INP(&H3FD) AND &H60) >0) THEN 60
70    REM Disable transmitter by resetting DTR
80    OUT &H3FC, (INP(&H3FC) AND &HEF)
90    RETURN
```

c.) Receive one character from COM1

```
10    REM Check COM1: receiver buffer
20    IF LOF(1)<256 THEN 70
30    REM Receiver buffer is empty
40    INPSTR$”
50    RETURN
60    REM Read one character from COM1: buffer
70    INPSTR$=INPUT$(1,#1)
80    RETURN
```

10.SSD TYPES SUPPORTED & INDEX

10.1 SSD TYPES SUPPORTED

The following list contains SRAMs supported by the AR-B1474:

AKM	AKM628128	(128Kx8, 1M bits)
HITACHI	HM628128	(128Kx8, 1M bits)
NEC	UPD431000A	(128Kx8, 1M bits)
SONY	CXK581000P/M	(128Kx8, 1M bits)
HITACHI	HM628512	(512Kx8, 4M bits)
NEC	UPD434000	(512Kx8, 4M bits)
SONY	CXK584000P/M	(512Kx8, 4M bits)

The following list contains large page 5V FLASHs supported by the AR-B1474:

AMD	Am29F512	(64Kx8, 512K bits)
AMD	Am29F010	(128Kx8, 1M bits)
AMD	Am29F020	(256Kx8, 2M bits)
AMD	Am29F040	(512Kx8, 4M bits)

The following list contains small page 5V FLASHs supported by the AR-B1474:

ATMEL	AT29C512	(64Kx8, 512K bits)
SST	PH29EE512	(64Kx8, 512K bits)
ATMEL	AT29C010	(128Kx8, 1M bits)
SST	28EE010	(128Kx8, 1M bits)
SST	28EE011	(128Kx8, 1M bits)
SST	PH29EE010	(128Kx8, 1M bits)
WINBOND	W29EE011	(128Kx8, 1M bits)
ATMEL	AT29C020	(256Kx8, 2M bits)
ATMEL	AT29C040	(512Kx8, 4M bits)
ATMEL	AT29C040A	(512Kx8, 4M bits)
SST	PH28SF040	(512Kx8, 4M bits)

The following list contains EPROMs supported by the AR-B1474:

AMD	Am27C010	(128Kx8, 1M bits)
ATMEL	AT27C010	(128Kx8, 1M bits)
FUJITSHU	MBM27C1001	(128Kx8, 1M bits)
HITACHI	HN27C101	(128Kx8, 1M bits)
INTEL	D27C010	(128Kx8, 1M bits)
MITSHUBISHI	M5M27C101	(128Kx8, 1M bits)
NEC	D27C1001	(128Kx8, 1M bits)
NS	NM27C010	(128Kx8, 1M bits)
SGS-THOMSON	M27C1001	(128Kx8, 1M bits)
TI	TMS27C010	(128Kx8, 1M bits)
TOSHIBA	TCS711000	(128Kx8, 1M bits)
AMD	Am27C020	(256Kx8, 2M bits)
ATMEL	AT27C020	(256Kx8, 2M bits)
FUJITSU	MBM27C2001	(256Kx8, 2M bits)
HITACHI	HN27C201	(256Kx8, 2M bits)
INTEL	D27C020	(256Kx8, 2M bits)
MITSHUBISHI	M5M27C201	(256Kx8, 2M bits)
NEC	D27C2001	(256Kx8, 2M bits)
NS	NM27C020	(256Kx8, 2M bits)

SGS-THOMSON	M27C2001	(256Kx8, 2M bits)
TI	TMS27C020	(256Kx8, 2M bits)
TOSHIBA	TCS712000	(256Kx8, 2M bits)
AMD	Am27C040	(512Kx8, 4M bits)
ATMEL	AT27C040	(512Kx8, 4M bits)
FUJITSU	MBM27C4001	(512Kx8, 4M bits)
HITACHI	HN27C401	(512Kx8, 4M bits)
INTEL	D27C040	(512Kx8, 4M bits)
MITSUBISHI	M5M27C401	(512Kx8, 4M bits)
NEC	D27C4001	(512Kx8, 4M bits)
NS	NM27C040	(512Kx8, 4M bits)
SGS-THOMSON	M27C4001	(512Kx8, 4M bits)
TI	TMS27C040	(512Kx8, 4M bits)
TOSHIBA	TCS714000	(512Kx8, 4M bits)
ATMEL	AT27C080	(1Mx8, 8M bits)

The following list contains 12V FLASHs supported by the AR-B1474:

AMD	Am28F512	(64Kx8, 512K bits)
INTEL	P28F512	(64Kx8, 512K bits)
SGS-THOMSON	M28F512	(64Kx8, 512K bits)
AMD	Am28F010	(128Kx8, 1M bits)
INTEL	P28F010	(128Kx8, 1M bits)
SGS-THOMSON	M28F1001	(128Kx8, 1M bits)
MXIC	MX28F1000	(128Kx8, 1M bits)
AMD	Am28F020	(256Kx8, 2M bits)
INTEL	P28F020	(256Kx8, 2M bits)
SGS-THOMSON	M28F2001	(256Kx8, 2M bits)
MXIC	MX28F2000	(256Kx8, 2M bits)

10.2 INDEX