AR-B1440
INDUSTRIAL GRADE
CPU BOARD
User’ s Guide

Edition: 1.0

Table of Contents

0.PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

April 2000

Acrosser Technology makes no representations or warranties with respect to the contents hereof and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Furthermore, Acrosser Technology reserves the right to revise this publication and to make changes from time to time in the contents hereof without obligation of Acrosser Technology to notify any person of such revisions or changes.

Possession, use, or copying of the software described in this publication is authorized only pursuant to a valid written license from Acrosser or an authorized sublicensor.

This document was produced with Adobe Acrobat 3.01.

0.2 WELCOME TO THE AR-B1440 CPU BOARD

This guide introduces the Acrosser AR-B1440 CPU board.

Use the information describes this card's functions, features, and how to start, set up and operate your AR-B1440. You also could find general system information here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B1440, refer to the Chapter 3, "Setting Up the System" in this guide. Check the packing list, make sure the accessories in the package.

AR-B1440 diskette provides the newest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification and hardware & software information, and adding the description or modification of product function after manual published.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing of your product by following these guidelines:

1. Include your name, address, telephone and facsimile number where you may be reached during the day.
2. A description of the system configuration and/or software at the time is malfunction.
3. A brief description is in the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

Please send your comments to Acrosser Technology Co., Ltd. or your local sales representative.

Internet electronic mail to: **webmaster@acrosser.com**

0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "System Setting", describes how to adjust the jumper, and the connectors setting.
- Chapter 4, "Installation", describes the configuration and installation procedure using LCD display.
- Chapter 5, "BIOS Console", describes setup procedures including information on the utility diskette.
- Chapter 6, "Specifications", providing the BIOS options setting.
- Chapter 7, Placement & Dimensions
- Chapter 8, Chapter 9, Programming RS-485 & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system component, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B1440 is an all-in-one 486 (PC/104) industrial grade CPU module that has been designed to withstand continuous operation in harsh environments. This board can stand alone as a CPU card or be used with other PC/104 compatible cards. The total on-board memory for the AR-B1440 can be configured from 8MB to 64MB by using 144-pin SoDIMM-type EDO DRAM.

The 8 layer PCB CPU card is equipped with an IDE HDD interface, a floppy disk interface , 2 parallel port**s**, **4** serial ports, an Ethernet port, and a watchdog timer. Its dimensions are as compact as 145mm X 102mm. Its highly condensed features make it an ideal cost/performance solution for high-end commercial and industrial applications where CPU speed and mean time between failures is critical.

The AR-B1440 provides 1 bus interface: a PC/104 compatible expansion bus, which can be turned into an ISA bus with the addition of an adapter. Based on the PC/104 expansion bus, you could easily install thousands of PC/104 modules from hundreds of venders around the world. You can also directly connect the power supply to the AR-B1440 on-board power connector in standalone applications.

A watchdog timer, which has a software programmable time-out interval, is also provided on this CPU card. It ensures that the system does not hang up if a program can not execute normally.
The system implements the LAN function onboard, which supports auto-detection of 10 Mbps and 100 Mbps data transfer rates.

Especially the AR-B1440's on-board VGA, offers the most exciting possibilities yet to the industry. The on-board VGA/LCD controller brings about a whole new dimension of industrial computing. No longer do you have to worry about adding an extra card to your system.

1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B1440 board, take a moment to make sure that the following items have been included inside the AR-B1440 package.

- The quick setup manual
- 1 AR-B1440 all-in-one single CPU board
- 1 Hard disk interface cable
- 1 Floppy disk cable
- 2 Parallel port interface cable
- 1 PS/2 mouse adapter
- 4 phone-jack to DB-9 adapter
- 1 Software utility diskette.
- 1 Power cable.

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- Supports ST STPC industrial 66 MHz
- On chip UMA-system VGA (On-board CRT and TFT-LCD panel display 640 x 480 LCD)
- Supports IDE hard disk drives
- Supports floppy disk drives
- Supports 2 bi-directional parallel port
- 100/10-BaseT, shielded RJ-45 edge connector
- PC/AT compatible keyboard
- Programmable watchdog timer
- AMI Flash BIOS
- Multi-layer PCB for noise reduction
- 4 COM ports: 1 of 4 is switchable to RS-485/RS-232
  1 of 4 is switchable to Power Mode/RS-232
  1 of 4 supports IrDA compatible transmissions
- Dimensions : 145mmX102mm

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1440 CPU board. The following topics are covered:

- Single PC Chipset
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port
- LAN Controller

2.1 SINGLE PC CHIPSET

The single PC Chipset integrates a fully static X86 processor, which is fully compatible with X86 processors and is combined with a powerful chipset, graphics and video pipelines to provide a PC compatible subsystem on a single device. The performance of the device is comparable with the performance of a typical P5 generation system. This device is packaged in a 388 Ball Grid Array (PBGA). At the heart of the Single PC Chipset is an advanced 64-bit processor block, dubbed the 5ST86. The 5ST86 includes a powerful X86 processor core along with a 64-bit DRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI local-bus controller and industry standard PC chipset functions (Interrupt Controller, DMA Controller, Interval Timer and ISA bus) and an EIDE Controller.

The single PC Chipset makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and a graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system. System performance is also generally improved, due to the higher memory bandwidth allowed by attaching the graphics engine directly to 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus. Graphics functions are controlled through the on chip graphics engine and the monitor display is produced through the 2D graphics display engine. The graphics resolution supported is a maximum of 1280X1024 at a 75Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate the above display resolution. The frame buffer can occupy a space anywhere in the first four Mbytes of physical main memory.

The 64-bit wide memory array provides the system with 200Mb/s bandwidth, double that of an equivalent 32-bit system. This allows for higher resolution screens and greater color depth.
The standard PC chipset functions (DMA, Interrupt controller, timers, power management logic) are integrated together with the X86 processor core. Additional functions are accessed by the single PC Chipset via the ISA bus. An EIDE port is provided for storage devices such as hard disks and CD-ROMs, bridging directly to the PCI bus.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B1440 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

Following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send and receive routines.

2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1440 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

Interrupt Level	Description
NMI	Parity check
CTRL1	CTRL2
IRQ 0	System timer interrupt from timer 8254
IRQ 1	Keyboard output buffer full
IRQ 2	Rerouting to IRQ8 to IRQ15
	IRQ8 : Real time clock
	IRQ9 : Serial port 4
	IRQ10 : LAN adapter
	IRQ11 : Serial port 3
	IRQ12 : Reserved for PS/2 mouse
	IRQ13 : Math. coprocessor
	IRQ14 : Hard disk adapter
	IRQ15 : Reserved for Serial port 5
IRQ 3	Serial port 2
IRQ 4	Serial port 1
IRQ 5	Parallel port 2
IRQ 6	Floppy disk adapter
IRQ 7	Parallel port 1

Figure 2-1 Interrupt Controller

2.4.1 I/O Port Address Map

Hex Range	Device
000-00F	DMA controller 1
020-021	Interrupt controller 1
040-043	Timer 1
060-060	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-090	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
1F0-1F7	Fixed disk Controller
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
378-37F	Parallel printer port 1 (LPT 1)
3B0-3BB	STPC Industrial
3C0-3DF	STPC Industrial
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)
FE00-FEFF	LAN adapter

Table 2-2 I/O Port Address Map

2.4.2 Real-Time Clock and Non-Volatile RAM

The AR-B1440 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved

Address	Description
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-3 Real-Time Clock & Non-Volatile RAM

2.4.3 Timer

The AR-B1440 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required handle the communications link.

The following table is summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-4 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-5 Serial Port Divisor Latch

2.6 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-6 Registers' Address

(2) Printer Interface Logic

The parallel port of the NSPC87309 is for attaching various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

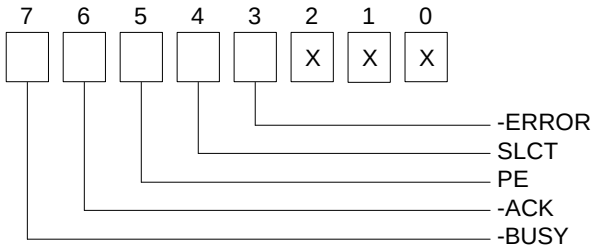


Figure 2-2 Printer Status Buffer

NOTE: X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

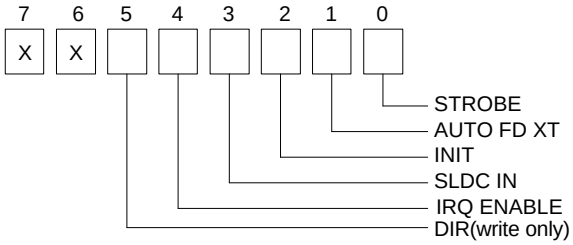


Figure 2-3 Bit's Definition

NOTE: X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3.SYSTEM SETTING

This chapter describes pin assignments for system's external connectors and the jumpers setting.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B1440 is all-in-one ST STPC industrial 66 CPU board. This section provides hardware's jumpers setting, the connectors' locations, and the pin assignment.

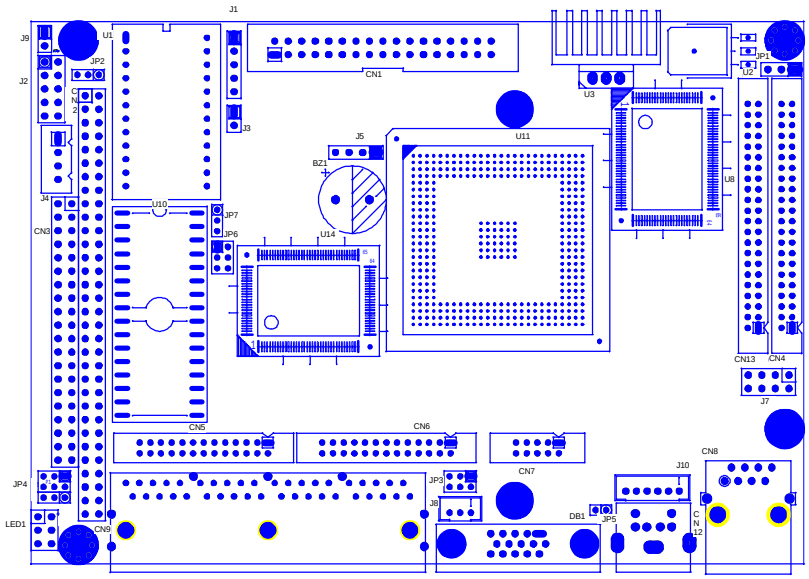


Figure 3-1 External System Location

3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1440 jumper pins, and the factory-default setting.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.2.1 Keyboard Connector

(1) 6-Pin Mini DIN Keyboard Connector (CN12)

CN12 is a Mini-DIN 6-pin connector. This keyboard connector is PS/2 type keyboard connector. This connector is also for a standard IBM-compatible keyboard that used the keyboard adapter cable.

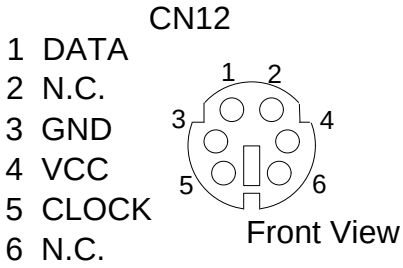


Figure 3-2 CN12: 6-Pin Mini Din Keyboard Connector

3.2.2 PS/2 Mouse Connector (J10)

To use the PS/2, an adapter cable has to be connected to the J10 (6-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1440 package. The connector for the PS/2 mouse is a Mini-DIN 6-pin connector. Pin assignments for the PS/2 port connector are as follows:

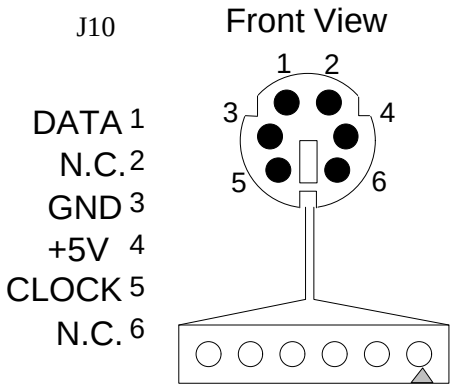


Figure 3-3 J10: PS/2 Mouse Connector

3.2.3 Hard Disk (IDE) Connector (CN4)

A 44-pin header type connector (CN4) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use the BIOS Setup program to select. The following table illustrates the pin assignments of the hard disk drive's 44-pin connector.

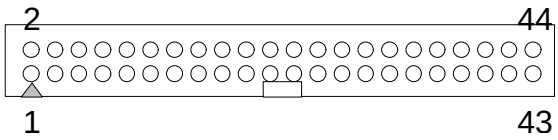


Figure 3-4 CN4 Hard Disk (IDE) Connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	Not Used
21	Not Used	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	CHRDY A	28	DALE
29	Not Used	30	GROUND
31	-IRQ 14	32	-IO16
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41	VCC	42	VCC
43	GROUND	44	Not Used

Table 3-7 CN4: Hard Disk (IDE) Connector

3.2.4 FDD Port Connector (CN1)

The AR-B1440 provides a 34-pin header type connector for supporting up to two floppy disk drives.

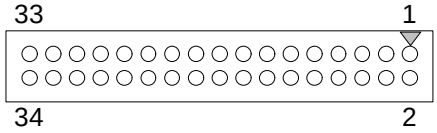


Figure 3-5 CN1: FDD Port Connector

Pin	Signal	Pin	Signal
1-33 (odd)	GROUND	18	-DIRECTION
2	DRVEN 0	20	-STEP OUTPUT PULSE
4	NOT USED	22	-WRITE DATA
6	DRVEN 1	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE 0	28	-WRITE PROTECT
12	-DRIVE SELECT 1	30	-READ DATA
14	-DRIVE SELECT 0	32	-SIDE 1 SELECT
16	-MOTOR ENABLE 1	34	-DISK CHANGE

Table 3-8 CN1: FDD Port Connector

3.2.5 Parallel Port Connector (CN5&CN6)(LPT1&LPT2)

To use the parallel port, an adapter cable has connected to the CN5&6 (26-pin header type) connector. This adapter cable is mounted on two bracket and is included in your AR-B1440 package. The connector for the parallel port is a 25 pin D-type female connector.

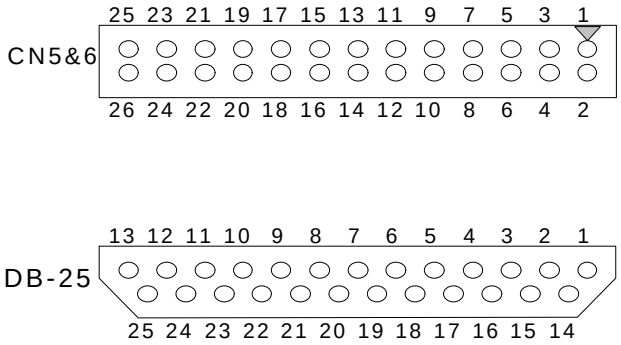


Figure 3-6 CN5&6: Parallel Port Connector

CN5&6	DB-25	Signal	CN5&6	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	- Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	No Used

Table 3-9 Parallel Port Pin Assignment

3.2.6 Serial Port

(1) Full RS-232 Signal / Power Select for COM-B (JP3)

JP3 select the full RS-232 signal or power select for COM-B, if the user chooses the power supported then the COM-B's RTS will be instead of the +12VDC signal; and the COM B's CTS will be instead of the +5VDC signal.

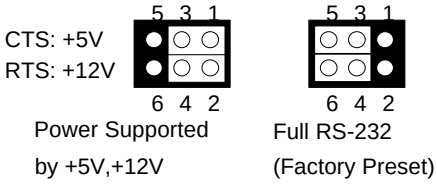


Figure 3-7 JP3: Full RS-232 Signal / Power Select for COM-B

(2) RS-232/RS-485 Select for COM-D (JP4)

JP4 select the on-board RS-232/RS-485 for COM D

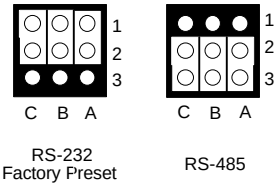


Figure 3-8 JP4: RS-232/RS-485 Select for COM-D

(3) RS-485 Terminator Select (JP5)

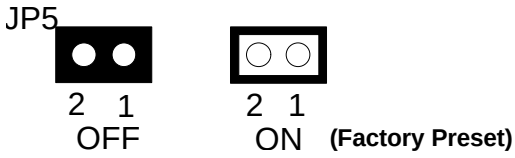
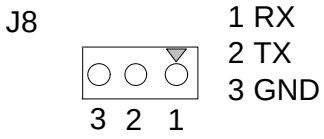


Figure 3-9 JP5: RS-485 Terminator Select

(4) Touch Screen Connector COM-C (J8)



(5) RS-232C Connector (CN9)

There are four serial ports with EIA RS-232C interface on the AR-B1440. COM A, COM B and COM C use three on-board serial port Phone-Jack 10-pin female connector (CN9) which is located at the right top side of the card. To configure these four serial ports, use the BIOS Setup program to do well, and COM D can be adjust the jumpers on JP4 for choice RS-485 or RS-232C.

The pin assignments of the CN9 for serial port A, B, C & D are as follows:

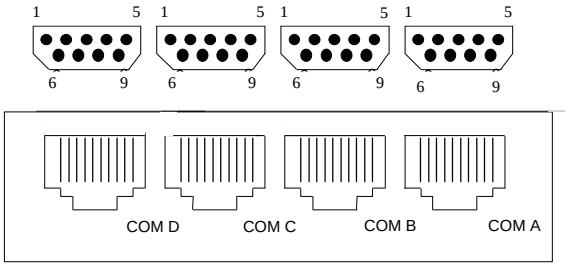


Figure 3-10 CN9: RS-232C Connector

CN9-A	DB-9	Signal	CN9-A	DB-9	Signal
1	1	-DCD	2	8	-CTS
3	7	-RTS	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	- DTR	8	5	GND
9	5	GND	10	9	-RI

Table 3-10 Serial Port RS-232 COM A Pin Assignment

CN9-B	DB-9	Signal	CN9-B	DB-9	Signal
1	1	-DCD	2	8	-CTS/ +5V
3	7	-RTS/+12V	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	-DTR	8	5	GND
9	5	GND	10	9	-RI

Table 3-11 Serial Port RS-232 COM B Pin Assignment

CN9-C	DB-9	Signal	CN9-C	DB-9	Signal
1	1	-DCD	2	8	-CTS
3	7	-RTS	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	- DTR	8	5	GND
9	5	GND	10	9	-RI

Table 3-12 Serial Port RS-232 COM B Pin Assignment

CN9-D	DB-9	Signal	CN9-D	DB-9	Signal
1	1	-DCD	2	8	-CTS
3	7	-RTS / 485N+	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	-DTR / 485N-	8	5	GND
9	5	GND	10	9	-RI

Table 3-13 Serial Port RS-232/RS-485 COM D Pin Assignment

(8) IrDA Header (J1)

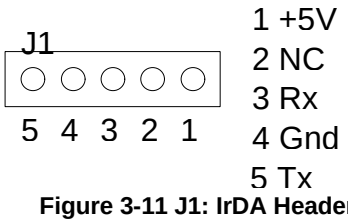


Figure 3-11 J1: IrDA Header

3.2.7 Network Setting

(2) Ethernet RJ-45 Connector (CN8)

The CN8 connects with RJ-45 header, it' s the standard network header. The following table is CN8 pin assignment.

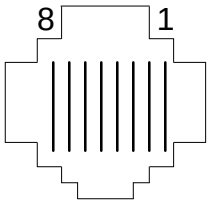


Figure 3-12 CN8: RJ-45 Connector

PIN (CN8)	FUNCTION
1	TPTX+
2	TPTX -
3	TPRX+
4	Not Used
5	Not Used
6	TPRX -
7	Not Used
8	Not Used

Table 3-14 RJ-45 Pin Assignment

3.2.8 Reset Header (J3)

J3 is used to connect to an external reset switch. Shorting these two pins will reset the system.

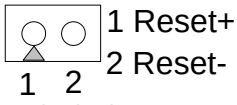


Figure 3-13 J3: Reset Header

3.2.9 External Speaker Header (J5)

Besides the on-board buzzer, you can use an external speaker by connecting J5 header directly.

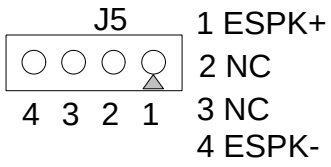


Figure 3-14 J5: External Speaker Header

3.2.10 Power Connector (J4)

J4 is a 4-pin power connector. Using the J4, you can connect the power supply to the on board power connector for stand alone applications directly.

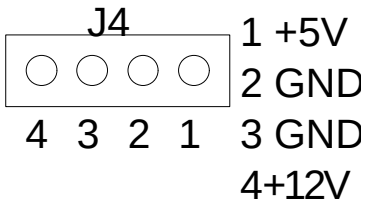


Figure 3-15 J4: 4-Pin Power Connector

This chapter describes the configuration and installation procedure using LCD and CRT display.

- LCD Flat Panel Display
- CRT & LCD Display

3.3 LCD FLAT PANEL DISPLAY

Using the Flash Memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default setting for different types of LCD panel. And then set your system properly and configure the AR-B1440 VGA module for the right type of LCD panel you are using.

The sample LCD models listed on the table are just some of the LCD panel models. If you are using a different LCD panel other than those listed, choose from the panel description column which type of LCD panel you are using.

The following shows the block diagram of using AR-B1440 for LCD display.

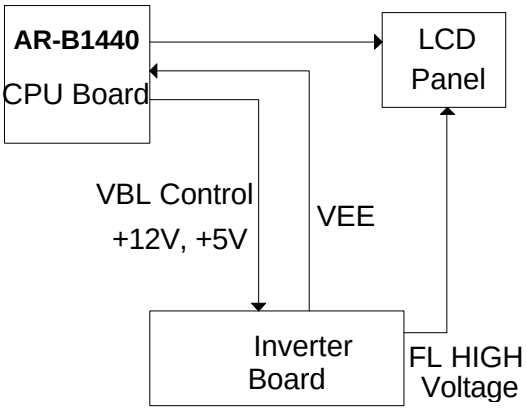


Figure 3-1 LCD Panel Block Diagram

The block diagram shows that AR-B1440 still needs components to be used for LCD panel. The inverter board provides the control for the brightness and the contrast of the LCD panel while the inverter is the one that supplies the high voltage to drive the LCD panel. Each item will be explained further in the section.

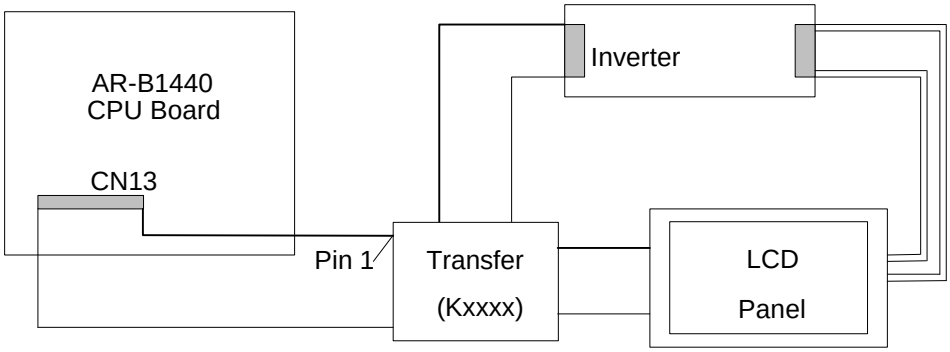


Figure 3-2 LCD Panel Cable Installation Diagram

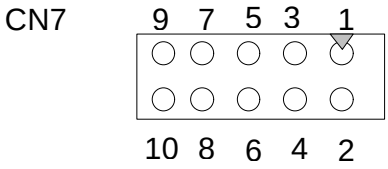
NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable is usually with different color.

3.4 CRT & LCD DISPLAY

The AR-B1440 supports CRT colored monitor, and TFT panel. It can be connected to create a compact video solution for the industrial environment. The CRT and LCD resolution of 640X480 is for standard, your monitor must possess certain characteristics to display the mode you want.

3.4.1 CRT Connector (DB1)

CN7&DB1 is used to connect with a VGA monitor when you are using the on-board VGA controller as display adapter. Pin assignments for the DB1 connector is as follows:



1:RED	2:VCGD
3:GREEN	4:GND
5:BLUE	6:Analog GND
7:HS	8:DDC DAT
9:VS	10:DDC CLK

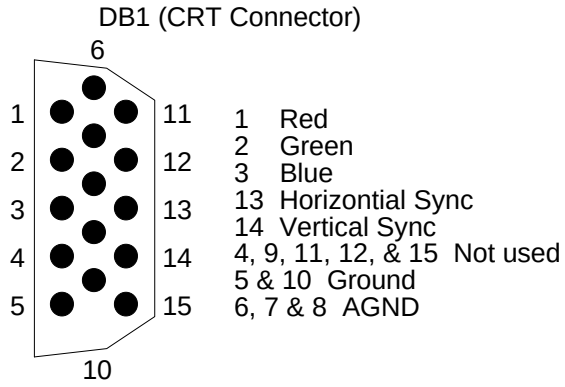


Figure 3-3 DB1: CRT Connector

3.4.2 LCD Panel Display Connector (CN13)

Attach a display panel connector to this 44-pin connector with pin assignments as shown below:

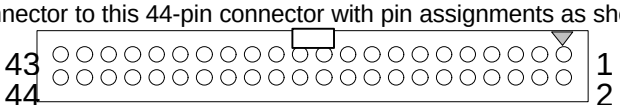
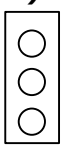


Figure 3-4 CN13: LCD Display Connector

Pin	Signal	Pin	Signal
1	GND	2	SHFCLK
3	GND	4	LP
5	FLM	6	GND
7	P0	8	P1
9	P2	10	P3
11	P4	12	P5
13	GND	14	P6
15	P7	16	P8
17	P9	18	P10
19	P11	20	GND
21	P12	22	P13
23	P14	24	P15
25	P16	26	P17
27	GND	28	P18
29	P19	30	P20
31	P21	32	P22
33	P23	34	GND
35	VCC	36	VCC
37	+12V	38	+12V
39	GND	40	GND
41	DE	42	ENABLK
43	GND	44	Not Used

Table 3-12 LCD Display Assignment

3.4.3 LED(LED1)



When LED Power on, the red light is on. Enable the Watchdog, the red light is flashing. When access is HDD, the green light is On. When access is LAN, the yellow light is On.

3.4.4 D.O.C. Memory Address Select

This section provides the information about how to use the D.O.C. (DiskOnChip). There divided two parts: hardware setting and software configuration.

1: Use JP6 to select D.O.C.

2: Use JP2 to select the correct D.O.C. memory address.

3: Insert programmed DiskOnChip into socket U10 setting as DOC.

3.4.5 SRAM Memory Address Select

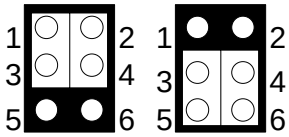
1: Use JP6 to select SRAM.

2: Use JP2 to select the correct SRAM memory address.

3: Use JP7 to select SRAM size.

4: Insert SRAM into socket U10 setting as SRAM.

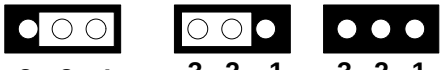
D.O.C/SRAM SELECT(JP6)



SRAM: 1-3&2-4

D.O.C: 3-5&4-6 (Factory preset)

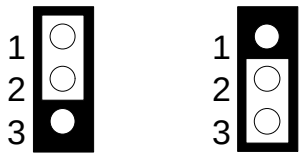
D.O.C./SRAM ADDRESS SELECT(JP2)



C800H **D000H** **D800H**

1-2:C800H (Factory Preset)
2-3:D000H
1-2-3 Open: D800H

3.5 SRAM SIZE SELECT(JP7)



1M 4M

1-2:1M

2-3:4M (Factory Preset)

4. INSTALLATION

This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Utility Diskette
- Watchdog Timer

4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1440 CPU board. Please read the details of the CPU board's hardware descriptions before installation carefully, especially jumpers' setting, switch settings and cable connections.

Follow steps listed below for proper installation:

Step 1 : Read the CPU board's hardware description in this manual.

Step 2 : Set jumpers.

Step 3 : Make sure that the power supply connected to your passive CPU board is turned off.

Step 4 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

Step 5 : Connect the hard disk/floppy disk flat cables from the CPU board to the drives. Connect a power source to each drive.

Step 6 : Plug the keyboard into the keyboard connector.

Step 7 : Turn on the power.

Step 8: Configure your system with the BIOS Setup program then re-boot your system.

Step 9: If the CPU board does not work, turn off the power and read the hardware description carefully again.

Step 10: If the CPU board still does not perform properly, return the board to your dealer for immediate service.

4.2 UTILITY DISKETTE

The AR-B1440 provides one utility diskette.

4.2.1 VGA Driver

WIN 95 Driver

For the WIN95 operating system, the user must decompress the compressed files in DOS mode. And then follow these steps:

Step 1: Create a new directory for the VGA drivers.

```
C:\>MD VGAWIN95
```

Step 2: Insert the diskette. Change the working directory to the newly created directory, and extract the compressed file.

```
C:\>CD VGAWIN95
C:\VGAWIN95>A:\VGAWIN95.EXE
```

Step 3: Enter the WIN95 operating system. Please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.

```
C:\VGAWIN95
```

Step 4: And then you can find the <SGS-THOMSON STPC> item, select it and click the <OK> button.

Step 5: Finally, you can find the <DISPLAY> icon and then the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size> ..and other functions. Please refer to the messages during installation.

4.2.2 Network Utility

There are two auto-extract files for network utility. User must extract the files in DOS mode.

1. Autoextract the <ALL8139.EXE> file that includes the network drivers for various operating systems.

2. RSET8139.EXE diagnostic and modification program

4.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The AR-B1440 are equipped with a programmable time-out period watchdog timer User can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang, it will generate a reset signal to reset the system. The time-out period can be programmed to be 3 to 42 seconds.

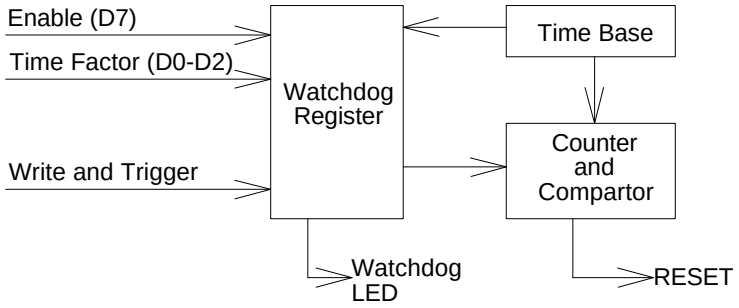


Figure 4-1 Watchdog Block Diagram

4.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog is times out.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out period.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 4-1 Time-Out Setting

If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table lists the relation of timer factors and time-out period. And if you use the IRQ15 signal to warn your program when the watchdog times out, enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> items must set to ***Primary***.

Time Factor	Time-Out Period (Seconds)
0C0H	3
0C1H	6
0C2H	12
0C3H	18
0C4H	24
0C5H	30
0C6H	36
0C7H	42

Table 4-2 Time-Out Setting

NOTE: 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.

2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

4.3.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 76H or Base Port+4. The following is a BASICA program which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000        REM Points to command register
1010              WD_REG% = 76H
1020        REM Timer factor = 84H (or 0C4H)
1030              TIMER_FACTOR% = %H84
1040        REM Output factor to watchdog register
1050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

4.3.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010              WD_REG% = 76H
2020        REM Timer factor = 84H (or 0C4H)
2030              TIMER_FACTOR% = &H84
2040        REM Output factor to watchdog register
2050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

4.3.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010              WD_REG% = BASE_PORT% + 4
3020        REM Timer factor = 0
3030              TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050              OUT WD_REG%, TIMER_FACTOR%
      ., etc.
```

5. BIOS CONSOLE

This chapter describes the AR-B1440 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power management
- Peripheral Setup
- Auto-Detect Hard Disks
- Change User Password
- Change Supervisor Password
- Auto Configuration with Optimal Settings
- Auto Configuration with Fail Safe settings
- Save Settings and Exit
- Exit Without Saving

5.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drives, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer is turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure(choose) the option and configure the functions.

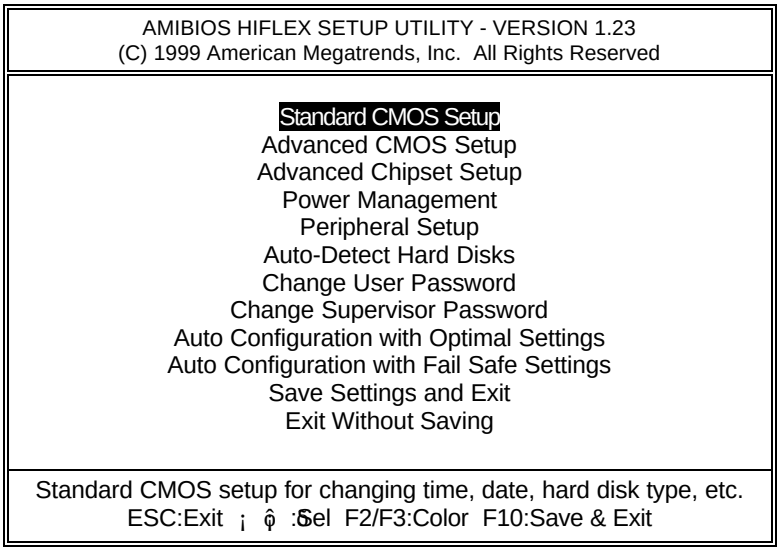


Figure 5-1 BIOS: Setup Main Menu

➥ **NOTE:**

(1) The AR-B1440 BIOS factory-default setting is set to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default settings, unless you are very familiar with the settings' functions, or you can contact a technical support engineer at Acrosser.

(2) If the BIOS losses the setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option has best-case values that should optimize system performance.

(3) The BIOS settings are described in detail in this section.

5.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

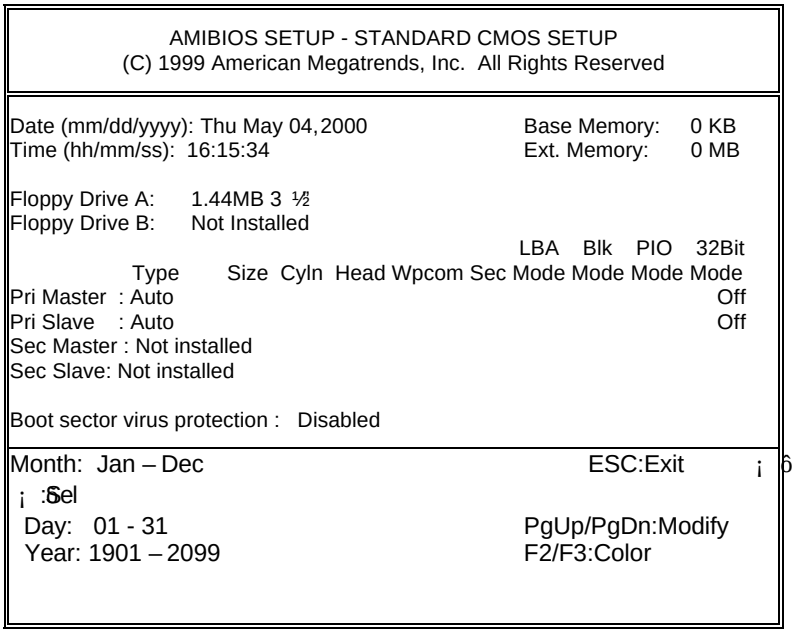


Figure 5-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the same process for the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types of USER settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk's jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any

allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is < . This setting is recommended because it can conflict with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

5.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board¡ s' design to remain in their default settings. It is suggested that you leave the settings on their factory defaults unless you are well versed in BIOS features.

AMIBIOS SETUP - ADVANCED CMOS SETUP
(C) 1999 American Megatrends, Inc. All Rights Reserved

Quick Boot	Enabled
1st Boot Device	IDE-0
2nd Boot Device	Floppy
3rd Boot Device	CD-ROM
4th Boot Device	Disabled
Try Other Boot Devices	Yes
Floppy Access Control	Read-Write
Hard Disk Access Control	Read-Write
BootUp Num-Lock	On
Floppy Drive Swap	Disabled
Floppy Drive Seek	Disabled
PS/2 Mouse Support	Enabled
Typematic Rate	Fast
System Keyboard	Absent
Primary Display	Absent
Password Check	Setup
Boot to OS/2	No
Wait For 'F1' If Error	Disabled
Hit 'DEL' Message Display	Enabled
Internal Cache	Writeback
C000, 16k Shadow	Enabled
C400, 16k Shadow	Enabled
C800, 16k Shadow	Disabled
CC00, 16k Shadow	Disabled
D000, 16k Shadow	Disabled
D400, 16k Shadow	Disabled
D800, 16k Shadow	Disabled
DC00, 16k Shadow	Disabled

Available Options :
Disabled
Enabled

ESC:Exit
PgUp/PgDn:Modify
F2/F3:Color
F1:Help

Figure 5-3 BIOS: Advanced CMOS Setup

Quick Boot

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to ***Enabled***, BIOS will shorten or skip some check items during POST.

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device
Try Other Boot Devices

These options determine which device the system searches first for an operating system during boot-up. When "Try Other Boot Devices" is set to "Yes," the system will search this device first than the above other devices.

Floppy Access Control

This option specifies the floppy access to be "read/write" (normal) or "read only."

Hard Disk Access Control

This option specifies the hard disk access to be "read/write" (normal) or "read only."

BootUp Num-Lock

This item is used to activate the Num-Lock function upon system bootup. If the setting is on, after a boot, the Num-Lock light is lit, and user can use the number key.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon bootup.

PS/2 Mouse Support

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

System Keyboard

This function specifies that a keyboard is attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Boot to OS/2

When using the OS/2 operating system with installed DRAM of greater than 64MB, you need to ***Enabled*** this option otherwise leave this on the setup default of ***Disabled***.

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 5-1 Internal Cache Setting

System BIOS Cacheable

When this option is set to ***Enabled***, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are ***Enabled*** or ***Disabled***. The Optimal default setting is ***Enabled***. The Fail-Safe default setting is ***Disabled***.

C000, 16k Shadow
C400, 16k Shadow
C800, 16k Shadow
CC00, 16k Shadow
D000, 16k Shadow
D400, 16k Shadow
D800, 16k Shadow
DC00, 16k Shadow

These options control the location of the contents of the 16KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 5-2 Shadow Setting

5.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

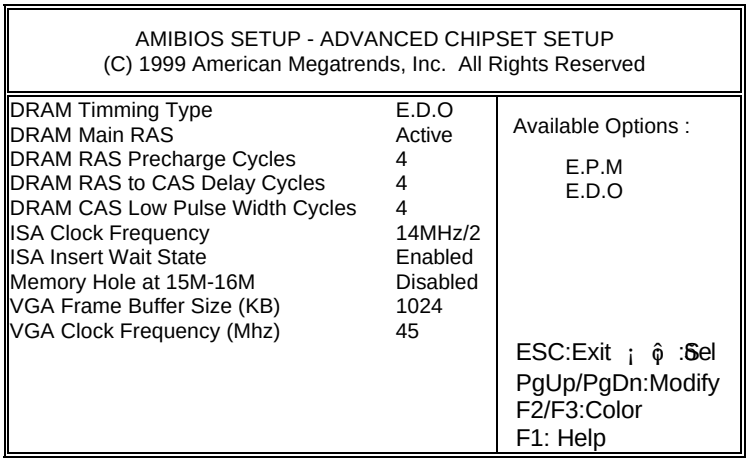


Figure 5-4 BIOS: Advanced Chipset Setup

Memory Type

There is 1 memory types: E.D.O. Specify the type used in the system.

Main RAS Active

The option controls if RAS is kept active after the current DRAM access.

RAS Precharge Time

This controls the idle clocks after issuing a precharge command to DRAM.

RAS to CAS Delay

This controls the latency between DRAM active command and the read/write command.

CAS Low Pulse Width

The 4 items are related to system memory internal operation. It is recommended to use the default settings.).

GCLKx2

This option is used to select the VGA bus clock rate.

ISACLK

This option is used to select the system ISA clock rate

Memory Hole at 15-16M

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

PCI to host read precharge

This option controls if all burst reads from a PCI master addressed to the East Bridge system memory will use the prefetch function.

PCI to host posting

This option controls if the memory writes from a PCI master addressed to the East Bridge system memory can be posted.

VGA Frame Buffer Size:

This option sets the VGA's occupied memory.

Note: If users have to use 800*600 resolution, please adjust the item " VGA Frame Buffer Size" under "Advanced Chipset setup" to 2MB.

5.5 POWER MANAGEMENT

This section is used to configure power management features. This <Power management Setup> option allows you to reduce power consumption. This feature turns off the video display and shuts down the hard disk after a period of inactivity.

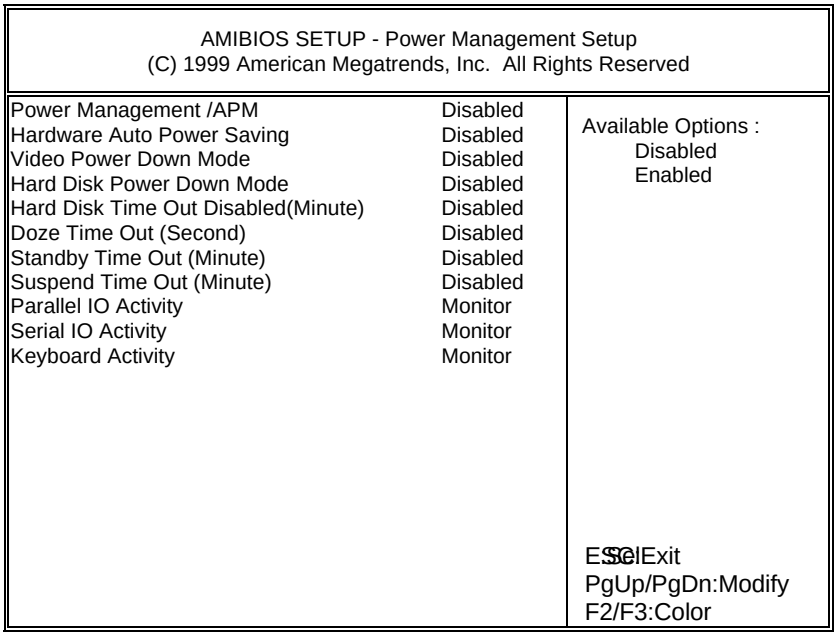


Figure 5-5 BIOS: Power Management Setup

Power Management /APM

This option is to enable the power management and APM (Advanced Power Management) features.

Video Power Down Mode

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity has expired.

Hard Disk Power Down Mode

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity has expired.

Hard Disk Time Out

This option specifies the length of a period of hard disk inactivity. When this period expired, the hard disk drive enters the power-conserving mode specified on the <Hard Disk Power Down Mode> option.

Doze Time Out
Standby Time Out
Suspend Time Out

The 3 options are all related to the system power-saving mode during system inactivity. Normally, if the 3 options are set to "Enabled," the sequence of the power-saving mode is Doze Mode Standby Mode, Suspend Mode. In Suspend mode, nearly all power used is curtailed.

BIOS Setup			Power Saving Mode
Doze Time out	**Standby Time out**	**Suspend Time out**	
Enabled	Enabled	Enabled	Doze Standby Suspend
Disabled	Disabled	Disabled	The system will not enter power saving mode.
Any of the options is set to **"Disabled"** with the other 2 **"Enabled."**			The system will sequentially enter the 2 modes set to "Enabled." Remember Doze mode is always the first mode system will enter and Suspend mode is the last.
Any of the options is set to **"Enabled"** with the other 2 **"Disabled."**			The system will only enter the mode that is set to "Enabled."

Table 5-3 Power Saving Mode

Full-On Clock Throttle Ratio

This option increases the system stability when power on. The system clock frequency may be divided when received into the chipset during bootup. .After the system enters the operation system, the frequency division in chipset will not exist and return to normal state.

Power –Down Clock Throttle Ratio

This option is related to the power saving state: Doze/ Standby/ Suspend modes. When the system is in one of these modes, the system clock will reduce the frequency for power saving.

STPCLK# Modulation Period

STPCLK is the system clock. When the option is set to "Enabled," the STPCLK modulation period is 64ms else. If "Disabled," the period is 64us.

Display Activity

This option controls the activity of display device.

DMA Activity

This option controls the activity of DMA device.

PCI Master Activity

This option controls the activity of PCI Master device.

Parallel IO Activity

When the system is in sleep mode, it can be re-started through a printer port device.

Serial IO Activity

When the system is in sleep mode, it is awakened whenever there is an action from COM port-based device.

Keyboard Activity

When the system is in sleep mode, it is awakened whenever there is an action from hard disk through keyboard device.

Floppy Disk Activity

This option controls the activity of floppy disk device.

Hard Disk Activity

This option controls the activity of hard disk device..

IRQ1-15
When the system is in sleep mode, it is awakened whenever there is an action from IRQ1-IRQ15.

System Timer Interrupt
This option controls the activity of system timer interrupt.

NMI Interrupt
This option controls the activity of the signal "NMI" emitted by CPU during power-on

5.6 PERIPHERAL SETUP

This section is used to configure peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP
(C) 1999 American Megatrends, Inc. All Rights Reserved

OnBoard IDE	Enabled	Available Options :
OnBoard FDC	Enabled	Disabled
OnBoard Serial Port	3F8h/COM1	Enabled
Serial Port1 IRQ	4	
OnBoard Serial Port2	2F8h/COM2	
Serial Port2 IRQ	3	
OnBoard Parallel Port1	378h	
Parallel Port1 Mode	Normal	
EPP Version	N/A	
Parallel Port1 IRQ	7	
Parallel Port1 DMA Channel	N/A	
OnBoard Serial Port3	3E8h/COM3	ESC:Exit ¡ ĝ :Sel
Serial Port3 IRQ	11	PgUp/PgDn:Modify
OnBoard Serial Port4	2E8h/COM4	F2/F3:Color
Serial Port4 IRQ	9	
IR Port Support	Auto	
IR Mode Select	IrDA	
IR IRQ Select	Auto	
IR DMA Select	N/A	
OnBoard Parallel Port2	278h	
Parallel Port2 Mode	Normal	
EPP Version	N/A	
Parallel Port2 IRQ	5	
Parallel Port2 DMA Channel	N/A	

Figure 5-7 BIOS: Peripheral Setup

Watch Dog Timer Output Control

This item controls Watch Dog Timer Output.

OnBoard VGA

This option is to enable the onboard VGA function.

Frame Buffer

This option specifies if the onboard VGA will share the system memory.

Frame Buffer Size

This option is to select the size of VGA memory shared from the system.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE1284 specifications.

OnBoard PCI IDE

This option specifies the onboard IDE controller channels that will be used.

5.7 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

5.8 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. The user can set either a Supervisor password or a User password.

5.8.1 Setting The Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after the BIOS is completed. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

5.8.2 Checking The Password

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. The user can enter a password by typing it on the keyboard. You should select Supervisor or User. The BIOS prompts for a password, the user must set the Supervisor password before the user can set the User password. Enter 1-6 characters as a password. The password does not appear on the screen when typed. Make sure you write it down.

5.9 LOAD DEFAULT SETTINGS

This section permits the user to select a group of settings for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

5.9.1 Auto Configuration With Optimal Settings

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

5.9.2 Auto Configuration With Fail Safe Settings

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

5.10 BIOS EXIT

This section is used to exit the BIOS main menu in two types of situation. After making your changes, you can either save them or exit the BIOS menu without saving the new values.

5.10.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

5.10.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

5.11 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1440 BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The AR-B1440 provides a FLASH BIOS update function for you to easily upgrade to a newer BIOS version. Please follow the operating steps for updating to a new BIOS:

Step 1: Insert the FLASH BIOS diskette into the floppy disk drive.
Step 2: If all steps are followed correctly, the system will reboot. But if the system did not boot up, please check everything and try again. If it still does not work, please contact your Acrosser distributor for technology support at once.

NOTE:

(1). The BIOS Flash disk is not a standard accessory. It can be used to add some functions. If it is necessary to use as an update in the future, you can download the suitable BIOS. The address is as follows:

http:\\www.acrosser.com

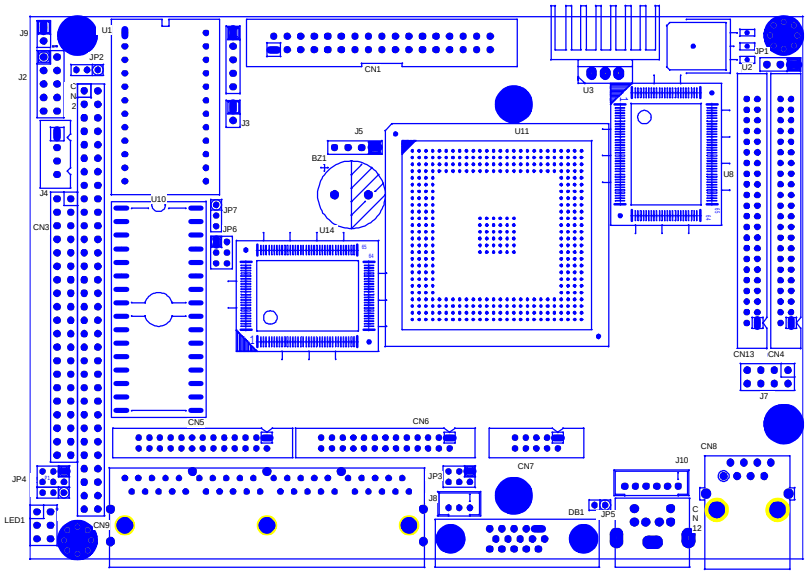
6.SPECIFICATIONS

AR-B1440--- 3.5" Disk Size All-In- One 486 CPU Board w/LAN/VGA/LCD/DOC.

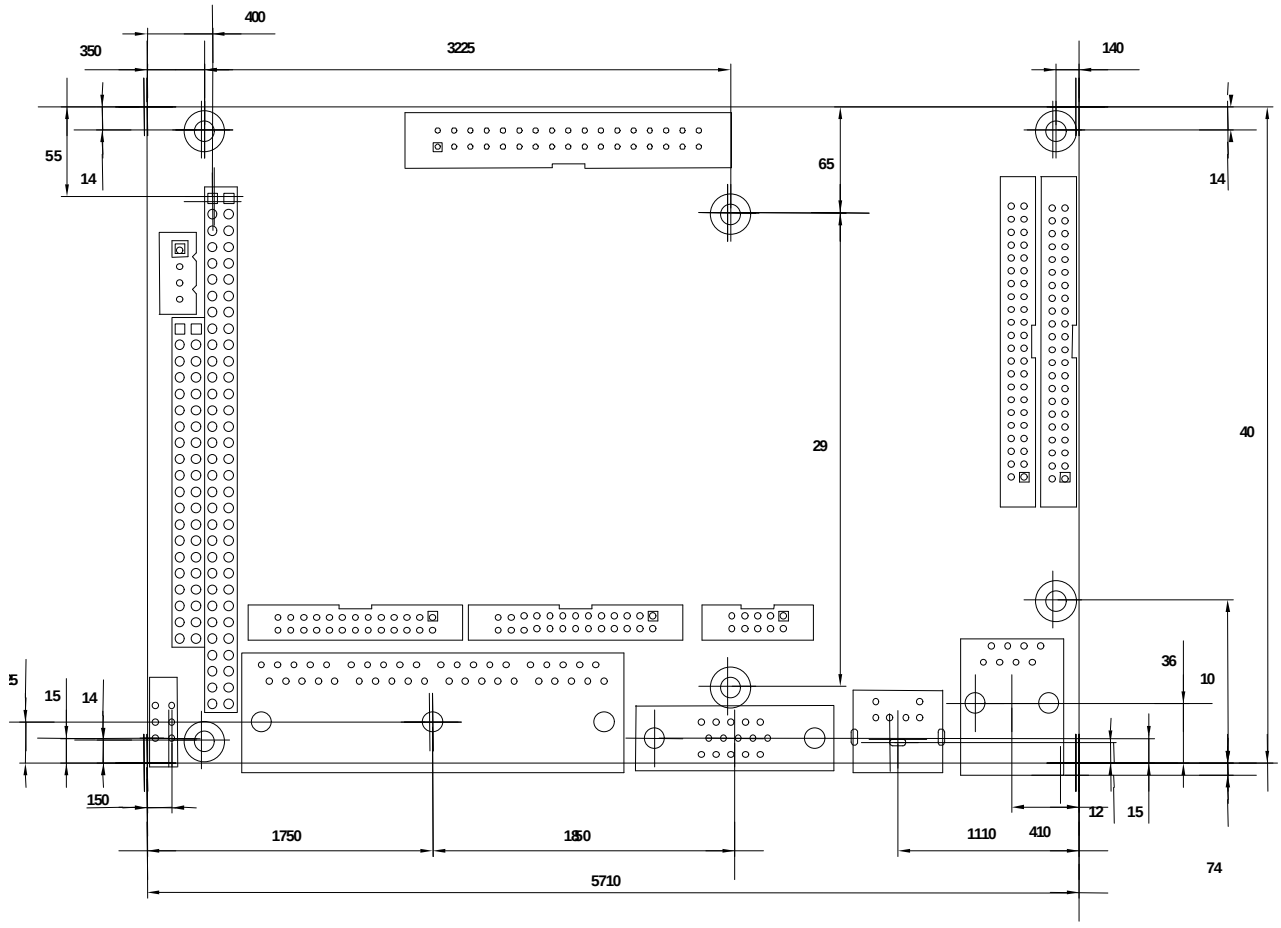
CPU & Chipset:	ST STPC industrial 66 MHz
Bus Interface:	Non-stack through PC/104 bus.
DRAM:	One 144-pin SoDIMM for 8MB to 64MB EDO RAM.
Ethernet:	Supports 100M/10M LAN with RJ-45 connector(100Base-T and 10Base-T).
VGA/LCD Display:	Built in STPC industrial chipset with 1MB to 4MB shared memory. CRT-with 15-pin HDB 15 connector. LCD- with 44-pin 2.0mm connector.
IDE Interface:	Supports one IDE with 44-pin 2.0mm connector supports up to 2 IDE drivers.
Floppy interface:	Supports 1 floppy drive with 34-pin 2.54mm connector.
Serial Port:	Supports 4 serial ports COM1-RS-232C COM2-RS-232C with +5V/+12V power output with 2*3 jumper. COM3-RS-232C or touch screen (3-pin 2.0mm JST connector). COM4-RS-232C or RS-485/ IrDA(5 pin header). All RS-232C/RS485 ports use PJ10P10C*4 connector.
Parallel Port:	Supports 2 SPP/EPP/ECP mode printer ports with 26-pin 2.0mm connectors.
Keyboard:	PS/2 compatible with 6-pin mini –DIN connector.
Mouse:	PS/2 compatible with 6-pin 2.0mm JST Connector.
Real Time Clock:	BQ3287MT or compatible chips
System BIOS:	AMI FLASH BIOS (including VGA/LCD BIOS).
Watchdog:	Programmable watchdog timer
Flash Disk:	Provides 1 socket for 2MB –144MB DiskOnChip. SMD DiskOnChip also available.
Speaker:	On-board buzzer and 4-pin header for external speaker.
PMM Function:	Supports clock decrease power management function.
TTL I/O:	4 TTL inputs and 4 TTL outputs with 10-pin header.
LED Indicator:	On-board power/watchdog, hard disk and LAN LEDs, also provides headers for external LEDs.
Power Connector:	One 4-pin(2.5mm) and one 8-pin (2.5mm) power connector
Other Headers:	2-pin reset. 2*4 –pin for power/watchdog, hard disk , LAN active and LAN speed LED.
Other Jumpers:	1*3-pin DiskOnChip memory mapping select.(C800h,D000h,D800h) 1*3-pin RS-485 terminator ON/OFF select, OFF for standard. 3*3-pin RS-232C/RS-485 select, RS-232C for standard.
CE Design–in:	PC/104-6TTL level loads maximum. (8 mil trace,6 mil trace minimum). Add EMI components to COM ports, Parallel port, CRT, Keyboard, and PS/2 mouse.
Power Req.:	+5V , 2.0A and 12V, 0.5A, typical
PC Board:	8 layers.
Dimensions:	3.5" disk size, 145mm * 102mm(5.71"X4.02")

7. PLACEMENT & DIMENSIONS

7.1 PLACEMENT



7.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

8. PROGRAMMING RS-485 & INDEX

8.1 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 proceeds the transmission which needs control the TXC signal, and the installing steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: Please refer to the section of the "Serial Port" in the chapter "System Control" for the detail description of the COM port's register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the AR-B1440 CPU card's DTR signal to the RS-485 ¡ 3TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

(4) Receive data

The RS-485's operation of receiving data is in the same of the RS-232's.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10      OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20      REM Reset DTR
30      OUT &H2EC, (INP(%H2EC) AND &HFA)
40      RETURN
```

b.) Send out one character to COM4

```
10      REM Enable transmitter by setting DTR ON
20      OUT &H2EC, (INP(&H2EC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H2ED) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H2EC, (INP(&H2EC) AND &HEF)
90      RETURN
```

c.) Receive one character from COM4

```
10      REM Check COM4: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
50      RETURN
60      REM Read one character from COM4: buffer
70      INPSTR$=INPUT$(1,#1)
80      RETURN
```

8.2 INDEX