# Intel® Atom™ Processor D400 and D500 Series

## Thermal/Mechanical Specifications and Design Guidelines

*December 2009*

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# Revision History

| Revision Number | Description | Revision Date |
|:---:|:---|:---:|
| 001 | • Initial release. | December 2009 |

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# 1    *Introduction*

## 1.1    Document Goals and Scope

In this document mechanical and thermal specifications for the processor are included.

The components described in this document include:

- The thermal and mechanical specifications for the Intel® Atom™ D400 and D500 series processors. (D400 series: single core, D500 series: dual core)

- The reference design thermal solution (passive heatsink) for the processors and associated retention components.

### 1.1.1    Importance of Thermal Management

The objective of thermal management is to ensure that the temperatures of all components in a system are maintained within their functional temperature range. Within this temperature range, a component is expected to meet its specified performance. Operation outside the functional temperature range can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limit of a component may result in irreversible changes in the operating characteristics of this component.

In a system environment, the processor temperature is a function of both system and component thermal characteristics. The system level thermal constraints consist of the local ambient air temperature and airflow over the processor as well as the physical constraints at and above the processor. The processor temperature depends in particular on the component power dissipation, the processor package thermal characteristics, and the processor thermal solution.

All of these parameters are affected by the continued push of technology to increase processor performance levels and packaging density (with more transistors and smaller size). As operating frequencies increase and packaging size decreases, the power density increases while the thermal solution space and airflow typically become more constrained or remains the same within the system. The result is an increased importance on system design to ensure that thermal design requirements are met for each component, including the processor, in the system.

## 1.1.2　Document Goals

Depending on the type of system and the chassis characteristics, new system and component designs may be required to provide adequate cooling for the processor. The goal of this document is to provide an understanding of these thermal characteristics and discuss guidelines for meeting the thermal requirements imposed on single processor systems using Intel Atom D400 and D500 series processors.

The concepts given in this document are applicable to any system form factor. Specific examples used will be the Intel enabled reference solution for a system.

## 1.1.3　Document Scope

This specifications and design guide supports Intel Atom D400 and D500 series processors.

In this document when a reference is made to "the processor" it is intended that this includes all the processors supported by this document. If needed for clarity, the specific processor will be listed.

In this document, when a reference is made to "EDS", the reader should refer to  the Intel Atom processor D400 and D500 Series External Design Specification.. If needed for clarity, the specific processor EDS will be referenced.

In this document, when a reference is made to the "the reference design" it is intended that this includes all reference designs supported by this document. If needed for clarify, the specific reference design will be listed.

# 1.2　Definition of Terms

**Table 1. Definition of Terms**

| Term | Description |
|------|-------------|
| $T_A$ | The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink. |
| $T_J$ | Processor junction temperature. |
| $\Psi_{JA}$ | Junction-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_J - T_A)$ / TDP.<br><br>Note: Heat source must be specified for $\Psi$ measurements. |
| $\Psi_{JS}$ | Junction-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_J - T_S)$ / TDP.<br><br>Note: Heat source must be specified for $\Psi$ measurements. |

| Term | Description |
|------|-------------|
| $\Psi_{SA}$ | Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_A)$ / TDP.<br><br>Note: Heat source must be specified for $\Psi$ measurements. |
| TIM | Thermal Interface Material: The thermally conductive compound between the heatsink and the processor die surface. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor die surface to the heatsink. |
| TDP | Thermal Design Power: a power dissipation target based on worst-case applications. Thermal solutions should be designed to dissipate the thermal design power. |
| IDP | Internet-centric Design Power: a power dissipation target based on internet-centric applications. Thermal solutions should only be designed to dissipate the design power if the usage model of system is specified to Nettop usage model. |
| $P_{D-UP}$ | Amount of processor power dissipation through TIM and heatsink, which is certain percentage of TDP. Normally the value is determined by thermal simulation results. |
| $P_{D-DOWN}$ | Amount of processor power dissipation through package substrate; solder joints and motherboard, which is certain percentage of TDP. Normally the value is determined by thermal simulation results. |

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# 2 Package Mechanical Specifications

## 2.1 Package Mechanical Specifications

The processor is packaged in a Flip-Chip Ball Grid Array (FCBGA) package, as shown in following figure. The processor uses a FCBGA package technology that directly solder down to a PCB surface.

**Figure 1. Processor Package Assembly Sketch**



Intel® Atom™ Processor D500 Series (DC) Package Sketch

Package Width 22mm

Processor Die Size 9.56 mm x 9.06 mm
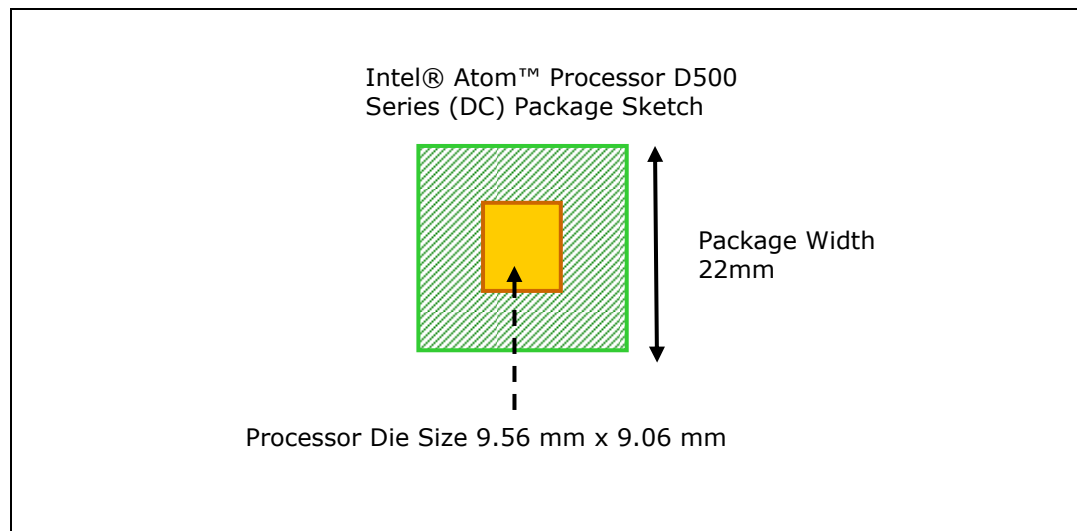
## 2.2 Package Mechanical Drawing

Figure 2 shows the basic dual core package layout. Basic mechanical dimensions of the dual core package are listed in Table 3. Dimensions necessary to design a thermal solution for the processor are shown in the detailed mechanical package mechanical drawings in Appendix B. including Intel Atom D400 & D500 series drawing.

## Figure 2. Basic Package View
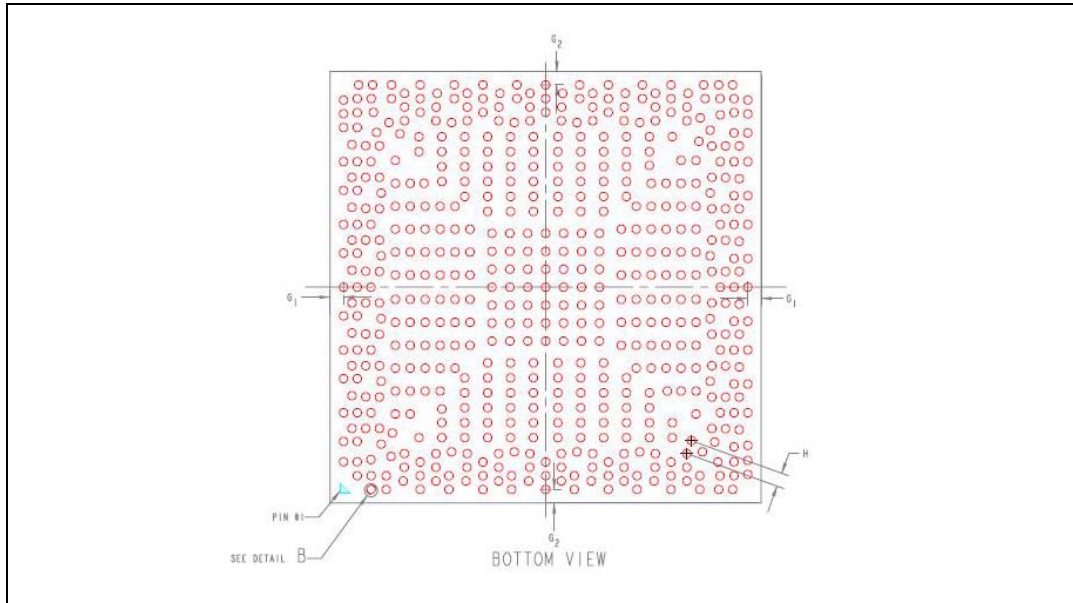


**NOTE**:   Dimensions are subject to change.

## Table 2. Package Mechanical dimensions

| Symbol | Parameter | Min | Max | Unit | Figure |
|--------|-----------|-----|-----|------|--------|
| A | Package overall height (ball to die surface) | 1.91 | 2.35 | mm | Refer to Appendix B |
| A1 | Ball height | 0.2 | 0.4 | mm | |
| A2 | Substrate thickness | 0.905 | 1.045 | mm | |
| B1 | Package substrate width | 21.95 | 22.05 | mm | |
| B2 | Package substrate length | 21.95 | 22.05 | mm | |
| C1 | Die width | 9.56 | | mm | |
| C2 | Die length | 9.06 | | mm | |
| G1 | BGA Pad Center to Package Edge | 0.686 | | mm | |
| G2 | BGA Pad Center to Package Edge | 0.686 | | mm | |
| H | Minimum Pitch for Balls Anywhere Pattern | 0.7 | | mm | |
| b | Ball Diameter | 0.35 | 0.55 | mm | |
| W | Die mass | 1.6 | | gram | |

**NOTE**:
1.   All dimensions are subject to change.
2.   Overall height as delivered. Values were based on design specifications and tolerances. Final height after surface mount depends on OEM motherboard design and SMT process.

### 2.2.1 Processor Component Keep-Out Zones

The FCBGA package may have capacitors placed in the area surrounding the processor die. The die-side capacitors, which are only slightly shorter than the die height, are electrically conductive and contact with electrically conductive materials should be avoided. The use of an insulating material between the capacitors and any thermal and mechanical solution should be considered to prevent capacitors shorting. A thermal and mechanical solution design must not intrude into the required keep-out zones as specified in Figure 14 and Figure 19.

## 2.3 Package Mechanical Loading Specifications

The processor package has mechanical load limits, maximum static and dynamic load limits, which should not be exceeded during their respective stress conditions. These include heatsink installation, removal, mechanical stress testing, and standard shipping conditions.

- When a compressive static load is necessary to ensure thermal performance of the thermal interface material between the heatsink base and the processor die, it should not exceed the corresponding specification.

- When a compressive static load is necessary to ensure mechanical performance, it should remain in the minimum/maximum range specified.

No portion of the substrate should be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

**Table 3**. Processor Loading Specifications

| Parameter | Minimum | Maximum | Notes |
|---|---|---|---|
| Static Compressive Load | 24N [5.4 lbf] | 67N [15 lbf] | 1, 2, 3 |

**NOTES**:
1. These specifications apply to uniform compressive loading in a direction normal to the processor die.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.

## 2.3.1 Package Handling Guidelines

The following table provides package handling guidelines in terms of maximum recommended loads for the processor substrate. These recommendations should be followed in particular for heatsink removal operations.

**Table 4. Package Handling Guidelines**

| Parameter | Maximum | Notes |
|-----------|---------|-------|
| Tensile | 45N [10 lbf] | – |

# 2.4 Processor Mass Specification

The typical mass of the Intel Atom D500 series processor is 1.6 grams. This mass [weight] includes all the components that are included in the package.

# 2.5 Processor Markings

Following figure shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

**Figure 3. Intel Atom D400/500 series Processor Top-Side Markings**



SAMPLE MARKING INFORMATION:
GRP1LINE1: INTEL{M}{C}'YY {e1}
GRP2LINE1: {FPO} SSPEC PROC#
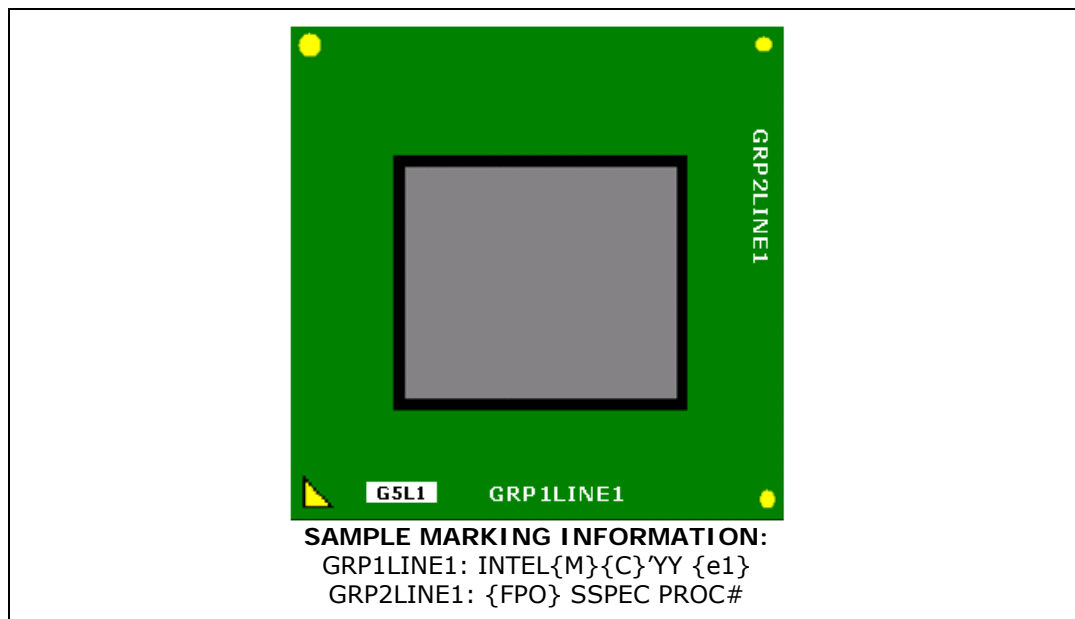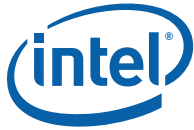
# 2.6 Processor Land Coordinates

Following figure shows the bottom view of the processor package.

**Figure 4. Processor Package Lands Coordinates**



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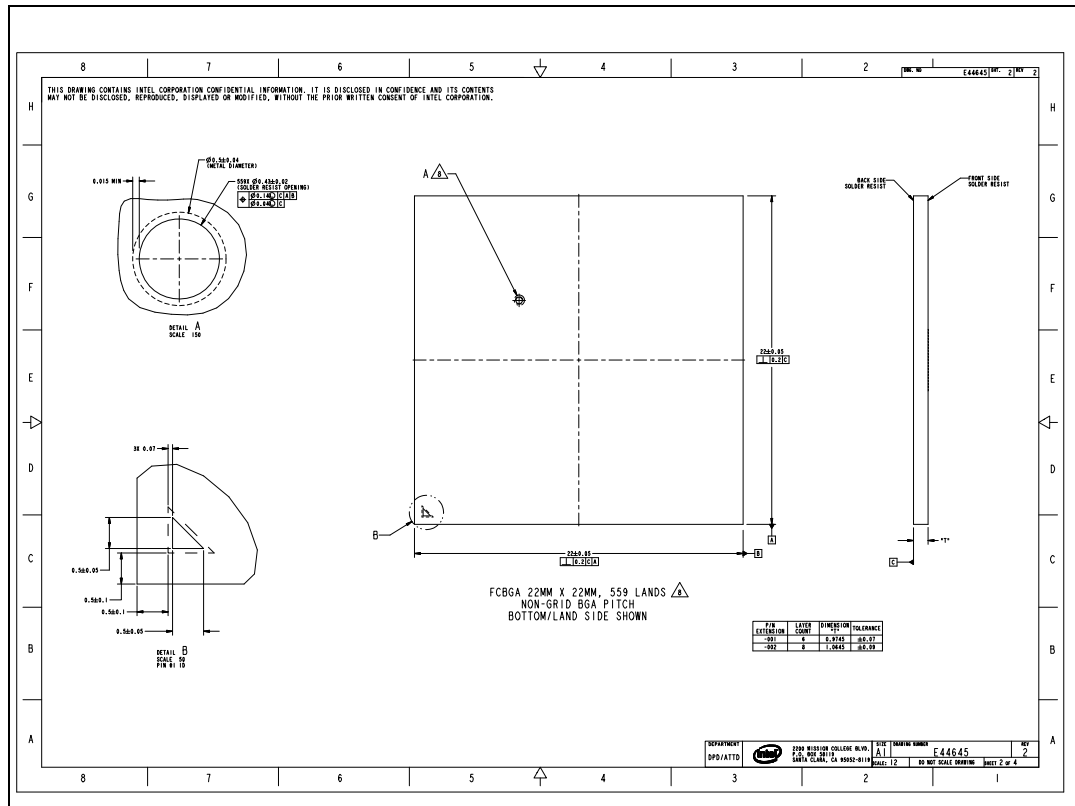
# 3    *Thermal Specifications*

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is crucial to reliable, long term system operation.

## 3.1    Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should keep the processor within the minimum and maximum junction temperature ($T_{JUNCTION-MAX}$) specifications at any processor power level as listed in section. Designing to this specification allows optimization of thermal designs for processor performance.

The thermal limits for the processor are the junction temperature ($T_{JUNCTION}$). The max junction temperature is defined at the max temperature within the processor package. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in the following table, instead of the maximum processor power consumption. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time, refer to Section 3.2.2 for more details on the usage of this feature. In all cases, it's strongly suggested that the Intel Thermal Monitor feature must be enabled for the processor to remain within specification at all times as specified in this document.

### 3.1.1    Processor Junction Temperature

**Table 5. Thermal Specifications for Intel Atom Processors**

| Processor family | Processor Number | Core Frequency and Voltage | Internet-centric design power (W) | Thermal Design Power (W) | Thermal specification $T_{junction}$ Min/Max |
|---|---|---|---|---|---|
| Intel® Atom™ | D510 | 1.66 (GHz) | 11.7 | 13 | 0 / 100 (°C) |
| Intel® Atom™ | D410 | 1.66 (GHz) | 9.6 | 10 | 0 / 100 (°C) |

**NOTE:**
1. Thermal Design Power (TDP) should be used for general thermal solution design targets. The TDP is not the maximum theoretical power the processor can generate.
2. Internet-centric design power (IDP) should only be used for internet-centric usage model, please check chapter 3.1.2 for detail definition and application.
3. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
4. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum processor operating has been reached.
5. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
6. $T_{junction}$ and TDP, IDP values provided in this table are pre-silicon estimation and are subject to change. Please contact your Intel field representative for any updates that could occur prior to the next revision of this document.

## 3.2    Processor Thermal Features

### 3.2.1    Processor Power Dissipation

An increase in processor operating frequency not only increases system performance, but also increases the processor power dissipation. The relationship between frequency and power is generalized in the following equation:

$P = CV^2F$

(where P = power, C = capacitance, V = voltage, F = frequency)

From this equation, it is evident that power increases linearly with frequency and with the square of voltage. In the absence of power saving technologies, ever increasing frequencies will result in processors with power dissipations in the hundreds of watts. Fortunately, there are numerous ways to reduce the power consumption of a processor, and Intel is aggressively pursuing low power design techniques. For example, decreasing the operating voltage, reducing unnecessary transistor activity, and using more power efficient circuits can significantly reduce processor power consumption.

An on-die thermal management feature called Thermal Monitor is available on the processor. It provides a thermal management approach to support the continued

increases in processor frequency and performance. By using a highly accurate on-die temperature sensing circuit and a fast acting Thermal Control Circuit (TCC), the processor can rapidly initiate thermal management control. The Thermal Monitor can reduce cooling solution cost, by allowing thermal designs to target TDP.

## 3.2.2    Thermal Monitor Implementation

The thermal monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active. With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor.

In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously. The Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There is only one automatic mode called Intel Thermal Monitor 1 (TM1). This mode is selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation. The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the Intel® Atom™ processors. When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

**The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processors. TM1 feature can be referred to as Adaptive Thermal Monitoring features.**

The Thermal Monitor consists of the following components:

- A highly accurate on-die temperature sensing circuit

- A bi-directional signal (PROCHOT#) that indicates if the processor has exceeded its maximum temperature or can be asserted externally to activate the Thermal Control Circuit (TCC)

- A Thermal Control Circuit that will attempt to reduce processor temperature by rapidly reducing power consumption when the on-die temperature sensor indicates that it has exceeded the maximum operating point.

- Registers to determine the processor thermal status.

## 3.2.3    PROCHOT# Signal

The primary function of the PROCHOT# signal is to provide an external indication the processor has exceeded its maximum operating temperature. While PROCHOT# is asserted, the TCC will be active. Assertion of the PROCHOT# signal is independent of any register settings within the processor. It is asserted any time the processor die temperature reaches the trip point.

PROCHOT# can be configured via BIOS as an output or bi-directional signal. As an output, PROCHOT# will go active when the processor temperature of either core exceeds its maximum operating temperature. This indicates the TCC has been activated. As an input, assertion of PROCHOT# will activate the TCC for both cores. The TCC will remain active until the system de-asserts PROCHOT#

As an output, the temperature at which the PROCHOT# signal goes active is individually calibrated during manufacturing. The power dissipation of each processor affects the set point temperature and once configured in manufacturing process, the temperature at which the PROCHOT# signal is asserted is not re-configurable.

One possible application is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) which activates the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# signal only as a backup in case of system cooling failure.

*Note:*   A thermal solution designed to meet the thermal specifications should rarely experience activation of the TCC as indicated by the PROCHOT# signal going active.

## 3.2.4    Thermal Control Circuit

The Thermal Control Circuit portion of the Thermal Monitor must be enabled for the processor to operate within specifications. The Thermal Monitor's TCC, when active, will attempt to lower the processor temperature by reducing the processor power consumption. In the original implementation of thermal monitor this is done by changing the duty cycle of the internal processor clocks, resulting in a lower effective frequency. When active, the TCC turns the processor clocks off and then back on with a predetermined duty cycle. The duty cycle is processor specific, and is fixed for a particular processor. The maximum time period the clocks are disabled is ~3 $\mu$s. This time period is frequency dependent and higher frequency processors will disable the internal clocks for a shorter time period. Figure 5 illustrates the relationship between the internal processor clocks and PROCHOT#.

Performance counter registers, status bits in model specific registers (MSRs), and the PROCHOT# output pin are available to monitor the Thermal Monitor behavior.

**Figure 5. Concept for Clocks under Thermal Monitor Control**
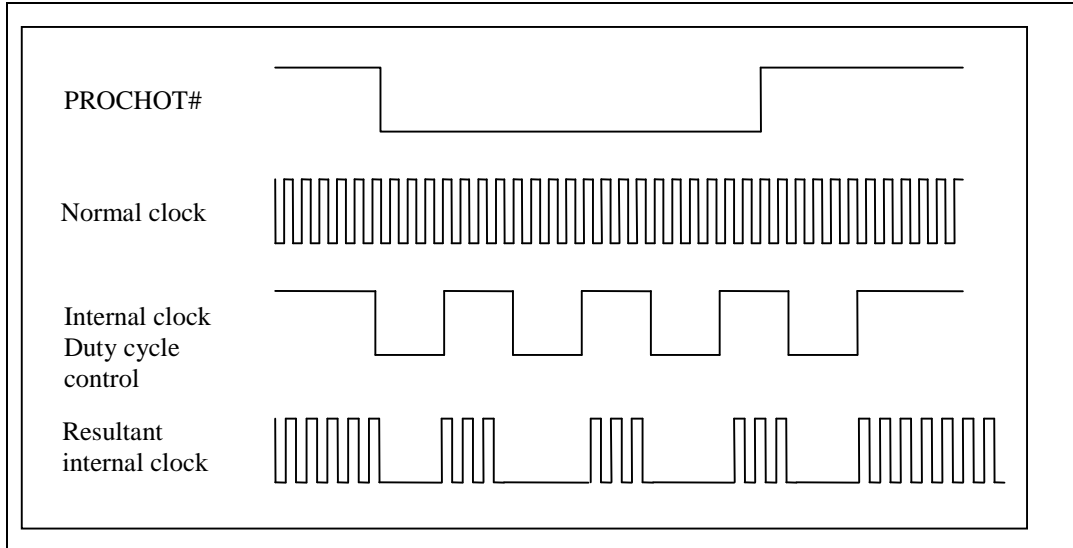


## 3.2.5    Operation and Configuration

To maintain compatibility with previous generations of processors, which have no integrated thermal logic, the Thermal Control Circuit portion of Thermal Monitor is disabled by default. During the boot process, the BIOS must enable the Thermal Control Circuit. Thermal Monitor must be enabled to ensure proper processor operation.

The Thermal Control Circuit feature can be configured and monitored in a number of ways. OEMs are required to enable the Thermal Control Circuit while using various registers and outputs to monitor the processor thermal status. The Thermal Control Circuit is enabled by the BIOS setting a bit in an MSR (model specific register). Enabling the Thermal Control Circuit allows the processor to attempt to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines. When the Thermal Control Circuit has been enabled, processor power consumption will be reduced after the thermal sensor detects a high temperature (i.e., PROCHOT# assertion). The Thermal Control Circuit and PROCHOT# transitions to inactive once the temperature has been reduced below the thermal trip point, although a small time-based hysteresis has been included to prevent multiple PROCHOT# transitions around the trip point. External hardware can monitor PROCHOT# and generate an interrupt whenever there is a transition from active-to-inactive or inactive-to-active. PROCHOT# can also be configured to generate an internal interrupt which would initiate an OEM supplied interrupt service routine. Regardless of the configuration selected, PROCHOT# will always indicate the thermal status of the processor.

The power reduction mechanism of thermal monitor can also be activated manually using an "on-demand" mode. Refer to Section 3.2.6 for details on this feature.

## 3.2.6 On-Demand Mode

For testing purposes, the thermal control circuit may also be activated by setting bits in the ACPI MSRs. The MSRs may be set based on a particular system event (e.g., an interrupt generated after a system event), or may be set at any time through the operating system or custom driver control thus forcing the thermal control circuit on. This is referred to as "on-demand" mode. Activating the thermal control circuit may be useful for thermal solution investigations or for performance implication studies. When using the MSRs to activate the on-demand clock modulation feature, the duty cycle is configurable in steps of 12.5%, from 12.5% to 87.5%.

For any duty cycle, the maximum time period the clocks are disabled is ~3 $\mu$s. This time period is frequency dependent, and decreases as frequency increases. To achieve different duty cycles, the length of time that the clocks are disabled remains constant, and the time period that the clocks are enabled is adjusted to achieve the desired ratio. For example, if the clock disable period is 3 $\mu$s, and a duty cycle of ¼ (25%) is selected, the clock on time would be reduced to approximately 1 $\mu$s [on time (1 $\mu$s) ÷ total cycle time (3 + 1) $\mu$s = ¼ duty cycle]. Similarly, for a duty cycle of 7/8 (87.5%), the clock on time would be extended to 21 $\mu$s [21 ÷ (21 + 3) = 7/8 duty cycle].

In a high temperature situation, if the thermal control circuit and ACPI MSRs (automatic and on-demand modes) are used simultaneously, the fixed duty cycle determined by automatic mode would take precedence.

## 3.2.7 System Considerations

Intel requires the Thermal Monitor and Thermal Control Circuit to be enabled for all processors. The thermal control circuit is intended to protect against short term thermal excursions that exceed the capability of a well designed processor thermal solution. Thermal Monitor should not be relied upon to compensate for a thermal solution that does not meet the thermal profile up to the thermal design power (TDP).

Each application program has its own unique power profile, although the profile has some variability due to loop decisions, I/O activity and interrupts. In general, compute intensive applications with a high cache hit rate dissipate more processor power than applications that are I/O intensive or have low cache hit rates.

The processor TDP is based on measurements of processor power consumption while running various high power applications. This data is used to determine those applications that are interesting from a power perspective. These applications are then evaluated in a controlled thermal environment to determine their sensitivity to activation of the thermal control circuit. This data is used to derive the TDP targets published in the processor Datasheet.

A system designed to meet the thermal specification of $T_{JUNCTION-MAX}$ values published in the processor Datasheet greatly reduces the probability of real applications causing the thermal control circuit to activate under normal operating conditions. Systems that do not meet these specifications could be subject to more frequent activation of the thermal control circuit depending upon ambient air temperature and application power profile. Moreover, if a system is significantly under designed, there is a risk that the Thermal Monitor feature will not be capable of maintaining a safe operating temperature and the processor could shutdown and signal THERMTRIP#.

### 3.2.8 Operating System and Application Software Considerations

The Thermal Monitor feature and its thermal control circuit work seamlessly with ACPI compliant operating systems. The Thermal Monitor feature is transparent to application software since the processor bus snooping, ACPI timer, and interrupts is active at all times.

### 3.2.9 THERMTRIP# Signal

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon temperature has reached its operating limit. At this point the system bus signal THERMTRIP# goes active and power must be removed from the processor. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. Refer to the processor Datasheet for more information about THERMTRIP#.

The temperature where the THERMTRIP# signal goes active is individually calibrated during manufacturing. The temperature where THERMTRIP# goes active is roughly parallel to the thermal profile and greater than the PROCHOT# activation temperature. Once configured, the temperature at which the THERMTRIP# signal is asserted is neither re-configurable nor accessible to the system.

### 3.2.10 Cooling System Failure Warning

It may be useful to use the PROCHOT# signal as an indication of cooling system failure. Messages could be sent to the system administrator to warn of the cooling failure, while the thermal control circuit would allow the system to continue functioning or allow a normal system shutdown. If no thermal management action is taken, the silicon temperature may exceed the operating limits, causing THERMTRIP# to activate and shut down the processor. Regardless of the system design requirements or thermal solution ability, the Thermal Monitor feature must still be enabled to ensure proper processor operation.

### 3.2.11 Digital Thermal Sensor

The Intel Atom D400/D500 processor embedded the Digital Thermal Sensor (DTS) as the on-die sensor to use for processor temperature monitoring. The Processor will have both the DTS and thermal diode enabled. The DTS is monitoring the same sensor that activates the TCC (see Section 3.2.4). The readings from the DTS are relative to the activation of the TCC. The DTS value where TCC activation occurs is 0 (zero).

The Intel Atom D400/D500 DTS can only be accessed via a MSR. The value read via the MSR is an unsigned number of degrees C away from activating TCC. Multiple digital thermal sensors can be implemented within the package without adding a pair of signal pins per sensor as required with the thermal diode. The digital thermal sensor is easier to place in thermally sensitive locations of the processor than the thermal diode. This is achieved due to a smaller foot print and decreased sensitivity to noise. Since the DTS is factory set on a per-part basis there is no need for the health monitor components to be updated at each processor family.

## 3.2.12    Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode", with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement.

Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the $T_J$ temperature can change. Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events.

This offset is different than the diode $T_{offset}$ value programmed into the Intel® Atom™ processor Model Specific Register (MSR).Table 5 and Table 6 below provide the diode interface and specifications. The transistor model parameters shown in Table 6 provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

**Table 6. Thermal Diode Interface**

| Signal Name | Pin/Ball Number | Signal Description |
|---|---|---|
| • THERMDA_1 | D30 | Thermal diode anode |
| • THERMDA_2 | C30 | Thermal diode anode (applied for dual core only) |
| • THERMDC_1 | E30 | Thermal diode cathode |
| • THERMDC_2 | D31 | Thermal diode cathode (applied for dual core only) |

**Table 7. Thermal Diode Parameters using Transistor Model**

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|--------|-----------|-----|-----|-----|------|-------|
| IFW | Forward Bias Current | 5 | | 200 | µ A | 1 |
| IE | Emitter Current | 5 | | 200 | µ A | 1 |
| nQ | Transistor Ideality | 0.997 | 1.001 | 1.015 | | 2,3,4 |
| Beta | | 0.25 | | 0.65 | | 2,3 |
| RT | Series Resistance | 2.79 | 4.52 | 6.24 | Ω | 2,5 |

**NOTES**:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:
   IC = IS * (e qVBE/nQkT −1)
   where IS = saturation current, q = electronic charge, VBE = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, RT, provided in the Diode Model Table (Table 6) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 9. In most sensing devices, an expected value for the diode ideality is designed into the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called $n_{trim}$) will be 1.000. Given that most diodes are not perfect, the designers usually select an $n_{trim}$ value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the $n_{trim}$, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

Terror(nf) = Tmeasured * (1 - nactual/ntrim)

where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, $n_{actual}$ is the measured ideality of the diode, and $n_{trim}$ is the diode ideality assumed by the temperature sensing device.

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# 4 Reference Thermal Solution

*Note:* The reference thermal mechanical solution information shown in this document represents the current state of the data and may be subject to changes. The information represents design targets, not commitments by Intel.

This section describes the overall requirements for the heatsink reference thermal solution supporting the Intel Atom D400/D500 processor.

## 4.1 Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- The area of the surface on which the heat transfer takes place. Without any enhancements, this is the surface of the processor die. One method used to improve thermal performance is by attaching a heatsink to the die. A heatsink can increase the effective heat transfer surface area by conducting heat out of the die and into the surrounding air through fins attached to the heatsink base.

- The conduction path from the heat source to the heatsink fins. Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package die and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become stricter. Thermal interface material (TIM) is used to fill in the gap between the die and the bottom surface of the heatsink, and thereby improve the overall performance of the stack-up (die-TIM-heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure applied to it. Please refer to Section 4.1.3 for further information.

- The heat transfer conditions on the surface on which heat transfer takes place. Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, and the local air velocity over the surface. The higher the air velocity over the surface, and the cooler the air, the more efficient is the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes in particular the fin faces and the heatsink base.

**Active heatsinks** typically incorporate a fan that helps manage the airflow through the heatsink.

**Passive heatsink** solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks are cooled by air with lower air speed. These heatsinks are therefore typically larger (and heavier) than active heatsinks due to the increase in fin surface required to meet a required performance. As the heatsink fin density

(the number of fins in a given cross-section) increases, the resistance to the airflow increases: it is more likely that the air travels around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area can be an effective method for controlling airflow through the heatsink.

## 4.1.1　Heatsink Size

The size of the heatsink is dictated by height restrictions for installation in a system and by the real estate available on the motherboard and other considerations for component height and placement in the area potentially impacted by the processor heatsink. The height of the heatsink must comply with the requirements and recommendations published for the motherboard form factor of interest. Designing a heatsink to the recommendations may preclude using it in system adhering strictly to the form factor requirements, while still in compliance with the form factor documentation.

For the ATX/microATX compatible form factor, it is recommended to use:

• The ATX motherboard keep-out footprint definition and height restrictions for enabling components, defined for the platforms designed with the FCBGA of this design guide.

• The motherboard primary side height constraints defined in the ATX Specification V2.2 and the microATX Motherboard Interface Specification V1.2 found at http://www.formfactors.org/.

The resulting space available above the motherboard is generally not entirely available for the heatsink. The target height of the heatsink must take into account airflow considerations (for fan performance for example) as well as other design considerations (air duct, etc.).

## 4.1.2　Thermal Interface Material

Thermal interface material application between the processor die and the heatsink base is generally required to improve thermal conduction from the die to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier and allow direct heatsink attach, without the need for a separate thermal interface material dispense or attach process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures the entire processor die area is covered. It is important to compensate for heatsink-to-processor attach positional alignment when selecting the proper thermal interface material size.

When pre-applied material is used, it is recommended to have a protective film applied. This film must be removed prior to heatsink installation.

The TIM used in reference thermal solution for the Intel Atom D400 and D500 series processor is Honeywell PCM45F (pad version).

## 4.1.3 Heatsink Attach Mechanism Design Considerations

### 4.1.3.1 General Guidelines

There are no features on the FCBGA package for direct heatsink attachment: a mechanism must be designed to attach the heatsink directly to the motherboard. In addition to holding the heatsink in place on top of the processor die, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:

- Ensuring thermal performance of the thermal interface material (TIM) applied between the processor die and the heatsink. TIMs based on phase change materials are very sensitive to applied pressure: the higher the pressure, the better the initial performance. Designs should incorporate a possible decrease in applied pressure over time due to potential structural relaxation in retention components (creep effect causing clip to lose its preload and causing anchor pull-out). It is not recommended to utilize TIMs such as thermal greases onto small bare die package, due to the TIM "pump-out" concern after heatsink is assembled.

- Ensuring system electrical, thermal, and structural integrity under shock and vibration events. The mechanical requirements of the heatsink attach mechanism depend on the mass of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the motherboard and the system should be considered in designing the heatsink attach mechanism. The design should provide a means for protecting the solder joints.

### 4.1.3.2 Attach Mechanism Design Considerations

In addition to the general guidelines given above, the heatsink attach mechanism for the processor should be designed to the following guidelines:

- Heatsink should be held in place under mechanical shock and vibration events and applies force to the heatsink base to maintain desired pressure on the thermal interface material. Note that the load applied by the heatsink attach mechanism must comply with the package specifications described in this document. One of the key design parameters is the height of the top surface of the processor die above the motherboard, is expected in the range of 1.845 mm ± 0.078 mm. This data is provided for information only, and should be derived from:

The height of the package, from the package seating plane to the top of the die, need to be accounting for its nominal variation and tolerances of the manufacturing process that are given.

- Engages easily, and if possible, without the use of special tools. In general, the heatsink is assumed to be installed after the motherboard has been installed into the chassis.

- Minimizes contact with the motherboard surface during installation and actuation to avoid scratching/damaging the motherboard.

## 4.2 System Thermal Solution Considerations

### 4.2.1 Chassis Thermal Capabilities

The reference thermal solution for Intel Atom D400 and D500 series is a passive heatsink design, which allows for fanless system design in a purpose-built and effectively designed chassis while ensuring operational stability and reliability of the processor. Please refer to section 4.2.2 for more chassis design details. It is the system integrator or designer's duty to insure a proper chassis design enabling the proper use of the reference thermal solution (see table 10.).

*Note:* The TDP and IDP value of the Intel Atom D400 and D500 series can be found in Section 3.1.. Considering the target market segment for the Nettop platform, the reference thermal solution for the processor is designed to meet IDP for acoustic performance & cost optimization.  .

**Table 8. System Thermal Solution Design Requirement**

| Platform | System Thermal Solution Design Requirement | Note |
|---|---|---|
| Pine Trail-D Platform | When external ambient is 35 °C, local ambient temp is $\leq$ 47 °C | 1 |
| | $T_{JUNCTION\text{-}MAX} \leq 100$ °C | 2, 3 |

**NOTE:**
1. The thermal requirement for reference thermal solution is based on internet-centric power and vertical chassis orientation vented at the top and bottom sides. (longitudinal fins should be parallel to gravity direction)
2. For the implementation of any customized thermal solution in the processor, $T_{JUNCTION\text{-}MAX}$ is thermal design criteria to ensure the stability and reliability of the processor whether the design is based on IDP or TDP.
3. For the implementation of any customized thermal solution using either thermal interface material, clip, or heatsink design that is different from the Intel reference thermal solution as mentioned in this document.

In order to evaluate the system thermal capability of a given chassis, the system designer is recommended to conduct in-chassis system thermal test.

In a system using customized thermal solution on the processor, the thermal pass requirement for a given chassis can be met, if

$$T_{junction} \leq T_{junction\text{-}MAX}$$

## 4.2.2 Improving Chassis Thermal Performance

The heat generated by components within the chassis must be removed to provide an adequate operating environment for the processor and all other components in the system. Moving airflow through the chassis brings in fresh cool air from the external ambient environment and transports the heat generated by the processor and other system components out of the system. Therefore, the number, size and relative position of fans and/or vents determine the chassis thermal performance, and the resulting ambient temperature around the processor.

### 4.2.2.1 Fanless System Operation

In order to create a fanless Nettop system, the reference design may be utilized in a well-designed chassis. Specifically, the chassis should be oriented vertically such that the longitudinal direction of the heatsink fins is parallel with the gravity vector. In addition, the chassis should have copious venting on the top and bottom sides with adequate inlet space below the bottom-side intake vents. Figure 6 shows a simplified illustration of an appropriately oriented chassis.

**Figure 6. Chassis Orientation & Venting for Fanless Implementation of Reference Design Heatsink**
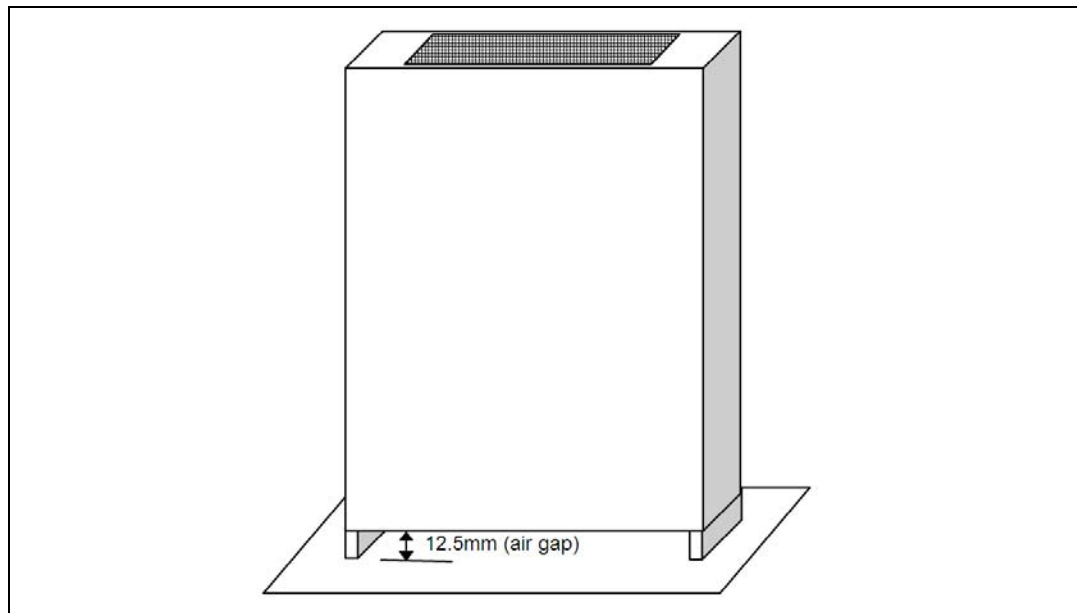


While the exact amount of venting has not been thoroughly investigated, it is generally recommended to target the maximum amount of venting possible on the top and bottom surfaces with a Free Area Ratio (FAR) ranging from 35 to 65%. For purposes of the reference design development, minimal top side and bottom side venting was found to be 45 cm$^2$ with a FAR of 35% (actual vent size was approximately 30% of the available surface.)

The system integrator or chassis designer should also consider component and peripheral placement within the system to enable fanless design. For most Nettop

systems, the highest powers can be found in the core region (processor, VR, and memory heat) as well as the HDD's and any DC-DC daughter cards. It is recommended that the core region and the HDD's be separated in distance such that they have little influence over each other. For example, an HDD placed over the region of the reference design heatsink will contribute to higher ambient temperatures seen by the heatsink and degrade its performance. An alternative layout would consider placing the drives in the same plane as the board so as to separate these highest power components. Similarly, the DC-DC card or components should be place near the inlet vent of the chassis. This arrangement allows for the lowest temperature air to cool the VR components to maximize their efficiency and reliability. Extensive evaluation of optimal chassis layouts has not been conducted and these recommendations should be treated as general guidelines only.

## 4.2.2.2    Passive System Operation

While the reference design heatsink was optimized for use in a fanless natural convection environment, it can also be used in a passive system design which utilizes forced convection by means of system or PSU fans. The reference design heatsink is capable of passive operation in all three dimensional flow directions with best results provided with air flow parallel to the fins. In the case of passive system implementation, the combination of ambient temperature and air velocity must be assessed in order to ensure the thermal requirements are met. For the reference design oriented parallel to the direction of airflow, the heatsink performance curve can be estimated by the following equation.

$$\theta_{sa} = 10.993 * V^{-0.3195}$$

Where:
— $\theta_{sa}$ is defined as (Ts – Ta)/ $P_{up}$
— Ts – Temperature of the heatsink bottom side at its geometric center
— Ta – Average inlet ambient temperature to the heatsink
— $P_{up}$ – portion of the heat transferred through the heatsink
— V: Velocity, unit: LFM

When used in a passive system, the orientation and venting of the chassis is not restricted by the guidelines set forth in the above section. However, it is important to consider the airflow paths through the system that minimize the internal air temperature and provide effective airflow for all major subcomponents of the system.

## 4.2.3    Summary

In summary, heatsink design considerations for Intel Atom D400/D500 processor include:

• For the implementation of any customized thermal solution using either a thermal interface material, or clip, or heatsink design that is different from the Intel® reference thermal solution described in this document, it is recommended to use the junction temperature (TJUNCTION-MAX) for the processor as the criteria to judge the thermal performance of the processor when operated at TDP or IDP (dependent on usage) at an external ambient temperature of 35$^{o}$C . TJUNCTION-MAX must be compliant in all times in order to ensure processor reliability.

- Heatsink interface to die surface characteristics, such as flatness and roughness, influences the contact resistance of the heatsink to the die. The reference design specifies a heatsink flatness of X.

- The resistance of the thermal interface material used between the heatsink and the die is a large portion of the heatsink performance. Intel recommends use of Honeywell PCM45F with sufficiently high preload applied by the retention mechanism described in the next statement.

- The required heatsink clip static preload is 11.3 lbf ± 3.6 lbf at the beginning of life (Please refer to Section 4.1.4.3 for further information).

- The surface area of the heatsink should be adequate to provide sufficient convective cooling whether in natural or forced convection environment. The reference design maximizes the fin area while minimizing the weight of the heatsink.

- While the material used to construct the heatsink is generally important, the expected operating condition of the reference design heatsink is such that aluminum is more than adequate for proper conduction in the heatsink. At low flow rates, the resistance of the heatsink is largely limited by its convective resistance rather than conduction.

- Proper venting is required on the chassis to ensure sufficient air flow for the passive heatsink and other thermal critical components within the system. Adequate venting and chassis orientation is especially critical for fanless system design.

- The reference design heatsink has been designed for use in fanless systems having certain orientations and venting characteristics. However, it should be noted that the heatsink design also enables forced convection cooling in all three dimensional directions.

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# 5 Thermal Metrology

This section discusses guidelines for testing thermal solutions, including measuring processor temperatures.

## 5.1 Digital Thermal Sensor measurement ($T_{JUNCTION-MAX}$ Methodology)

For the system integrator or designer, to validate their thermal solution design on Intel Atom Processor D500 series dual core processor, it is suggested to monitor the processor's junction temperature ($T_{JUNCTION}$). To ensure functionality and reliability, the thermal solution should be able to maintain $T_{JUNCTION}$ in the processor to be at or below the maximum temperature listed in Table 5.

It is with reasonable accuracy and aligned with the Intel Thermal Monitor function to use DTS as an indicator of $T_{JUNCTION}$ temperature and validate thermal design via DTS value. About the definition of DTS value, please see section 3.2.11. To provide a more convenient way for system designer to monitor DTS value, Intel will support system designer with a software tool to read out the DTS value in real time when conducting thermal tests, please contact your Intel representatives for more detail and getting this tool. Even without Intel's SW tool, system designer can always access DTS value via MSR.

## 5.2 Local Ambient Temperature Measurement Guidelines

The local ambient temperature $T_A$ is the temperature of the ambient air surrounding the processor. For a passive heatsink, $T_A$ is defined as the heatsink approach air temperature; for an actively cooled heatsink, it is the temperature of inlet air to the active cooling fan.

It is worthwhile to determine the local ambient temperature in the chassis around the processor to understand the effect it may have on the die temperature.

$T_A$ is best measured by averaging temperature measurements at multiple locations in the heatsink inlet airflow. This method helps reduce error and eliminate minor spatial variations in temperature. The following guidelines are meant to enable accurate determination of the localized air temperature around the processor during system thermal testing.

For **active heatsinks**, it is important to avoid taking measurement in the dead flow zone that usually develops above the fan hub and hub spokes. Measurements should be taken at four different locations uniformly placed at the center of the annulus formed by the fan hub and the fan housing to evaluate the uniformity of the air temperature at the fan inlet. The thermocouples should be placed approximately 3 mm to 8 mm [0.1 to 0.3 in] above the fan hub vertically and halfway between the

fan hub and the fan housing horizontally as shown in Figure 7 (avoiding the hub spokes). Using an open bench to characterize an active heatsink can be useful, and usually ensures more uniform temperatures at the fan inlet. However, additional tests that include a solid barrier above the test motherboard surface can help evaluate the potential impact of the chassis. This barrier is typically clear Plexiglas*, extending at least 100 mm [4 in] in all directions beyond the edge of the thermal solution. Typical distance from the motherboard to the barrier is 81 mm [3.2 in]. For even more realistic airflow, the motherboard should be populated with significant elements like memory cards, graphic card, and chipset heatsink. If a barrier is used, the thermocouple can be taped directly to the barrier with a clear tape at the horizontal location as previously described, half way between the fan hub and the fan housing. If a variable speed fan is used, it may be useful to add a thermocouple taped to the barrier above the location of the temperature sensor used by the fan to check its speed setting against air temperature. When measuring $T_A$ in a chassis with a live motherboard, add-in cards, and other system components, it is likely that the $T_A$ measurements will reveal a highly non-uniform temperature distribution across the inlet fan section.

For **passive heatsinks**, thermocouples should be placed approximately 13 mm to 25 mm [0.5 to 1.0 in] away from processor and heatsink as shown in Figure 8. The thermocouples should be placed approximately 51 mm [2.0 in] above the baseboard. This placement guideline is meant to minimize the effect of localized hot spots from baseboard components.

*Note:* Testing an active heatsink with a variable speed fan can be done in a thermal chamber to capture the worst-case thermal environment scenarios. Otherwise, when doing a bench top test at room temperature, the fan regulation prevents the heatsink from operating at its maximum capability. To characterize the heatsink capability in the worst-case environment in these conditions, it is then necessary to disable the fan regulation and power the fan directly, based on guidance from the fan supplier.

**Figure 7. Locations for Measuring Local Ambient Temperature, Active Heatsink**
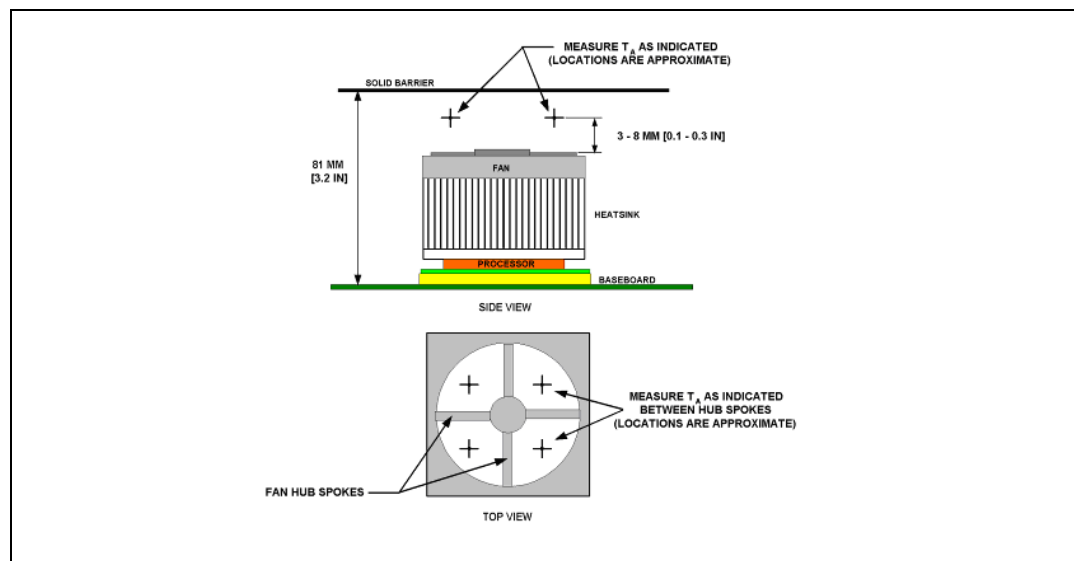


**NOTE:**   Drawing Not to Scale

**Figure 8. Locations for Measuring Local Ambient Temperature, Passive Heatsink**
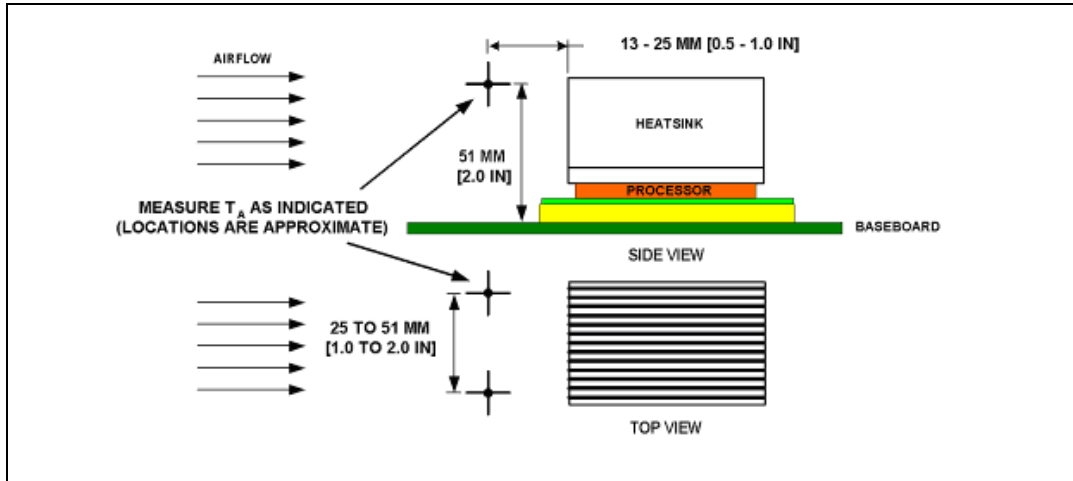


**NOTE:**   Drawing Not to Scale

**Figure 9. Locations for Measuring Local Ambient Temperature, Fanless Heatsink**
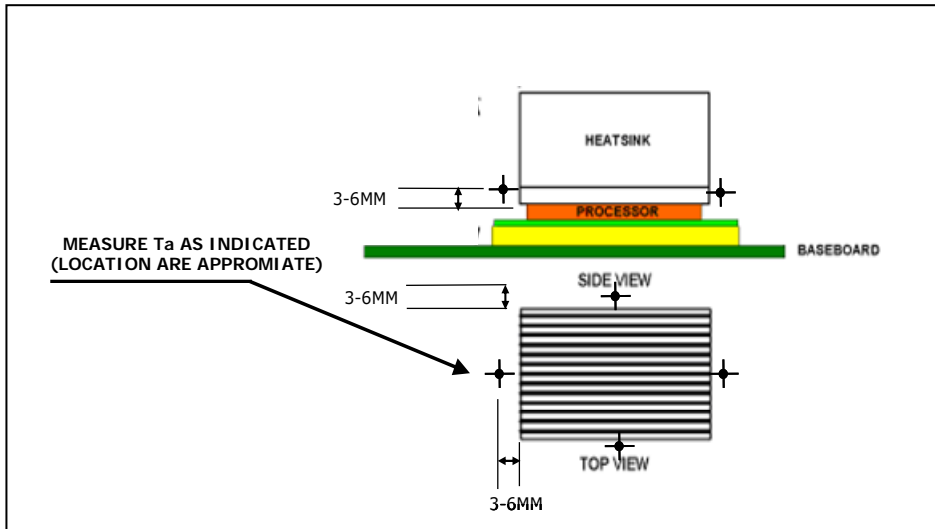


**NOTE:**   Drawing Not to Scale

It is recommended that full and routine calibration of temperature measurement equipment be performed before attempting to perform temperature measurement. Intel recommends checking the meter probe set against known standards. This should be done at 0ºC (using ice bath or other stable temperature source) and at an elevated temperature, around 80ºC (using an appropriate temperature source).

Wire gauge and length also should be considered as some less expensive measurement systems are heavily impacted by impedance. There are numerous resources available throughout the industry to assist with implementation of proper controls for thermal measurements.

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# 6 System Thermal/Mechanical Design Information

## 6.1 Overview of the Reference Design

This chapter will document the requirements for designing a passive heatsink that meets the maximum usage power consumption (IDP) that mentioned in Section 3.1. The reference thermal solution (Figure 15 & Figure 20.) satisfies the specified thermal requirements for the Intel Atom D400 and D500 series processor.

*Note:* The part numbers provided in this document is for reference only. The revision number -001 may be subject to change without notice. OEMs and System Integrators are responsible for thermal, mechanical and environmental validation of this solution on their platform (please refer to Sections 6.1.2 and 6.2).

The reference thermal solution for the Intel Atom D400 and D500 series processor, take advantage of cost savings and the thermal solution supports the unique and smaller desktop PCs including small and ultra small form factors, down to a 5L system size.
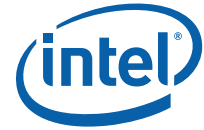
## 6.1.1 Altitude

Many companies design products that must function reliably at high altitude, typically 1,500 m [5,000 ft] or more. Air-cooled temperature calculations and measurements at the test site elevation must be adjusted to take into account altitude effects like variation in air density and overall heat capacity. This often leads to some degradation in thermal solution performance compared to what is obtained at sea level, with lower fan performance and higher surface temperatures. The system designer needs to account for altitude effects in the overall system thermal design to make sure that $T_{JUNCTION-MAX}$ requirement for the processor is met at the targeted altitude for reference thermal solution.

For a customized thermal solution, the system designer needs to account for altitude effects in the overall system thermal design to make sure that $T_{JUNCTION-MAX}$ requirement for the processor is met at the targeted altitude.

## 6.1.2 Heatsink Thermal Validation

Intel recommends evaluation of the heatsink within the specific boundary conditions based on the methodology described Section 5.

Testing is done on bench top test boards at ambient laboratory temperature.

The test results, for a number of samples, are reported in terms of a worst-case mean + 3σ value for thermal characterization parameter using real processors.

# 6.2 Environmental Reliability Testing

## 6.2.1 Structural Reliability Testing

Structural reliability tests consist of unpackaged, board-level vibration and shock tests of a given thermal solution in the assembled state. The thermal solution should meet the specified thermal performance targets after these tests are conducted; however, the test conditions outlined here may differ from your own system requirements.

### 6.2.1.1 Random Vibration Test Procedure

- Duration: 10 min/axis, 3 axes
- Frequency Range: 5 Hz to 500 Hz
- Power Spectral Density (PSD) Profile: 3.13 G RMS

**Figure 10. Random Vibration PSD**
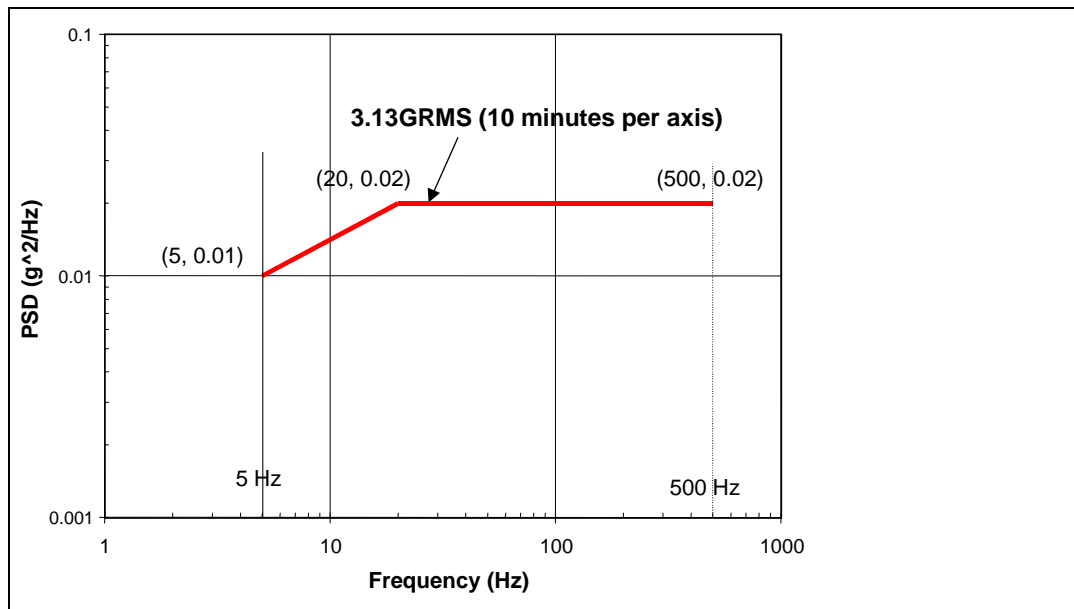
## 6.2.1.2    Shock Test Procedure

Recommended performance requirement for a motherboard:

- Quantity: 3 drops for + and - directions in each of 3 perpendicular axes (i.e., total 18 drops).

- Profile: 50 G trapezoidal waveform, 170 in/sec minimum velocity change.

- Setup: Mount sample board on test fixture.

**Figure 11. Shock Acceleration Curve**
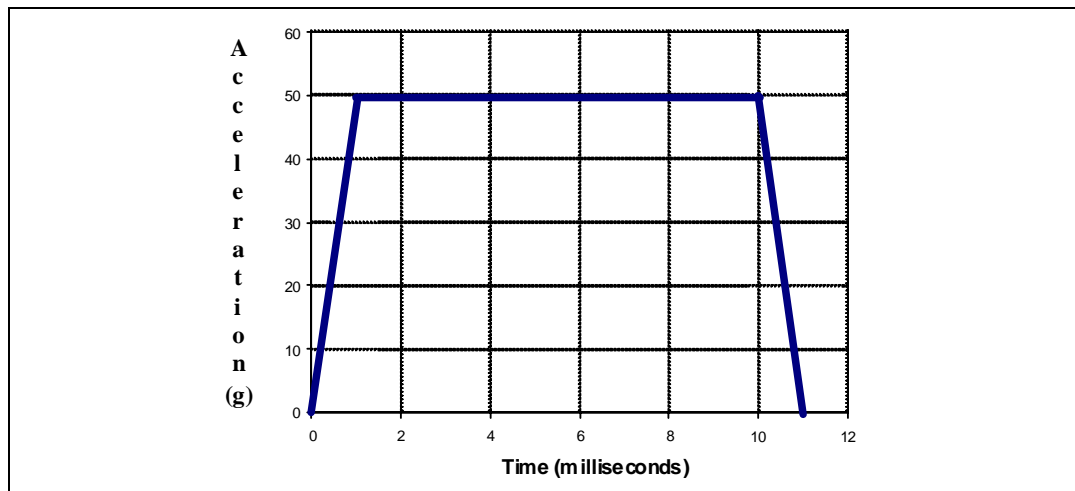


### 6.2.1.2.1    Recommended Test Sequence

Each test sequence should start with components (i.e. motherboard, heatsink assembly, etc.) that have never been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly, and BIOS/CPU/Memory test (refer to section 6.2.1.2.2 below).

Prior to the mechanical shock & vibration test, the units under test should be preconditioned for 72 hours at 45 ºC. The purpose is to account for load relaxation during burn-in stage.

The stress test should be followed by a visual inspection and then BIOS/CPU/Memory test.

### 6.2.1.2.2    Post-Test Pass Criteria

The post-test pass criteria are:

1.  No significant physical damage to the heatsink attach mechanism (including such items as clip and motherboard fasteners).
1.  Heatsink must remain attached to the motherboard.
2.  Heatsink remains seated and its bottom remains mated flatly against die surface. No visible gap between the heatsink base and processor die. No visible tilt of the heatsink with respect to its attaching mechanism.
3.  No signs of physical damage on motherboard surface due to impact of heatsink or heatsink attach mechanism.
4.  No visible physical damage to the processor package.
5.  Successful BIOS/Processor/memory test of post-test samples.
6.  Thermal compliance testing to demonstrate that the case temperature specification can be met.

## 6.2.2    Recommended BIOS/CPU/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational motherboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

*   Appropriate system motherboard

*   Processor

*   All enabling components, including thermal solution parts

*   Power supply

*   Disk drive

*   Add-in card

*   DIMM

*   Keyboard

*   Monitor

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors.

## 6.3    Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (e.g., polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Material used shall not have deformation or degradation in a temperature life test.

Any plastic component exceeding 25 grams must be recyclable per the European Blue Angel recycling standards.

## 6.4    Safety Requirements

Heatsink and attachment assemblies shall be consistent with the manufacture of units that meet the safety standards:

- UL Recognition-approved for flammability at the system level. All mechanical and thermal enabling components must be a minimum UL94V-2 approved.

- CSA Certification. All mechanical and thermal enabling components must have CSA certification.

- All components (in particular the heatsink fins) must meet the test requirements of UL1439 for sharp edges.

- If the International Accessibility Probe specified in IEC 950 can access the moving parts of the fan, consider adding safety feature so that there is no risk of personal injury.

## 6.5    Reference Attach Mechanism

### 6.5.1    Structural Design Strategy

Structural design strategy for the Intel reference thermal solution is to minimize upward and downward board deflection during shock test.

The design uses a high clip stiffness that resists local board curvature under the heatsink, and minimizes, in particular, upward board deflection.
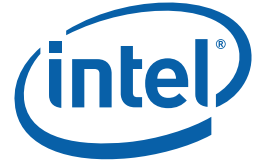
## 6.5.2 Mechanical Interface to the Reference Attach Mechanism

The attach mechanism component from the reference thermal solution can be used by other 3$^{rd}$ party cooling solutions. The attach mechanism consists of:

1. 4 fasteners (for example: ITW P/N:83FT-02-37-9909)
2. Intel Atom D400 and D500 series heatsink mass ≤ 80 grams

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*(intel®)*

# *Appendix A Mechanical Drawings*

The following table lists the mechanical drawings included in this appendix. These drawings refer to the reference thermal mechanical enabling components for the processor.

*Note:* Intel reserves the right to make changes and modifications to the design as necessary.

| Drawing Description | Page Number |
|---|---|
| Motherboard Keep-out and Keep-in zone for Intel Atom D500 Series | 41 |
| Motherboard Keep-out and Keep-in zone for Intel Atom D400 Series | 46 |
| Non-Processor components Keep-in zone for the Intel Atom D500 Series | 42 |
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| Keep-out zone Heatsink for the Intel Atom D500 Series | 43 |
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| Intel Atom D400 Series Reference Heat sink Design | 49 |
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## Figure 12. Motherboard Keep-out and Keep-in zone for Intel Atom D500 Series

**Figure 13. Non-Processor Components Keep-in zone for Intel Atom D500 Series**

**Figure 14. Heatsink Keep Out Zone for Intel Atom D500 Series**

**Figure 15. Intel Atom D500 Series Reference Heatsink (Assembly)**

**Figure 16. Intel Atom D500 Series Reference Heatsink  (P/N: E51968-001)**
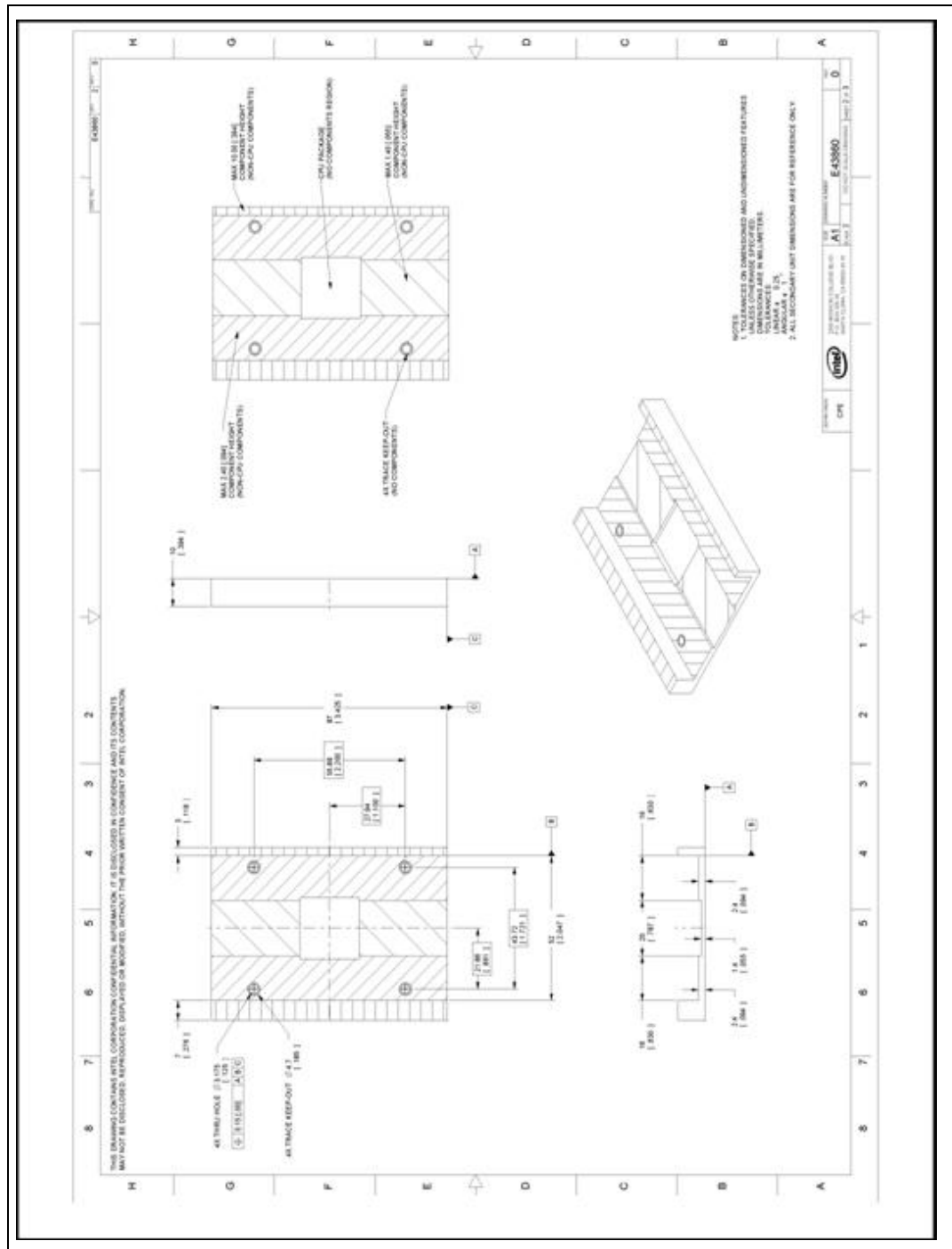
**Figure 17. Motherboard Keep-out and Keep-in zone for Intel Atom D400 Series**

**Figure 18. Non-Processor Components Keep-in zone for Intel Atom D400 Series**
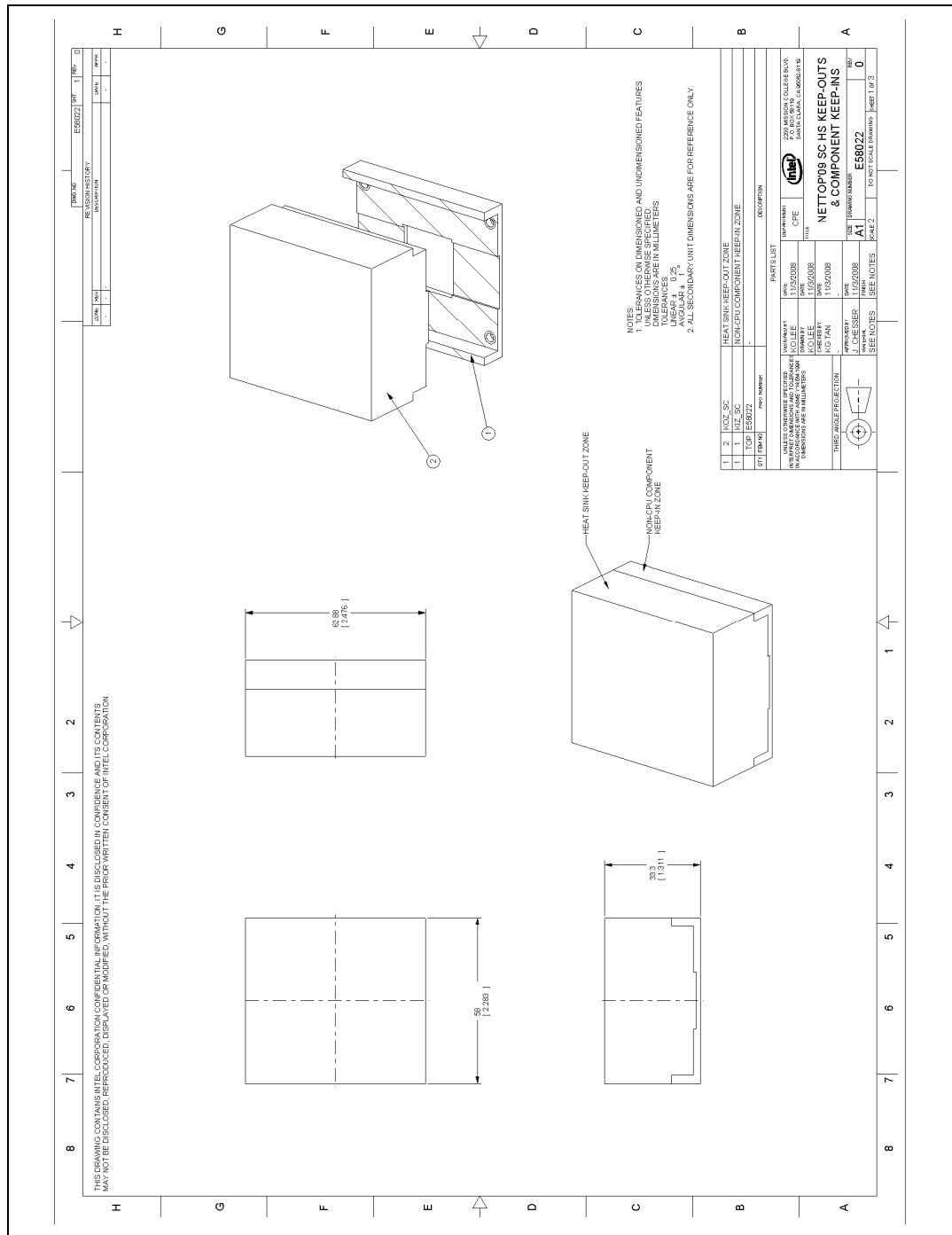
**Figure 19. Heatsink Keep-out Zone for Intel Atom D400 Series**

*Mechanical Drawings*
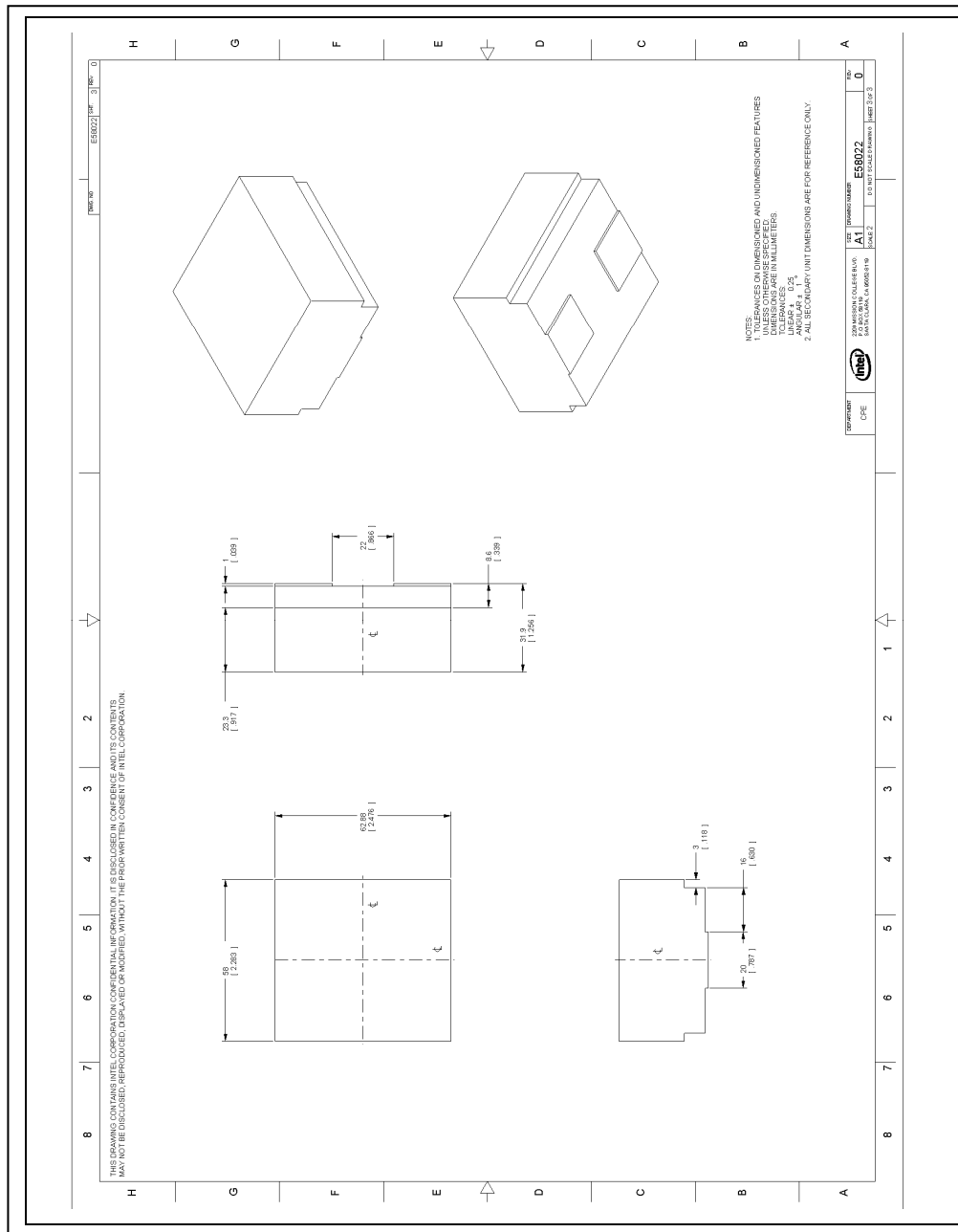
**Figure 20. Intel Atom D400 Series Reference Heatsink (Assembly)**



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**Figure 21. Intel Atom D400 Series Reference Heatsink (P/N: E57774-001)**



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# Appendix B Package Mechanical Drawings

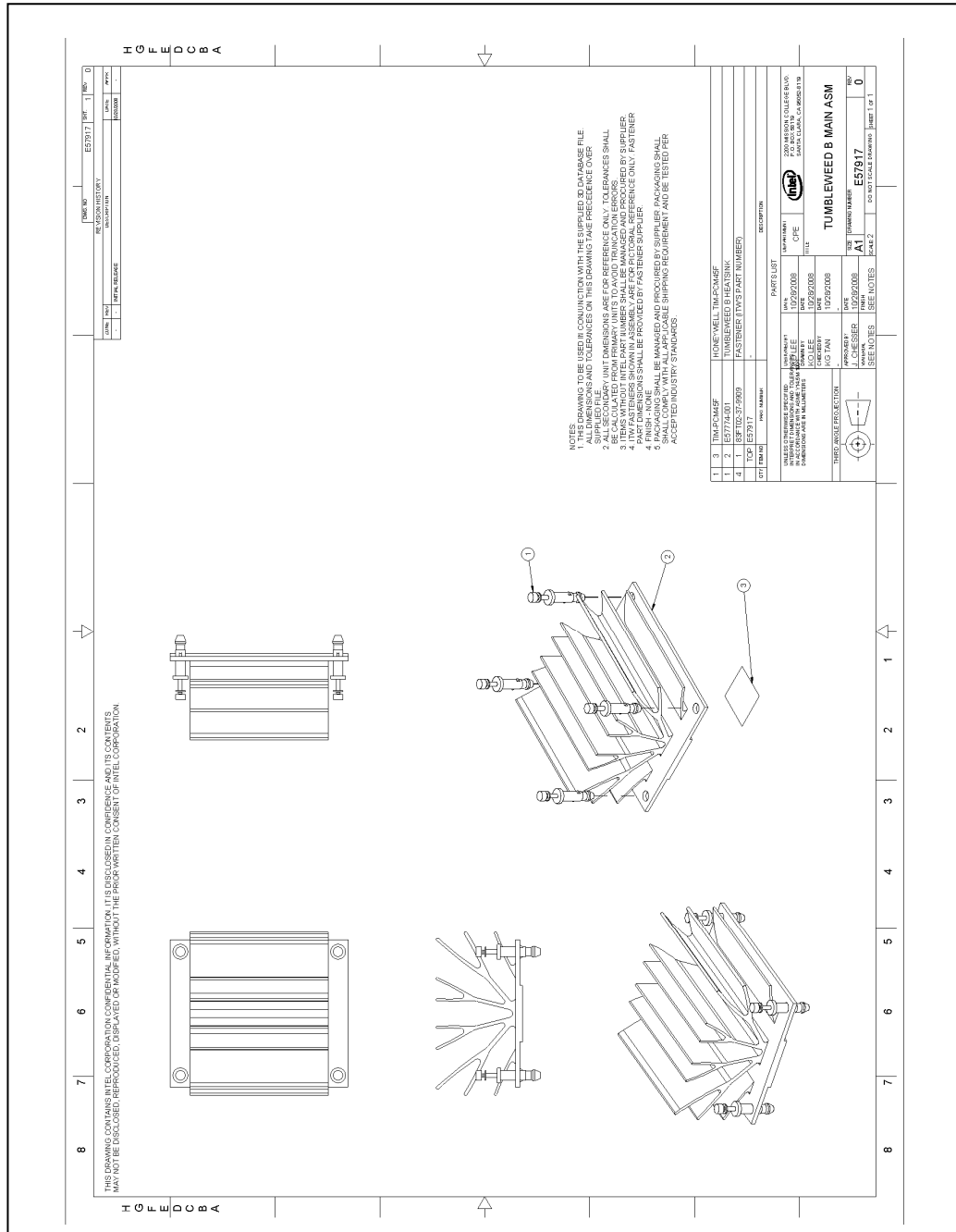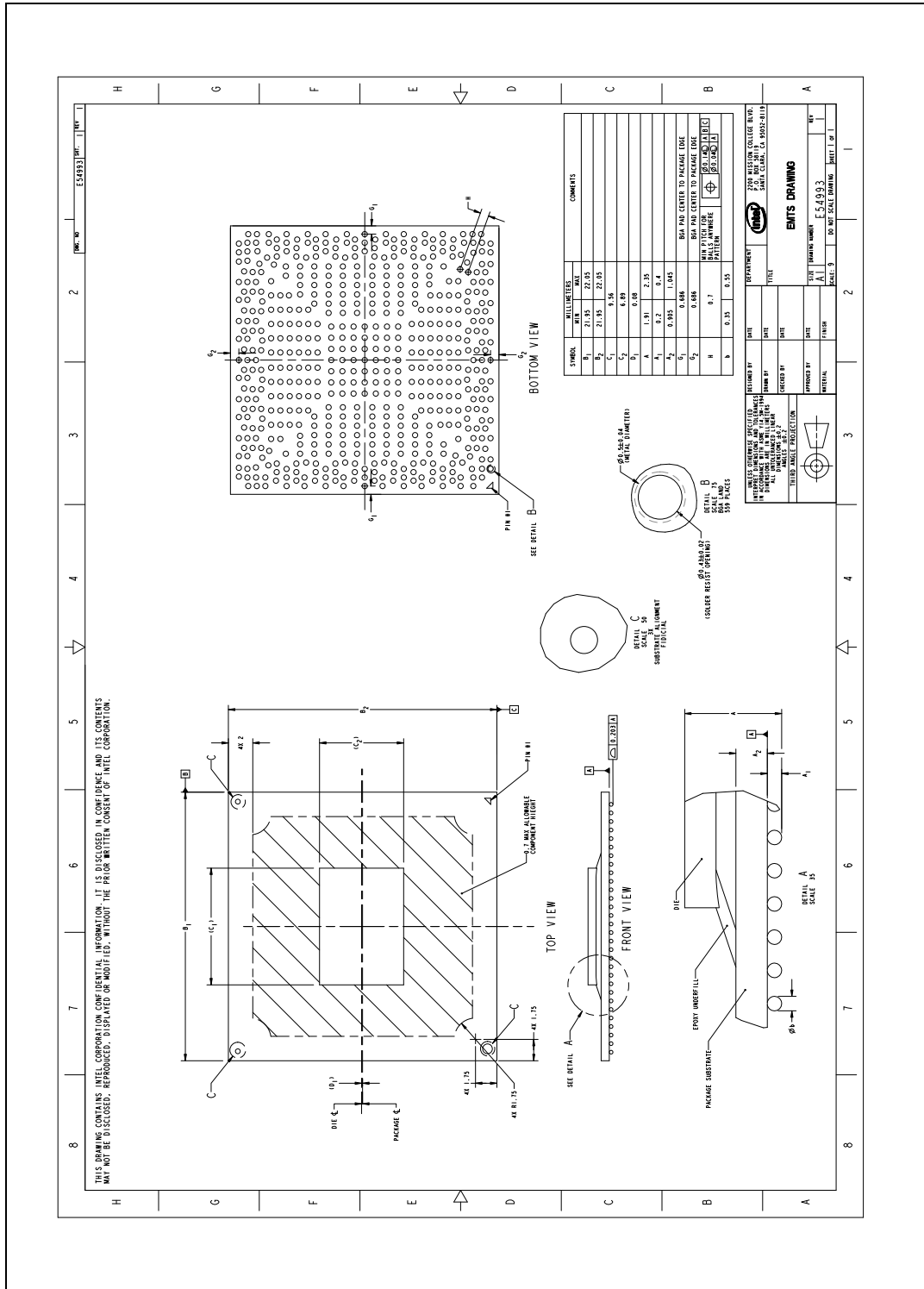Figure 22. Intel Atom D500 Processor Package Drawing

**Figure 23. Intel Atom D400 Processor Package Drawing**

# *Appendix C Heatsink Retention Load Metrology*

## C.1     Overview

The primary objective of the preload measurement is to ensure the preload designed into the retention mechanism is able to meet minimum and does not violate the maximum specifications of the package. (Please refer to section 2.)

## C.2     Test Preparation

### C.2.1     Heatsink Preparation

The following components are required to validate a generic fastener solution:

1.  Thermal solution heatsink (for example, PN: E51968-001 for Intel Atom D500 series)
2.  Fastener (for example, ITW PN: 83FT02-37-9909 for Intel Atom D500 series)
3.  Customized top plate to allow fastener attachment and package simulator

### C.2.2     Typical Test Equipment

For the heatsink clip load measurement, the equivalent test equipments on the following list works as a reference.

**Table 9. Typical Test Equipment**

| Item | Description | Part Number (Model) |
|---|---|---|
| Load cell<br>Notes: 1, 5 | • Honeywell*-Sensotec* Model 13 subminiature load cells, compression only<br><br>• Select a load range depending on load level being tested.<br><br>• www.sensotec.com | AL322BL |
| Data Logger (or scanner)<br><br>Notes: 2, 3, 4 | Vishay* Measurements Group Model 6100 scanner with a 6010A strain card (one card required per channel). | Model 6100 |

| Item | Description | Part Number (Model) |
|------|-------------|---------------------|
| Clip Force Measurement machine<br><br>Notes: 654 | Customized machine that houses load cell for force measurement. Top side plate can be modified to accommodate various attach pattern | CFM-001<br><br>(Cool Star Technology) |

**NOTES**:
1.   Select load range depending on expected load level. It is usually better, whenever possible, to operate in the high end of the load cell capability. Check with your load cell vendor for further information.
2.   Since the load cells are calibrated in terms of mV/V, a data logger or scanner is required to supply 5 volts DC excitation and read the mV response. An automated model will take the sensitivity calibration of the load cells and convert the mV output into pounds.
3.   With the test equipment listed above, it is possible to automate data recording and control with a 6101-PCI card (GPIB) added to the scanner, allowing it to be connected to a PC running LabVIEW* or Vishay's StrainSmart* software.
4.   **IMPORTANT**: In addition to just a zeroing of the force reading at no applied load, it is important to calibrate the load cells against known loads. Load cells tend to drift. Contact your load cell vendor for calibration tools and procedure information.
5.   When measuring loads under thermal stress (bake for example), load cell thermal capability must be checked, and the test setup must integrate any hardware used along with the load cell. For example, the Model 13 load cells are temperature compensated up to 71°C, as long as the compensation package (spliced into the load cell's wiring) is also placed in the temperature chamber. The load cells can handle up to 121°C (operating), but their uncertainty increases according to 0.02% rdg/°F.
6.   Clip force measurement machine is recommended to be calibrated before usage. Standard weights should be used to check for preload cell accuracy and consistency.

# C.3     Test Procedure Examples

The following procedure is for a generic fastener solution using the clip force measurement machine at room temperature:

1.   Prepare and then fasten top plate onto the clip force measurement machine. Place package simulator on top of the preload cell as well.

2.   Place the heatsink (remove any TIM material) on top of the package simulator. Power on the clip force measurement machine.

3.   Install the fasteners and record down the measured preload. Make sure measurement is taken after the reading stabilized. Remove all fasteners and repeat 2 times (in total 3 times) to ensure consistency.

4.   Repeat step4 for remaining fastener samples. Recommended minimum samples are 10 sets of fastener samples.

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# *Appendix D Thermal Solution Supplier Information*

This appendix includes supplier information for Intel enabled vendors.

Following Table 10 lists the suppliers who can provide the processor reference thermal solution components. The part numbers listed below identifies these reference components. End-users are responsible for the performance verification of the Intel enabled component offerings with the supplier. OEMs and System Integrators are responsible for thermal, mechanical, and environmental validation of these solutions.

**Table 10. Reference Thermal Solution enabled components**

| Item | Intel® Part Number | CCI PN | ITW PN |
|------|--------------------|--------|--------|
| Intel Atom D500 Series reference heatsink | E51968-001 | E51968-001 | N/A |
| Intel Atom D400 Series reference heatsink | E57774-0001 | E57774-0001 | N/A |
| Fastener | 83FT02-37-9909 | N/A | 83FT02-37-9909 |

**Table 11. Supplier Contact Information**

| Supplier | Contact | Phone | Email |
|----------|---------|-------|-------|
| CCI | Monica Chih | +886-2-2995-2666 | monica_chih@ccic.com.tw |
| ITW | Perry Lo | +886-7-8119206 ext. 17 | perry@itwasia.com.tw |

These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

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