Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478)

Design Guidelines

October 2001

Order Number: 249890-002

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1. Introduction

1.1. Objective

This document defines a surface mount, ZIF (Zero Insertion Force) socket intended for performance and value desktop platforms based on future Intel microprocessors. The socket provides I\O, power and ground contacts. The 478 socket contacts with a cavity in the center of the socket. The socket has solder balls/surface mount features for surface mounting with the motherboard. The mPGA478 socket contacts have 50mil pitch with regular pin array, to mate with a 478-pin processor package.

1.2. Purpose

To define functional, quality, reliability, and material (that is, visual, dimensional and physical) requirements and design guidelines mPGA478 Socket in order to develop a low cost, low risk, robust, HVM (High Volume Manufacturable) socket solution available from multiple sources.

1.3. Scope

This design guideline applies to all mPGA478 sockets purchased to the requirements of this design guideline.

2. Assembled Component and Package Description

Information provided in this section is to ensure dimensional compatibility of the socket and actuation mechanism with the integrated package assembly. Zero insertion force will be required for placement of the mPGA478 package into the socket prior to actuation.

2.1. Assembled Component Description

The assembled component may consist of a heatsink, EMI, Clips, Fan, RM (retention mechanism), and processor. Specific details can be obtained from the Intel® Pentium® 4 Processor in 478-Pin Package Thermal Design Guidelines, consult your Intel field representative to obtain this document. The heatsink will be statically loaded onto the package after the package is mated with the socket and actuated. For mechanical details refer to Section 3 –*Mechanical Requirements*.

2.2. Package Description

The outline of the package that can be used with mPGA478 Socket is illustrated in Section 7 – *Appendix Z.1*. It will contain a 26 x 26 array of pins (with a center cavity gap of a 14 x14 array of pins) contained in a substrate that is 36.5 mm x 36.5 mm maximum. The pin length is 2.03 mm nominal.

3. Mechanical Requirements

3.1. Mechanical Supports:

The socket must carry a load of 45.36Kg, compressive, during the shock and vibration conditions outlined in Section 5. The socket must pass the mechanical shock and vibration and the other use condition requirements listed in Section 5 with the associated heatsink and applicable retention mechanism or simulation thereof in place and with out board support. The socket can only be attached by the socket contacts to the motherboard. No external methods (i.e. screw, extra solder, adhesive....) to attach the socket are acceptable

3.2. Materials

3.2.1. Socket Housing

Thermoplastic or equivalent, UL 94V-0 flame rating, temperature rating and design capable of withstanding reflow solder process. The material must have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high operating temperature, mounted on FR4-type motherboard material.

3.2.2. Color

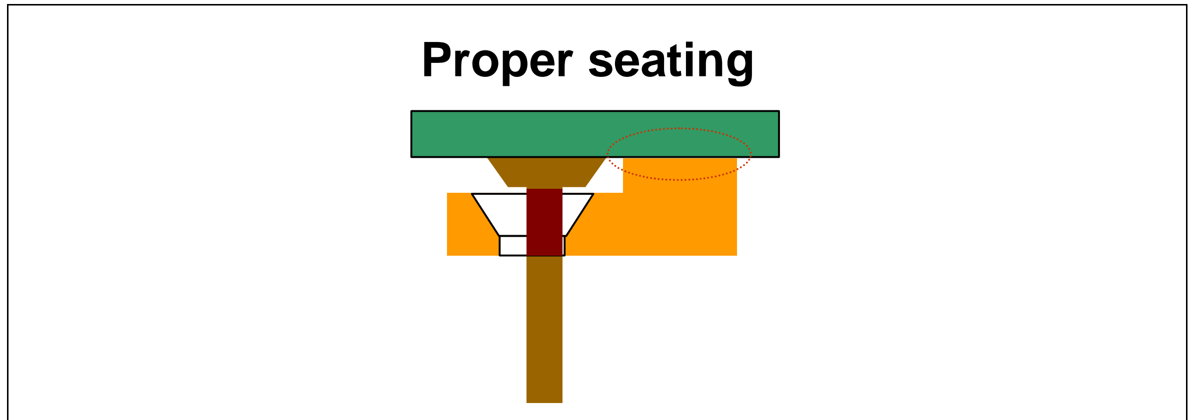
The color of the socket can be optimized to provide the contrast needed for OEM's pick and place vision systems. The base and cover of the socket may be different colors as long as they meet the above requirement.

3.2.3. Cutouts For Package Removal

Recessed cutouts are required in the side of the socket to provide better access to the package substrate, and facilitate the manual removal of inserted package. (See attached socket drawing Section 8 – *Appendix Z.2*).

3.2.4. Socket Standoff Height

Socket stand off height, cover lead in and cover lead in depth must not interfere with package pin shoulder height at worst case conditions. (See Figure 7-4– *Appendix Z.1* for the package solder fillet dimensions.)



3.3. Markings

3.3.1. Name

mPGA478 (Font size is 8-14 point Bold, Font type is Helvetica) on all development mPGA478 sockets.

Manufacturer's insignia (font size at supplier's discretion).

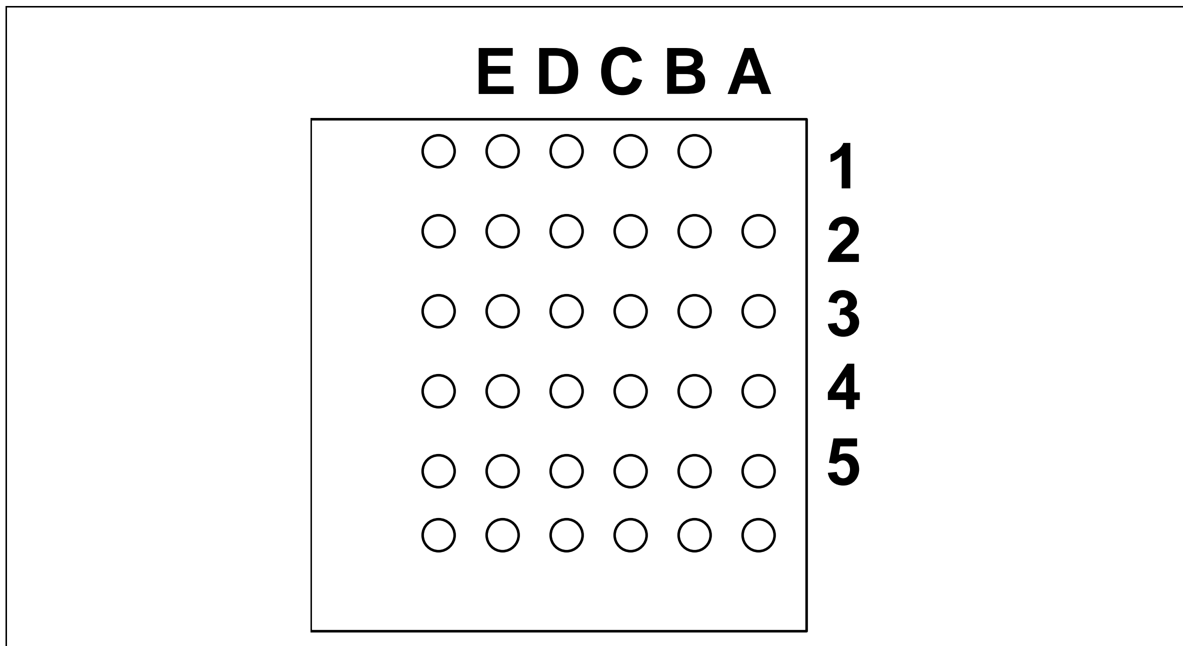
These marks will be molded or laser marked into the socket housing and must pass Environmental Requirements of Section 5.3 – *Solvent Resistance*. Any requests for variation from this marking requires a written description (detailing size and location) to be provided to Intel for approval.

3.3.2. Mechanical Keying Map and Markings For mPGA478 Sockets

mPGA478X (Font size is 8-14 point Bold, Font type is Helvetica) First X= Pin count second X= Version. This shall be on all relative products.

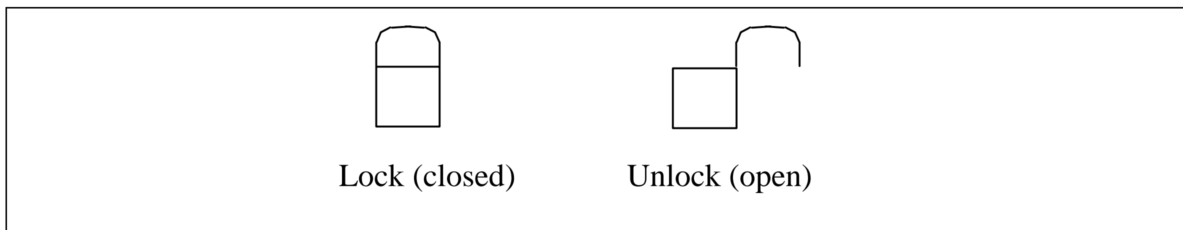
(Example – Version C product shall have mPGA478C)

Version	Depopulated Pins	Name
A	A1, A2	mPGA478A
B	A1, B1	mPGA478B
C	A1, B2	mPGA478C



3.3.3. Lock (closed) and Unlock (open) Markings

For lock an unlock positions on the socket they are to be marked with the universal symbol of the locked and unlocked pictures. Clear indicator marks must be located on the actuation mechanism that identifies the lock (closed) and unlock (open) positions of the cover as well as the actuation direction. These marks should still be visible after a package is inserted into the socket.



3.3.4. Lot Traceability

Each socket will be marked with a part number and lot identification code that will allow traceability of all components, date of manufacture (year and week), and assembly location. This mark can be an ink mark or a laser mark but must be able to pass Environmental Requirements of Section 5 – *Environmental Requirements*. The mark must be placed on a surface that is visible when mounted on a printed circuit board. In addition, this identification code must be marked on the exterior of the box in which the units ship.

3.3.5. Socket Size

The mPGA478 Socket must meet the dimensions as shown in Section 8 – *Appendix Z.2*, including actuation mechanism, allowing insertion of the pins in the socket, without interference between the socket and the pin field. The processor must sit flush on the socket standoffs and the pin field cannot contact the standoffs. The height of the socket in the contact area is 4mm +/- 0.2mm post SMT; this height is from the motherboard to the top of the socket contact surface.

3.3.6. Socket / Package Translation during Actuation

The Socket will be built so that the post-actuated package pin to motherboard pad distance (Y-axis) is in the range of 0.30mm to 0.71mm. Movement will be along Y direction (refer to axes as indicated in Section 8 – *Appendix Z.2*), and will be away from the point of actuation. No Z-axis travel (lift-out) of the package is allowed during actuation.

3.3.7. Orientation in Packaging

Packaging media needs to support high volume manufacturing.

3.4. Contact Characteristics

3.4.1. Number of Contacts

Total number of contacts: 478

3.4.2. Base Material

High strength copper alloy.

3.4.3. Contact Area Plating

Contact area plating consists of 0.762mm (30min) (min) gold plating over 1.27mm (50min) (min) nickel underplate in critical contact areas (area on socket contacts where processor pins will mate). No contamination by solder in the contact area is allowed during solder reflow.

3.4.4. Solder Ball/Surface Mount Feature Characteristics

Solder ball material of Tin/Lead (either 63/37 or 60/40)

3.4.5. Lubricants

For the final product, no lubricants shall be allowed on the socket contacts. If lubricants are used elsewhere within the socket assembly, these lubricants must not be able to migrate to the socket contacts.

3.5. Material and Recycling Requirements

Cadmium shall not be used in the painting or plating of the socket.

CFCs and HFCs shall not be used in manufacturing the socket. It is recommended that any plastic component exceeding 25g must be recyclable as per the European Blue Angel recycling design guidelines.

3.6. Socket Manufacturability Requirements

The mPGA478 Socket must be a surface mount socket design; double-sided reflow capability is not required.

3.7. Overall Assembly Sequence

1. Mount socket to motherboard using a surface mount process.
2. Place retention mechanism (if required) around socket and secure to motherboard.
3. Insert package into socket.
4. Actuate socket using lever.
5. Load heat sink onto package and secure.

3.8. Socket Engagement/Disengagement Force

The force on the actuation lever arm must not exceed 4.5Kg to engage or disengage the package into the 478 Pin Socket. Movement of the cover limited to the plane parallel to the motherboard. The processor package must not be utilized in the actuation of the socket.

3.9. Visual Aids

The socket top will have markings identifying open and closed positions for the actuation lever arm.

The socket top will have markings identifying Pin 1. This marking will be represented by a symbol and/or the socket will have a notched feature identifying Pin 1. Section 8 – *Appendix Z.2* – identifies the location of the Pin 1 identifying mark.

3.10. Equipment Pick and Place

The socket must be capable of being used in a high-volume manufacturing environment. A pick and place solution is required with the following options recommended for vacuum pick and place: Flat cover attached to socket, tape attached to socket, or addition of flat plastic on socket for vacuum cup pick up. The preferred pick and place solution is to use the socket housing without added features.

3.11. Socket BGA Co-Planarity

203 mm coplanarity maximum over the entire ball field (this requirement includes all balls/surface mount feature on the underside of the socket).

3.12. Solder Ball/Surface Mount Feature True Position

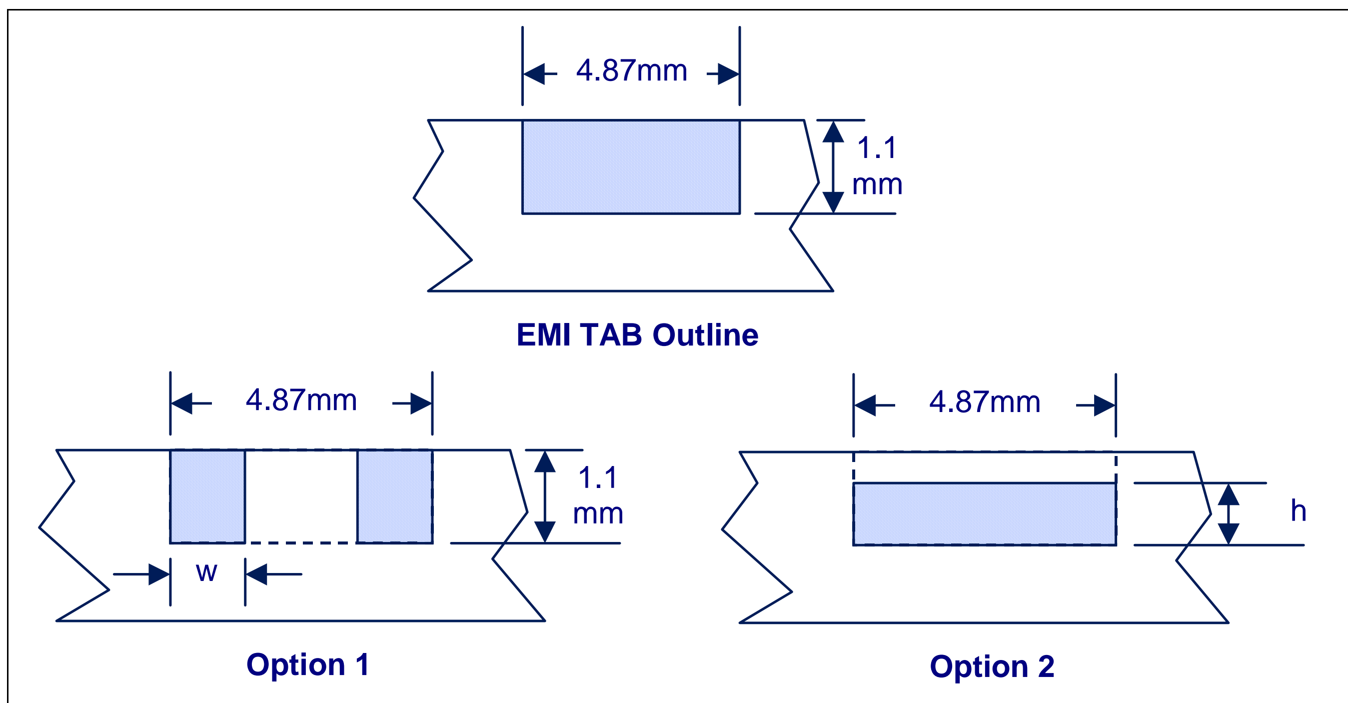
The solder balls/surface mount features have a 254 mm diametrical true position requirement with respect to Datum. See Section 8 – *Appendix Z.2*.

3.13. EMI Tab Socket Requirements

The principal functionality of the EMI Tab is a potential locating feature by which the EMI ground frame component could be assembled to the socket prior to heat sink installation. The socket EMI Tab shall retain EMI component through environmental testing.

3.13.1. Tab Size

Material MUST be maintained in the two lower corners of the rectangular cross-section. w = 1.5 mm MIN or, h = 0.5 mm MIN See Section 8 – *Appendix Z.2* – for location on the socket.



3.13.2. Tab Shape

The shape of the two lower corners must be square (radius 0.76 max allowed) Vendors may modify the geometry in one of the following ways (NOT BOTH):

1. Introducing a vertical channel located exactly at the CL of the socket so long as the resulting tabs have a minimum width of 1.5 mm
2. Shortening the height of the rectangle to a minimum of 0.5 mm (with the caveat that this will affect the lead-in angle of the tab and may significantly increase the assembly force when installing the EMI component).

3.14. Assembly Requirements to the Motherboard

3.14.1. Surface Mountable

The socket must be a surface mount socket design.

3.14.2. Reflow Characteristics

Max Temperature: 240°C

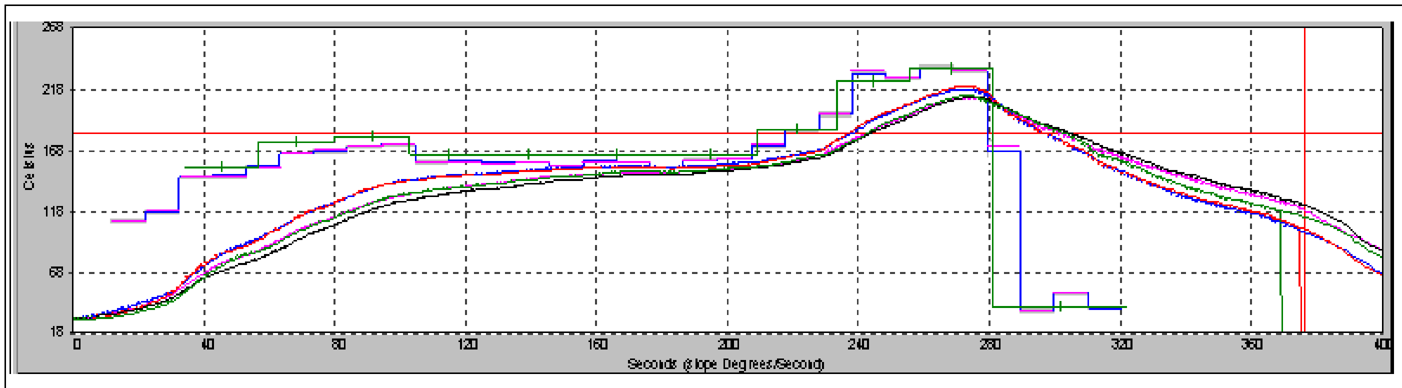


Figure 3-1. Typical Reflow Profile for 63Sn/37Pb solder

3.14.3. Shipping/Handling:

Shipping/Handling media needs to support high volume manufacturing.

3.15. Critical To Function Dimensions:

The socket shall accept a 478-pin package pin field. All dimensions are metric; English units are shown for reference only. mPGA478 Socket dimensions are shown in Section 8 – *Appendix Z.2*.

Each of the dimensions must meet the requirements given in Table 3-1 – *Socket Critical to Function Dimensions*. These dimensions will be verified as part of the validation process. Also, supplier will provide and maintain Critical Process Parameters controlling these CTFs or will provide direct measurements to meet ongoing quality requirements.

Note: If for any reason there is a conflict between this table and the drawing, the drawing is correct.

Table 3-1. Socket Critical to Function Dimensions

Dimension	Minimum	Nominal	Maximum
Socket height beneath package (post reflow, from contact surface to motherboard)	3.8 mm	4.0 mm	4.2 mm

Dimension	Minimum	Nominal	Maximum
Cam Height Above Substrate Shelf (from contact surface to top surface of socket)			1.5 mm
Socket overall width (X without lever)	36.8mm	37mm	37.2 mm
Socket overall length (Y without lever)			45 mm
Post actuated pin to motherboard pad distance (Y)	0.30 mm		0.71 mm
Assembled Cover Flatness			0.20 mm
Cover Standoff height	0.25mm[1]	0.30mm[1]	0.35mm[1]
Co-planarity — Lead / Surface Mount Feature — Solder Ball			 0.15 mm 0.20 mm
Solder Ball/lead Diametrical True Position — Pattern Locating — Feature Relating			 0.406 mm 0.25 mm
Gold plating thickness	0.762µm (30µin)		
Nickel plating thickness	1.27µm (50µin)		
Cover Hole Diameter	Design Specific		Design Specific
Cover Hole Virtual Condition (Pattern Locating) Guarantee ZIF condition	Design Specific[1]		
Cover Hole Virtual Condition (Feature Relating) Guarantee ZIF condition	Design Specific[1]		
Cover Hole Lead in Diameter	Design Specific[1]	Design Specific[1]	Design Specific[1]
Cover Hole Lead in Depth	Design Specific[1]	Design Specific[1]	Design Specific[1]
Contact Gap	Design Specific	Design Specific	Design Specific
Contact True Position	Design Specific	Design Specific	Design Specific
Contact Inner Loop TP	Design Specific	Design Specific	Design Specific
Contact Pin Acceptance Inscribed Circle	Design Specific	Design Specific	Design Specific
Contact Angle	Design Specific	Design Specific	Design Specific
Base Flatness	Design Specific	Design Specific	Design Specific
Through Cavity Y (in open and closed position)	15.05 mm		Design Specific
Through Cavity X (in open and closed position)	15.05 mm		Design Specific
Socket overall width, including lever			41 mm

NOTES:

1. See 3.2.4 – *Socket Standoff Height*

Manufacturer is required to monitor these critical to function (CTF) parameters as a part of on-going Quality Control.

4. Electrical Requirements

In order to meet the performance requirements, the socket must meet the following electrical requirements listed in Table 4-1 – *Electrical Requirements*. These parameters are determined to be a unique function of the socket geometry and material property and correctly define the socket electrical characteristics. The definitions for these are given in Table 4-2, and the details for the measurement procedure to achieve these values are listed in the following sections.

4.1. Electrical Requirements

Table 4-1. Electrical Requirements

Item	Parameter	Limit	Note
1.	Mated loop inductance, Lloop	<3.3nH	
2.	Maximum mutual capacitance, C	≤ 1.1 pF	Refer to Section 4.2 – *Definitions*
3.	Final mated connection resistance for Kovar pin daisy chain Package Test Vehicle (average of minimum 40 pin/connector mated connections)	≤ 25 mΩ	
	Final mated connection resistance for Cu alloy pin daisy chain Package Test Vehicle (average of minimum 40 pin/connector mated connections)	≤ 17 mΩ	
4.	Socket minimum current rating @ 1.0A	Read and Record	Testing shall be measured per EIA 364, Test Procedure 70, Method 1.
5.	Pin-to-Pin/Connector-to-Connector insulation resistance (min)	> 800 MΩ	Insulation resistance shall be a minimum requirement of 800MΩ as measured per EIA 364, Test Procedure 21
6.	Measurement frequency for Pin-to-Pin/Connector-to-Connector capacitance.	400 MHz	
7.	Measurement frequency(s) for Pin-to-Pin/Connector-to-Connector inductance.	1GHz	

4.2. Definitions

Table 4-2. Electrical Definitions

Item	Parameter	Definition
1.	Mated loop inductance, Lloop	The inductance calculated for two conductors, considering one forward conductor and one return conductor.
2.	Maximum mutual capacitance, C Refer to Section 4.2 – *Definitions*	The capacitance between two pins/connectors.
3.	Final mated connection resistance (average of minimum 40 pin/connector connections)	This is the final resistance after any environmental and/or shock & vibration testing. The final mated connection resistance specifications listed in Table 4-1 must be met for either the Kovar or Cu alloy pin daisy chain Package Test Vehicle. **Socket:** The resistance of the socket contact, interface resistance to the pin, and the entire pin to the point where the pin enters the package; gaps included.
4.	Measurement frequency(s) for capacitance.	Capacitively dominant region. This is usually the lowest measurable frequency. This should be determined from the measurements done for the feasibility.
5.	Measurement frequency(s) for inductance.	Linear region. This is usually found at higher frequency ranges. This should be determined from the measurements done for the feasibility.

4.3. Socket Electrical Characterization

Socket electrical requirements are measured from the socket-seating plane of the package to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket pin, but includes effects of adjacent pins where indicated. Pin and socket inductance includes exposed pin from mated contact to bottom of the processor pin field.

4.4. Electrical Resistance

Figure 4-1 and Figure 4-2 (*below*) show the proposed methodology for measuring the final electrical resistance. The methodology requires measuring package Test vehicle (PTV) flush-mounted directly to the motherboard fixtures, so that the pin shoulder is flush with the motherboard, to get the averaged jumper resistance, R_{jumper}. The R_{jumper} should come from a good statistical average of 30 PTV fixtures flush mounted to a motherboard fixture. The same measurements are then made with an PTV fixture mounted on a supplier's socket, and both are mounted on a motherboard fixture; this provides R_{Total}. The resistance requirement, R_{Req}, can be calculated for each chain as will be explained later.

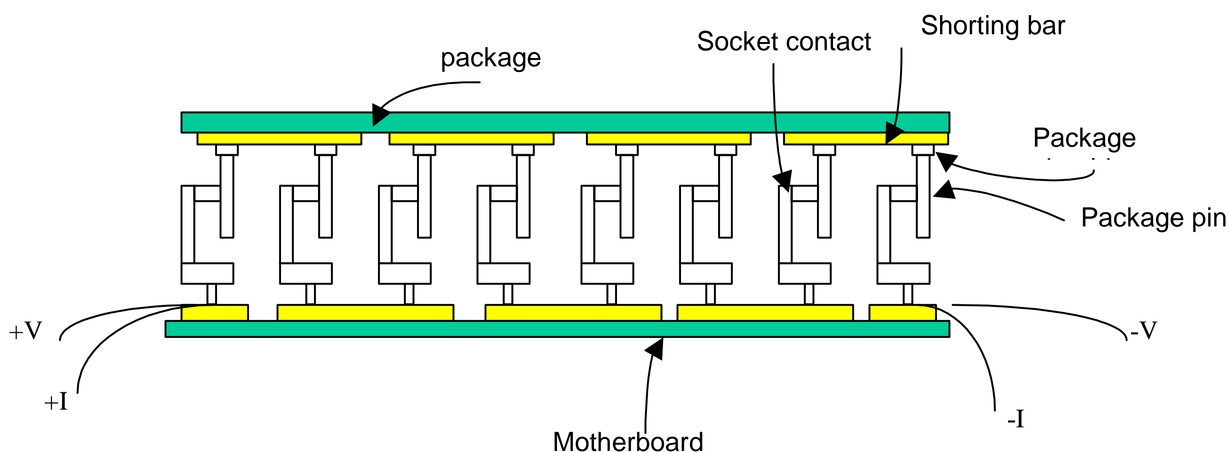


Figure 4-1. Methodology for Measuring Total Electrical Resistance

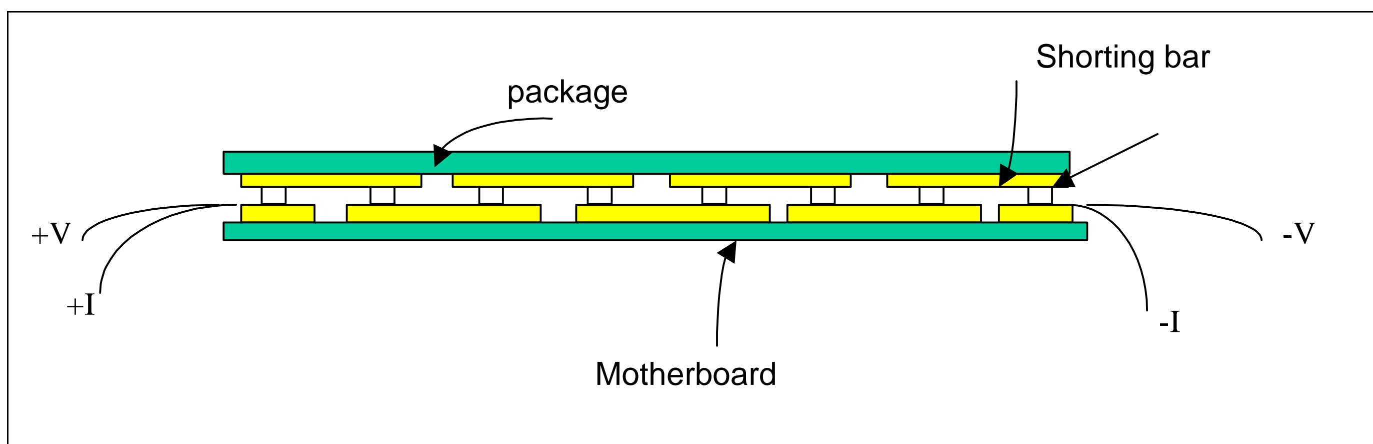


Figure 4-2. Methodology for Measuring Electrical Resistance of the Jumper

Four types of jumpers (Type A, B1, B2 and PJRC) are used in the Package test vehicle (PTV) and are shown in Figure 4-3 (*below*). The mean of Rjumper is therefore different for each type in the calculation of the single pin resistance (See below for calculating single pin resistance).

Figure 4-3. Four Different Jumpers Used in the Package Test Vehicle

Figure 4-4 (*below*) shows the physical locations (Pin side view) of the four types of jumpers in the Package test vehicle. Care must be taken to make sure that the correct value of R_{jumper} (mean) is subtracted from the daisy chains type (A, B1 or B2).

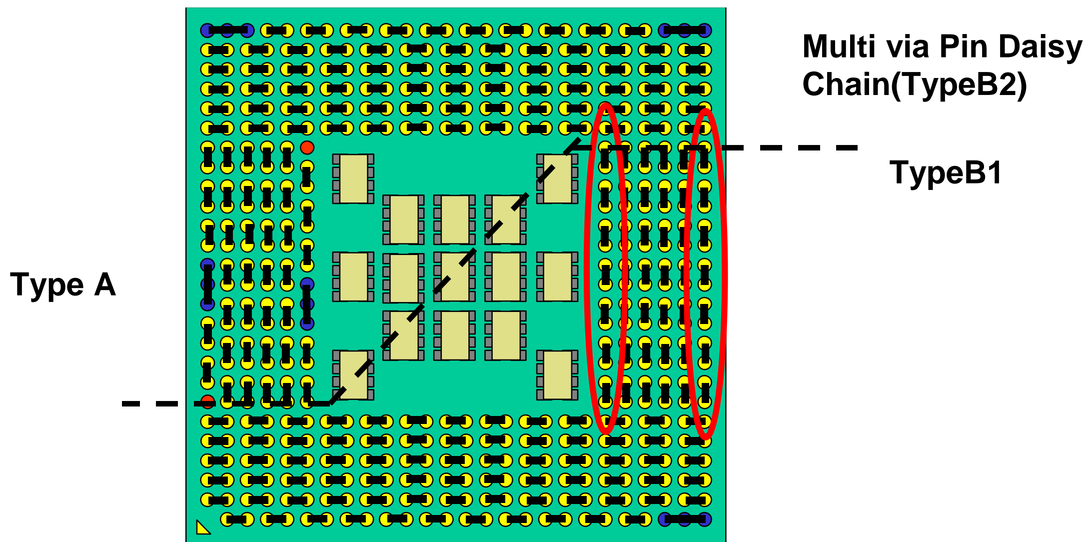


Figure 4-4. Location of type A, B1, B2 and PJRC daisy chains from pin side of PTV

Figure 4-3 – *Four Different Jumpers Used in the Package Test Vehicle* – shows the top view of the test vehicle (Concho) that will be used for resistance measurement. There are 36 daisy chain configurations on resistance test board. Table 4-3 shows these configurations with the number of pins per each chain and netlist.

Figure 4-5. Electrical Resistance test vehicle top view

Table 4-3. Socket Positions Daisy Chained

Chain No.	Socket Positions Daisy Chained	# of pins/chain	DC Endpoints at Socket		Edge Finger: Hi		Edge Finger: Low	
			Hi	*Low*	*+I*	*+V*	*-I*	*-V*
1	A13-A14, A15-A16, A17-A18, A19-A20, A21-A22, A23-A24	12	A13	A26	A125	A126	A101	A102
2	B14-B15, B16-B17, B18-B19, B20-B21, B22-B23, B24-B25	14	B13	B26	A123	A124	A99	A100
3	C14-C15, C16-C17, C18-C19, C20-C21, C22-C23, C24-C25	14	C13	C26	A121	A122	A97	A98
4	D14-D15, D16-D17, D18-D19, D20-D21, D22-D23, D24-D25	14	D13	D26	A119	A120	A95	A96
5	E14-E15, E16-E17, E18-E19, E20-E21, E22-E23, E24-E25	14	E13	E26	A117	A118	A93	A94
6	F14-F15, F16-F17, F18-F19, F20-F21, F22-F23, F24-F25	14	F13	F26	A115	A116	A91	A92
7	H21-J21, K21-L21, M21-N21, P21-R21, T21-U21, V21-W21	14	G21	Y21	A113	A114	A89	A90
8	H22-J22, K22-L22, M22-N22, P22-R22, T22-U22, V22-W22	14	G22	Y22	A111	A112	A87	A88
9	H23-J23, K23-L23, M23-N23, P23-R23, T23-U23, V23-W23	14	G23	Y23	A109	A110	A85	A86
10	H24-J24, K24-L24, M24-N24, P24-R24, T24-U24, V24-W24	14	G24	Y24	A107	A108	A83	A84
11	H25-J25, K25-L25, M25-N25, P25-R25, T25-U25, V25-W25	14	G25	Y25	A105	A106	A81	A82
12	H26-J26, K26-L26, M26-N26, P26-R26, T26-U26, V26-W26	14	G26	Y26	A103	A104	A79	A80
13	NOT USED				A51	A52	A77	A78
[1]14	Pin Joint Resistance Circuit	[1]not defined	M1	P1	A49	A50	A75	A76
[1]15	Pin Joint Resistance Circuit	[1]not defined	L6	N6	A47	A48	A73	A74
[1]16	Pin Joint Resistance Circuit	[1]not defined	A26	A24	A45	A46	A71	A72
17	NOT USED				A43	A44	A69	A70
[1]18	Pin Joint Resistance Circuit	[1]not defined	AF24	AF26		A42		A68
[1]19	Pin Joint Resistance Circuit	[1]not defined	AF1	AF3		A40		A66
20	AA14-AA15, AA16-AA17, AA18-AA19, AA20-AA21, AA22-AA23, AA24-AA25	14	AA13	AA26	A37	A38	A63	A64
21	AB14-AB15, AB16-AB17, AB18-AB19, AB20-AB21, AB22-AB23, AB24-AB25	14	AB13	AB26	A35	A36	A61	A62
22	AC14-AC15, AC16-AC17, AC18-AC19, AC20-AC21, AC22-AC23, AC24-AC25	14	AC13	AC26	A33	A34	A59	A60

Chain No.	Socket Positions Daisy Chained	# of pins/chain	DC Endpoints at Socket		Edge Finger: Hi		Edge Finger: Low	
			Hi	*Low*	*+I*	*+V*	*-I*	*-V*
23	AD14-AD15, AD16-AD17, AD18-AD19, AD20-AD21, AD22-AD23, AD24-AD25	14	AD13	AD26	A31	A32	A57	A58
24	AE14-AE15, AE16-AE17, AE18-AE19, AE20-AE21, AE22-AE23, AE24-AE25	14	AE13	AE26	A29	A30	A55	A56
25	AF13-AF14, AF15-AF16, AF17-AF18, AF19-AF20, AF21-AF22, AF23-AF24	12	AF13	AF26	A27	A28	A53	A54
26	A3-A4, A5-A6, A7-A8, A9-A10, A11-A12	12	A13	A2	A125	A126	A149	A150
27	B2-B3, B4-B5, B6-B7, B8-B9, B10-B11, B12-B13	12	B13	B1	A123	A124	A147	A148
28	C2-C3, C4-C5, C6-C7, C8-C9, C10-C11, C12-C13	12	C13	C1	A121	A122	A145	A146
29	D2-D3, D4-D5, D6-D7, D8-D9, D10-D11, D12-D13	12	D13	D1	A119	A120	A143	A144
30	E2-E3, E4-E5, E6-E7, E8-E9, E10-E11, E12-E13	12	E13	E1	A117	A118	A141	A142
31	F2-F3, F4-F5, F6-F7, F8-F9, F10-F11, F12-F13	12	F13	F1	A115	A116	A139	A140
32	NOT USED					A114		A138
						A113		A137
33	NOT USED					A112		A136
						A111		A135
34	NOT USED					A110		A134
						A109		A133
35	NOT USED					A108		A132
						A107		A131
36	NOT USED					A106		A130
						A105		A129
37	NOT USED					A104		A128
						A103		A127
38	NOT USED					A52		A2
						A51		A1
[1]39	H6-J6, K6-L6, N6-P6, R6-T6, U6-V6	12	G6	W6		A50		A26
[1]40	H5-J5, K5-L5, M5-N5, P5-R5, T5-U5, V5-W5	14	G5	Y5		A48		A24
[1]41	H4-J4, K4-L4, M4-N4, P4-R4, T4-U4, V4-W4	14	G4	Y4		A46		A22

Chain No.	Socket Positions Daisy Chained	# of pins/chain	DC Endpoints at Socket		Edge Finger: Hi		Edge Finger: Low	
			Hi	*Low*	*+I*	*+V*	*-I*	*-V*
42	H3-J3, K3-L3, M3-N3, P3-R3, T3-U3, V3-W3	14	G3	Y3		A44		A20
[1]43	H2-J2, K2-L2, M2-N2, P2-R2, T2-U2, V2-W2	14	G2	Y2		A42		A18
[1]44	J1-K1, L1-M1, P1-R1, T1-U1, V1-W1	12	H1	Y1		A40		A16
45	AA2-AA3, AA4-AA5, AA6-AA7, AA8-AA9, AA10-AA11, AA12-AA13	12	AA13	AA1	A37	A38	A13	A14
46	AB2-AB3, AB4-AB5, AB6-AB7, AB8-AB9, AB10-AB11, AB12-AB13	12	AB13	AB1	A35	A36	A11	A12
47	AC2-AC3, AC4-AC5, AC6-AC7, AC8-AC9, AC10-AC11, AC12-AC13	12	AC13	AC1	A33	A34	A9	A10
48	AD2-AD3, AD4-AD5, AD6-AD7, AD8-AD9, AD10-AD11, AD12-AD13	12	AD13	AD1	A31	A32	A7	A8
49	AE2-AE3, AE4-AE5, AE6-AE7, AE8-AE9, AE10-AE11, AE12-AE13	12	AE13	AE1	A29	A30	A5	A6
50	AF3-AF4, AF5-AF6, AF7-AF8, AF9-AF10, AF11-AF12	12	AF13	AF1	A27	A28	A3	A4

NOTES:

1. Pin Joint Resistance Circuit (Figure 4-3 – *Four Different Jumpers Used in the Package Test Vehicle*) – Not the correct set up for 4-wire measurement to define the number of pins.

Daisy chains from Table 4-3 (*above*) are categorized as:

TYPE A Daisy Chain: Chain No. 20,21,22,23,24,25,42,45,46,47,48,49,50.

TYPE B1 Daisy Chain: Chain No. 1,2,3,4,5,6,8,9,10,11,26,27,28,29,30,31.

TYPE B2 Multi Via Pin Daisy Chain: Chain No. 7,12.

Chains 14,15,16,18,19(Pin Joint Resistance circuit), 39,40,41,43,44(TYPE A) are eliminated from the socket electrical validation because the set up for 4-wire measurement is not correct. These are also eliminated in the EOL Q&R test but will be monitored for FA analysis.

4.5. Determination of Maximum Average Resistance

This section provides a guideline for the instruments used to take the measurements.

Note: The instrument selection should consider the guidelines in EIA 364-23A.

a) These measurements use a 4-wire technique, where the instruments provide two separate circuits. One is a precision current source to deliver the test current. The other is a precision voltmeter circuit to measure the voltage drop between the desired points.

b) These separate circuits can be contained within one instrument, such as a high quality micro-ohmmeter, a stand-alone current source and voltmeter, or the circuits of a data acquisition system.

c) Measurement accuracy in W is specified as ± 0.1% of reading, or ± 0.1 mW, whichever is greater. The vendor is responsible for demonstrating that their instrument(s) can meet this accuracy.

d) Automation of the measurements can be implemented by scanning the chains through the edge or cable test connector using a switch matrix. The matrix can be operated by hand, or through software.

e) Measure R_{Total} for each daisy chain of "package + socket + motherboard" unit.

f) Measure R_{jumper} for each daisy chain of 30 "package + motherboard" units. Calculate the mean of R_{jumper} ($\overline{R}_{jumper}$) from 30 measured sandwich units for each daisy chain.

g) For each socket unit, calculate

$$R_{Req} = \frac{R_{Total} - \overline{R}_{jumper}}{N}$$

h) R_{Req} is the average contact resistance for each pin of the socket.

i) N is the number of pins per chains.

j) $R_{jumberBar}$ is the average resistance per chain of 30 measured sandwich units.

4.6. Inductance

Loop inductance of the socket pin is measured from the solder ball side of the socket using a resistance daisy chain test fixture to short the two socket pins as shown in Figure 4-6 (*below*). Figure 4-6 (*below*) shows the inductance measurement fixture cross-section and the inductance measurement methodology. The first figure shows the entire assembly. The second figure shows the assembly without the socket. This is used to calibrate out the fixture contribution. The materials for the fixture must match the materials used in the processor. The probe pads are the solder balls of the socket, and the shorting plane exists on the bottom side of the daisy chain test fixture. The resistance daisy chain test fixture is cut into 24x6 pins configuration and mounted on the socket as shown in Figure 4-7 – *Inductance Fixture Design mounted on the socket*. Loop inductance is measured from the ball side of any two pins that are shorted through a shorting bar of the daisy chain test fixture, as shown in Figure 4-8 – *Test fixture mounted bottom view with the pins cut*.

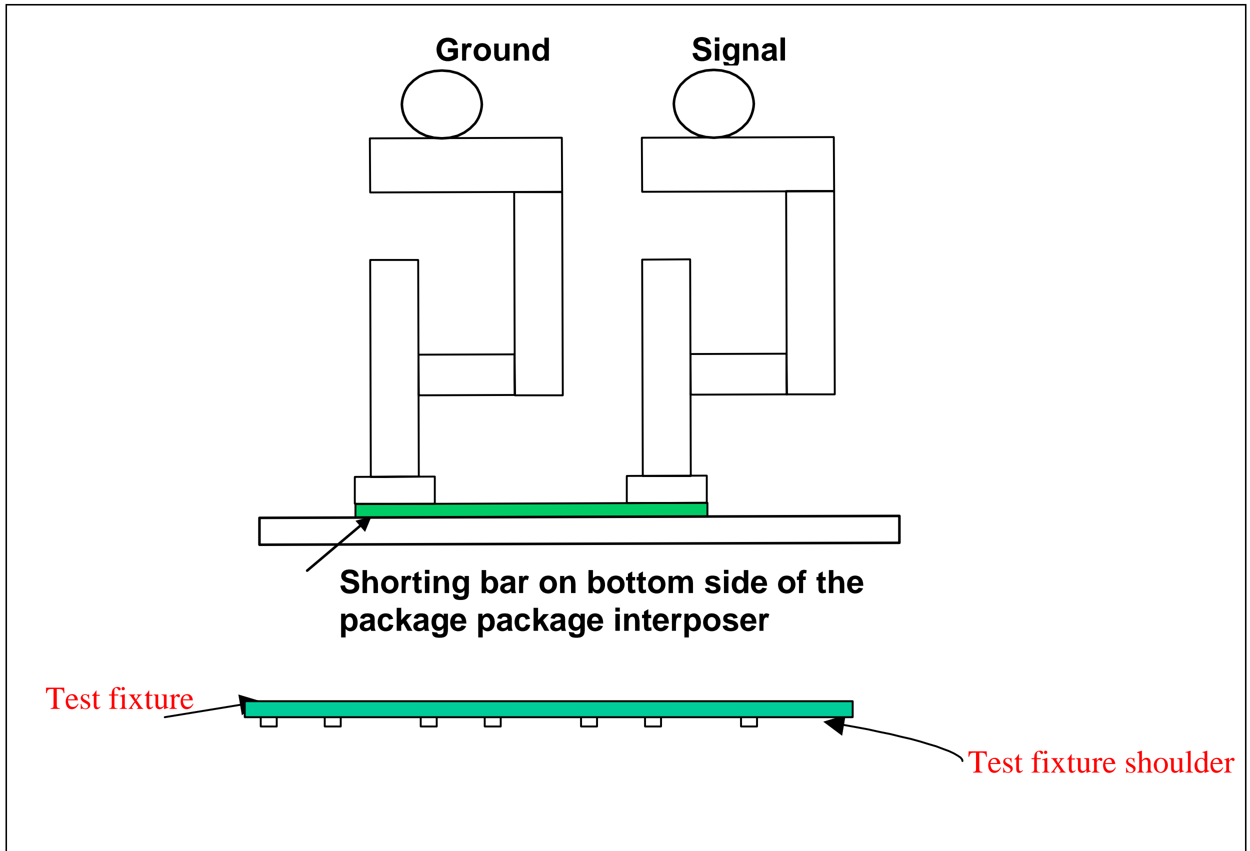


Figure 4-6. Inductance Measurement Fixture Cross-section

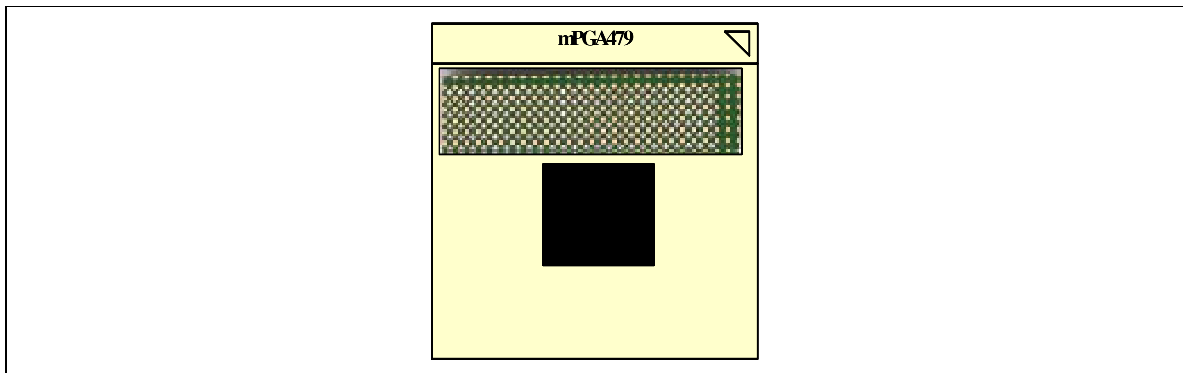


Figure 4-7. Inductance Fixture Design mounted on the socket

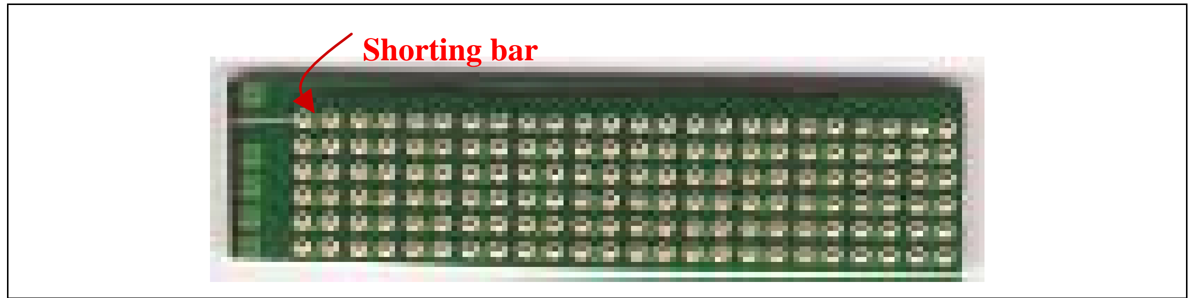


Figure 4-8. Test fixture mounted bottom view with the pins cut

4.6.1. Procedure for Inductance Measurements:

The measurement equipment required to perform the qualification is:

- Equipment - HP8753D Vector Network Analyzer or equivalent
- Robust Probe Station (GTL4040) or equivalent
- Probes - GS1250 & GSG1250 Air-Co-Planar or equivalent
- Calibration – Cascade Calibration Substrates or equivalent
- Measurement objects – Package test vehicles, sockets, motherboards

Measurement Steps:

(a) Equipment setup

(i) Cables should be connected to the network analyzer and to the probes using the appropriate torque wrench to ensure consistent data collection every time the measurement is performed

(b) Set VNA

(i) Bandwidth = 300KHz – 3GHz with 801 points

(ii) Averaging Factor = 16

(c) Perform Open/Short/Load calibration

(i) Calibration should be performed at the start of any measurement session.

(ii) Please refer to Intel Calibration Document

(iii) Create Calibration Kit if necessary for 1st time

(iv) Do not perform port extension after calibration

(d) Check to ensure calibration successfully performed

(e) Measure the inductance by probing on the solder ball side of the socket with the test fixture mounted on it. (Figure 4-6 – *Inductance Measurement Fixture Cross-section*).

(i) Call this $L_{\text{socket assembly}}$.

(ii) Export data into MDS/ADS or (capture data at frequency specified in item 6 of Table 4-1 – Electrical Requirements)

(f) Measure the inductance by probing on the shoulder of the test fixture with the pins cut (Figure 4-6 – *Inductance Measurement Fixture Cross-section*).
Call this L_{sandwich}.

(i) Measure 30 units.
The package for 30 units must be chosen from different lots. Use 5 different lots, 6 units from each lot.

(ii) Export data into MDS/ADS or (capture data at frequency specified in item 7 of Table 1).

(iii) Calculate $\overline{L}_{\text{sandwich}}$.

(iv) For each socket unit, calculate

$$L_{\text{socket}} = L_{\text{socket assembly}} - \overline{L}_{\text{sandwich}}$$

It means $\overline{L}_{\text{sandwich}}$ will be subtracted from each $L_{\text{socket assembly}}$ and the result will be compared with spec value for each individual socket unit.

4.6.2. Correlation of measurement and model data Inductance

To correlate the measurement and model data for loop inductance, one unit of measured socket assembly (socket and shorted test fixture) and one unit of measured sandwich (shorted test fixture) will be chosen for cross sectioning. Both units will be modeled based on data from cross sectioning using Ansoft* 3D. The sandwich inductance will be subtracted from socket assembly inductance for both measured and modeled data. This procedure results in loop inductance for socket pin + interposer pin. This final result can be compared with the loop inductance from the supplier model for the socket. The shoulder of the interposer is not included in the electrical modeling. If there is any difference between them, it will be called the de-embedded correction factor. Adding the interposer to the socket and then eliminating the contribution of the fixture creates this correction factor because inductance is not linear.

4.7. Pin-to-Pin Capacitance:

Pin-to-pin capacitance shall be measured using the top fixture (test vehicle) shown in Figure 4-8 – *Test fixture mounted bottom view with the pins cut* –, which contains pins that will connect to the socket. Figure 4-9 – *Top view of the Test vehicle* – shows the capacitance measurement fixture cross-section and the capacitance measurement methodology. The first figure shows the entire assembly. The second figure shows the assembly without the socket, pins cut on the test vehicle. This is used to calibrate out the fixture contribution. Figure 4-10 – *Capacitance measurement fixture cross section* – represents the capacitance fixture design and

measurement configuration. The part that is cut from the top fixture (Figure 4-8 – *Test fixture mounted bottom view with the pins cut*) and mounted on the socket with the structure for capacitance measurement is shown in Figure 4-11 – *Capacitance Measurement Configuration*. Capture data at frequency specified in item 6 of Table 4-1 – *Electrical Requirements*. The part number of the test fixture shown in Figure 4-8 – *Test fixture mounted bottom view with the pins cut* – is 739901-002.

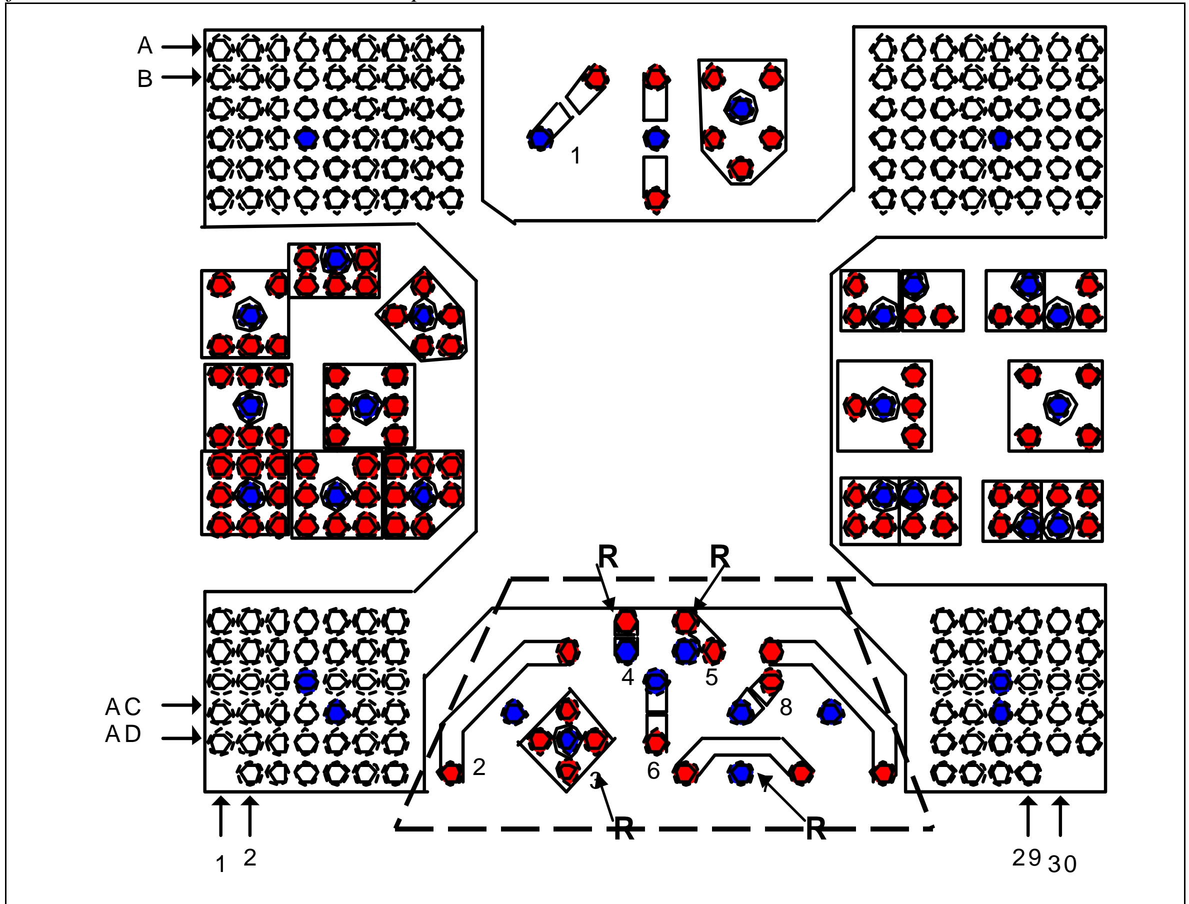


Figure 4-9. Top view of the Test vehicle

Figure 4-10. Capacitance measurement fixture cross section

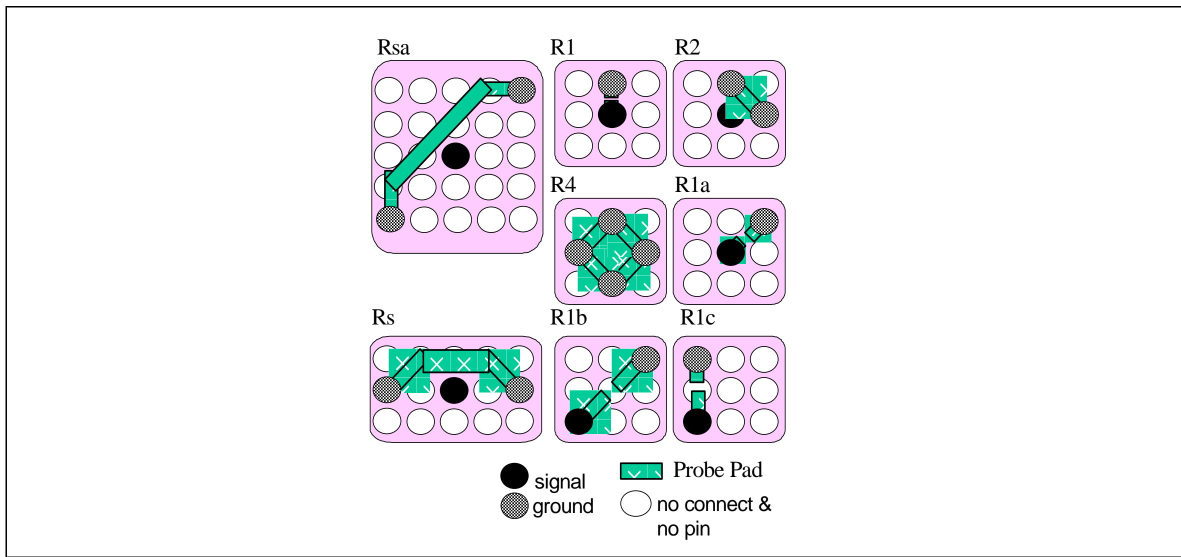


Figure 4-11. Capacitance Measurement Configuration

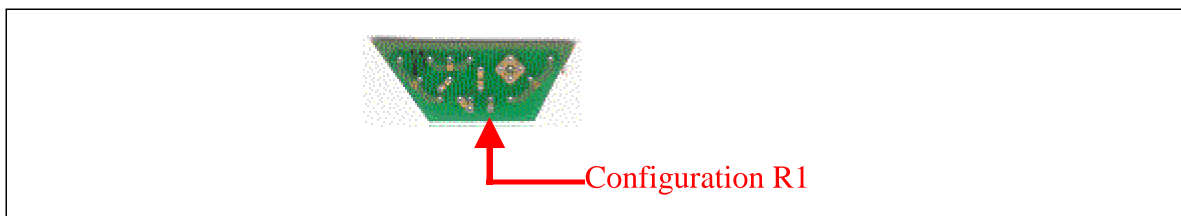


Figure 4-12. Capacitance Fixture Design and Measurement Configuration

4.7.1. Procedure for Capacitance Measurements:

Measurement equipment and steps in this section are the same as the procedure for inductance measurements in section 0 through step d. The following procedure must be completed after that point.

Measurement Steps:

(a) Measure the capacitance of the test vehicle mounted on the socket (Figure 4-9 – *Top view of the Test vehicle*) for the Configuration R1. Call this Csocket_assembly. Export data into the MDS/ADS or (capture data at frequency specified in item 6 of Table 4-1 – *Electrical Requirements*).

(b) Measure the capacitance of the test vehicle with the pins cut (Figure 4-9 – *Top view of the Test vehicle*) for the configuration R1. Call this Ctest_vehicle. Measure 30 units. The test vehicle for 30 units must be chosen from different lots. Use 5 different lots, 6 units from each lot. Export data into MDS/ADS or (capture data at frequency specified in item 6 of Table 4-1 – *Electrical Requirements*).

(c) For each socket unit, calculate

Csocket = Csocket_assembly – Ctest_vehicle

Ctest_vehicle will be subtracted from each Csocket_assembly and the result will be compared with the spec value for each individual socket unit.

4.8. Dielectric Withstand Voltage

No disruptive discharge or leakage greater than 0.5 mA is allowed when subjected to 360 V RMS. The sockets shall be tested according to EIA-364, Test Procedure 20A, Method 1. The sockets shall be tested unmounted and unmated. Barometric pressure shall be equivalent to Sea Level. The sample size is 25 contact-to-contact pairs on each of 4 sockets. The contacts shall be randomly chosen.

4.9. Insulation Resistance

The Insulation Resistance shall be greater than 800 M Ohm when subjected to 500 V DC. The sockets shall be tested according to EIA-364, Test Procedure 21. The sockets shall be tested unmated and unmounted. The sample size is 25 contact-to-contact pairs on each of 4 sockets. The contacts shall be randomly chosen.

4.10. Contact Current Rating

Trise < 45°C when the socket is subjected to rated current of 1.0A. The sockets shall be tested according to EIA-364, Test Procedure 70A, Test Method 1. The sockets shall be mounted on a test board and mated with a package and 200 pins must be chained together. Tambient = 45°C. Contact temp must be less than 90°C.

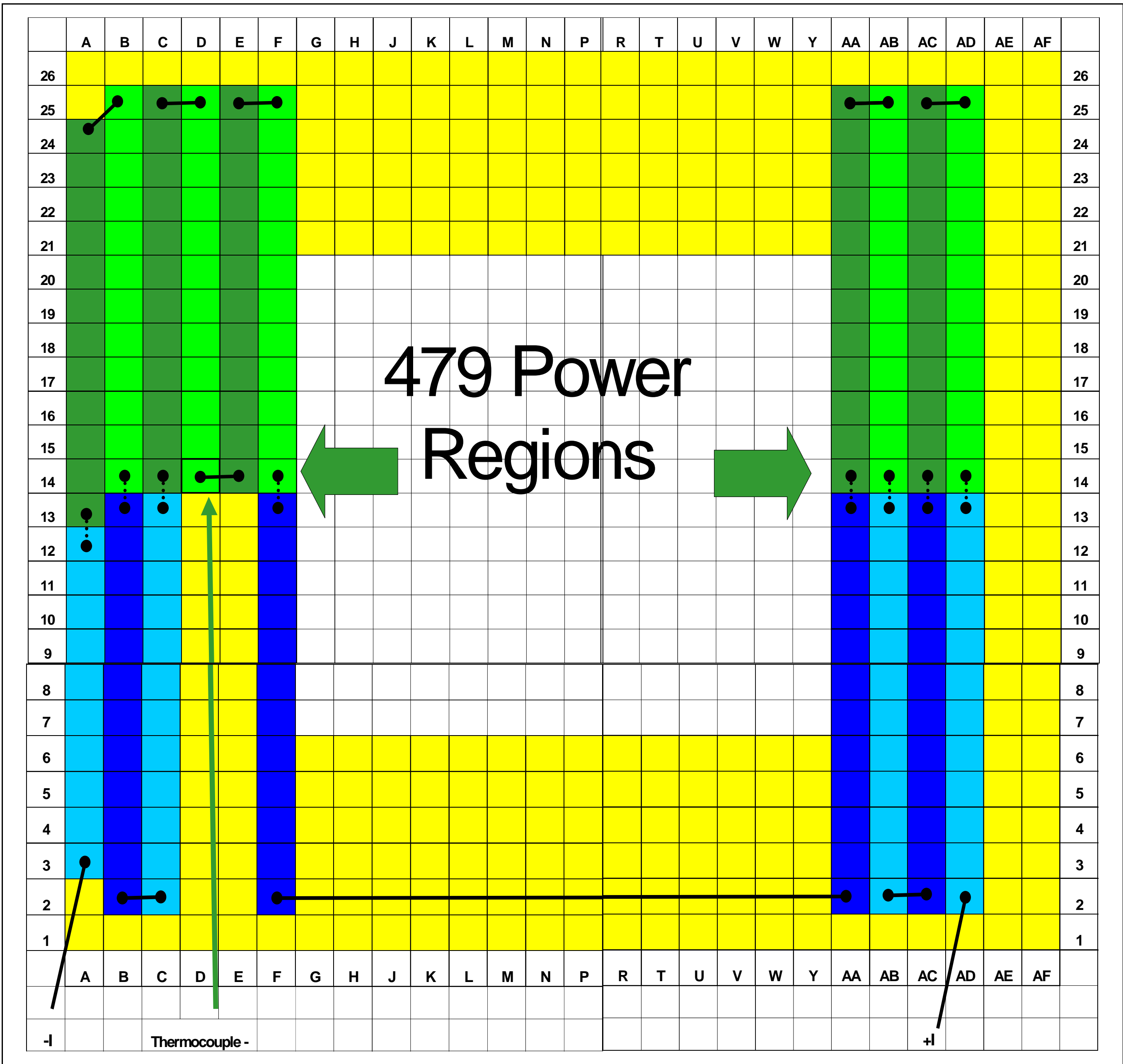


Figure 4-13.

5. Environmental Requirements

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

The reliability targets in this section are based on the expected field use environment for a desktop product. The test sequence for new sockets will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in Figure 5-1 (*below*).

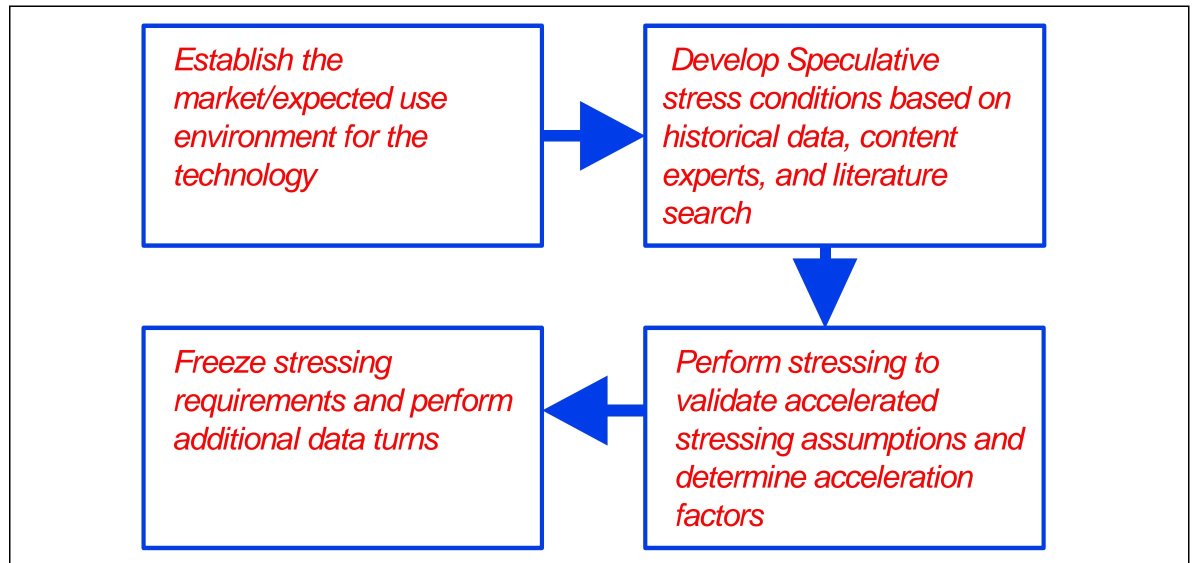


Figure 5-1. Flow chart of Knowledge-based Reliability Evaluation Methodology

A detailed description of this methodology can be found at:
http://developer.intel.com/design/packtech
The use environment expectations assumed are for desktop processors, based on an expected life of 7 to 10 years, are listed in Table 5-1 (*below*). The target failure rates are <1% at 7 years and <3% at 10 years.

Table 5-1. Use conditions environment

Use Environment	Speculative Stress Condition	7 year life expectation	10 year life expectation
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated)	Temperature Cycle	1500 cycles with a mean ΔT = 40°C	2150 cycles with a mean ΔT = 40°C
High ambient moisture during low-power state (operating voltage)-	THB / HAST	62,000 hrs at 30°C, 8%RH	89,000 hrs at 30°C, 85%RH
High Operating temperature and short duration high temperature exposures	BAKE	62,000 hrs at Tjmax	89,000 hrs at Tjmax

Use Environment	Speculative Stress Condition	7 year life expectation	10 year life expectation
Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)	Power Cycle	7,500 cycles	11,000 cycles
Shipping & Handling	Mechanical Shock 50g trapezoidal profile; 170"/sec Velocity change; 11 msec duration pulse	3 drops / axis, 6 axis	
Shipping & Handling	Random Vibration 3.13 gRMS, random, 5 Hz - 20 Hz .01 g2/Hz sloping up to .02 g2/Hz 20 Hz - 500 Hz .02 g2/Hz	10 min / axis, 3 axis	

5.1. Porosity Test

5.1.1. Porosity Test Method

Use EIA 364, Test Procedure 53A, Nitric acid test. Porosity test to be performed for 20 contacts, randomly selected per socket, 5 sockets.

5.1.2. Porosity Test Criteria

Maximum of two pores per set of 20 contacts, as measured per EIA 364, Test Procedure 60.

5.2. Plating Thickness

Measure various plating thickness on contact surface per EIA 364, Test Procedure 48, Method C or Method A. Test to be performed using 20 randomly selected contacts per socket, 5 sockets. No plating thickness measured shall be less than the minimum plating thickness specified in Section 3.4.3 – *Contact Area Plating*.

5.3. Solvent Resistance

Requirement: No damage to ink markings if applicable.

EIA 364, Test Procedure 11A.

5.4. Durability

Per EIA specification 364, test procedure 9, (referenced in EIA 540), the total durability requirement is 20 cycles. The durability testing is performed with 4 separate devices, each undergoing 5 sequential durability cycles. Measure contact resistance when mated in the 1st and 20th cycles. The package should be removed at the end of each de-actuation cycle and reinserted into the socket.

Design, including materials, shall be consistent with the manufacture of units that meet the following safety design guidelines:

- UL 1950 most current editions
- CSA 950 most current edition
- EN60 950 most current edition and amendments
- IEC60 950 most current edition and amendments
- SEMI S2-93 Product Safety Guidelines most current edition and amendments

6. Documentation Requirements

The socket supplier shall provide Intel with the following documentation:

- Multi-Line Coupled SPICE models for socket.
- Product design guidelines incorporating the requirements of these design guidelines.
- Recommended board layout guidelines for the socket consistent with low cost, high volume printed circuit board technology.
- The test facility shall provide Intel and the supplier with the following document:
- Validation testing and test report supporting successful compliance with these design guidelines.

7. Appendix Z.1

NOTES:
1. (THIS NOTE NOT USED)
2. (THIS NOTE NOT USED)
3. REFERENCE DRAWING A07095 FOR FCPGA2 SUBSTRATE DETAIL.
4. TOTAL THICKNESS INCLUDES SOLDER RESIST COATING ON EXTERIOR SURFACES.
5. TOOLING KEEPOUT ZONE FOR PIN-SIDE PASSIVE COMPONENTS.
6. ACTUAL PIN PATTERN WILL VARY. SEE MECHANICAL KEYING TABLE IN DRAWING A07095 FOR DETAILS.
7. HANDLING EXCLUSION ZONE. THERE SHALL BE NO COMPONENTS OR EPOXY ALLOWED.
8. SUCTION CUP HANDLING EXCLUSION ZONE (CROSS-HATCHED AREA). THERE SHALL BE NO COMPONENTS OR EXPOSED METAL ALLOWED EXCEPT FOR FIDUCIALS.
9. PERFECT FORM AT MMC NOT REQUIRED.

VIEW C-C

SHEET 3, ZONE B7

SECTION A-A

ASSEMBLY, FCPGAX, 35mm X 35mm, W/O IHS,

Figure 7-1. 478-Pin FC-PGA2 Package Keepouts (IHS not shown)

NOTES:

1. (THIS NOTE NOT USED)
2. REFERENCE DRAWING A10399 FOR IHS DETAIL.
3. REFERENCE DRAWING A07095 FOR FCPGA2 SUBSTRATE DETAIL.
4. TOTAL THICKNESS INCLUDES SOLDER RESIST COATING ON EXTERIOR SURFACES.
5. TOOLING KEEPOUT ZONE FOR PIN-SIDE PASSIVE COMPONENTS.
6. ACTUAL PIN PATTERN WILL VARY. SEE MECHANICAL KEYING TABLE IN DRAWING A07095 FOR DETAILS.

15.5

15.5

PIN #1 ID ON SUBSTRATE

(31)

(35)

(31)

(35)

VIEW C-C

VIEW C-C
SHEET 3, ZONE B7

1.25 MAX

13.97 SQ

SECTION A-A

B
SHEET 3
ZONE A3

UNLESS OTHERWISE SPECIFIED: INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994. DIMENSIONS ARE IN MILLIMETERS.
TOLERANCE: .X± 0.2 .XX± 0.13 .XXX± 0.05 ANGLES: ± 0.2°

THIRD ANGLE PROJECTION

intel CORP. 5000 W. CHANDLER BLVD. CHANDLER, ARIZONA 85226

TITLE: ASSEMBLY, FCPGAX, 35mm X 35mm, W/IHS

SIZE D | CAGE CODE 34649 | DRAWING NUMBER A10288

SCALE: NONE | DO NOT SCALE DRAWING

Figure 7-2. 478-Pin FC-PGA Package (Top View)

ITEM	6 LAYER (2-2-2) PACKAGE WITH 1.5MM IHS + POLYMER TIM	6 LAYER (1-4-1) PACKAGE WITH 1.5MM IHS + POLYMER TIM
"A"	1.08±0.06	1.06±0.06
"B"	0.1±0.025	0.1±0.025
"C" *	0.74±0.025	0.74±0.025
"D"	0.038±0.012	0.038±0.012
"E"	1.5±0.05	1.5±0.05
"T" (WC)	3.458±0.172	3.438±0.172
(RSS)	3.458±0.087	3.438±0.087

* ADD 0.05mm FOR 300mm WAFERS

Figure 7-3. 478-Pin FC-PGA Package (Bottom View)

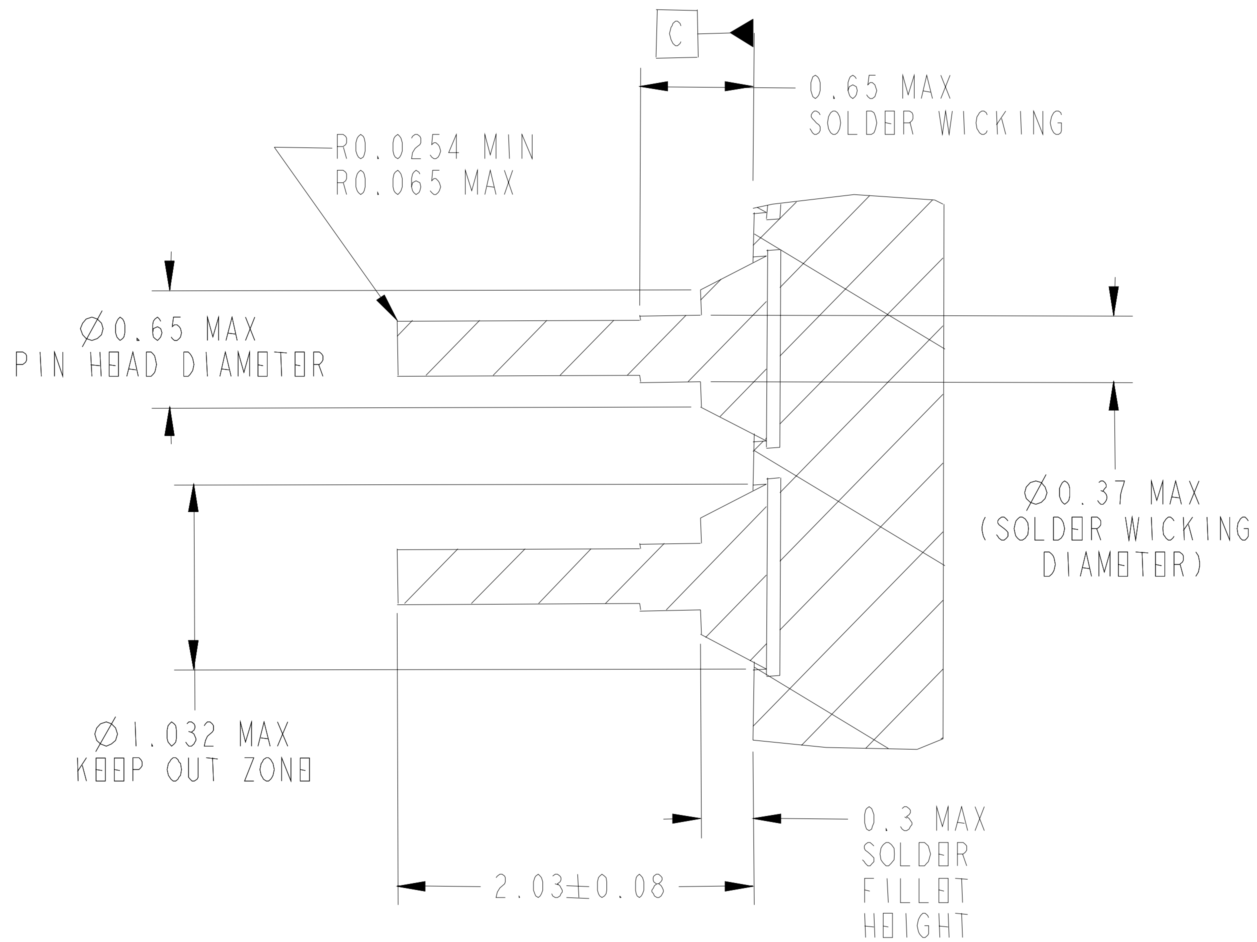


Figure 7-4. Package Pin Shoulder Dimensions

8. Appendix Z.2

NOTES:

1. THE PURPOSE OF THIS DRAWING IS TO ESTABLISH THE MECHANICAL FORM FACOR OF THE SOCKET. DRAWING IS NOT INTENDED TO SHOW INTERNAL DETAIL OF SOCKET WHICH MAY VARY FROM SUPPLIER TO SUPPLIER.

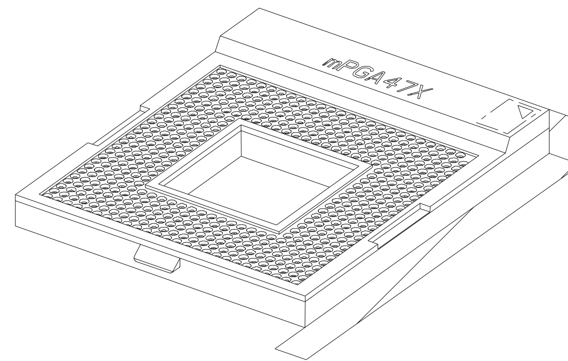


Figure 8-1. mPGA478 Socket (Top Isometric View)

"X"	BASIC DIMENSION, SHALL BE DETERMINED BY SUPPLIER AND REPORTED TO INTEL
"Y"	BASIC DIMENSION, SHALL BE DETERMINED BY SUPPLIER AND REPORTED TO INTEL

LEAD TYPE	"P"
LEAD	0.15
SOLDER BALL	0.20

MECHANICAL KEYING TABLE		
VERSION	UNPOPULATED CONTACT LOCATIONS	NAME
A	A1, A2	mPGA478A
B	A1, B1	mPGA478B
C	A1, B2	mPGA478C
D	A1	mPGA479
E	A1, A2, B1, B2	mPGA476

TOP VIEW (INSERTION SIDE)
SHOWN IN ACTUATED (CLOSED) POSITION

SECTION C-C

BOTTOM VIEW (ATTACHMENT SIDE)

SECTION D-D

DETAIL A
SCALE 20:1

DETAIL B
SCALE 10:1

DETAIL MECHANICAL KEYING
SCALE 10:1

DO NOT TOOL TO THIS DRAWING
FOR REVIEW ONLY

Figure 8-2. mPGA478 Socket Critical-to-Function (CTF) Measurements