# 370-Pin Socket (PGA370) Design Guidelines

**Order Number: 244410-002**

**April, 1999**

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**Revision history**

| Date | Revision | Description |
|---|---|---|
| Nov 1998 | -001 | Initial Release |
| April 1999 | -002 | Change Figure 2b to reflect new handle height requirement. |

# 1 Introduction

## 1.1 Objective

The purpose of this document is to provide the basic information necessary to produce PGA370 so that it will reliably support Intel microprocessors that will be used in conjunction with this socket.

# 2 Socket Description

## 2.1 Operation

PGA370 is a Zero Insertion Force socket (ZIF). It will have Single Lever Actuation as described below. Actuating force shall require less than 10lb without lubricant.

## 2.2 Pin-Out and Orientation Diagram

The pin-out for PGA370 is shown in Figure 1. This diagram is viewed from the TOP of the SOCKET. Locations designated as "**PLUGS**" should have a base that will accept a contact, but the top plate should NOT have pin openings and NO contact should be placed in the base. The socket has 370 pins with 2 plugs. Two pin locations, A1 and AN1, are identified as PLUGS.

## 2.3 Electrical Performance specifications

2.3.1 The contact design of PGA370 must be capable of meeting the following performance characteristics.

2.3.2 Specifications are from the top of the socket to the top of test board to which it is attached.

2.3.3 All specifications are MAX (unless otherwise stated) for a single socket pin, but include effects of adjacent pins where indicated.

2.3.4 Signal-to-$V_{SS}$ pin ratio is 3:1 and signal-to-combined $V_{ss}/V_{cc}$ pin ratio is 1.5:1

2.3.5 Pin and socket inductance include exposed pin from mated contact to bottom of PPGA.

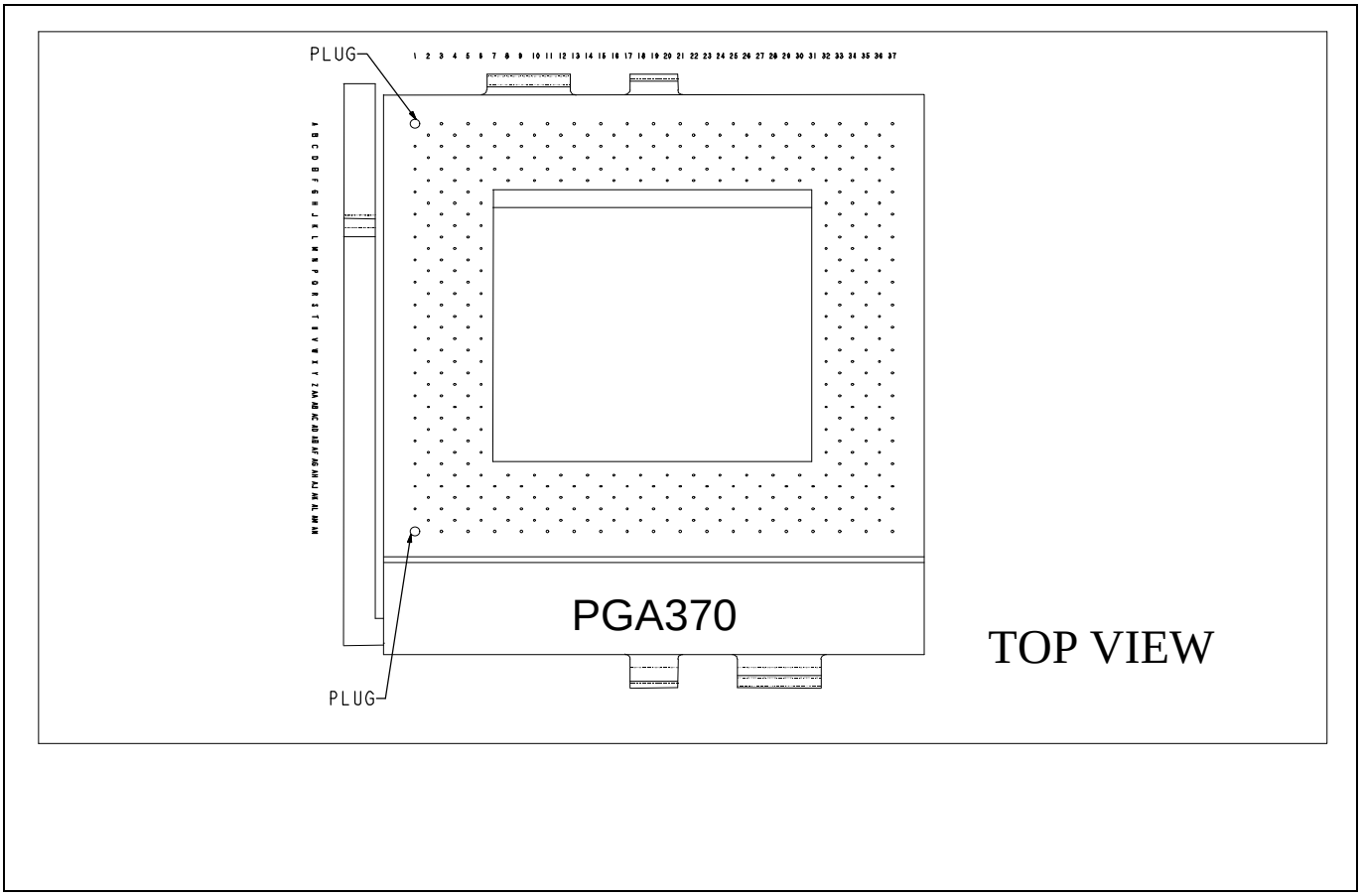



**Figure 1.** Schematic of the 370-pin socket

**Table 1 Electrical requirements for PGA370.**

| | | |
|---|---|---|
| Inductance, socket only | 3.5nH | Refer to 5.1.1 |
| Capacitance, *pin to all surrounding pins* | 1.0pF | Refer to 5.1.2 |
| Capacitance, pin-pin | 0.5pF | Refer to 5.1.2 |
| Characteristic Impedance range (target value, socket only) | 35-75Ω | Refer to 5.1.3 |
| Initial contact resistance | ≤ 20mΩ | Refer to 5.1.4 and 5.1.5 |
| Final contact resistance | ≤ 25mΩ | Refer to 5.1.4 and 5.1.6 |
| Socket minimum current rating and test voltage | 1.0A/pin @ ≤ 2V and < 20°C temp rise due to Joule heating | Refer to 5.1.7 |
| Dielectric withstand voltage (minimum) | 1000Vac | Refer to 5.1.8 |
| Pin-to-Pin insulation resistance (minimum) | 1000MΩ | Refer to 5.1.9 |
| Propagation. | Delay < 120ps | Refer to 5.1.10 |

## 2.4 Temperature Ratings

Operating Temperature: 0 to 85°C
Withstanding Temperature: 240°C solder reflow

Note: For board assembly processing environments, including wave soldering, infrared and convection reflow, the socket shall withstand temperatures above 183°C for a minimum of 60 seconds, with a peak temperature of 240°C for 30 seconds.

## 2.5 Marking

2.5.1 "PGA370" shall be marked in the cam area with the following:
**PGA370** (font type is Helvetica - 18 point BOLD).

2.5.2 The manufacturer's logo (font and size at supplier discretion) will be molded into the cam housing. Marking orientation is shown in **Figure 1**. Any requests for variation from this marking require a written description (detailing the size and location) to be provided to Intel for approval.

2.5.3 Lot Traceability: Each socket will be marked with a lot identification code that will allow traceability of all components that make up the socket, date of manufacture, and assembly location. This mark can be an ink mark or a heat stamp. It must be placed on a surface that is visible when mounted on a printed circuit board. In addition, this identification code must be marked on the exterior of the box in which the units are shipped.

## 2.6 Socket Color

PGA370 should be an off-white, natural color. The color requirement does not apply to actuation lever arm.

### 2.7 Contacts

Contact material: high strength copper alloy.

### 2.8 Contact Plating

Gold plating shall be capable of passing the porosity requirement as well as the other durability and environmental tests per the Socket Qualification Requirements specification.

Plating used in the solder tail area is at the discretion of the socket supplier. This plating must also be capable of passing the solderability requirement per the Socket Qualification Requirements specification.

### 2.9 Socket Tabs for Heat Sink Clips

**Figure 2** illustrates the socket tab details required on PGA370. These features are required to support a 130g heat sink. Any requests for variation to the features as specified requires a detailed drawing (detailing the size and location) to be provided to Intel for approval.

## 3 Package Description

Information provided in this section is to ensure dimensional compatibility of 370-pin socket with that of the PPGA package. The 370-pin socket must be insertable with this PPGA package with zero insertion force when the lever arm is not actuated.

### 3.1 Package Outline

#### 3.1.1 PPGA

The outlines of the processor packages that can be used with PGA370 are illustrated in **Figure 3.** These drawings **do not** include potential heat sinks since these are used at the OEM's discretion.

### 3.2 Package Pins

#### 3.2.1 Pin Dimensions

Details of the pin dimensions are shown in **Figure 3.**

#### 3.2.2 Pin Plating

Pins are plated with a minimum of 8µin gold with a nickel underplate.

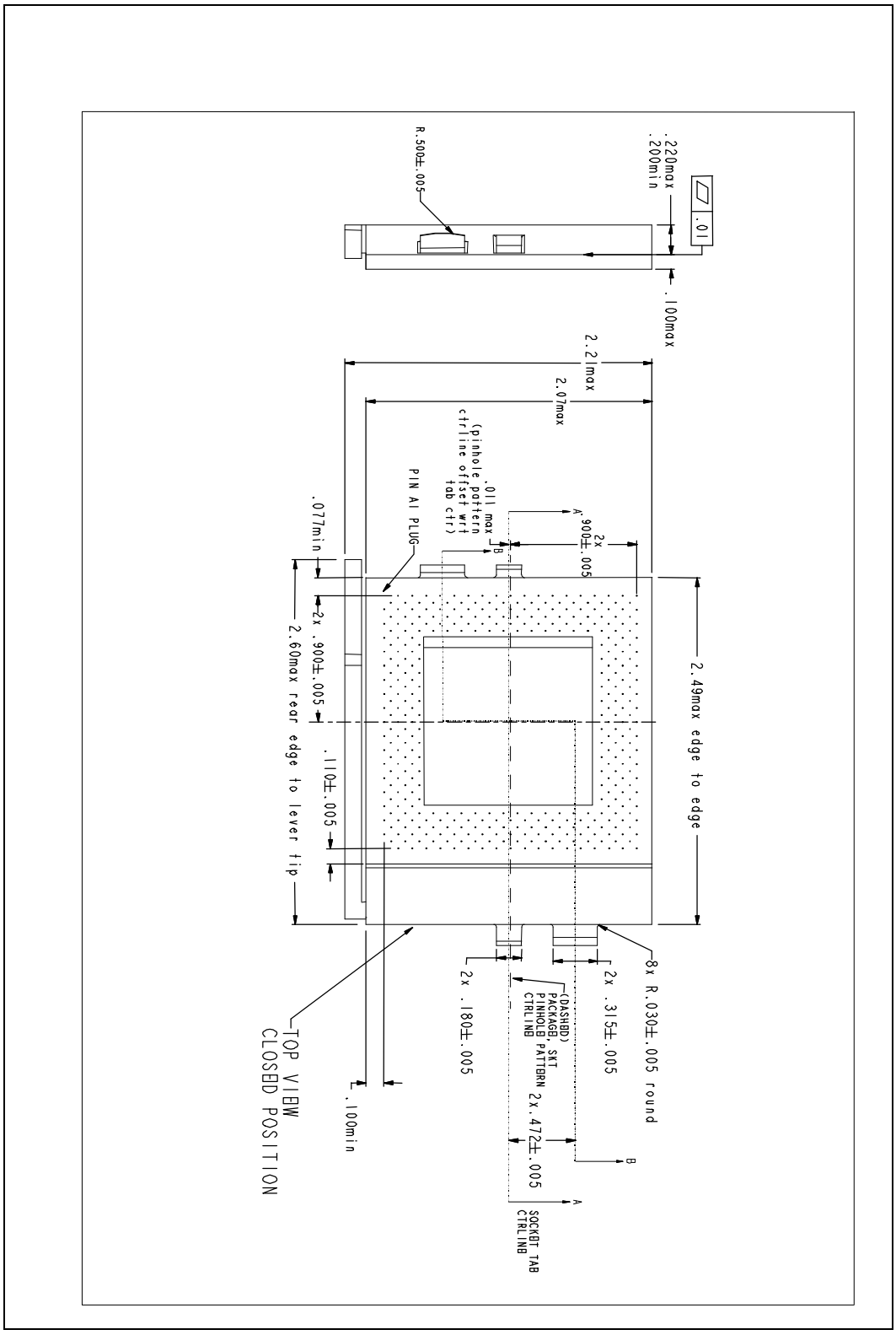



**Figure 2a.** 370-pin socket critical-to-function dimensions. (a) outline of the socket; (b) outline of the heat sink tab

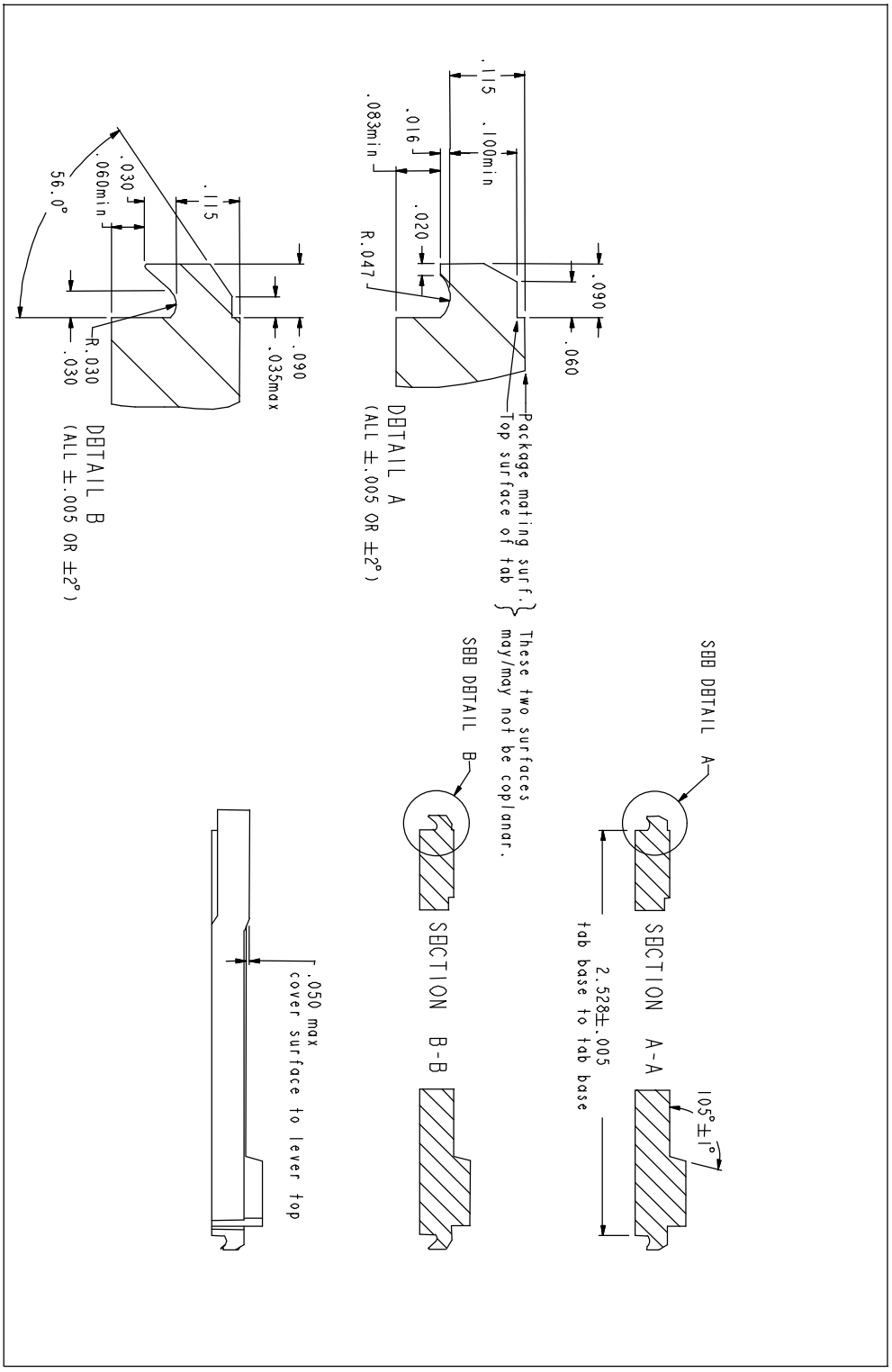



**Figure 2b.** 370-pin socket critical-to-function dimensions. (a) outline of the socket; (b) outline of the heat sink tab

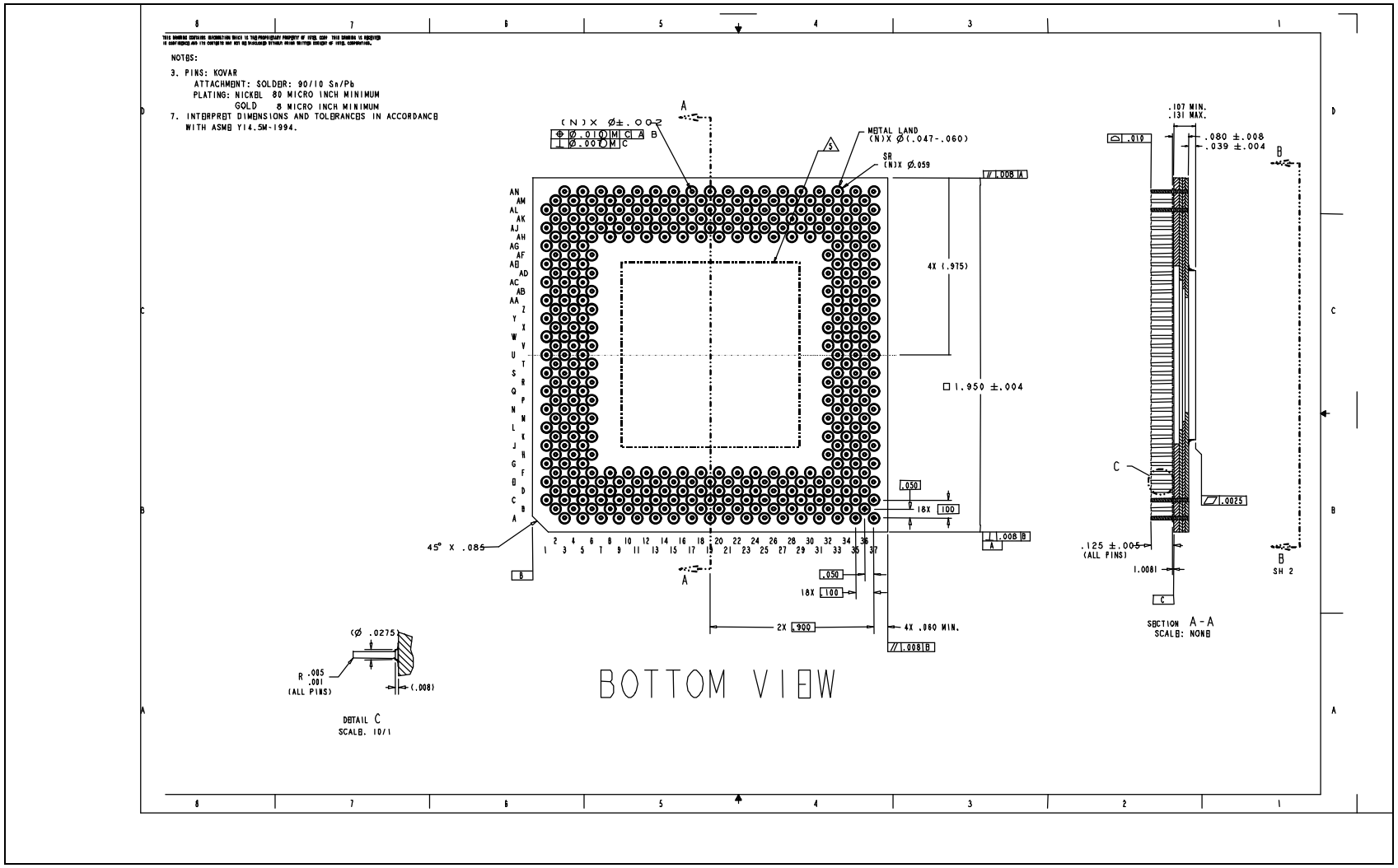



**Figure 3.** Outline of the processor packages that can be used with the 370-pin socket

# 4 Development Process

## 4.1 Socket Design Verification

At the earliest possible date, a detailed drawing of the socket supplier's PGA370 must be provided to Intel for review. This drawing should include all of the features called out in this specification (marking, pinout, cam location, date code location and explanation, etc.), as well as dimensional and board layout information. This drawing will be used to confirm compliance to this specification.

## 4.2 Socket Qualification Testing

PGA370 must pass socket qualification testing to be considered for inclusion on the Intel List of Qualified Sockets. The details of the tests are outlined in the Socket Qualification Requirements in Section 5.

### 4.2.1 Mating Devices

During socket qualification testing, sockets will use mechanical PPGA packages, heat sinks, **Figure 4** (or suitable mock-ups that approximate size and mass of the

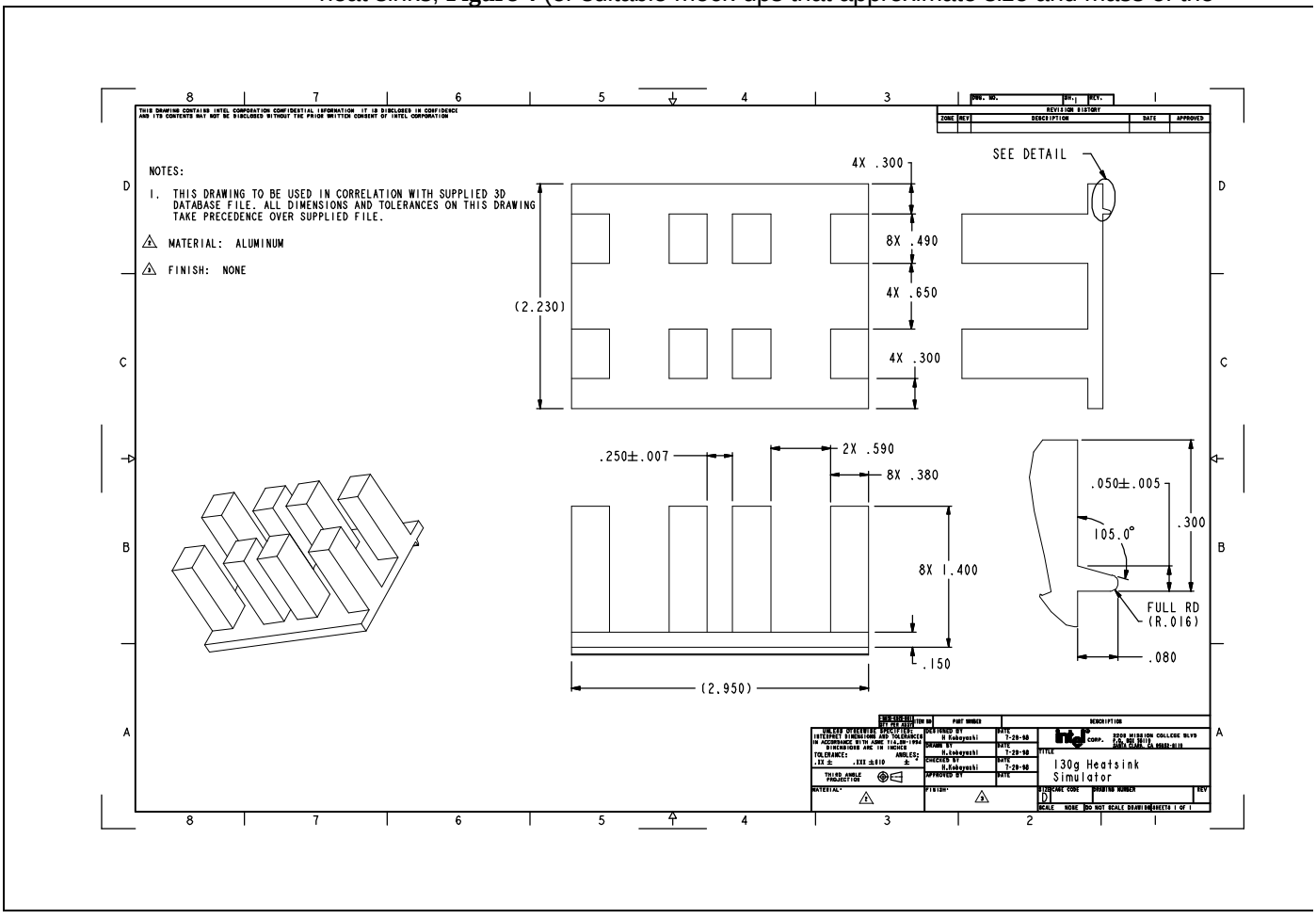



**Figure 4.** Schematic of heat sink simulator for mechanical shock and vibration tests.

planned heat sink) and heat sink clips (or other attaching mechanisms specified by Intel). The target mass for the heat sink (heat sink mock-ups) for PGA370 is 130g. Intel will specify these devices.

#### 4.2.2 Submission of PGA370 for Socket Qualification Testing

The socket supplier's PGA370 will be sent to Intel's designated test facility for socket qualification testing. The sockets submitted must be per the drawing required in section 4.1 and must be reviewed and approved (for submittal) by Intel before the start of testing. Sockets from two separate molds and contact stamping and plating lots will both be required to undergo socket qualification testing.

### 4.3 Quality Assurance Requirements

The OEM's will work with the socket supplier(s) they choose to ensure socket quality.

## 5 Socket Qualification Requirements

### 5.1 Electrical Qualification Requirements

For the propagation delay test, use the test board defined in this document. All other tests described below will be completed either unmated or mated to a test fixture designed for that specific measurement. All measurements are to be made at 200-, 500- and 750Mhz with the exception of the Impedance measurement, which will be 200- and 500Mhz only. Also, the pin groupings selected and defined in **Figure 5** can be moved, with the exception of the crosstalk corner structure, to other areas of the socket provided the relative pin groupings do not change or interfere with other pin groups.

#### 5.1.1 Inductance

5.1.1.1 Contact inductance in free-air (self inductance) shall be measured for five contacts per socket. Inductance measurements shall be taken at 200, 500, and 750 MHz.

5.1.1.2 All specifications are a maximum value, with the exception of impedance, Zo, which is a target, where the value is subject to actual L and C measurements.

5.1.1.3 The unmated mutual inductance is measured between two adjacent pins. This includes both self and mutual (canceling) terms.

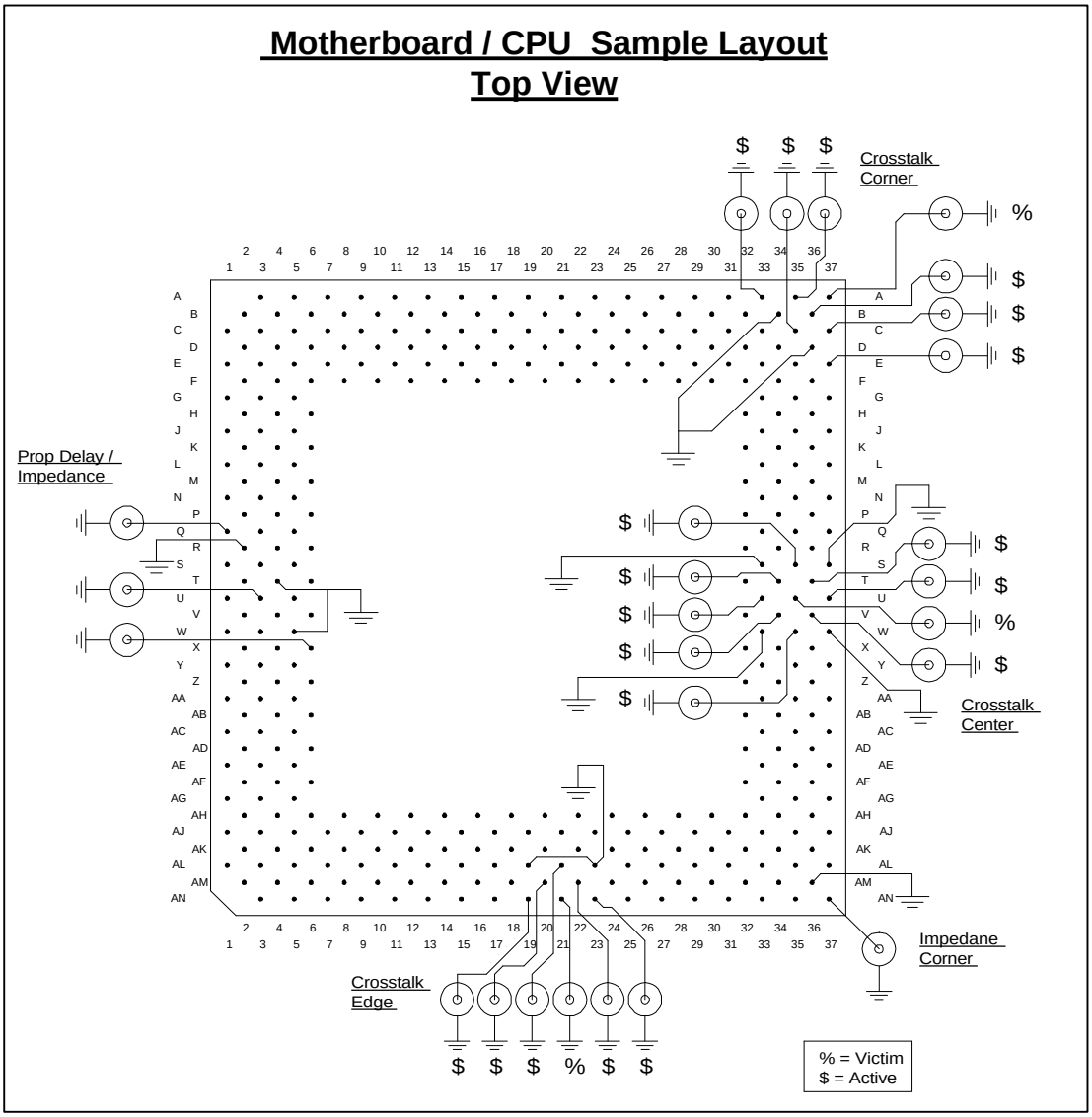
5.1.2 Capacitance

Pin-to-pin capacitance is for the socket only, and is measured between adjacent pins.

Capacitance, pin-pin, is between two pins only (one of them grounded).

Capacitance, pin to all surrounding pins, is with all surrounding pins grounded and the measured pin capacitance with respect to the group of surrounding grounded pins.

Pin-to-pin capacitance shall be measured as per EIA 364, Test procedure 30. Five (5) measurements each shall be made between random lateral, diagonal and vertical




adjacent pins for a total of fifteen (15) measurements. This measurement is on the socket only in unmated condition (no substrate mated).

**Figure 5.** Socket parasitic test board layout.

5.1.3 Characteristic Impedance

Use the four “Impedance” locations in **Figure 5** to measure the characteristic Impedance.

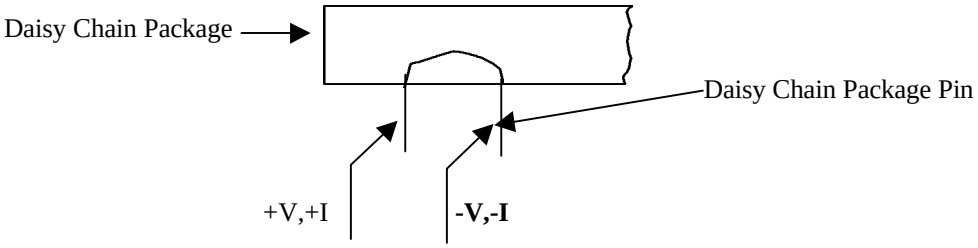
This measurement will be done in the frequency domain using 200- and 500MHz frequencies.

Board trace impedance shall not exceed a tolerance of ±10% from the specified value of 50Ω. All terminations shall not exceed a tolerance of ±5% from the specified values.

Zo is a target value, subject to actual L and C values. Provide values for the socket min/max Zo.

5.1.4 Contact resistance

**Trace resistance $R_t$ in daisy chain package**




**Total circuit resistance $R_i$**

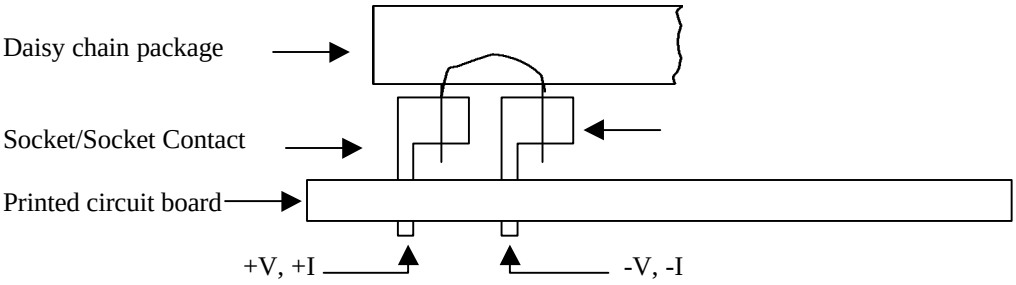



**Figure 6.** Schematic of contact resistance measurement.

The contact resistance is for the socket plus engaged PPGA pins, and can be measured using 4 wire Low-Level Contact Resistance technique (LLCR).

Step one: Contact resistance of twenty-five (25) pairs will be measured per socket. Measure total circuit resistance $\mathbf{R_i}$ for each of the twenty five (25) contact pairs and corresponding 25 pairs of daisy chained trace resistance as shown in **Figure 6**. When measuring $\mathbf{R_t}$, the probe should be placed on the package pin where the contact is made with the socket contact per drawing of the suppliers. To determine contact resistance for each contact in a contact pair,

$R_c = (\mathbf{R_i} - \mathbf{R_t}) / 2$

Step two: Measure and record the total circuit resistance $\mathbf{R_i}$ change between initial and final on all 185 pairs per socket**.**

5.1.5 Initial Contact Resistance:

Measured immediately after the first insertion of the PPGA and engagement of the socket lever arm.

Requirement for the measured 25 contact pairs: No contact can exceed initial contact resistance 20mΩ.

5.1.6 Final Contact Resistance:

Measured after the required environmental tests, including all tests specified in section 5 per the test flow in section 6.9.2.

Requirement for the measured 25 contact pairs: Final contact resistance not to exceed 25mΩ per contact.

5.1.7 Test Voltage and Current Rating

Test to be performed at 1.0 A/contact. Voltage can vary to a maximum of 2.0V during test to attain 1.0A. Less than 20°C rise in temperature due to Joule heating.

Once the current rating of 1.0 amp IDC is established, monitor the contact temperature for 5 minutes. Measure the temperature rise after stabilization. Contact current rating shall be measured for five contacts per socket. Testing shall be measured as per EIA 364, test procedure 70, method 13.

5.1.8 Dielectric Withstand Voltage

- A minimum requirement of 1000 Vac as measured per EIA 364, Test Procedure 20.
- Pin dielectric withstand voltage shall be measured between adjacent random lateral, diagonal and vertical adjacent pins.
- Five (5) measurements shall be made for each of the above three options for a total of fifteen (15) measurements.
- This measurement is on socket only in unmated condition (no substrate mated).

5.1.9 Pin-to-Pin Insulation Resistance

- A minimum requirement of 1000MΩ, as measured per EIA 364, Test Procedure 21.
- Pin-to-pin insulation resistance shall be measured between adjacent random lateral, diagonal and vertical pins.
- Five (5) measurements shall be made for each of the above three options to a total of fifteen (15) measurements.
- This measurement is on socket only in unmated condition (no substrate mated).

5.1.10 Propagation Delay

Propagation delay shall be measured per EIA Test Procedure 103 (under approval) using the following test parameters:

- Propagation delay across the socket shall be less than 100pS at the 50% source amplitude level. Use a test rise time of 100 ps (10%-90%).
- Use a TDR measurement (or equivalent technique). Board trace impedance shall be $Z_0$= 50 Ω.
- The adjacent ground/power contact should be grounded. The adjacent signal contact should be terminated to 50 Ω.

- Drive the signal contact from a 50Ω source, through the socket into a 50Ω load.
- Schematic for this test is shown in **Figure 5**.
- Board trace impedance shall not exceed tolerance of ±10% of the specified value of 50Ω. All terminations shall not exceed tolerance of ±5% of the specified value

## 5.2 Environmental Requirements

Design, including materials, shall be consistent with the manufacture of units which meet the following environmental reference points.

### 5.2.1 Temperature Range:

Operating: 0°C to +85°C.
Shipping and Storage: -40°C to +70°C**.**

### 5.2.2 Temperature Life:

The sockets shall withstand a minimum of 240 hours of the maximum operating temperature plus the maximum recommended temperature rise for the contact due to Joule heating. Normally, this is 85°C plus 20°C rise = 105°C.

## 5.3 Visual Inspection

Socket must meet requirements as specified in Section 2.5.

## 5.4 Vibration

Frequency Range: 5Hz to 500Hz. Vibration test to be performed for two durations:

**Duration 1**: 10min/axis, Power Spectral Density (PSD) Profile: 3.13GRMS. **Figure 7** presents the PSD curves used for the vibration testing. Sample Size: 4 for contact resistance, 4 for electrical discontinuity.

**Duration 2**: 45min/axis, PSD Profile: 2.2GRMS. **Figure 7** presents the PSD curves used for the vibration testing. Sample Size 4 for contact resistance, 4 for electrical discontinuity

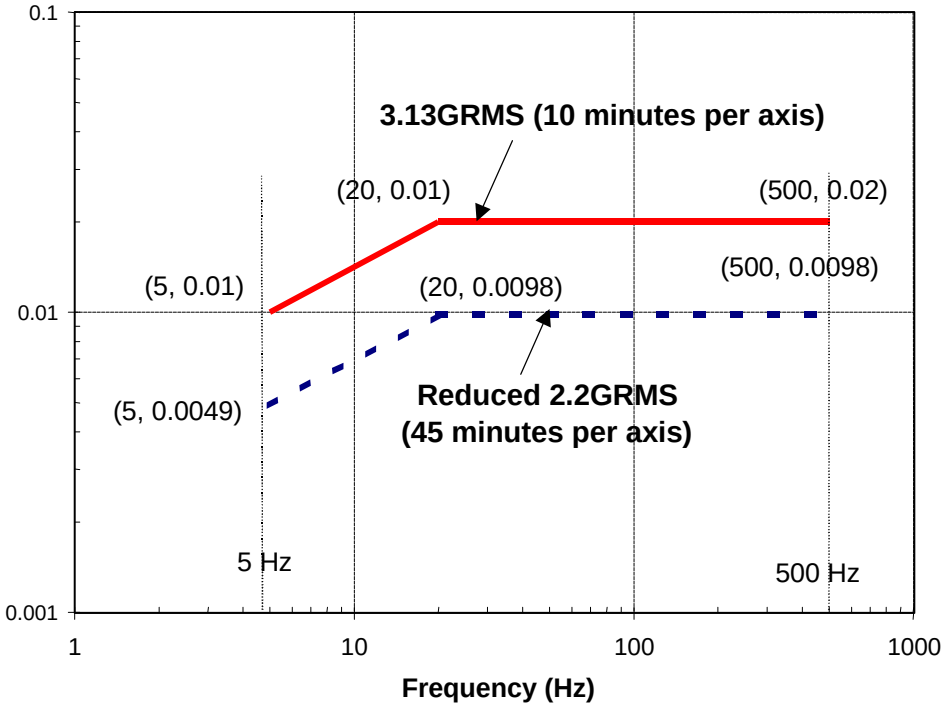



**Figure 7.** Power spectral density ( PSD) curve for vibration tests**.**

Platform board layout and socket pin footprint are shown in **Figure 8**. The board thickness tolerances are 0.062" + 0.008" –0.005".

Input Accelerometer Location: Input (Control) accelerometer to be mounted on the vibration table.

Socket to be mounted to ATX motherboard in **Figure 8**. The motherboard shall be mounted on the shock/vibration table on ¾" standoff in the mounting hole locations.

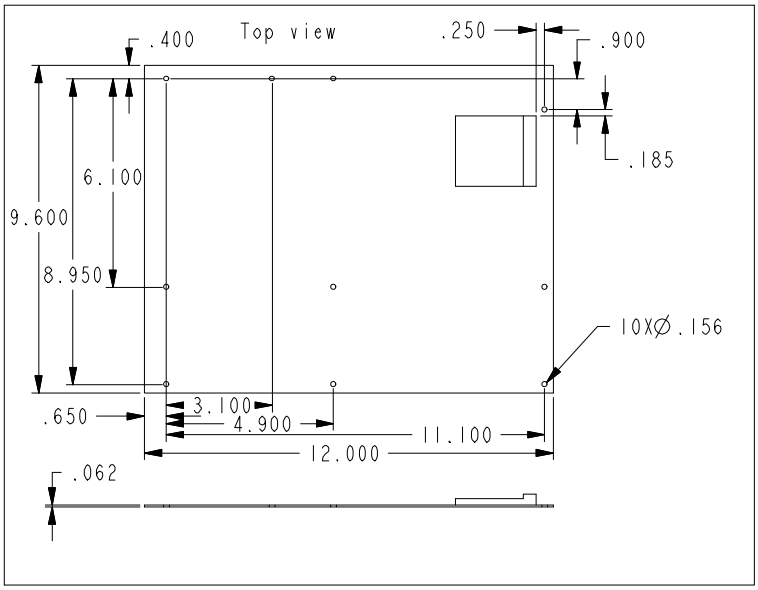



Figure 8(a)

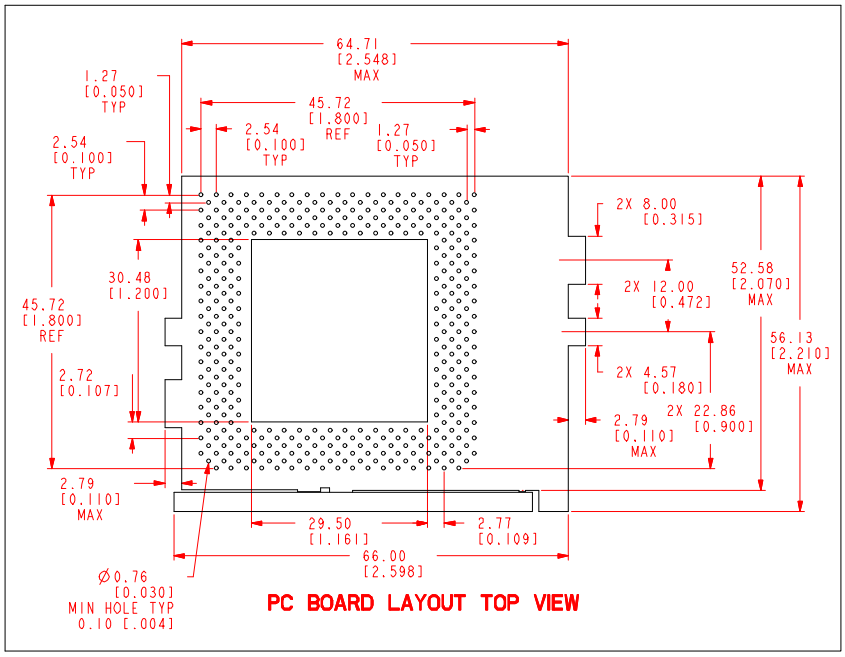



**Figure8**(b)

**Figure 8.** Test board dimensions (a) and socket foot print (b) for mechanical shock and vibration. All dimensions are in inches. The board is a full ATX form factor board. The socket shown in **Figure 1** is to be oriented by 90 degrees counterclockwise to align with the orientation shown in the board. The top-right corner of the socket location is fixed with respect to the board and its mounting holes**.**

The socket must meet all electrical contact resistance requirements following random vibration testing.

No electrical discontinuities > 1.0µs.

The socket must be mated with the mechanical sample outlined in **Section 3.1,** and retained with mechanical supports outlined in **Section 4.2.**

## 5.5 Shock

Test Condition: 50G,11ms duration, Trapezoidal waveform shown in **Figure 9**. Total minimum velocity change must be 170in/sec.

Three shocks applied in each of three perpendicular axes (18 total).

No electrical discontinuities > 1.0µs.

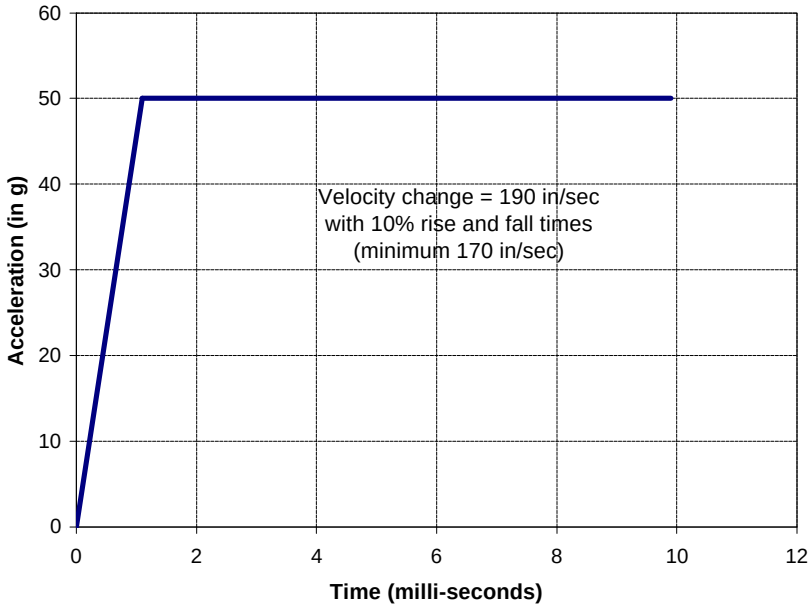



**Figure 9.** Trapezoidal shock wave form for the board level mechanical shock test**.**

The socket must be mated with the PPGA outlined in **Figure 3** and heat sink (heat sink mock-up) outline in **Figure 4**.

The platform test board dimensions and socket foot print on the board are outlined in **Figure 8** for mechanical shock and vibration.

5.6 Durability:

Mate and unmate samples for 49 cycles at a rate of 500 cycles per hour (max), using the same socket. On the 50th cycle, use a new PPGA.

5.7 Thermal Shock:

–55°C to +85°C, 5 cycles per EIA 364, Test Procedure 32: Test Group 3 unmated and unmounted for this test. Test group 4 mated and mounted for this test.

5.8 Humidity Temperature Cycling

25°C to 65°C at 90% to 95% RH (non-condensing) for 10 days per EIA 364, Test Procedure 31, Method 3.

5.9 Temperature Life

Mated samples exposed to 105°C air temperature for 240 hr per EIA 364, Test Procedure 17. See Section 4.1.3. Precondition samples with three insertion/extractions (minimum).

5.10 Withstand Temperature

Ramp temperature at rate of 1°C/sec to 3°C/sec to 145°C for two minutes, then ramp to 240°C for 48 sec. Test per EIA 364, Test Procedure 56, Procedure 5.

## 5.11 Porosity

For Au plating over Ni under-plate, test follows EIA 364, Test Procedure 53, Nitric Acid Test. For Au flash over Pd/Ni over Ni under-plate, test follows EIA 364, Test Procedure 60, Procedure 1.1.2 Sulfur Dioxide Test.

Requirement: No evidence of any porosity.

## 5.12 Plating Thickness

Record thickness of plating on contact surface per EIA 364, Test Procedure 48, Method C.

## 5.13 Solvent Resistance

EIA 364, Test Procedure 11.

Requirement: No damage to ink markings if applicable.

## 5.14 Normal Force

EIA 364, Test Procedure 4.
Requirement: Calculate normal force using nominal thickness processor substrate.

## 5.15 Solderability

EIA 364, Test Procedure 52, Class 2, Category 3. Requirement: 95% coverage.

## 5.16 Contact Retention

EIA 364, Test Procedure 29, 300gm (min) load per individual contact. Requirement: No movement > 0.38mm (.015in).

## 5.17 Withdrawal retention

Purpose: To ensure that the socket meets the minimum requirement to retain the mating device.

Requirements: No evidence of physical damage or unseating of the mating device from the socket when a 12.2lb (pound) axial force is applied.

To run this test, the mating device shall be inserted into the 370 pin socket and actuated to secure the device within the socket. The mated test samples shall be fixtured to the base plate of the test stand and applicable force gauge. The fixturing shall be accomplished in a manner to prevent bowing of the test sample during the performance of the test. An axial force shall be applied at a rate of 1.0 pound per second until the specified load is reached. The specified load shall be maintained for 5 seconds.

## 5.18 Visual Inspection of PPGA

Post Shock & Vibrations: Remove the PPGA from the socket. There shall be no visual evidence of fretting corrosion on any contact. To pass shock & vibration, there shall be no “black spot -

evidence of fretting corrosion" on any of the socket contacts and PPGA pins. At the discretion of the test facility, the substrate may be sent out for surface analysis if a pass/fail decision can not be made based on visual inspection of the substrate.

# 6 Qualification Testing Requirements

This section of the document outlines the tests that must be successfully completed in order for the socket supplier's socket to pass the qualification process. It provides the test plan and procedure required to reach and maintain a qualified test status.

## 6.1 Applicable Documents

EIA-364-C
300/66 & 333/66 Mendocino PPGA Processor Electrical, Mechanical, and Thermal Specifications (EMTS).

## 6.2 Production Lot Definition

A production lot is defined as a separate process run through the major operations including molding, contact stamping, contact plating and assembly. These lots should be produced on separate shifts or days of the week. Lot identification marking needs to be provided to Intel as verification of this process.

## 6.3 Testing Facility

Testing will be performed by Intel's designated third-party test facility.

## 6.4 Funding

The socket supplier will fund socket qualification testing for their socket. Any additional testing that is required due to design modifications will also be at the expense of the supplier.

## 6.5 Reporting

Test reports of the socket qualification testing will be provided directly from the independent test facility to Intel and suppliers. Intel will also be given access to contact the test facility directly to obtain: socket qualification status, explanation of test results and recommendations based on the test results.

## 6.6 Process Changes

Any significant change to the socket will require submission of a detailed explanation of the change at least 60 days prior to the planned implementation. Intel will review the modification and establish the necessary requalification procedure that the socket must pass. Any testing that is required MUST be completed before the change is implemented. Typical examples of significant changes include, but are not limited to the following: Plastic material changes including base material or color; contact changes including: base material, plating material or thickness and design modifications.

## 6.7 Socket Test Plan

### 6.7.1 Test Flow

The test flow is outlined in 6.9.2. Sample sizes and test requirements are given for each test group. For specific test procedures, please refer to the applicable test specifications referenced in section 6.1.

### 6.7.2 Retest Restrictions

Failures of particular sections of the test plan for a given socket footprint will require re-testing of at least a portion of the test flow defined in section 6.9.2. The definition of the tests required will be at Intel's discretion. The modifications that will be made to the socket to improve a failing condition must be provided to Intel in writing and must be approved by Intel prior to retest. If failures occur after retest, further testing will be at Intel's discretion.

### 6.7.3 Mechanical Samples

A mechanical sample of the PPGA, and heat sink (or suitable mockups that approximate size and mass of the planned heat sink) will be used during the mated socket qualification testing. The recommended maximum weight for PPGA heat sink is 130g. See 300/66 & 333/66 Mendocino PPGA Processor Electrical, Mechanical, and Thermal Specifications (EMTS) and related documentation for further information on heat sinks, thermal solutions and mechanical support.

## 6.8 Socket Qualification Notification

Upon completion of the test flow and receipt of test data, Intel will prepare a summary report for the socket supplier who will provide notification as to whether the socket has passed or failed socket qualification testing.

## 6.9 Socket Qualification

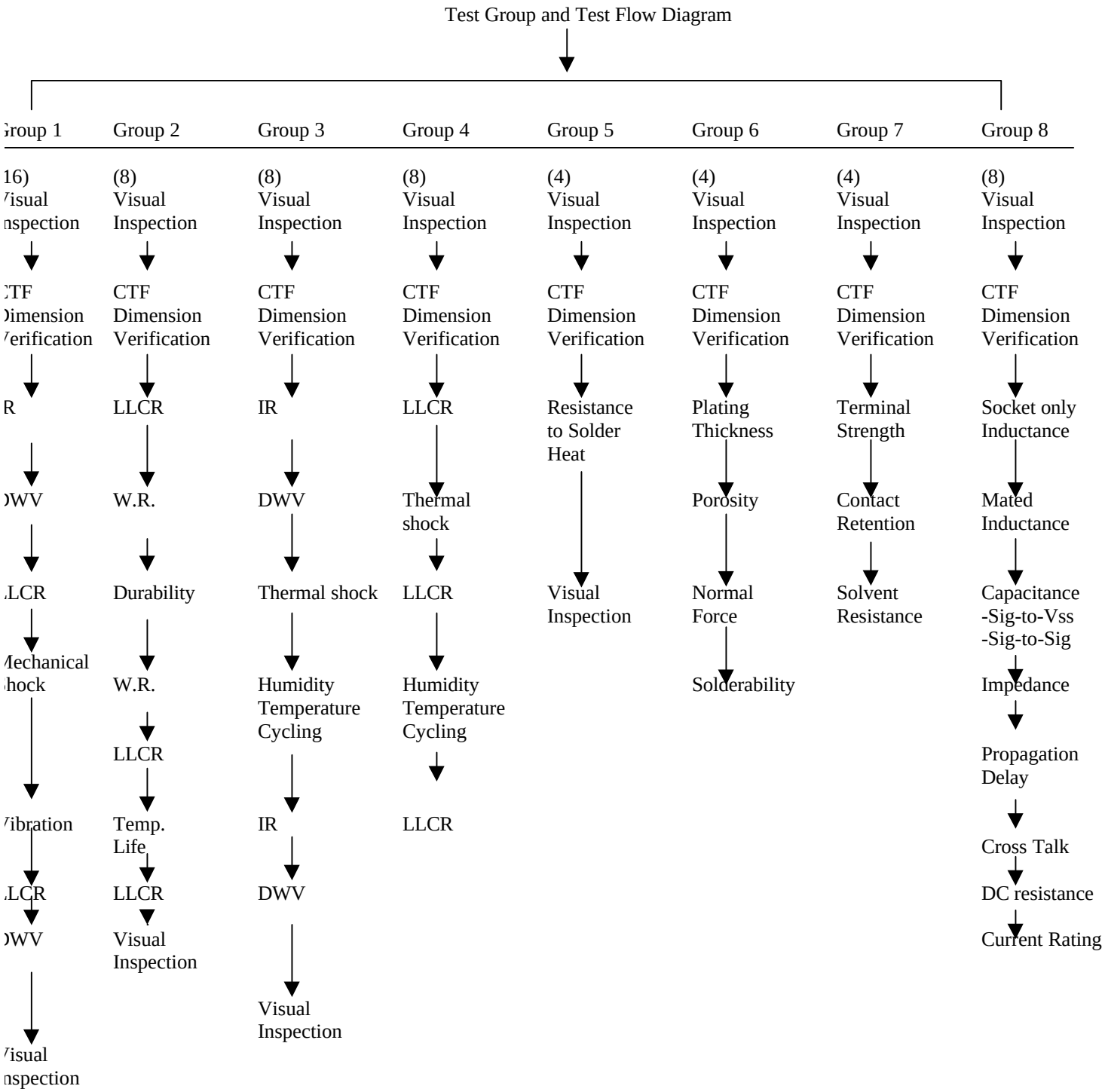
### 6.9.1 Sample size per group

Sample size is shown at top of each test group in Section 6.9.2.

Test samples are to be taken from two different lots. Example: if 8 samples are required, 4 samples will be used from two different lots. Each sample shall be prepared in accordance to the documents specified in Section 6.1, and selected at random per Section 6.2.

### 6.9.2 Qualification tests and test flows

Each group of samples is tested per the sequence shown in the test flow diagram as follows.




LLCR: Low level Contact Resistance
DWV: Dielectric Withstanding Voltage
IR: Insulation Resistance
W.R.: Withdrawal Retention

# 7 SAFETY REQUIREMENTS

Design, including materials, shall be consistent with the manufacture of units, which meet the following safety standards.

UL Recognition.

CSA Certified.

# 8 DOCUMENTATION REQUIREMENTS

The socket supplier shall provide Intel with the following documentation:

Multi-Line SPICE models for the socket.

Product specification incorporating the requirements of these specifications.

Recommended board layout guidelines for the socket consistent with low cost, high volume printed circuit board technology.

The test facility shall provide Intel and the supplier with the following document: Qualification Testing and Test Report supporting successful compliance with this specification.

**UNITED STATES, Intel Corporation**
**2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119**
**Tel: +1 408 765-8080**

**JAPAN, Intel Japan K.K.**
**5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26**
**Tel: + 81-29847-8522**

**FRANCE, Intel Corporation S.A.R.L.**
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**Rexdale, Ontario M9W 6H8**
**Tel: +416 675-2438**

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**Av. das Nações Unidas, 12.901 - 18o. andar - Brooklin Novo**
**04578.000 São Paulo - S.P. – Brasil**
**Tel: +55-11-5505-2296**