UTRON Technology Inc.

UT85C501
UT85C502

Pentium PCI/ISA Chipset

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Data Sheet

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Table of Contents

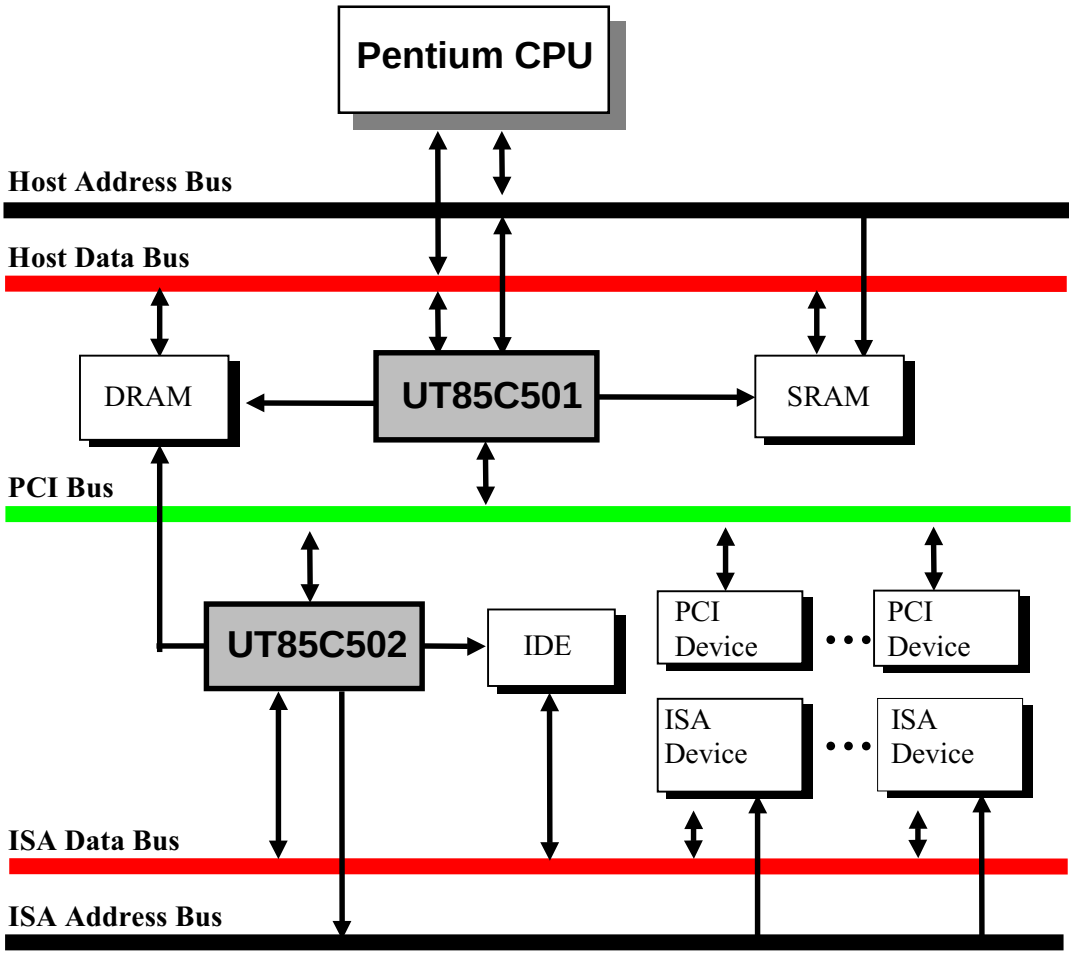
1. Overview

The UT85C501 and UT85C502 are two 208pins PQFP chipset for a very low real estate requirement, low cost and high performance solution for any Pentium compatible PC system. This chipset consists of CPU to PCI bridge, PCI to ISA bridge, Cache controller, DRAM controller, PCI IDE controller, full functions of 206, integrated Real Time Clock(RTC) and Keyboard controller(KBC). No TTL is required.

Typical Motherboard active components:

- UT85C501/502 chipset (2x208 pin PQFP with integrated RTC, EIDE and Keyboard controller)
- EPROM or FLASH
- Clock Generator

1.1 System Block



1.2 Feature

Support Pentium Compatible CPU:
- _ Support Intel P54C/P55C MMX
- _ Support AMD K5/K6 CPU
- _ Support Cyrix/IBM 6x86/MX

CPU to PCI Controller:
- _ 4 level buffered write to PCI
- _ 0 wait state burst write on PCI
- _ CPU write cycle collection
- _ 2 64 bit read-ahead buffer
- _ Burst Read
- _ 0 wait state PCI read if hit
- _ 1M frame buffer decoder

Integrated PCI to ISA Bridge

PCI Master to Memory Controller:
- _ 0 wait state PCI burst read/write
- _ 4K contiguous bursting space

PCI Interface:
- _ 4 requests/grants
- _ Level triggered ABCD interrupts

Synchronous Cache Controller:
- _ 3,1,1,1 Pipeline Cache access
- _ 256-512K Cache memory

DRAM Controller:
- _ EDO mode and Fast Page Mode
- _ Asymmetric DRAM support
- _ Flexible Bank Installation

Power Management:
- _ Full SMI support with Transparent Power Management Scheme achieves power saving without loss of Network Connection

Enhanced PIO IDE Controller:
- _ Mode 4, 32 bit data transfer
- _ Programmable Data-IOR/precharge time
- _ Programmable Data-IOW/precharge time
- _ Programmable Control Command time

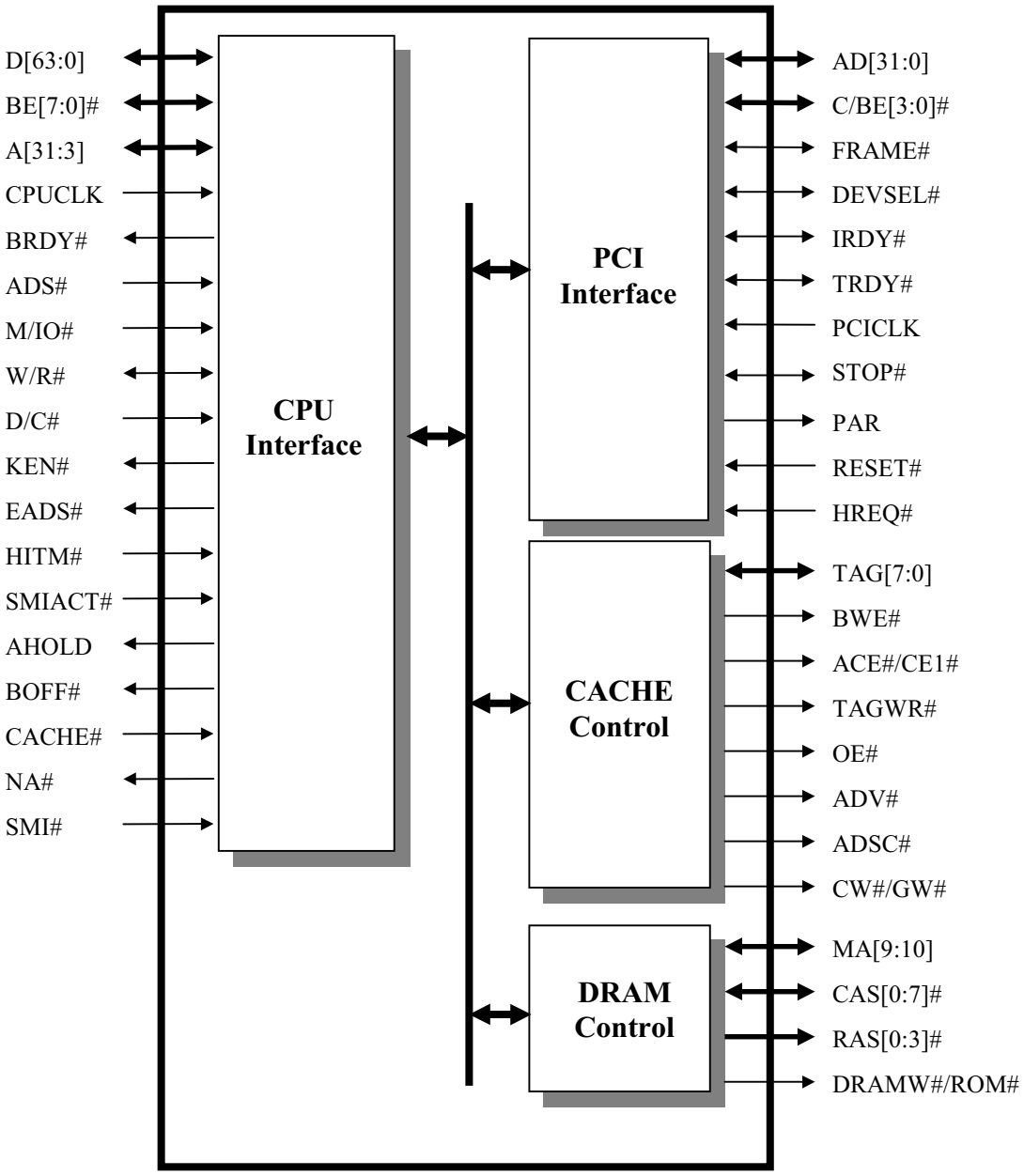
All-in-One application:
- _ Built-in two 8/16 bit DMA controller
- _ Built-in two 82C59 interrupt controller
- _ Support three programmable 16bit counters
- _ Supports combining Flash EPROM, Video/Peripheral BIOS at C000 Segment
- _ Support 1Mb Flash ROM interface

Full Function ISA Controller:
- _ Built-in Keyboard Controller
- _ Built-in Real Time Clock

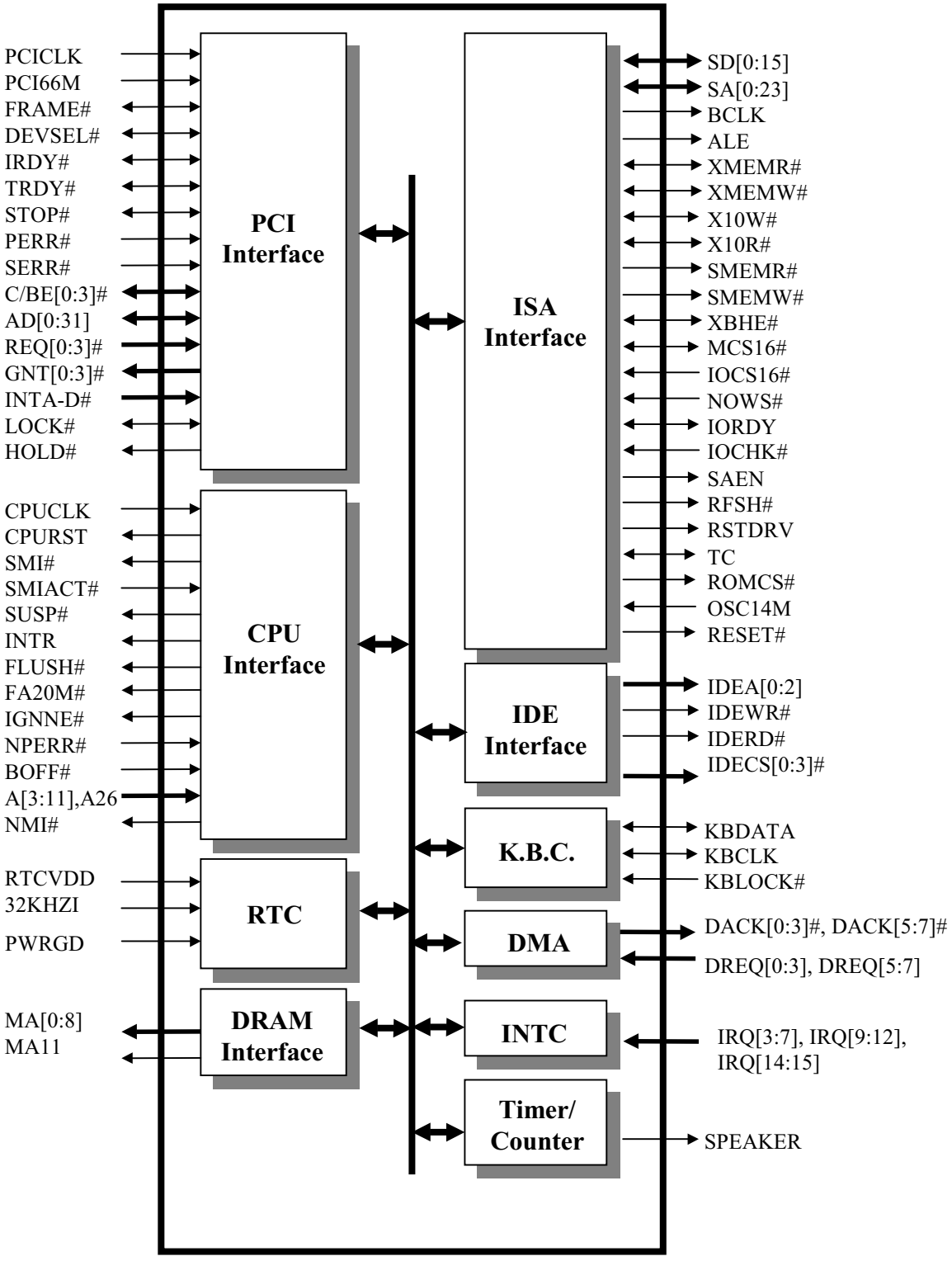
Chipset Configuration:
- _ Two 208 pin PQFP, 0 TTL solution using 3.3V DRAM and Synchronous Cache RAM.

1.3 Block Diagram

1.3.1 UT85C501 Block Diagram



1.3.2 UT85C502 Block Diagram



2. Function Description

2.1 Cache Controller

The UT85C501/502 can support write-back direct mapped cache. Cache sizes supported are 256K and 512K. The cache line-size is always set at 32 bytes (256 bits). Such design allows the use of 8K Tag SRAM to support 256K data cache.

Cache Memory Initialization
The UT85C501/502 has a FORCE CACHE HIT control bit (Reg. D1h, bit 2) which when enabled, will force the cache controller to generate Cache Hit valid for all main memory address space access cycles without address comparison. This bit is particularly useful for initial cache sizing or applications that require only Static Memory. When this control bit is enabled, there will be no access to DRAM.

Tag Memory
The UT85C501/502 supports 8 bit variable tag configuration so that Tag SRAM usage can be optimized. It also supports a 7 bit tag and 1 dirty bit.
The following table depicts tag address mapping, cache size, tag size and cacheable memory size inter-relationship:

Tag Address Map	Tag: 32byte linesize	Cache Size	Cacheable Mem.
TA 18-25	8Kx8*	256K	64M***
TA 19-26	16Kx8*	512K	128M***
TA 18-24 + dirty	8Kx8*	256K	32M***
TA 19-25 + dirty	16Kx8*	512K	64M***

*** When the main memory size is larger than that of cacheable memory, the excess memory is automatically non-cacheable.

Cacheable Region
All accessible main memory are cacheable. Therefore the 384K memory below the 1M address, unless specifically specified, is not cacheable. If the 15M-16M region is disabled as main memory, this region will be cacheable neither.

2.2 DRAM Controller

The UT85C501/502 supports upto 256M fast page mode and EDO DRAM with fast write and flexible memory configurations.

Fast DRAM Write
If page hit, the UT85C501/502 allows for 1 CPU clock write pulse into the DRAM during a CPU memory write cycle. This option is controlled by Reg. D2h, bit 2.

Flexible Memory Configuration and BANK Installation

The UT85C501/502 provides easy memory configuration. Bank0 can be located in any of the DRAM banks. A configuration option (reg. D3, bit 5-4) allow the relation of the bank0 to any of the available banks. Subsequent memory installation is very flexible and the next bank of memory can be installed at any remaining bank. The software can program the upper bound of each memory bank while the upper bound of the previous bank is used as the lower bound. The first bank always assumes address 0 to be the lower bound. If the bank does not exist, the upper bound is simply programmed to be the same as the upper bound of the previous bank.

DRAM Type Support

The UT85C501/502 supports upto 256M of DRAM. The DRAM sizes supported are:

8M, 32M, 128M and their Derivatives.

The Smallest Type of DRAM supported should be set in the configuration register after the memory used in each bank is determined.

DRAM Address Organization

DRAM	Address	MA 11	MA 10	MA 9	MA 8	MA 7	MA 6	MA 5	MA 4	MA 3	MA 2	MA 1	MA 0
8M	RAS	a25	a23	a21	a20	a19	a18	a17	a16	a15	a14	a13	a22
	CAS	a26	a24	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3
32M	RAS	a25	a23	a21	a20	a19	a18	a17	a16	a15	a14	a24	a22
	CAS	a26	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3
128M	RAS	a25	a23	a21	a20	a19	a18	a17	a16	a15	a26	a24	a22
	CAS	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3

Basic DRAM Timing Options

Refer to the DRAM Control section of the Register Definition for detailed descriptions of available DRAM timing control options.

The following summarizes some basic DRAM timing supported:

RAS precharge time option: 4,5,6 clocks
read CAS access time option: 2,3,4 clocks
write CAS access time option: 1,2 clocks

RAS Timeout

RAS timeout is optionally supported. The timeout period is about 8 micro second. Reg D1h, bit 0 controls this option.

Refresh

The UT85C501/502 supports transparent CAS before RAS refresh and refresh rate is fully programmable at Register C1. For a 33Mhz PCI and a refresh rate of about 15us, this register should be programmed to 2.

Main Memory Mask

The standard 384K memory below the 1M address is masked as main memory unless specifically enabled through shadow RAM control.

15M-16M addressing space can be masked out by using control bit at Reg. E2h, bit 3.

ROM Space
ROM segments is set as 128K. The ROM space is at:
FFFE000 - FFFFFFF and 000E000 - 000FFFF

Flash EPROM Support
Flash EPROM is supported. Write protection is provided as an option to the ROM space. The control bit is at Reg 60H, bit 1.

Video BIOS Incorporation
Video or other Peripheral BIOS can be incorporated in the BIOS space through activating the C0000H-C7FFFH segment as ROM space. The control bit is at Reg. 60h, bit 0.

Shadow RAM
The following segments are supported:

1. 000C000 - 000C7FF
2. 000C800 - 000CFFF
3. 000D000 - 000D7FF
4. 000D800 - 000DFFF
5. 000E000 - 000EFFF
6. 000F000 - 000FFFF

Each segment can be individually programmed to be:

1. Read Enable
2. Write Enable
3. CPU cache Enable
4. External cache Enable

Once shadowed, the area will become part of main memory under the programmed active mode. For example, if Read Enable is active and Write Enable is not active, the associated segment is Read Only while any write to the same location is not considered local memory access, but instead, a Bus access.

2.3 Power Management

2.3.1 Function Description of Power Management

Important: Before any access to any power management registers at anytime, before or after system boot up and chipset initialization, make sure that the Master SMI (Reg. 83, bit 7) is disabled.

One of the most significant feature of the UT85C501/502 during power saving mode is its ability, when the system has gone into suspend mode, to allow the system to keep track of

accurate time and date as well as to keep the network station in standby instead of being logged out. This is achievable because of Utron's Transparent Power Management scheme. This feature is available in both the SMI Green or Hardware Green Operation of the UT85C501/502.

The UT85C501/502 supports both SMI driven green operations as well as a pure hardware green operation. Most of the controls for activating the SMI Green or Hardware Green share common activity detection and wake up sources.

The UT85C501/502 also supports upto 7 external wakeup trigger sources and can control upto 7 external devices through programmed registers. Such controls can be done either through software within or outside of the SMI routines. In a typical PC application, usable external trigger source pins and external devices control pins are reduced to 6 and 6 respectively.

2.3.2 Transparent Power Management (TPM)

Transparent Power Management achieves Suspend Mode Power Saving with Standby Mode responsiveness.

Utron's (TPM) Transparent Power Management breaks the barrier of having to Suspend the CPU and of needing the system to react to periodic timer interrupt or network interrupts that should not cause a system to get out of power saving mode. By allowing the system to automatically wakeup periodically for a short duration, the system can then be able to respond to most of such bookkeeping activity without ever having to return to READY mode. The system can effectively be put into Suspend over 95% of the time. Such an approach achieves our unique **TPM Standby Mode** because although the CPU is suspended most of the time, it is not shutdown completely and therefore it can still reacts to software execution. The system will still be able to respond to all the memory or IO trapping activity in addition to external triggered wake up sources. Therefore the system is effectively maintaining a Standby ability to all software and hardware activity. Such feature also allows for putting the CPU to Suspend effectively in between key strokes and also not mission critical phase of the software execution.

Reg 83 bit 3-4 control the wakeup duration so that different CPU or application requirement can be addressed.

2.3.3 Stop Clock Control Pin

The UT85C501/502 has a specially designed STOP CLOCK control pin which is fully optimized as a very speed critical pin. Such speed optimation allows a UT85C501/502 based system to be able to stop or restart a high speed CPU clock without lossing its reliability or generating a glitch. The typical input clock to STOP CLOCK output delay is 5 ns.

Reg 82h, bit 0 controls the STOP CLOCK pin. STOP CLOCK is only active when the hardware sequencer enters into SUSPEND State after the STOP CLOCK function is enabled. This function is applicable in both the SMI GREEN Mode or Hardware Green Mode. However the CPU used must support Stop Clock function.

Power Management Triggering Sources

The following is a list of events that the UT85C501/502 hardware will respond to:

1. Video frame buffer write, address A0000H-BFFFFH

2. Keyboard controller read from I/O port 60h or write to port 64h
3. Serial port access: read 3F8H, 2F8H, 3E8H, 2E8H, write 3F8H-3FFH, 2F8H-2FFH, 3E8H-3EFH, 2E8H-2EFH
4. Parallel port access, I/O port 378H-37FH, 278H-27FH, 3BCH-3BFH
5. IDE access, I/O port 1F0H-1F7H, 170H-177H
6. Interrupts
7. Floppy access read write to 3F5H
8. VESA slave access
9. Coprocessor access
10. Programmable I/O address with programmable size coverage
11. External Sources, such as Switch (Sampled only during Refresh Time)

Access to the above resources can occur while the power management routine is trying to setup the necessary parameters for power management purpose. For example, the SMI routine may try to send a command via the VGA controller to shutdown or suspend the monitor. Such an access to the Video space should not cause a wake up. This can be achieved by turning off the particular activity detection, or by simply turning off all activity detection during the power management access other peripheral controllers.

2.4 DMA Controller

UT85C502 contains two high performance and programmable DMA controllers that fully compatible with 82C37 and total support seven DMA channels. The channel 0 to 3 is for 8-bit DMA devices and channel 5 to 7 is for 16-bit DMA devices. Each DMA channel can be programmed for four transfer modes : single, block, demand and cascade. The DMA controller also supports two different priority modes for serving DMA request: fixed priority and routing priority mode

2.5 Interrupt Controller

UT85C502 contains two programmable interrupt controllers which compatible with 82C59. The master interrupt controller(INTC#1) provides IRQ0 to IRQ7 and the slave interrupt controller(INTC#2) provides IRQ8 to 15. These two interrupt controllers are connected in cascaded mode. The following table is the typical interrupt source for each interrupt request.

IRQ No.	INTC	Normal Interrupt Request Source
IRQ0	1	Timer/Counter 0 output

IRQ1	1	Keyboard controller
IRQ2	1	Interrupt controller #2
IRQ3	1	Serial port #2 (COM2)
IRQ4	1	Serial port #1 (COM1)
IRQ5	1	I^2C bus
IRQ6	1	Floppy Disk
IRQ7	1	Parallel port
IRQ8	2	Real Time Clock
IRQ9	2	Reserved
IRQ10	2	Reserved
IRQ11	2	Reserved
IRQ12	2	PS2 mouse
IRQ13	2	Coprocessor Error
IRQ14	2	IDE Primary channel
IRQ15	2	IDE Secondary channel

The PCI interrupt request INTA# to INTD# can be programmed independently to route to one of the eleven interrupts (IRQ3-7, IRQ9-12, IRQ14-15) through configuration register 6C and 6D.

2.6 Timer / Counter

UT85C502 contains a three channels programmable interval timer (PIT) which compatible with 82C54. The counter 0 is connected to the interrupt controller (IRQ0) to provide a system timer. The counter 1 generates a refresh request that used for DRAM refresh. The counter 2 generated a tone and connected via a gate to the amplifier that drives the speaker.

2.7 PCI IDE Controller

UT85C502 integrated a high performance IDE controller which support up to 4 IDE devices. It supports IDE PIO mode1 to mode5. In the IDE PIO mode, it provides independent timing control for each IDE device that including active time and recovery time. The following table is the access status of the IDE interface.

Primary Channel :

Port	**IDE Chip select**		**IDE Address**			**Read**		**Write**	
I/O	IDECS0#	IDECS1#	IDEA2	IDEA1	IDEA0	IDERD#	IDEWR#	IDERD#	IDEWR#

1F0	0	1	0	0	0	0	1	1	0
1F1	0	1	0	0	1	0	1	1	0
1F2	0	1	0	1	0	0	1	1	0
1F3	0	1	0	1	1	0	1	1	0
1F4	0	1	1	0	0	0	1	1	0
1F5	0	1	1	0	1	0	1	1	0
1F6	0	1	1	1	0	0	1	1	0
1F7	0	1	1	1	1	0	1	1	0
3F6	1	0	1	1	0	0	1	1	0

Secondary Channel :

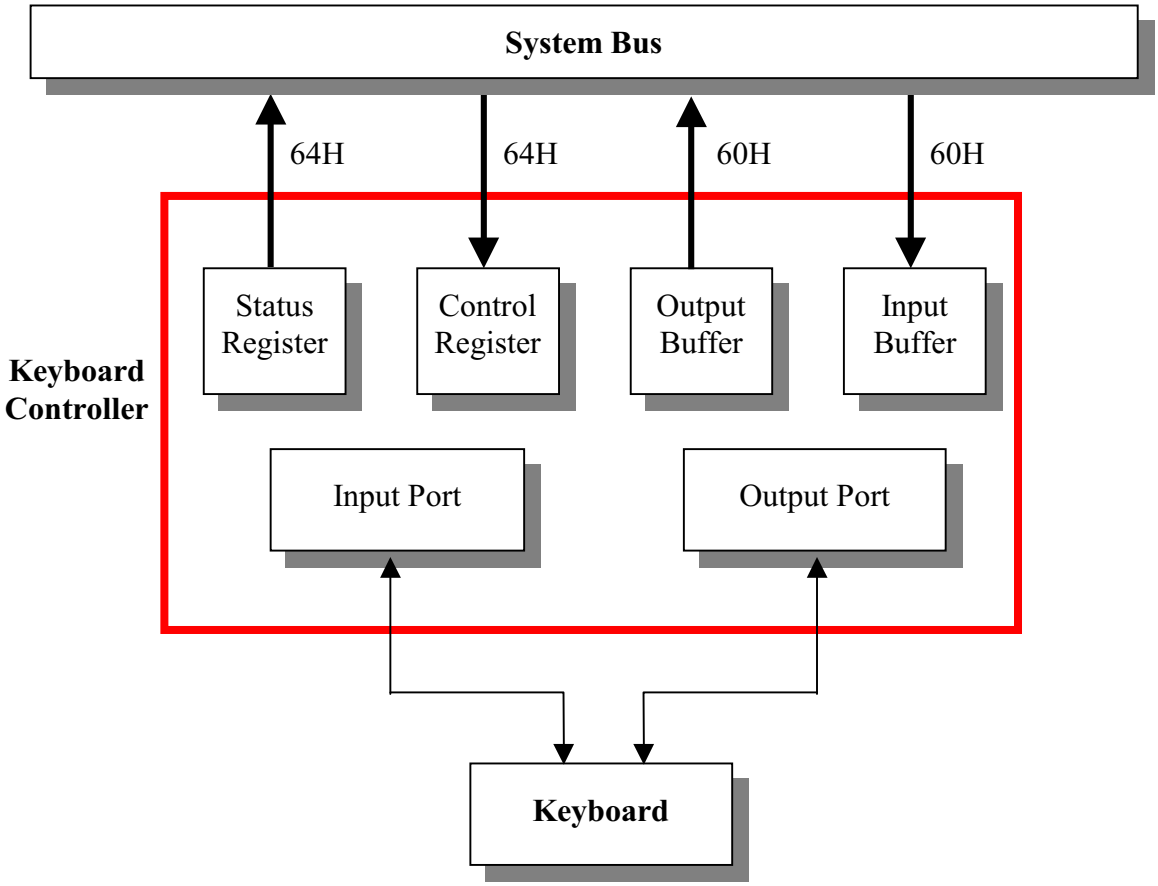
Port	**IDE Chip select**		**IDE Address**			**Read**		**Write**	
I/O	IDECS2#	IDECS3#	IDEA2	IDEA1	IDEA0	IDERD#	IDEWR#	IDERD#	IDEWR#
170	0	1	0	0	0	0	1	1	0
171	0	1	0	0	1	0	1	1	0
172	0	1	0	1	0	0	1	1	0
173	0	1	0	1	1	0	1	1	0
174	0	1	1	0	0	0	1	1	0
175	0	1	1	0	1	0	1	1	0
176	0	1	1	1	0	0	1	1	0
177	0	1	1	1	1	0	1	1	0
376	1	0	1	1	0	0	1	1	0

2.8 Keyboard Controller

The UT85C502 Keyboard Controller supports the standard PCAT and MFII keyboard. It detects command sequences sent to the keyboard controller and intercepts such commands. When commands are being intercepted, no Keyboard Chip Select is generated.
CPU reset can be generated when there is a IO write to port 64h with data 1111xxx0.

Emulation A20 Mask occurs when there is an IO write to port 64h with data D1h, then followed by an IO write to port 60h with data bit1 = 0.
Keyboard emulation reset time is fixed at 6us..

The following is the KBC system.



[Status Register] : (64H)

Bit	Description
7	PARE : Parity error of the last byte from keyboard/auxiliary device (PS2 only) 1 = Last byte with parity error 0 = Last byte without parity error
6	TIM : General time-out 1 = Error 0 = No time-out error
5	AUXB : Output buffer for auxiliary device (PS2 only) 1 = Hold data for auxiliary device 0 = Holds keyboard data
4	KEYL : Keyboard lock status 1 = Keyboard free 0 = Keyboard locked
3	C/D : Command / Data 1 = Command byte written via port 64h 0 = Data byte written via port 60h

2	SYSF : System flag 1 = Self-test successful 0 = Power-on reset
1	INPB : Input buffer state 1 = CPU data in input buffer 0 = Input buffer empty
0	OUTB : Output buffer state 1 = Keyboard controller data in output buffer 0 = Output buffer empty

[Control Register] : (64H)

Bit	Description
7-0	Control bit7-0

[Input and Output Buffer] : (60H)

Bit	Description
7-0	Date bit7-0

[Input Port] :

Bit	Description
7	KBLK : Keyboard lock 1 = Keyboard no locked 0 = Kkeyboard locked
6	C/M : Color / monochrome 1 = Monochrome 0 = Color
5-2	Reserved
1	AUXD : Input date from auxiliary (PS2 only)
0	KBDI : Input data from keyboard

[Output Port] :

Bit	Description
7	KBDO : Output date to keyboard
6	KCLK : Keyboard clock
5	AUXB : Output buffer of auxiliary device full (PS2 only)
4	OUTB : Output buffer full
3	ACLK : Auxiliary device clock (PS2 only)
2	AXDO : Output data to auxiliary device (PS2 only)
1	GA20 : Gate for A20 1 = On (A20 enable) 0 = Off
0	SYSR : Processor reset 1 = Execute reset 0 = No reset

2.9 Real Time Controller

UT85C502 contains a real time clock which compatible with MC146818. It contains two banks of 128 byte CMOS RAM. The first 14 of the CMOS RAM are reserved for the date and time, as well as the control and status registers of the RTC. The following are the CMOS RAM descriptions and the formats of register A to D.

CMOS RAM Address	Bank	Description
00H	0	Seconds
01H	0	Seconds alarm
02H	0	Minutes
03H	0	Minutes alarm
04H	0	Hours
05H	0	Hours alarm
06H	0	Date of week
07H	0	Date of month
08H	0	Month
09H	0	Year
0AH	0	Register A
0BH	0	Register B
0CH	0	Register C
0DH	0	Register D
0EH	0	General purpose register
.	.	.
.	.	.
.	.	.
7FH	0	General purpose register
00H	1	General purpose register
.	.	.
.	.	.
.	.	.
7FH	1	General purpose register

[Register A]: Status Register

Bit	Description

7	UIP : Update flag (update in progress) 1 = Date/time is updated 0 = Date/time can be accessed
6-4	BASE: Time base. These three bits control the divider chain for the oscillator. Standard value 010 = 32.768Hz
3-0	RATE : Rate select = $65.536Hz/2^{rate}$ Standard value 0110 = 1.024Hz ($=65.536/2^6$)

[Register B]: Status Register

Bit	Description
7	Set : Set update cycle 1 = Disable 0 = Enable(default)
6	PI : Periodic interrupt 1 = Disable 0 = Enable(default)
5	AI : Alarm enable 1 = Disable 0 = Enable(default)
4	UI : Update interrupt 1 = Disable 0 = Enable(default)
3	SQU :Square-wave signal 1 = Disable 0 = Enable(default)
2	DM : Date mode 0 = Date/time BCD coded(standard) 1 = Binary coded
1	24h : Time mode 1 = 24-hour-clock(default) 0 = 12-hour-clock
0	DLS : Daylight saving 1 = Enabled 0 = Disabled(default)

[Register C]: Status Register

Bit	Description
7	IRQ : Interrupt request 1 = Interrupt requested 0 = No interrupt requested

6	PS : Source of IRQ is periodic interrupt 1 = Yes 0 = No
5	AS : Source of IRQ is alarm interrupt 1 = Yes 0 = No
4	US : Source of IRQ is update interrupt 1 = Yes 0 = No
3-00	Reserved

Note: The interrupt signal output of the RTC is connected via IRQ8 to the salve 82C59 PIC. It is internally routed within the UT85C502.

[Register D]: Status Register

Bit	**Description**
7	Val : Data in CMOS RAM 1 = Valid (This bit is set to one when the PWRGD(power good) signal provided is high) 0 = Invalid
6-0	Reserved

3. Configuration Registers

3.1 Configuration Register Access

Using CPU I/O space and cycles

0CF8H - 0CFBH: -- Configuration Address Port (dword access only)
0CFCH - 0CFFH: -- Configuration Data Port (byte, word, dword access)

Configuration address port values for accessing UT85C501/UT85C502 registers

Bit	Description
31	Enable bit : set to 1
30-24	Reserved
23-16	Bus Select : set to 0
15-11	Device Select : set to 00101b
10-8	Function Number : set to one of the following values 000 = UT85C501 configuration space access 001 = UT85C502 configuration space access 010 = IDE configuration space access 011-111 = Reserved
7-2	Register address in the configuration space
1-0	Reserved

Configuration Cycle Protocol:
AD16 is used to signal a system configuration cycle.
UT85C501 and UT85C502 decode the configuration address and write to the appropriate registers during the write cycle.

During the system configuration read cycle, UT85C502 provides all the PCI timing control. UT85C502 will output its data if the address is from 0 to 00BFH. Otherwise, UT85C501 will respond by driving its data onto the PCI data bus.

The system configuration space is subdivided into the following sections:

Func.	Register Address	Description
0	0000H - 003FH	UT85C502 : PCI standard specification for CPU-PCI bridge
1	0000H - 003FH	UT85C502 : PCI standard specification for CPU-ISA bridge
2	0000H - 003FH	UT85C502 : PCI standard specification for IDE drive
1	0040H - 007FH	UT85C502 : PCI arbitration, IDE timing, UT85C502 miscellaneous.
1	0080H - 00BFH	UT85C502 : ISA block / DMA / Power Management.
0	00C0H - 00CFH	UT85C501 : memory controller / CPU-PCI controller.

UT85C501/UT85C502 does not respond to the configuration cycle with function number 3 through 7. Any reserved register is returned with a value of 0.

PCI Configuration Space:

Numbers inside square brackets represent byte addresses within the configuration space. All multi-byte numeric fields follow *little-endian* ordering.(Addresses are in hex notation)

3.2 UT85C502 Registers

[1-0]: VID - Vendor Identification Register (programmable)
[3-2]: DID - Device Identification Register (programmable)
NOTE: DID of the Function #0 has the programmed value. DID of the function #1 has the programmed value + 1. DID of the function #2 has the programmed value + 2.

[5-4]: COM - Command Register

Bit	Description
15-10	Reserved
9-0	Fixed: 007h -bit 2: bus master ability enabled -bit 1: memory space access enabled -bit 0: I/O space access enabled

[7-6]: DS - Device Status Register
***NOTE**: Reads to this register behave normally. Writes can only reset bits.*
A bit is reset whenever it is written with a 1.

Bit	Description
15	PARITY ERROR 1 = Parity error occurred
14	SERREVT 1 = System error occurred
13	MAEVT 1 = Master abort, target device does not respond
12	RTAEVT 1 = Target-abort, error occurred in target device
11	Reserved
10-9	DEVSEL timing (DEVTIM), read-only 00 = Fast 01 = Medium 10 = Slow
8-7	Reserved
6-0	Reserved

[8]: RID - Revision Identification Register

[B-9]: Class Code Register

[D]: Latency Timer:

Bit	Description

7-4	LATTIM : Maximum duration of FRAME during burst 0000 = No duration limit 0001 = 1 x 16 PCLK 0010 = 2 x 16 PCLK 0011 = 3 x 16 PCLK 0100 = 4 x 16 PCLK 0101 = 5 x 16 PCLK 0110 = 6 x 16 PCLK 0111 = 7 x 16 PCLK 1000 = 8 x 16 PCLK 1001 = 9 x 16 PCLK 1010 = 10 x 16 PCLK 1011 = 11 x 16 PCLK 1100 = 12 x 16 PCLK 1101 = 13 x 16 PCLK 1110 = 14 x 16 PCLK 1111 = 15 x 16 PCLK
3-0	Reserved

[Function #1: 60]: PCI Timing Control / Miscellaneous

Bit	Description
7-6	DEVSEL sense time for subtractive decode 00 = Fast (1 clock after FRAME) 01 = Medium (2 clocks after FRAME) 10 = Slow (3 clocks after FRAME)
5	PCI bus master lock bit 1 = Ignore PCI bus master lock
4	Enable PCI Special Cycle 1 = PCI Special Cycle 0 = Normal cycle

3	Enable broken state detection
	1 = After GNT# is asserted, wait 16 CLK. If FRAME # is not detected within this time (PCI master is "broken") GNT# is deasserted.
	0 = Always wait for PCI master cycle

2	Enable PCI parity check 1 = Enable PCI parity check
1	ROM write 1 = Enable ROM write 0 = Disable ROM write
0	System VGA ROM 1 = Incorporate VGA ROM into system

[Function #1: 61]: PCI Timing Control/Miscellaneous

Bit	Description
7	IDE start timing 1 = Start IDE cycle 1 PCI clock early

6	ISA bus clock to PCI clock ratio 1 = ISA BUS clock = 1/3 PCI clock 0 = ISA BUS clock = 1/4 PCI clock
5	Enable ISA pre-charge 1 = No pre-charge for ISA IO commands
4	ISA64K 1 = 64K BIOS area 0 = 128K BIOS area
3	IOR 16 timing 1 = add 1/2 PCLK to IOR16 timing
2	IOW 16 timing 1 = add 1/2 PCLK to IOW16 timing
1	Enable Secondary IDE (IDE#3 and IDE#4) 1 = Enable Secondary IDE 0 = Disable Secondary IDE
0	Enable Primary IDE (IDE#1 and IDE#2) 1 = Enable Primary 0 = Disable Primary

IDE Timing Table:

Value	**Description**
0000	15 PCI clocks
0001	14 PCI clocks
0010	13 PCI clocks
0011	12 PCI clocks
0100	11 PCI clocks
0101	10 PCI clocks
0110	9 PCI clocks
0111	8 PCI clocks
1000	7 PCI clocks
1001	6 PCI clocks
1010	5 PCI clocks
1011	4 PCI clocks
1100	3 PCI clocks
1101...	2 PCI clocks
1110	1 PCI clock
1111	Reserved

[Function #1: 65]: IDE 16-Bit IOR Timing

Bit	**Description**
7-4	IOR16PT precharge IOR timing *see IDE timing table*
3-0	IOR16AT active IOR timing *see IDE timing table*

[Function #1: 66]: IDE 16-Bit IOW Timing

Bit	**Description**
7-4	IOW16PT precharge IOW timing *see IDE timing table*

3-0	IOW16AT active IOW timing *see IDE timing table*

[Function #1: 67]: IDE 8-Bit Timing

Bit	Description
7-4	IO8PT precharge timing *see IDE timing table*
3-0	IO8AT active timing *see IDE timing table*

Priority Control:
Priority control is divided into 3 groups. Priorities within each group can be specified, and can be rotated or fixed. Devices are grouped as follows:

Group A: REQ0 and ISA priority
Group B: REQ1 and CPU priority
Group C: Group A, Group B, REQ2, REQ3 priority

[Function #1: 68]: Priority Control

Bit	Description
7-5	PRTYC Group C priority highest... lowest --- 000 = grpA grpB REQ2 REQ3 001 = grpB REQ2 REQ3 grpA 010 = REQ2 REQ3 grpA grpB 011 = REQ3 grpA grpB REQ2 100 = grpA grpB REQ3 REQ2 101 = grpB grpA REQ2 REQ3 110 = REQ2 grpA grpB REQ3 111 = grpA REQ2 grpB REQ3
4	Rotate group C option 1 = Rotate Group C priority 0 = Fixed
3	Group B priority setting 0 = CPU higher priority 1 = REQ1 higher priority
2	Rotate group B option 1 = Rotate Group B priority 0 = Fixed
1	Group A priority setting 0 = ISA higher priority 1 = REQ0 higher
0	Rotate group A option 1 = Rotate Group A priority 0 = Fixed

[Function #1: 69]: Arbiter Control

Bit	Description
7	16 bit IDE option 1 = Force 16-bit IDE when access to IDE is detected as a word transfer
6-5	Grant mask PCI request is blocked for the specified number of clocks after previous GRANT 00 = Immediate if possible 01 = 16CLK 10 = 32CLK 11 = 64CLK
4	Enable ISA lock 1 = allow ISA to hold GRANT until the end of ISA MASTER cycle
3-0	PCI master grant time-out 0000 = Unlimited access 0001 = 1 x 32 CLK 0010 = 2 x 32 CLK 0011 = 3 x 32 CLK 0100 = 4 x 32 CLK 0101 = 5 x 32 CLK 0110 = 6 x 32 CLK 0111 = 7 x 32 CLK 1000 = 8 x 32 CLK 1001 = 9 x 32 CLK 1010 = 10 x 32 CLK 1011 = 11 x 32 CLK 1100 = 12 x 32 CLK 1101 = 13 x 32 CLK 1110 = 14 x 32 CLK 1111 = 15 x 32 CLK

[Function #1: 6A]: CPU Request Control

Bit	Description
7-4	Reserved

3-0	CPU request priority counter CPU will compete for the system bus after the specified number of clocks. 0000 = CPU request only if there is no PCI master or ISA DMA 0001 = 1 x 64 PCICLK 0010 = 2 x 64 CLK 0011 = 3 x 64 CLK 0100 = 4 x 64 CLK 0101 = 5 x 64 CLK 0110 = 6 x 64 CLK 0111 = 7 x 64 CLK 1000 = 8 x 64 CLK 1001 = 9 x 64 CLK 1010 = 10 x 64 CLK 1011 = 11 x 64 CLK 1100 = 12 x 64 CLK 1101 = 13 x 64 CLK 1110 = 14 x 64 CLK 1111 = 15 x 64 PCICLK

[Function #1: 6B]: Misc

Bit	Description
7-3	Reserved
2	1 = Test RTC
1	1 = Write protect Vendor ID and Device ID
0	1 = 66 MHz PCI

[Function #1: 6D-6C]: INTSTR Interrupt Routing Register

see interrupt routing table for valid values

Bit	Description
15-12	INTD
11-8	INTC
7-4	INTB
3-0	INTA

Interrupt Routing Table:

Value	Description

0000	Disabled
0001	Reserved
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110...	IRQ6...
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

Power Management

[Function #1: 80]: Idle Detector Control

Bit	**Description**
7	Software SMI delay option for software triggered SMI 0 = 16.7ms delay 1 = Immediately
6	Idle Detector Clock enable. Make sure that the Master SMI (Reg.83 bit 7) is turned off before accessing this register bit. 1 = Enable 0 = Disable
5-4	Idle Detector Clock base clock period selection. Make sure that the Master SMI (Reg. 83 bit 7) is turned off before accessing this register bit. 11 = 8.6 min clock 10 = 32 sec clock 01 = 2 sec clock 00 = 0.12 sec clock

3-0	Idle Time-out Count value. Make sure that the Master SMI (Reg. 83 bit 7) is turned off before accessing this register bit. 0000 = Time-out on 15.5 base clocks 0001 = Time-out on 14.5 base clocks 0010 = Time-out on 13.5 base clocks 0011 = Time-out on 12.5 base clocks 0100 = Time-out on 11.5 base clocks 0101 = Time-out on 10.5 base clocks 0110 = Time-out on 9.5 base clocks 0111 = Time-out on 8.5 base clocks 1000 = Time-out on 7.5 base clocks 1001 = Time-out on 6.5 base clocks 1010 = Time-out on 5.5 base clocks 1011 = Time-out on 4.5 base clocks 1100 = Time-out on 3.5 base clocks 1101 = Time-out on 2.5 base clocks 1110 = Time-out on 1.5 base clock 1111 = Reserved

[Function #1: 81]: Activity Mask

Bit	Description
7-0	IRQ 15, 14, 12, 11, 10, 9, 8, 7 1 = IRQ SMI will be Mask 0 = IRQ SMI Enable

[Function #1: 82]: Activity Mask

Bit	Description
7-4	IRQ 6, 5, 4 , 3 1 = IRQ SMI will be Mask, 0 = IRQ SMI Enable
3	Video memory access detection (address a0000-bffff) 1 = Disable 0 = Enable
2	Reserved
1	Software triggered SMI A 0-to-1 transition of value in this bit triggers the generation of SMI
0	Suspend State Initiation Only a 0→1 transition causes the hardware to enter SUSPEND State. Once entered into the SUSPEND State, only external trigger wake-up will get the hardware out of this state.

[Function #1: 83]: Control Register

Bit	Description

7	**Master SMI** enable 0 = SMI sources disable 1 = SMI sources enable **Important: Before any access to any power management control bits at anytime, all routines must make sure that this control bit has been disabled.** Only after all the power management options are setup, modified and the system is ready to be activated for power management action should this bit be enabled. Any time the system is not expected to react to power management activities, this bit must be disabled. If this bit is disabled, no SMI sources will cause any SMI regardless of the individual programming controls. Clearing the Master SMI enable will also clear all individual SMI activity status.
6	Software Periodic Suspend enable 0 = Disable, 1 = Enable When enabled, regardless of the current power management state of the hardware, the periodic suspend will be entered. The Suspend/Active timing is determined by bits 3-5 of this register. For SMI routine, this bit should be enabled upon an Idle timeout and should be disabled upon wake-up. This bit should not be enabled during Hardware green mode.
5	Periodic Suspend base clock period 0 = 200μs period 1 = 1ms period Suspend cycle is about 50 base clocks and the wake-up period is determined by bits 4-3 of this register.
4-3	Periodic suspend wake up period 00 = 8 base clocks 01 = 4 base clocks 10 = 2 base clocks 11 = 1 base clock
2	Idle Detector timeout triggers SMI (see Reg. 80, bits 0-6 for controls) 0 = Disable, 1 = Enable SMI will be asserted if no activity occurred for specified amount of time.
1	Idle Detector timeout triggers wake-up from suspend 0 = Disable, 1 = Enable Wake-up will be triggered if no activity occurred for specified amount of time. May be used to allow deeper levels of power down after a certain time. Master SMI should be enabled.
0	SMI Trigger upon Activity detection 0 = Disable (no SMI on activity) 1 = Enable (SMI generated if activity is detected) This control is useful for switching to Ready from Standby mode.

Registers 84h-86h are for 24-bit SMI timer testing. When testing, the timer must first be reset by outputting to port 87h with bit 0 = 1. The counter can then be set to the desired value using these registers.

[Function #1: 87]: (**Write only**): Status clear and SMI Timer Test

Bit	Description
7	SMI source clear 0 = No action 1 = Clear the source of all SMI This bit will clear only the SMI sources that were present at the time of entry into SMI. The SMI sources should have been read first before proceeding with the main SMI service routine.
6	CPU Suspend Status bit clear 0 = Status not cleared 1 = Status cleared Setting this bit will clear the hardware CPU Suspend status bit at Status Reg. bit 7
5-2	Reserved
+1	1= force 32khz clock for idle time counter at reg. 80h bit0-3
0	1= reset 24 bit SMI timer to 0

[Function #1: 87]: (**Read Only**):SMI/Wake-up Status Register

Bit	Description
7	0 = CPU did not go into suspend mode. 1 = CPU went into suspend mode. Hardware sets this bit high when CPU reaches Suspend Grant state. This is useful for SMI routine to check if it has come out of Suspend State. This bit is cleared by setting Reg. 87, bit 7
6-5	Reserved
4	0 = Not Idle Detector timeout triggered WAKEUP 1 = WAKEUP due to Idle Detector timeout
3	Reserved
2	0 = Not Software SMI request triggered SMI 1 = Software SMI request triggered SMI
1	0 = Not SMI from ACTIVITY 1 = SMI pending from ACTIVITY trigger The ACTIVITY here is defined by all the control bits in Reg. 0ah plus the programmable IO space trap defined by Reg. 04h
0	0 = Not Idle Detector timeout triggered SMI 1 = SMI pending due to Idle Detector timeout

3.3 UT85C501 Registers

[Function #0: C0]: CPU-PCI Control Register

Bit	Description
7	1 = Enable dynamic fast back to back decoder
6	Enable NA for PCI block 1 = Enable NA

5	Enable NA for Memory block 1 = Enable NA
4	Enable read ahead 1 = Enable read-ahead at PCI bus. (Not used in standard motherboard) This function will only work if registers C4-6 are set up correctly.
3	PCI 0 wait state read 1 = Enable 0 wait state PCI read
2	Enable burst cycle 1 = Enable burst cycle by translating CPU 64 bit cycle to a burst, two 32 bit PCI cycle
1	Enable buffer write 1 = Enable buffer write for both memory and IO cycles
0	Fast back to back 1 = Enable 0 wait state back to back write on PCI bus 0 = Always 1 idle clock in between PCI cycles

[Function #0: C1]: DRAM Refresh Register

Bit	Description
7-0	(RefReg) Holds a value used in setting the DRAM refresh rate, where DRAM Refresh rate = PCLK / 256 / RefReg

[Function #0: C6-C4]: (Not used in standard motherboard)

Bit	Description
23	1 = Extend DRAM Read by 1 CLK using AHOLD.
22	Enable linefill page hit logic 0 = linefill paging will never occur 1 = linefill paging may occur
21	Dirty write clock width 0 = Tag write is 1 clk during dirty write 1 = Tag write is 1/2 clk during dirty write (When set to 1, bit 20 should also be set to 1)
20	Write hit Ahold 1 = Ahold asserted during CPU dirty write hit (Should be set to 0 if clk->tagwr is 3-4ns otherwise should be set to 1)
18	EDO test 1 = Test for EDO
17	1 = Read ahead decoder enable
16-10	Read ahead space address[31-25]
9-5	read ahead space high bound address[24-20]
4-0	read ahead space lower bound address[24-20]

Cache Control

[Function #0: D0]: Cache Control Register

Bit	Description

7	Fast tag 0 = 2 clock 1 = 1 clock
6	Cache type 0 = Asynchronous Cache 1 = Pipelined Burst Cache
5	Burst reference 1 = use Cyrix CPU burst sequence 0 = use Intel CPU burst sequence
4	Cache size 0 = 256K SRAM 1 = 512K SRAM
3	Line Fill Enable, used to initialize cache too 0 = Disable 1 = Enable
2	2nd level cacheability control 0 = linefill will occur on every read miss 1 = linefill will occur if read miss and CPU cached (should not be set if Cyrix CPU is used)
1	Cache scheme 0 = Write back 1 = Write through
0	Cache Enable 0 = Disable 1 = Enable

DRAM Control

[Function #0: D1]: Timing Control #1

Bit	**Description**
7	Timeout Test Mode 0 = Normal CPU clock = 496 clocks 1 = Test mode = 16 clocks
6	RAS to CAS start delay 0 = 4 clock 1 = 3 clock
5-4	DRAM Page Size 00 = 1K (256K DRAM) 01 = 2K (1M / 2M DRAM) 10 = 4K (4M DRAM) 11 = 8K (16M DRAM)
3	Page Mode 0 = Enable 1 = Disable

2	Force Cache Hit without address comparison 0 = Disable 1 = Enable
1	DRAM start control 1 = Non clocked mode (fast and no VGA interface) 0 = Clocked (required if VGA interface)
0	RAS timeout after 8 micro seconds 0 = Disable 1 = Enable

[Function #0: D2]: Timing Control #2

Bit	**Description**
7	Reserved
6	Early MA1-0 0 = Standard MA1-0 timing 1 = MA1-0 is 1/2 clock early
5	Linefill early BRDY 0 = BRDY asserted after end of linefill 1 = BRDY asserted during each linefill subtransfer
4	Select DRAM type 1 = EDO DRAM 0 = Standard DRAM
3	CAS precharge for non write-back phase. (write-back always 2 clocks) 0 = 2 clock 1 = 1 clock
2	CAS write pulse width 0 = 2 clock 1 = 1 clock
1-0	CAS read pulse width 00 = 4 clock 01 = 3 clock 1x = 2 clock

[Function #0: D3]:

Bit	**Description**
7	AHOLD control during write 0 = AHOLD asserted until end of write 1 = AHOLD asserted until 1 clock before end of write
6	Reserved

5-4	Bank 0 swap 00 = Bank 0 -> RAS 0 01 = Bank 0-> RAS 1 Bank 1 -> RAS 0 10 = Bank 0 -> RAS 2 Bank 2 -> RAS 0 11 = Bank 0 -> RAS 3 Bank 3 -> RAS 3
3-2	RAS precharge time 0x = 6 clock 10 = 5 clock 11 = 4 clock
1	MA relationship with A24 (needed for matching VGA map to top of DRAM) 0 = positive 1 = inverted
0	MA relationship with A23 0 = positive 1 = inverted

[Function #0: D4]:

Bit	**Description**
7-6	Bank 3 MA option 00 = normal DRAM (balanced DRAM address) 01 = 4M x 4 unbalanced 1x = 1M x 4 unbalanced
5-4	Bank 2 MA option 00 = normal DRAM (balanced DRAM address) 01 = 4M x 4 unbalanced 1x = 1M x 4 unbalanced
3-2	Bank 1 MA option 00 = normal DRAM (balanced DRAM address) 01 = 4M x 4 unbalanced 1x = 1M x 4 unbalanced
1-0	Bank 0 MA option 00 = normal DRAM (balanced DRAM address) 01 = 4M x 4 unbalanced 1x = 1M x 4 unbalanced

[Function #0: E0]:

Bit	**Description**
7-4	Bank1 upper bound: defined by A23-26
3-0	Bank0 upper bound: defined by A23-26

[Function #0: E1]:

Bit	**Description**

7-4	Bank3 upper bound: defined by A23-26
3-0	Bank2 upper bound: defined by A23-26

[Function #0: E2]:

Bit	Description
7	SMI address space on Data Write disable 0 = No SMI address remap (Transparent) 1 = SMI address remap (force SMI address upon data write) When this bit is set to 1, all Data Write cycle will be directed to the conventional memory space instead of the remapped SMI memory space.
6	SMI address space on data read disable 0 = No SMI address remap 1 = SMI address remap When this bit is set to 1, all Data Read cycle will be from the conventional memory space instead of the remapped SMI memory space. **Note: currently different from 8006 for code execution. This chip will also access SMI space during code fetch if bit set to 1..**
5	SMI address space enable (for initialization of SMI routine) 0 = Disable (Transparent) 1 = Enable (SMI address mapped during normal access)
4	Reserved
3	Mask 15M - 16M range from main memory 0 = Disable 1 = Enable
2	Bank3 upper bound: defined by A27
1	Bank2 upper bound: defined by A27
0	Bank1 upper bound: defined by A27

[Function #0: E3]:

Bit	Description
7-0	Video Memory start address: defined by A20-A27 0x00 = Video memory at 1M+ 0xzz = Video memory at 0xzz+1

Shadow Control

[Function #0: E4]:

Bit	Description
7	C8000H-CFFFFH 486 CACHEABLE ENABLE: (no write protection) 0 = Disable, 1 = Enable
6	C8000H-CFFFFH CACHEABLE ENABLE: (write protection follows WRITE ENABLE) 0 = Disable, 1 = Enable
5	C8000H-CFFFFH WRITE ENABLE 0 = Disable, 1 = Enable

4	C8000H-CFFFFH READ ENABLE 0 = Disable, 1 = Enable
3	C0000H-C7FFFH 486 CACHEABLE ENABLE: (no write protection) 0 = Disable, 1 = Enable
2	C0000H-C7FFFH CACHEABLE ENABLE: (write protection follows WRITE ENABLE) 0 = Disable, 1 = Enable
1	C0000H-C7FFFH WRITE ENABLE 0 = Disable, 1 = Enable
0	C0000H-C7FFFH READ ENABLE 0 = Disable, 1 = Enable

[Function #0: E5]:

Bit	Description
7	D8000H-DFFFFH 486 CACHEABLE ENABLE: (no write protection) 0 = Disable, 1 = Enable
6	D8000H-DFFFFH CACHEABLE ENABLE: (write protection follows WRITE ENABLE) 0 = Disable, 1 = Enable
5	D8000H-DFFFFH WRITE ENABLE 0 = Disable, 1 = Enable
4	D8000H-DFFFFH READ ENABLE 0 = Disable, 1 = Enable
3	D0000H-D7FFFH 486 CACHEABLE ENABLE: (no write protection) 0 = Disable, 1 = Enable
2	D0000H-D7FFFH CACHEABLE ENABLE: (write protection follows WRITE ENABLE) 0 = Disable, 1 = Enable
1	D0000H-D7FFFH WRITE ENABLE 0 = Disable, 1 = Enable
0	D0000H-D7FFFH READ ENABLE 0 = Disable, 1 = Enable

[Function #0: E6]:

Bit	Description
7	F0000H-FFFFFH 486 CACHEABLE ENABLE: (no write protection) 0 = Disable, 1 = Enable
6	F0000H-FFFFFH CACHEABLE ENABLE: (write protection follows WRITE ENABLE) 0 = Disable, 1 = Enable
5	F0000H-FFFFFH WRITE ENABLE 0 = Disable, 1 = Enable
4	F0000H-FFFFFH READ ENABLE 0 = Disable, 1 = Enable
3	E0000H-EFFFFH 486 CACHEABLE ENABLE: (no write protection) 0 = Disable, 1 = Enable

2	E0000H-EFFFFH CACHEABLE ENABLE: (write protection follows WRITE ENABLE) 0 = Disable, 1 = Enable
1	E0000H-EFFFFH WRITE ENABLE 0 = Disable, 1 = Enable
0	E0000H-EFFFFH READ ENABLE 0 = Disable, 1 = Enable

Scratch Register

[Function #0: E7]: Scratch Register

Bit	Description
7-0	read/write

Special CCycles

ADDRESS phase : same as CPU address
DATA phase : special cycle code

AD[15:0] PCI specification
0000H : Shutdown
0001H : Halt
0002H : Intel specific, check AD[31:16] for detail

AD[31-16] Intel specification, same as the P5 address input
0001H : Flush
0003H : Write Back
0004H : Flush Ack
0005H : Branch Trace Message
0012H : Suspend GRANT

Byte Enable : same as CPU

3.4 DMA Register Access

DMA channel Extended Mode Register:
Channels 0-3 port address: 040BH
Channels 4-7 port address: 04D6H

Bit	Description
7	Reserved (must be 0)
6	EOP Input / Output 0 = EOP is an O/P for this channel 1 = EOP is an I/P for this channel

5-4	DMA Cycle Timing Mode 00 = compatible timing 01 = Type A 10 = Type B 11 = Type F
3-2	Addressing Mode 00 = 8-bit I/O, count by bytes (DMA1) 01 = 16-bit I/O, count by words (DMA2)(address shifted) 10 = Reserved 11 = 16-bit I/O, count by bytes
1-0	DMA Channel Select 00 = Channel 0(4) select 01 = Channel 1(5) select 10 = Channel 2(6) select 11 = Channel 3(7) select

Compatible Timing: run at 9 SYSCLKs(1080 ns/single cycle) and 8 SYSCLKs(960 ns/cycle)during the repeated portion of a BLOCK or DEMAND mode.

Type A Timing: run at 7 SYSCLKs(840 ns/single cycle) and 6 SYSCLKs(720 ns/cycle)during the repeated portion of a BLOCK or DEMAND mode.

Type B Timing: run at 6 SYSCLKs(720 ns/single cycle) and 4 SYSCLKs(480 ns/cycle)during the repeated portion of a BLOCK or DEMAND mode.

Type F Timing: run at 3 SYSCLKs(360 ns/single cycle) and 2 SYSCLKs(240 ns/cycle)during the repeated portion of a BLOCK or DEMAND mode.

DMA Memory High Page Register

DMA Memory Base High Page Register:
DMA Channel 0 port address: 0487H
DMA Channel 1 port address: 0483H
DMA Channel 2 port address: 0481H
DMA Channel 3 port address: 0482H
DMA Channel 5 port address: 048BH
DMA Channel 6 port address: 0489H
DMA Channel 7 port address: 048AH

These bits represent the eight most significant address bits when forming the full 332-bit address for a DMA transfer.

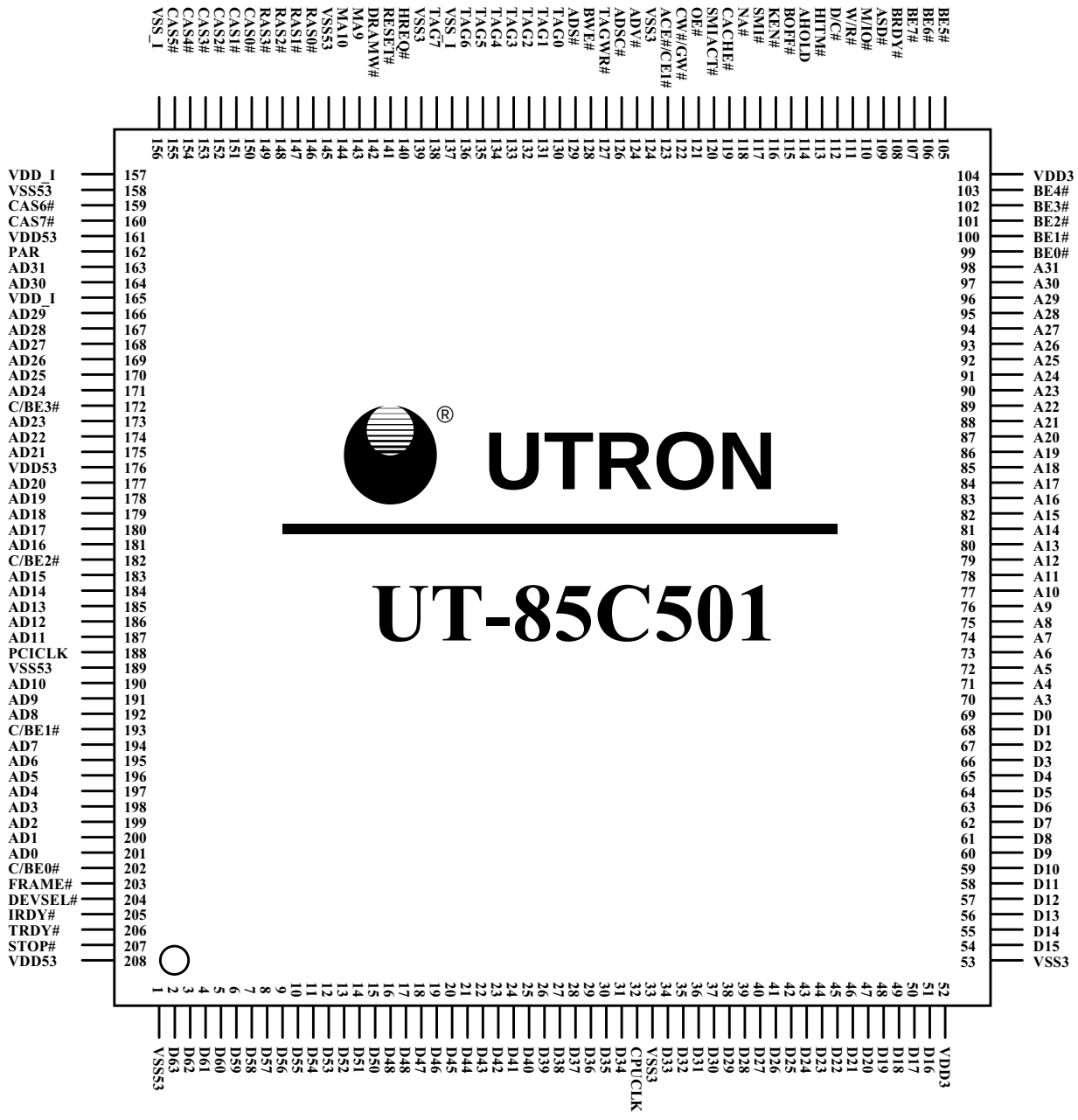
Interrupt Unit Edge/Level Control Register (ELCR):
Port 04D0H (R/W): INT Controller 1
Port 04D1H (R/W): INT Controller 2

Bit	Description
7	0 = IRQ<7(15)>Edge trigger 1 = IRQ<7(15)>Level trigger

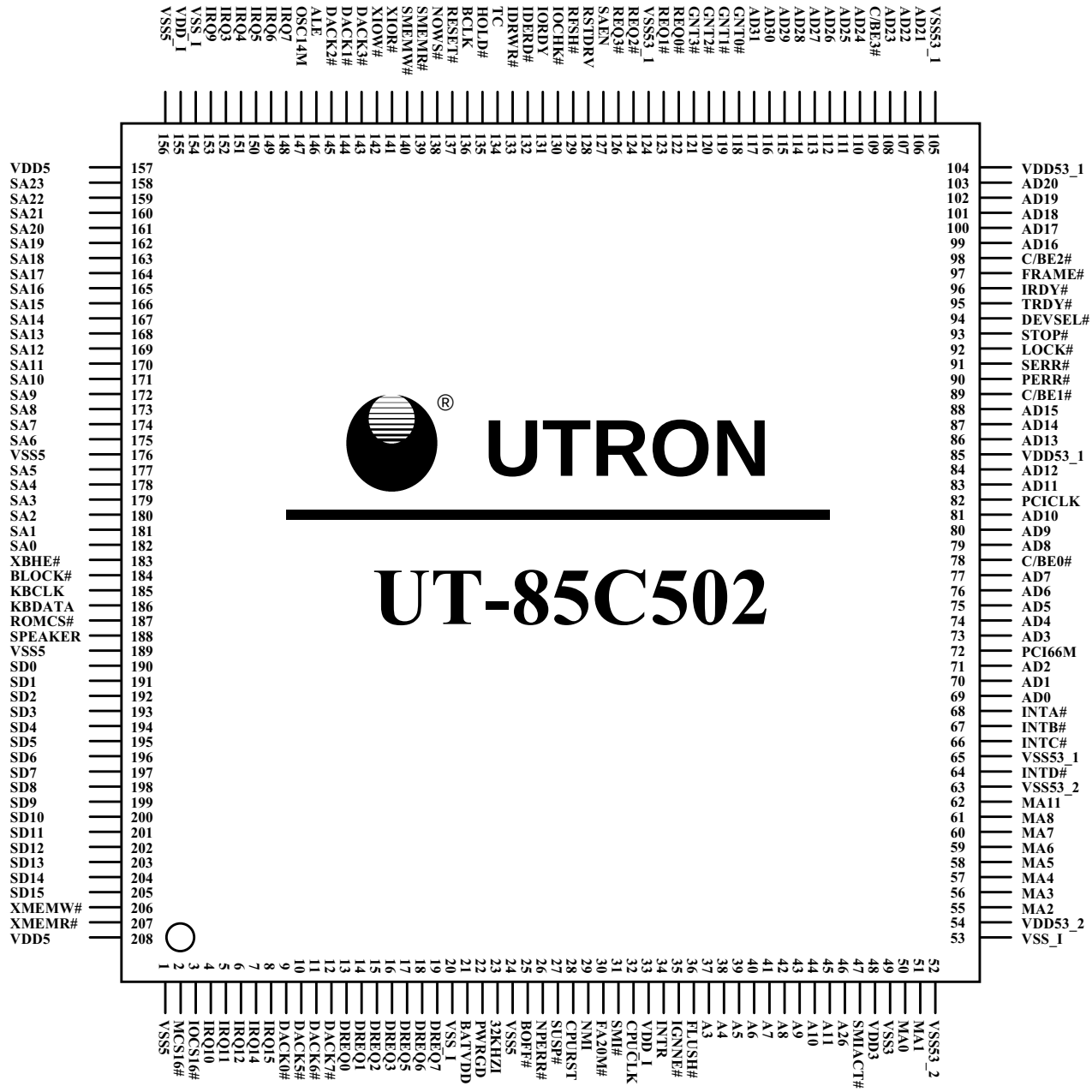
6	0 = IRQ<6(14)>Edge trigger 1 = IRQ<6(14)>Level trigger
5	0 = IRQ<5(13)>Edge trigger 1 = IRQ<5(13)>Level trigger
4	0 = IRQ<4(12)>Edge trigger 1 = IRQ<4(12)>Level trigger
3	0 = IRQ<3(11)>Edge trigger 1 = IRQ<3(11)>Level trigger
2	0 = IRQ<2(10)>Edge trigger 1 = IRQ<2(10)>Level trigger
1	0 = IRQ<1(9)>Edge trigger 1 = IRQ<1(9)>Level trigger
0	0 = IRQ<0(8)>Edge trigger 1 = IRQ<0(8)>Level trigger

4. Pin Assignment Diagram

4.1 UT85C501 Pin Diagram



4.2 UT85C502 Pin Diagram



Multiple functions pins :

Pin #158 : SA23 / IDECS3#
Pin #159 : SA22 / IDECS2#
Pin #160 : SA21 / IDECS1#
Pin #161 : SA20 / IDECS0#
Pin #162 : SA19 / IDEA2
Pin #163 : SA18 / IDEA1
Pin #163 : SA18 / IDEA0

5. Pin Lists

5.1 UT85C501 Pin Lists

No	Name	I/O	No	Name	I/O	No	Name	I/O
1	VSS53	GND	**71**	A4	5V	**141**	RESET#	5V
2	D63	5V	**72**	A5	5V	**142**	DRAMW# / ROM#	5V
3	D62	5V	**73**	A6	5V	**143**	MA9	5V
4	D61	5V	**74**	A7	5V	**144**	MA10	5V
5	D60	5V	**75**	A8	5V	**145**	VSS53	GND
6	D59	5V	**76**	A9	5V	**146**	RAS0#	5V
7	D58	5V	**77**	A10	5V	**147**	RAS1#	5V
8	D57	5V	**78**	A11	5V	**148**	RAS2#	5V
9	D56	5V	**79**	A12	5V	**149**	RAS3#	5V
10	D55	5V	**80**	A13	5V	**150**	CAS0#	5V
11	D54	5V	**81**	A14	5V	**151**	CAS1#	5V
12	D53	5V	**82**	A15	5V	**152**	CAS2#	5V
13	D52	5V	**83**	A16	5V	**153**	CAS3#	5V
14	D51	5V	**84**	A17	5V	**154**	CAS4#	5V
15	D50	5V	**85**	A18	5V	**155**	CAS5#	5V
16	D49	5V	**86**	A19	5V	**156**	VSS_I	GND
17	D48	5V	**87**	A20	5V	**157**	VDD_I	PWR
18	D47	5V	**88**	A21	5V	**158**	VSS53	GND
19	D46	5V	**89**	A22	5V	**159**	CAS6#	5V
20	D45	5V	**90**	A23	5V	**160**	CAS7#	5V
21	D44	5V	**91**	A24	5V	**161**	VDD53	PWR
22	D43	5V	**92**	A25	5V	**162**	PAR	5V
23	D42	5V	**93**	A26	5V	**163**	AD31	5V
24	D41	5V	**94**	A27	5V	**164**	AD30	5V
25	D40	5V	**95**	A28	5V	**165**	VDD_I	PWR
26	D39	5V	**96**	A29	5V	**166**	AD29	5V
27	D38	5V	**97**	A30	5V	**167**	AD28	5V
28	D37	5V	**98**	A31	5V	**168**	AD27	5V
29	D36	5V	**99**	BE0#	5V	**169**	AD26	5V
30	D35	5V	**100**	BE1#	5V	**170**	AD25	5V
31	D34	5V	**101**	BE2#	5V	**171**	AD24	5V
32	CPUCLK	5V	**102**	BE3#	5V	**172**	C/BE3#	5V
33	VSS3	GND	**103**	BE4#	5V	**173**	AD23	5V
34	D33	5V	**104**	VDD3	PWR	**174**	AD22	5V
35	D32	5V	**105**	BE5#	5V	**175**	AD21	5V
36	D31	5V	**106**	BE6#	5V	**176**	VDD53	PWR
37	D30	5V	**107**	BE7#	5V	**177**	AD20	5V
38	D29	5V	**108**	BRDY#	5V	**178**	AD19	5V
39	D28	5V	**109**	ADS#	5V	**179**	AD18	5V
40	D27	5V	**110**	M/IO#	5V	**180**	AD17	5V
41	D26	5V	**111**	W/R#	5V	**181**	AD16	5V
42	D25	5V	**112**	D/C#	5V	**182**	C/BE2#	5V
43	D24	5V	**113**	HITM#	5V	**183**	AD15	5V
44	D23	5V	**114**	AHOLD	5V	**184**	AD14	5V
45	D22	5V	**115**	BOFF#	5V	**185**	AD13	5V

46	D21	5V	**116**	KEN#	5V	**186**	AD12	5V
47	D20	5V	**117**	SMI#	5V	**187**	AD11	5V
48	D19	5V	**118**	NA#	5V	**188**	PCICLK	5V
49	D18	5V	**119**	CACHE#	5V	**189**	VSS53	GND
50	D17	5V	**120**	SMIACT#	5V	**190**	AD10	5V
51	D16	5V	**121**	OE#	5V	**191**	AD9	5V
52	VDD3	PWR	**122**	CW#/GW#	5V	**192**	AD8	5V
53	VSS3	GND	**123**	ACE#/CE1#	5V	**193**	C/BE1#	5V
54	D15	5V	**124**	VSS3	GND	**194**	AD7	5V
55	D14	5V	**125**	ADV#	5V	**195**	AD6	5V
56	D13	5V	**126**	ADSC#	5V	**196**	AD5	5V
57	D12	5V	**127**	TAGWR#	5V	**197**	AD4	5V
58	D11	5V	**128**	BWE#	5V	**198**	AD3	5V
59	D10	5V	**129**	ADS#	5V	**199**	AD2	5V
60	D9	5V	**130**	TAG0	5V	**200**	AD1	5V
61	D8	5V	**131**	TAG1	5V	**201**	AD0	5V
62	D7	5V	**132**	TAG2	5V	**202**	C/BE0#	5V
63	D6	5V	**133**	TAG3	5V	**203**	FRAME#	5V
64	D5	5V	**134**	TAG4	5V	**204**	DEVSEL#	5V
65	D4	5V	**135**	TAG5	5V	**205**	IRDY#	5V
66	D3	5V	**136**	TAG6	5V	**206**	TRDY#	5V
67	D2	5V	**137**	VSS_I	GND	**207**	STOP#	5V
68	D1	5V	**138**	TAG7	5V	**208**	VDD53	PWR
69	D0	5V	**139**	VSS3	GND			
70	A3	5V	**140**	HREQ#	5V			

5.2 UT85C502 Pin Lists

No	Name	I/O	No	Name	I/O	No	Name	I/O
1	VSS5	GND	**71**	AD2	5V	**141**	XIOR#	5V
2	MCS16#	5V	**72**	PCI66M	5V	**142**	XIOW#	5V
3	IOCS16#	5V	**73**	AD3	5V	**143**	DACK3#	5V
4	IRQ10	5V	**74**	AD4	5V	**144**	DACK1#	5V
5	IRQ11	5V	**75**	AD5	5V	**145**	DACK2#	5V
6	IRQ12	5V	**76**	AD6	5V	**146**	ALE	5V
7	IRQ14	5V	**77**	AD7	5V	**147**	OSC14M	5V
8	IRQ15	5V	**78**	C/BE0#	5V	**148**	IRQ7	5V
9	DACK0#	5V	**79**	AD8	5V	**149**	IRQ6	5V
10	DACK5#	5V	**80**	AD9	5V	**150**	IRQ5	5V
11	DACK6#	5V	**81**	AD10	5V	**151**	IRQ4	5V
12	DACK7#	5V	**82**	PCICLK	5V	**152**	IRQ3	5V
13	DREQ0	5V	**83**	AD11	5V	**153**	IRQ9	5V
14	DREQ1	5V	**84**	AD12	5V	**154**	VSS_I	GND
15	DREQ2	5V	**85**	VDD53_1	PWR	**155**	VDD_I	PWR
16	DREQ3	5V	**86**	AD13	5V	**156**	VSS5	GND
17	DREQ5	5V	**87**	AD14	5V	**157**	VDD5	PWR
18	DREQ6	5V	**88**	AD15	5V	**158**	SA23/IDECS3#	5V
19	DREQ7	5V	**89**	C/BE1#	5V	**159**	SA22/IDECS2#	5V
20	VSS_I	GND	**90**	PERR#	5V	**160**	SA21/IDECS1#	5V
21	BATVDD	PWR	**91**	SERR#	5V	**161**	SA20/IDECS0#	5V
22	PWRGD	3.3V	**92**	LOCK#	5V	**162**	SA19/IDEA2	5V
23	32KHZI	3.3V	**93**	STOP#	5V	**163**	SA18/IDEA1	5V
24	VSS5	PWR	**94**	DEVSEL#	5V	**164**	SA17/IDEA0	5V
25	BOFF#	3.3V	**95**	TRDY#	5V	**165**	SA16	5V
26	NPERR#	3.3V	**96**	IRDY#	5V	**166**	SA15	5V
27	SUSP#	3.3V	**97**	FRAME#	5V	**167**	SA14	5V
28	CPURST	3.3V	**98**	C/BE2#	5V	**168**	SA13	5V
29	NMI	3.3V	**99**	AD16	5V	**169**	SA12	5V
30	FA20M#	3.3V	**100**	AD17	5V	**170**	SA11	5V
31	SMI#	3.3V	**101**	AD18	5V	**171**	SA10	5V
32	CPUCLK	3.3V	**102**	AD19	5V	**172**	SA9	5V
33	VDD_I	PWR	**103**	AD20	5V	**173**	SA8	5V
34	INTR	3.3V	**104**	VDD53_1	PWR	**174**	SA7	5V
35	IGNNE#	3.3V	**105**	VSS53_1	GND	**175**	SA6	5V
36	FLUSH#	3.3V	**106**	AD21	5V	**176**	VSS5	GND
37	A3	3.3V	**107**	AD22	5V	**177**	SA5	5V
38	A4	3.3V	**108**	AD23	5V	**178**	SA4	5V
39	A5	3.3V	**109**	C/BE3#	5V	**179**	SA3	5V
40	A6	3.3V	**110**	AD24	5V	**180**	SA2	5V
41	A7	3.3V	**111**	AD25	5V	**181**	SA1	5V
42	A8	3.3V	**112**	AD26	5V	**182**	SA0	5V
43	A9	3.3V	**113**	AD27	5V	**183**	XBHE#	5V
44	A10	3.3V	**114**	AD28	5V	**184**	KBLOCK#	5V
45	A11	3.3V	**115**	AD29	5V	**185**	KBCLK	5V
46	A26	3.3V	**116**	AD30	5V	**186**	KBDATA	5V
47	SMIACT#	3.3V	**117**	AD31	5V	**187**	ROMCS#	5V
48	VDD3	PWR	**118**	GNT0#	5V	**188**	SPEAKER	5V
49	VSS3	GND	**119**	GNT1#	5V	**189**	VSS5	GND

50	MA0	5V	**120**	GNT2#	5V	**190**	SD0	5V
51	MA1	5V	**121**	GNT3#	5V	**191**	SD1	5V
52	VSS53_2	GND	**122**	REQ0#	5V	**192**	SD2	5V
53	VSS_I	GND	**123**	REQ1#	5V	**193**	SD3	5V
54	VDD53_2	PWR	**124**	VSS53_1	GND	**194**	SD4	5V
55	MA2	5V	**125**	REQ2#	5V	**195**	SD5	5V
56	MA3	5V	**126**	REQ3#	5V	**196**	SD6	5V
57	MA4	5V	**127**	SAEN	5V	**197**	SD7	5V
58	MA5	5V	**128**	RSTDRV	5V	**198**	SD8	5V
59	MA6	5V	**129**	RFSH#	5V	**199**	SD9	5V
60	MA7	5V	**130**	IOCHK#	5V	**200**	SD10	5V
61	MA8	5V	**131**	IORDY	5V	**201**	SD11	5V
62	MA11	5V	**132**	IDERD#	5V	**202**	SD12	5V
63	VSS53_2	GND	**133**	IDEWR#	5V	**203**	SD13	5V
64	INTD#	5V	**134**	TC	5V	**204**	SD14	5V
65	VSS53_1	GND	**135**	HOLD#	5V	**205**	SD15	5V
66	INTC#	5V	**136**	BCLK	5V	**206**	XMEMW#	5V
67	INTB#	5V	**137**	RESET#	5V	**207**	XMEMR#	5V
68	INTA#	5V	**138**	NOWS#	5V	**208**	VDD5	PWR
69	AD0	5V	**139**	SMEMR#	5V			
70	AD1	5V	**140**	SMEMW#	5V			

6. PIN Function Description

6.1 UT85C501 Signals

SIGNAL	PIN	I/O	DESCRIPTION
D[63:0]	2-31, 34-51, 54-69	I/O	Host CPU data bus
AD[31:0]	163,164 166-171, 173-175, 177-181, 183-187, 190-192, 194-201	I/O	PCI address/data bus
C/BE[3:0]#	172,182, 193,202	I/O	PCI command/byte enable. These pins indicate the PCI command during the address phase and the PCI byte enables during the data phase.
FRAME#	203	I/O	PCI cycle frame. This pin is an output to indicate the beginning of PCI access. When UT85C501 is PCI slave, it is input.
DEVSEL#	204	I/O	PCI device selects. When UT85C501 is PCI slave, this pin is an output. When UT85C501 is PCI master, it is input.
IRDY#	205	I/O	PCI initiator ready. This signal indicates the current CPU bus master is ability to complete the current data access. When UT85C501 is PCI slave, this pin is input. When UT85C501 is PCI master, it is an output.
TRDY#	206	I/O	PCI target ready. This signal indicates the target agent is ability to complete the current data access. When UT85C501 is PCI slave, this pin is an output. When UT85C501 is PCI master, it is input.
STOP#	207	I/O	PCI target request current transaction to stop. This signal indicates the bus master must stop the current PCI bus cycle and release the control of the PCI bus.
PCICLK	188	IN	PCI clock input.
BE[0:7]#	99-103, 105-107	I/O	CPU byte enables. These pins indicate which byte lanes on CPU data bus carry valid data during the current bus cycle.
A[3:31]	70-98	I/O	Address input from CPU, Bus masters or DMA controller. These pins are drive by CPU during CPU bus cycle. A17-23 can be programmed to output 1 or 0 during CPU Suspend at Reg. 1 bit 0.
CPUCLK	32	IN	System Clock Input

BRDY#	108	OUT	CPU Burst ready. This signal indicates the data are valid during a bus cycle.
ADS#	109	IN	CPU Address Strobe. This signal is driven by CPU to indicate the start of a CPU bus cycle.
M/IO#	110	IN	When high, this signal Memory access. When low, this signal I/O access
W/R#	111	I/O	When high, this signal Write access. When low, this signal Read access
D/C#	112	IN	When high, this signal indicate a data access. When low, this signal indicates a code access.
KEN#	116	O	This signal indicates the cache enable to CPU during CPU read cycle.
EADS#	129	OUT	Synchronous EADS# during DMA or Bus MASTER cycles.
HITM#	113	IN	Connect to HITM# pin of CPU. This signal indicates the snoop cycle hits a modified line in the L1 cache of CPU.
SMIACT#	120	IN	SMI acknowledgment input from CPU. This signal indicate that the SMI# was being acknowledged and the CPU is operating in the system management mode (SMM).
AHOLD	114	OUT	Active high to hold the address output from CPU.
BOFF#	115	OUT	Back-off output. This signal is connect to CPU and active low to stop the current CPU cycle.
CACHE#	119	IN	Cacheability input from CPU. This signal indicates an L1 internally cacheable read cycle or a burst write-back cycle.
NA#	118	OUT	Next address output. This pin is connect to CPU and indicate to CPU that it is ready to handle the second cycle.
HREQ#	140	IN	Hold request signal from UT85C502
RESET#	141	IN	Power-up reset
SMI#	117	IN	SMI request from UT85C502
TAG[0:7]	130-136, 138	I/O	Cache system tag
TAGWR#	127	OUT	Tag Write Enable
BWE#	128	OUT	Byte Write Enable, cache system
ACE#/CE1#	123	OUT	Cache signal
MA[9:10]	143,144	OUT	Used for DRAM access
RAS[0:3]#	146-149	I/O	DRAM RAS controls denoting the BANK being accessed. RAS2# pin can also be configured as IO pin A26 if the system has to support 128M total memory using 2 banks (RAS0-1#). In this mode, MA11 is always DRAM address and cannot be used as RAS3#.

CAS[0:7]#	150-155, 159-160	OUT	DRAM CAS controls defining the BYTE being accessed
DRAMW# / ROM#	142	OUT	DRAM Write enable ROM Write enable
CW# / GW#	122	OUT	Even or Single Bank Cache Write enable, becomes Global Write Enable when using synchronous SRAM.
OE#	121	OUT	Even or single bank output enable for PBSRAM to enable data read.
ADV#	125	OUT	Cache address advance for PBSRAM to advance the next data into the cache line.
ADSC#	126	OUT	Cache address strobe for synchronous PBSRAM.
PAR	162	OUT	Parity error output
VSS3	33,53, 124,139	PWR	GND pins
VSS_I	137,156	PWR	GND pins
VSS53	1,145, 158,189	PWR	GND pins
VDD3	52,104	PWR	3V Power pins
VDD_I	157,165	PWR	5V Power pin
VDD53	161,176, 208	PWR	3V/5V DRAM power pins

6.2 UT85C502 Signals

SIGNAL	PIN	I/O	DESCRIPTION
PCICLK	82	IN	PCI timing clock
PCI66M	72	IN	PCI clock speed selection input
FRAME#	97	I/O	PCI cycle frame. This pin is an output to indicate the beginning of PCI access. When UT85C502 is PCI slave, it is input.
DEVSEL#	94	I/O	PCI device select. When UT85C502 is PCI slave, this pin is an output. When UT85C502 is PCI master, it is input.
IRDY#	96	I/O	PCI initiator ready. This signal indicates the current CPU bus master is ability to complete the current data access. When UT85C502 is PCI slave, this pin is input. When UT85C502 is PCI master, it is an output.
TRDY#	95	I/O	PCI target ready. This signal indicates the target agent is ability to complete the current data access. When UT85C502 is PCI slave, this pin is an output. When UT85C502 is PCI master, it is input.

STOP#	93	I/O	PCI target request current transaction to stop. This signal indicates the bus master must stop the current PCI bus cycle and release the control of the PCI bus.
PERR#	90	I/O	PCI data parity error
SERR#	91	IN	PCI system errors input. This signal indicate that PCI device detect a system error condition.
C/BE[0:3]#	78,89, 98,109	I/O	PCI command/byte enable. These pins indicate the PCI command during the address phase and the PCI byte enables during the data phase.
AD[0:31]	69-71, 73-77, 79-81, 83-84, 86-88, 99-103, 106-108, 110-117	I/O	PCI address/data lines
REQ[0:3]#	122,123, 125,126	IN	PCI bus request from PCI devices, active low.
GNT[0:3]#	118-121	OUT	PCI bus grant. These signals indicate the PCI bus request that from PCI device has been granted.
LOCK#	92	IN	PCI lock. This signal indicates an exclusive bus operation that may require multiple transaction to complete.
INTA-D#	68,67, 66,64	IN	PCI interrupt inputs.
CPUCLK	32	IN	Host clock input.
CPURST	28	OUT	Synchronous CPU Reset. This is an active high output to reset CPU.
NMI	29	OUT	Non-maskable interrupt. This is an interrupt request to CPU to invoke a non-maskable interrupt.
SMI#	31	OUT	System management interrupt request. This pin is connected to CPU and active low to generate SMI interrupt.
SMIACT#	47	IN	SMI acknowledgment input from CPU. This signal indicate that the SMI# was being acknowledged and the CPU is operating in the system management mode (SMM).
SUSP#	27	OUT	Suspend request. This pin is connected to CPU and active low to generate suspends request.
INTR	34	OUT	Interrupt line to CPU.
FLUSH#	36	OUT	For Intel CPU mode, this is FLUSH. For AMD CPU mode, this is SMI Ready For Cyrix CPU mode, this is Suspend Acknowledge
FA20M#/	30	OUT	FAST A20 GATE output to CPU.

IGNNE#	35	OUT	This is ignore numeric error output and it is normally in high impedance state.
NPERR#	26	IN	Numeric processor error input.
BOFF#	25	IN	Back-off signal from UT85C501.
SPEAKER	188	OUT	Speaker output
OSC14M	147	IN	14.318MHz Oscillator input
PWRGD	22	IN	active high Power Good or Reset Switch input. This input is debounced by internal monostable
RESET#	137	OUT	Power-up reset
HOLD#	135	OUT	Connect to UT85C501 request signal
32KHZI	23	IN	32KHZ clock input
BATVDD	21	IN	Battery input
KBDATA	186	I/O	Keyboard data
KBCLK	185	I/O	Keyboard clock
KBLOCK#	184	IN	Keyboard inhibit
A[3:11], A26	37-46	IN	CPU address lines
IRQ[3:7], IRQ[9:12], IRQ[14:15]	152-148, 153,4-8	IN	Interrupt lines from external devices
DREQ[0:3], DREQ[5:7]	13-19	IN	DMA request, active high. These input pins are used by external device to indicate that they need internal DMA controller.
DACK[0:3]#, DACK[5:7]#	9,144, 145,43, 10,11,12	OUT	DMA acknowledge output, active low.
SD[0:15]	190-205	I/O	Slot data bus
SA[0:16]	182-177, 175-165	I/O	Slot address
SA[17:19] / IDEA[0:2]	164-162	I/O	ISA address bus. These pins are used as IDE address during the IDE cycle.
SA[20:23] / IDECS[0:3]#	161-158	I/O	ISA address bus. These pins are used as IDE device select during the IDE cycle. IDE[0:1]# are used for primary IDE. IDE[2:3]# are used for secondary IDE.
BCLK	136	OUT	Programmable Speed Bus Clock Output
ALE	146	OUT	ISA address latch enable. This pin is used on ISA bus to latch valid address from CPU.
XMEMR#	207	I/O	Slot Memory Read Command
XMEMW#	206	I/O	Slot Memory Write Command
XIOR#	141	I/O	Slot IO Read Command
XIOW#	142	I/O	Slot IO Write Command
SMEMR#	139	OUT	8 bit Slot Memory Read Command If Reg. 13h bit 1 is set to 1, this is address decoded less than 1M output active low output

SMEMW#	140	OUT	8 bit Slot Memory Write Command If Reg. 13h bit 1 is set to 1, this is Main memory access decoded active low output
XBHE#	183	I/O	Byte High Enable
MCS16#	2	I/O	ISA slot 16-bit memory device active. This pin is driven during access to main memory.
IOCS16#	3	IN	I/O 16-bit device select. This signal indicates the AT bus cycle is a 16-bit I/O access.
NOWS#	138	IN	ISA slot No Wait State input
IORDY	131	I/O	IO Channel Ready
IOCHK#	130	IN	IO Channel Check
SAEN	127	OUT	Slot address enable
RFSH#	129	I/O	ISA slot refresh. This signal is used to initiate a refresh cycle.
RSTDRV	128	OUT	Reset drive to slot
TC	134	I/O	Terminal count for DMA
IDERD#	132	OUT	IDE write command
IDEWR#	133	OUT	IDE read command
ROMCS#	187	OUT	BIOS control
MA[0:8], MA11	50,51, 55-62	OUT	DRAM address
VSS3	49	PWR	GND pin
VSS5	1,24, 156,176, 189	PWR	GND pins
VSS_I	20,53, 154	PWR	GND pins
VSS53_1 VSS53_2	65,105, 124, 52,63	PWR	GND pins
VDD3	48	PWR	3V power pin
VDD5	157,208	PWR	5V power pins
VDD_I	33,155	PWR	5V power pins
VDD53_1 VDD53_2	85,104, 54	PWR	DRAM 3V/5V power pins

7. Electrical Characteristic

7.1 Absolute Maximum Rating (Preliminary)

Permanent device damage may occur if absolute maximum ratings are exceeded.

Sym	Description	Ratings	Unit
VDD	Supply Voltage	-0.3 ~ +7.0	V
VI	Input Voltage	-0.3 ~ +0.3	V
VO	Output Voltage	-0.3 ~ +0.3	V
Topr	Operating Temperature	-40 ~ +70	°C
Tstg	Storage Temperature	-55 ~ +150	°C

Input/Output Capacitance

Sym	Description	Min	Typ	Max	Unit
Cin	Input Terminal		7	15	pF
Cout	Output Terminal		7	15	pF
Ci/o	I/O Terminal		7	15	pF

DC Characteristics

Sym	Description	Min	Typ	Max	Unit
Vil	Input Low Voltage (TTL level)	0.0		0.8	V
Vih	Input High Voltage (TTL level)	2.4		VDD	V
Vol	Output Low Voltage			0.4	V
Voh	Output High Voltage	2.4			V
Iil	Input Leakage Current			10	uA
Ioz	Tristate Leakage Current			10	uA
Ilp	Input/Tristate with Pull-up Leakage Current			20	uA

***PWRGD* Input (CMOS Schmitt)**

Vt+c	Input Low Threshold Voltage	1.0	2.1		V
Vt-c	Input High Threshold Voltage		2.9	4.0	V

High Drive Signal Groups

Signal Name: *MA0-11#, RAS0-2#, CAS0-3#, RAMWR#, CPURDY#, BRDY#, SD0-15, SA0-23, SALE, SMEMR#, SMEMW# , MCS16#*

Sym	Description	Min	Typ	Max	Unit
Ioh	Peak Output Current	-8			mA
Iol	Peak Input Current			24	mA

Signal Name: others

Sym	Description	Min	Typ	Max	Unit
Ioh	Peak Output Current	-2			mA
Iol	Peak Input Current			4	mA

7.2 AC Timing Characteristics (Preliminary)

Temperature: 0-70°C, VCC: 5V ± 5%, Typical PC Application Loading
Time unit in ***ns*** unless otherwise specificed.

CPU Interface

Sym	Description	Min	Typ	Max
T0	CLK↑ to CPURST active/inactive delay	5	10	15
T1	CLK↓ to CPURST active/inactive delay	5	10	15
T2	CLK↑ to BRDY# active/inactive delay	5	10	15
T3	CLK↑ to KEN# active/inactive delay	5	10	15
T4	CLK↑ to EADS# active/inactive delay	5		15
T5	CLK↑ to AHOLD active/inactive delay	5		15
T6	CLK↑ to BOFF# active/inactive delay	5		15
T7	CLK↑ to SMI active/inactive delay	5		15
T8	CLK↑ to SUSP# active/inactive delay	5		15
T9	CLK↑ to FLUSH# active/inactive delay	5		15

PCI Bus Interface

Sym	Description	Min	Typ	Max
T10	CLK↑ to AD0-31 active/inactive delay	5	8	15

Cache Interface

Sym	Description	Min	Typ	Max
T11	CLK↑ to GW# active delay	5	13	20
T12	CLK↑ to OE0# active/inactive delay	5	10	15
T13	CLK↑ to TAGOE# active/inactive delay	5	10	15
T14	CLK↑ to TAGWR# active/inactive delay	5	7	15

DRAM Interface

Sym	Description	Min	Typ	Max
T15	CLK↑ to RAS0-3# active/inactive delay	5	9	20
T16	CLK↑ to CAS0-3# active/inactive delay	5	9	20
T17	WR input valid to DRAMW# active delay	5	10	20
T18	CLK↑ to MA0-11 active/inactive delay	5		40

AT BUS Interface

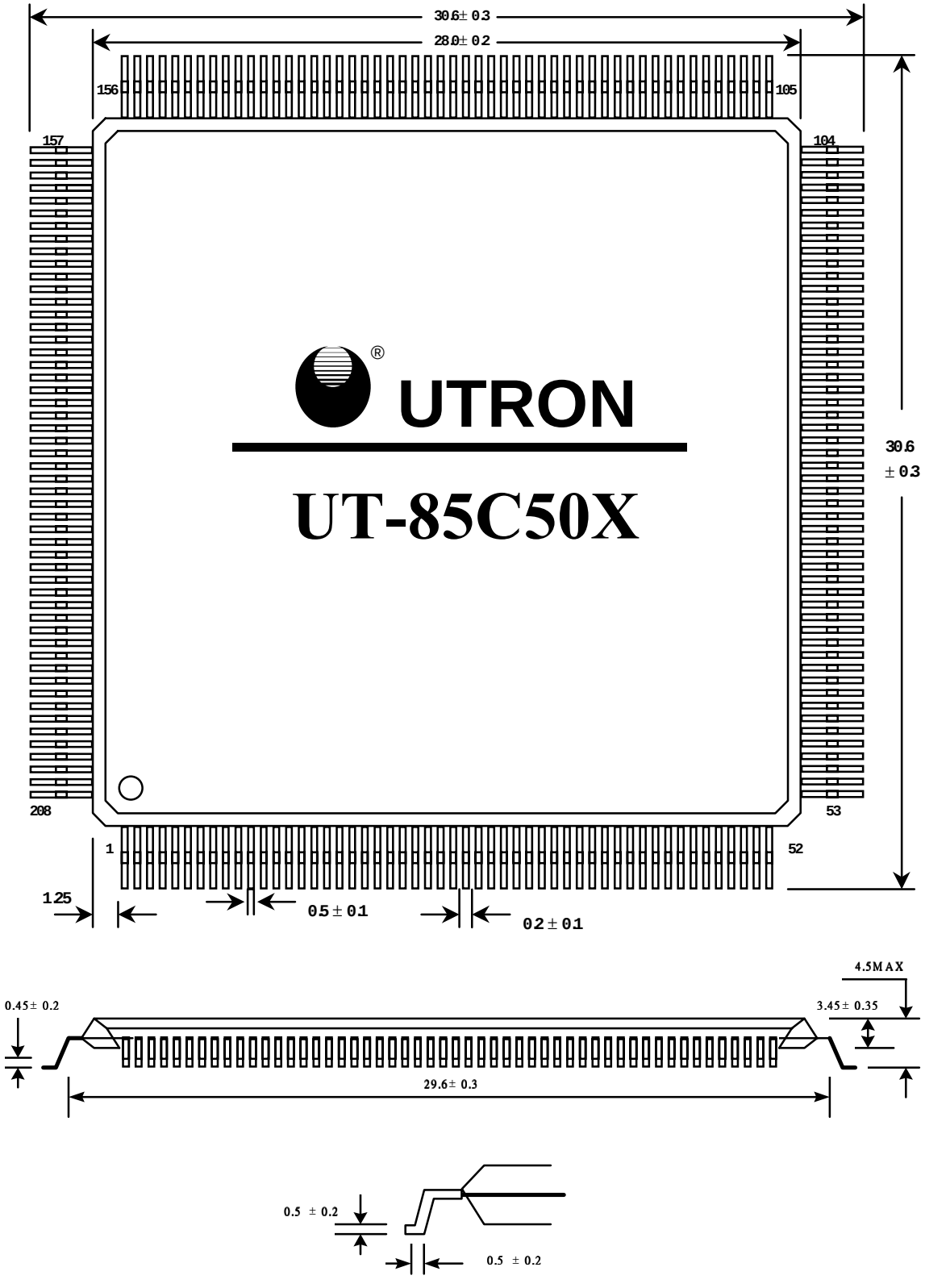
Sym	Description	Min	Typ	Max
T19	BCLK↑ to ALE active delay		4	30
T20	BCLK↓ to ALE inactive delay			30
T21	BCLK↑ to 16 bit CMD active/inactive delay		9	30
T22	BCLK↓ to 8 bit CMD active delay		9	30
T23	BCLK↑ to 8 bit CMD inactive delay			30
T24	BCLK↑ to RFSH# active/inactive delay			30
T25	NOWS# setup time to BCLK↑	10		
T26	NOWS# hold time from BCLK↑	10		
T27	MCS16# setup time to BCLK↑	10		
T28	MCS16# hold time from BCLK↑	10		
T29	IOCS16# setup time to BCLK↑	25		
T30	IOCS16# hold time from BCLK↑	10		
T31	IORDY# setup time to BCLK↑	10		
T32	IORDY# hold time from BCLK↑	10		

System Controls

Sym	Description	Min	Typ	Max
T33	CLK↑ to RESET inactive delay	5		40

8. Mechanical Dimension

208-Pin Plastic Flat Package (Unit:mm)



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