UM82C210 Series
386SX/286 AT Chip Set

Features

* 100% PC/AT compatible enhanced chip set for 12 Mhz, 16 Mhz and 20 Mhz systems.
* Supports Page Interleaved Mode & Single Bank Page Mode for memory access.
* Supports 16 Mhz 80286/80386SX systems with 100 ns DRAMs and 20 Mhz systems with 80 ns DRAMs.
* Separated CPU and AT Bus clocks.
* Supports LIM EMS 4.0.
* Programmable memory configuration , Command Delays , and Wait States.
* Supports Shadow RAM for Video ROM and BIOS.
* Optimized for OS/2 operation.

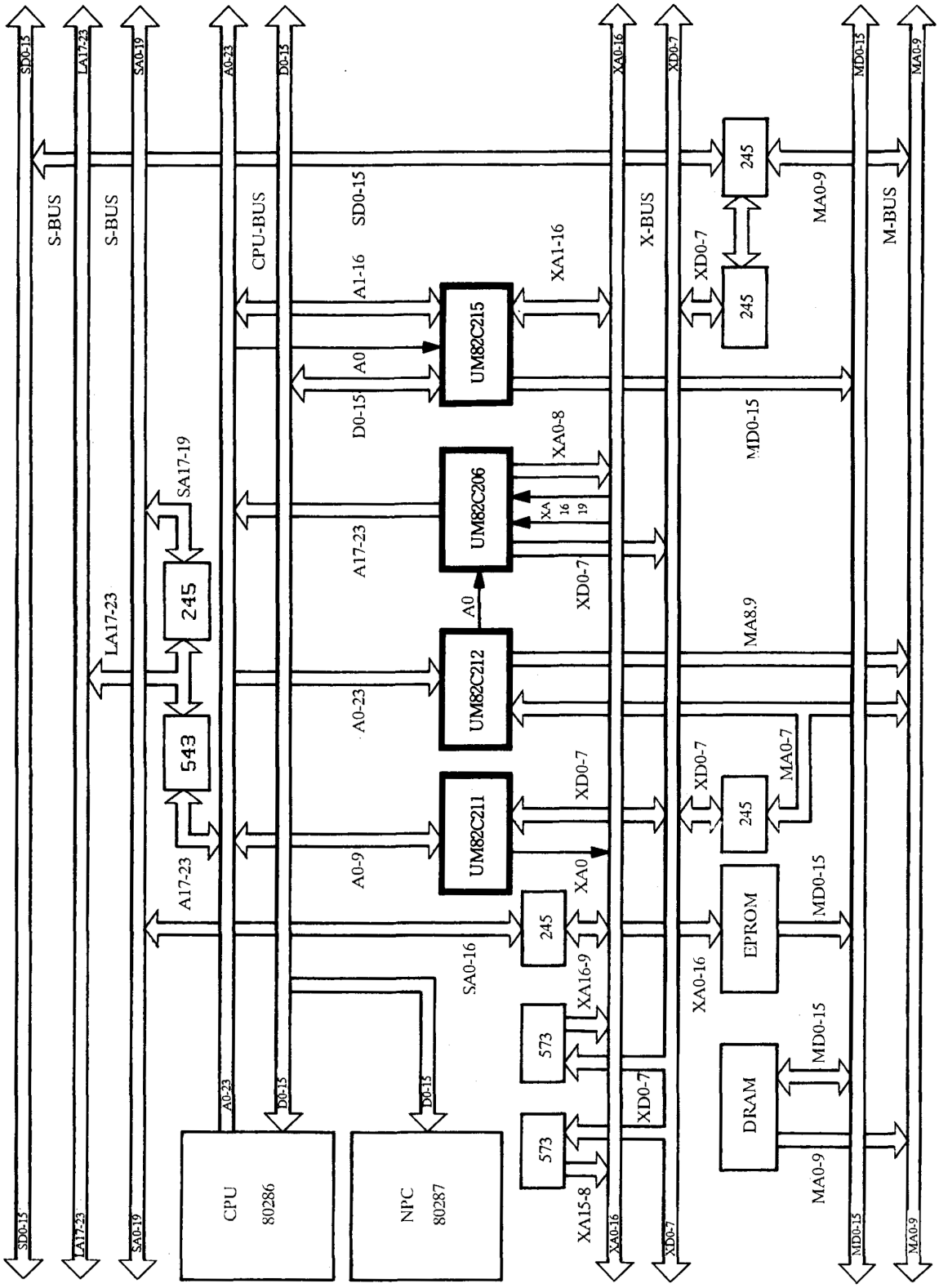
General Description

The UM82C210 is an enhanced PC/AT compatible chip set which is a highly integrated VLSI implementation of the control logic used in the IBM AT. Due to its flexible architecture, the UM82C210 can be used in any 80286 based systems. The UM82C210 chip set consists of three chips which are: UM82C211 (System Controller), UM82C212 (Memory Controller) , and UM82C215 (Data /Address Buffer).

The UM82C211 , System controller, provides all control signals for AT bus including bus synchronization. In order to meet timing requirements for different peripheral boards, the UM82C211 provides programmable command delays and wait states.

The UM82C212 , Memory Controller, provides both conventional memory access and Page Interleaved memory access. The UM82C212 also has LIM EMS features that support up to 8 MB of on-board DRAMs. In addition, the Shadow RAM feature of the UM82C212 allows faster execution BIOS codes.

The UM82C215, Data/Address Buffer, provides buffering and latching functions between address buses and data buses. It also generates the parity bit and detects parity errors.



16/20-MHZ AT System Block Diagram