Pentium PCI/AGP Chipset

SiS5591/5592

Preliminary

Rev. 1.0

January 9, 1998

1. SiS5591/5592 SiS5595 OVERVIEW

SiS5591/5592 ***PCI A.G.P. & CPU Memory Controller***
SiS5595 ***PCI SYSTEM I/O***

The SiS5591/5592 SiS5595 glueless P5 A.G.P. chipset provides a high performance/cost index Desktop/Mobile solution for the Intel Pentium P54C/P55C, AMD K5/K6, and Cyrix M1/M2 A.G.P. system.

The SiS5591/SiS5592 A.G.P./PCI controller integrated the Host-to-PCI bridge, the L2 cache controller, the DRAM controller, the Accelerated Graphics Port interface, and the PCI IDE controller. The L2 cache controller can support up to 1 M P.B. SRAM, and the DRAM controller can support EDO/FP/SDRAM memory up to 768 MB with optional ECC or parity check function. The A.G.P. 1.0 compliance interface supports both 1X, and 2X speed mode with sideband address capability. The built-in fast PCI IDE controller supports the ATA PIO/DMA, and the Ultra DMA/33 functionality.

SiS5591 and SiS5592 have some pin-out switching to facilitate the main-board layout. SiS5591 pin assignment is based on the ATX form factor, and SiS5592 pin assignment is based on the NLX form factor. Beside the pin-out switching, SiS5591 and SiS5592 is totally the same on the internal logic circuit.

The SiS5595 PCI system I/O integrates the PCI-to-ISA bridge with the DDMA, and Serial IRQ capability, the ACPI/Legacy PMU, the Data Acquisition Interface, the Universal Serial Bus host/hub interface, and the ISA bus interface which contains the ISA bus controller, the DMA controllers, the interrupt controllers, and the Timers. It also integrates the Keyboard controller, and the Real Time Clock (RTC). The built-in USB controller, which is fully compliant to OHCI (Open Host Controller Interface), provides two USB ports capable of running full/low speed USB devices. The Data Acquisition Interface offers the ability of monitoring and reporting the environmental condition of the PC. It could monitor 4 positive analogue voltage inputs, 2 Fan speed inputs, and one temperature input.

The following page will show the system block diagram.

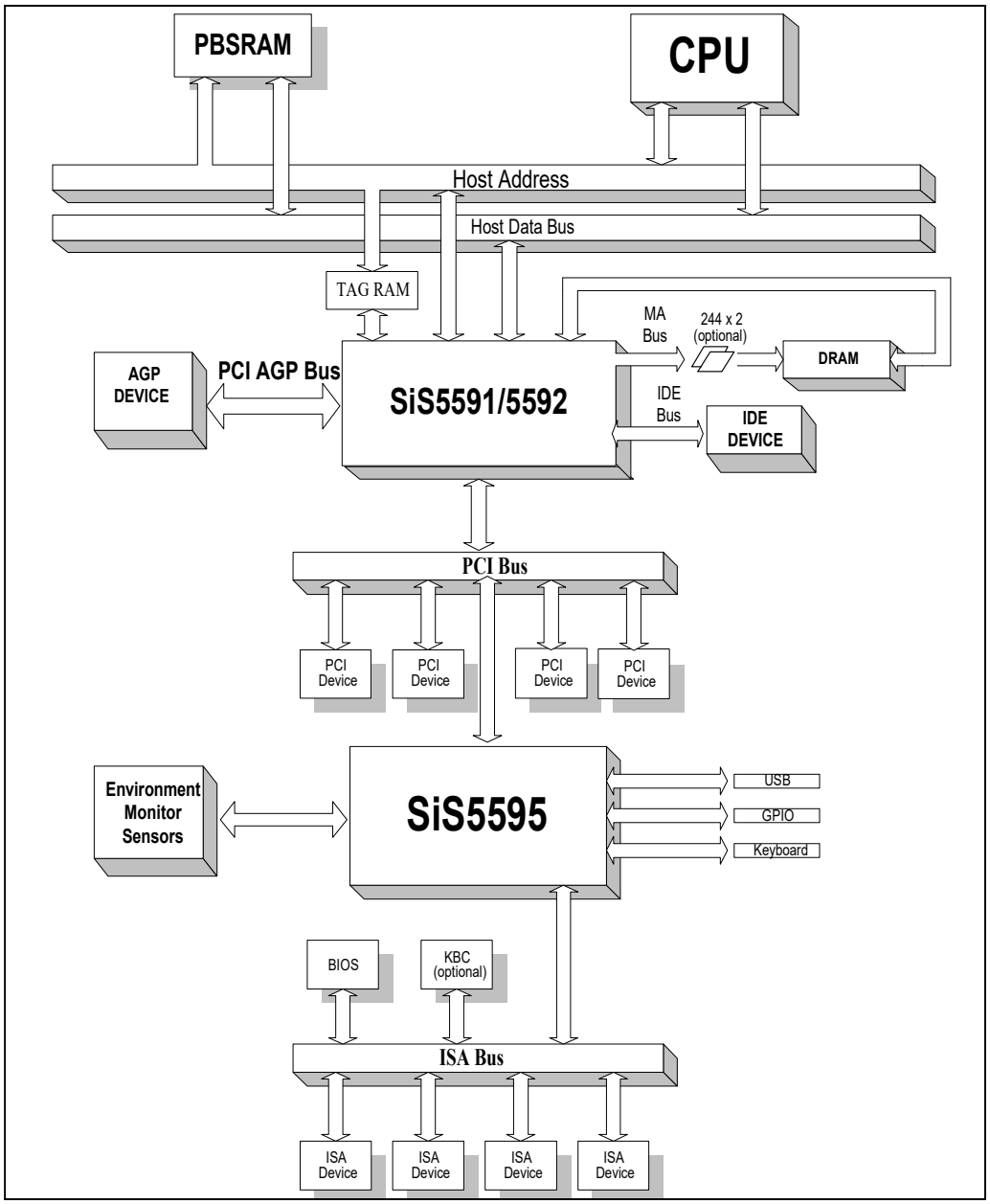


Figure 1-1 SiS5591/5592 SiS5595 System Block Diagram

2. FEATURE

2.1 SiS5591/5592 PCI A.G.P. CONTROLLER

- **Support Intel/AMD/Cyrix Pentium CPU and Other Compatible CPU Host Bus at 60/66 MHz and 3.3V Bus Interface**
  - Support the Pipelined Address of Pentium compatible CPU
  - Support the Linear Address Mode of Cyrix CPU
- **Support the Pipelined Address Mode of Pentium CPU**
- **Fully Compliant to A.G.P. Revision 1.0 Specification**
- **Meet PC97 Requirements**
- **Supports PCI Revision 2.1 Specification**
- **Integrated Second Level (L2) Cache Controller**
  - Write Back Cache Mode
  - Support L2 Cache Flushing for entire L2 cache or specific 4K page
  - 8 bits or 7 bits Tag with Direct Mapped Cache Organization
  - Integrated 32K bits Dirty SRAM
  - Integrated 32K bits Invalid SRAM
  - Support Pipelined Burst SRAM
  - Support 256K/512K/1MBytes Cache Sizes
  - Cache Hit Read/Write Cycle of 3-1-1-1
  - Cache Back-to-Back Read/Write Cycle of 3-1-1-1-1-1-1-1
  - Support Single Read Allocation for L2 Cache
  - Support Concurrency of CPU to L2 cache and A.G.P. master to DRAM accesses
- **Integrated DRAM Controller**
  - Support 6 RAS Lines for FPM/EDO/SDRAM DIMMs/SIMMs
  - Support 2Mbytes to 768Mbytes of main memory
  - Support Cacheable DRAM Sizes up to 256 MBytes.
  - Support 256K/512K/1M/2M/4M/8M/16Mx N FPM/EDO/SDRAM DRAM
  - Support 64 Mb DRAM Technology
  - Support Parity Checker or ECC Function
  - Support 3.3V or 5V DRAM
  - Supports Symmetrical and Asymmetrical DRAM
  - Support Concurrent Write Back
  - Support CAS before RAS Refresh, Self Refresh
  - Support Relocation of System Management Memory
  - Programmable CAS#, RAS#, RAMWE# and MA Driving Current
  - Fully Configurable for the Characteristic of Shadow RAM (640 KBytes to 1 MBytes)
  - Support FPM DRAM 5/6-3-3-3(-3-3-3-3) Burst Read Cycles
  - Support EDO DRAM 5/6-2-2-2(-2-2-2-2) Burst Read Cycles
  - Support SDRAM 5/6/7-1-1-1(-2/3-1-1-1) Burst Read Cycles

- Support X-1-1-1/X-2-2-2/X-3-3-3 Burst Write Cycles
- Two Programmable Non-cacheable Regions
- Option to Disable Local Memory in Non-cacheable Regions
- Shadow RAM in Increments of 16 Kbytes
- Pseudo Directory/Page Scheme for Mapping Graphical Texture Access to Physical Memory Address
- Built-in 8 Way Associative/16 Entries GART cache to Minimize the Number of Memory Bus Cycles Required for Accessing Graphical Texture Memory
- Programmable Counters to Ensure Guaranteed Minimum Access Time for A.G.P., CPU, and PCI accesses

v **Provides High Performance PCI Arbiter.**
- Support up to 5 PCI Masters
- Support Rotating Priority Mechanism
- Hidden Arbitration Scheme Minimizes Arbitration Overhead.
- Support Concurrency between CPU to Memory and PCI to PCI
- Support Concurrency between CPU to 33Mhz PCI Access and 33Mhz PCI to A.G.P. Access
- Support Concurrency between CPU to 66Mhz PCI Access and A.G.P. to 33Mhz PCI Access
- Programmable Timers Ensure Guaranteed Minimum Access Time for PCI Bus Masters, and CPU

v **Integrated Host-to-PCI Bridge**
- Support Asynchronous and Synchronous PCI Clock
- Translates the CPU Cycles into the PCI Bus Cycles
- Zero Wait State Burst Cycles
- Support IDE Posted Write
- Support Pipelined Process in CPU-to-PCI Access
- Support Advance Snooping for PCI Master Bursting
- Maximum PCI Burst Transfer from 256 Bytes to 4 Kbytes
- Support Memory Remapping Function for PCI master accessing Graphical Window

v **Integrated A.G.P. Compliant Target/66Mhz Host-to-PCI Bridge**
- Support Asynchronous and Synchronous A.G.P. Clock
- Support 1X, and 2X Mode for A.G.P. 66/133 MHz 3.3V device
- Support Graphic Window Size from 4Mbytes to 256Mbytes
- Different arbitration policy for A.G.P. devices and 66Mhz PCI devices.
- Translates Sequential CPU-to-A.G.P. Memory Write Cycles into A.G.P. Bus (PCI66) Burst Cycles
- Zero Wait State Burst Cycles
- Support Pipelined Process in CPU-to-A.G.P. Access
- Support Advance Snooping for A.G.P. Master initiate system memory access with PCI Cycles
- Support 8 Way, 16 Entries Page Table Cache to enhance A.G.P. Read/Write Performance
- Support Both 1-Level and 2-Level GART(Graphic Address Re-Mapping Table)
- Maximum PCI Burst Transfer from 256 Bytes to 4 Kbytes
- Programmable Counters to Ensure Guaranteed Minimum Access Time for Low Priority Request, CPU to A.G.P./and A.G.P. Master Transaction
- Support PCI-to-PCI bridge function for memory write from 33Mhz PCI bus to A.G.P. bus

v **Integrated Posted Write Buffers and Read Prefetch Buffers to Increase System Performance**

- CPU-to-Memory Posted Write Buffer (CTMFF) with 8 QW Deep, Always Sustains 0 Wait Performance on CPU-to-Memory
- CPU-to-Memory Read Buffer with 4 QW Deep
- CPU-to-PCI Posted Write Buffer(CTPFF) with 8 DW Deep
- PCI-to-Memory Posted Write Buffer(PTHFF) with 8 QW Deep, Always Streams 0 Wait Performance on PCI-to/from-Memory Access
- PCI-to-Memory Read Prefetch Buffer(CTPFF) with 8 QW Deep
- CPU-to-PCI66 Posted Write Buffer(CTAFF) with 8 DW Deep
- PCI66-to-Memory Posted Write Buffer(ATHFF) with 8 QW Deep
- A.G.P. Request Queue With the Depth of 32
- A.G.P. High Priority Write Queue with 64 QW Deep
- A.G.P. Low Priority Write Queue with 64 QW Deep
- A.G.P. High Priority Read Return Queue with 64 QW Deep
- A.G.P. Low Priority Read Return Queue with 64 QW Deep

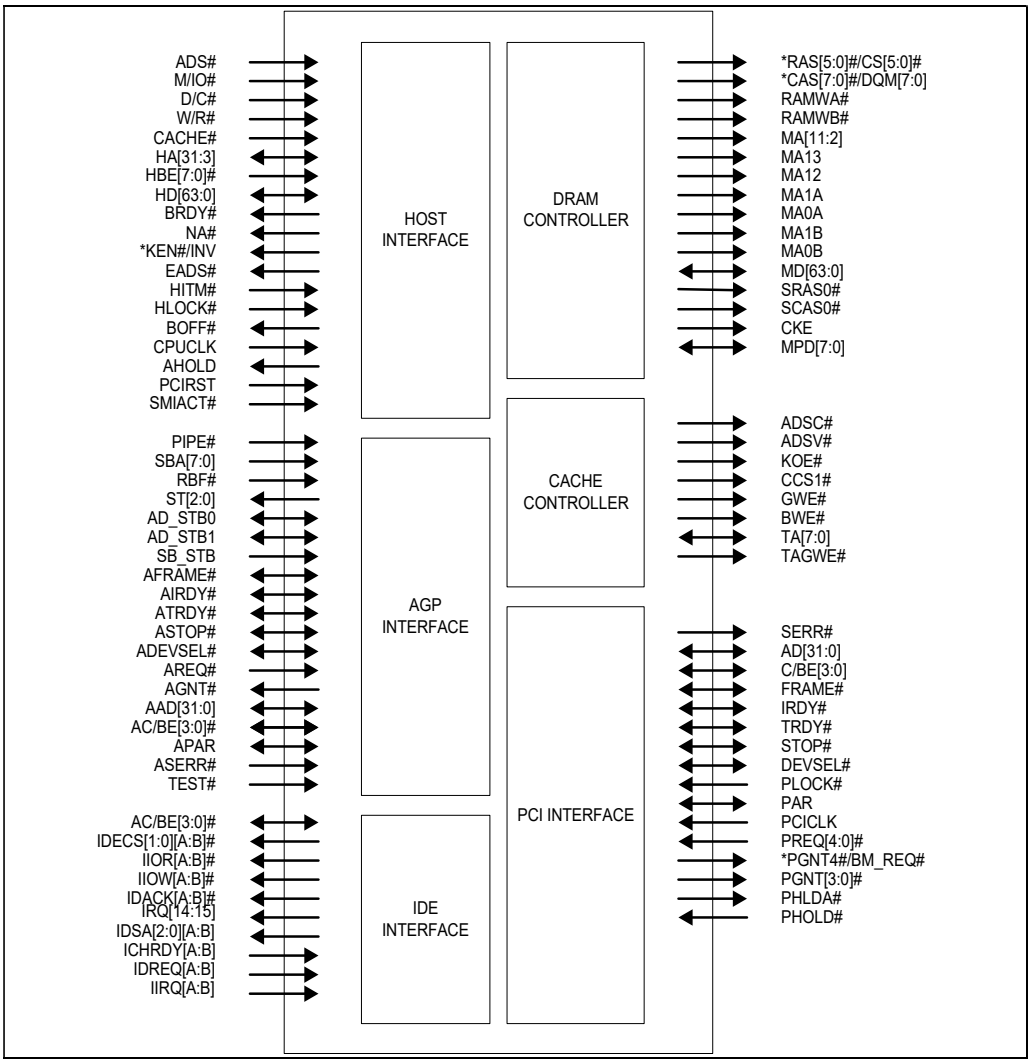
v **Fast PCI IDE Master/Slave Controller**
- Bus Master Programming Interface for ATA Windows 95 Compliant Controller
- Plug and Play Compatible
- Support Scatter and Gather
- Support Dual Mode Operation - Native Mode and Compatibility Mode
- Support IDE PIO Timing Mode 0, 1, 2 ,3 and 4
- Support Multiword DMA Mode 0, 1, 2
- Support Ultra DMA/33
- Two Separate IDE Bus
- Two 16 DW FIFO for PCI Burst Transfers.

v **Support NAND Tree for Ball Connectivity Testing**

v **553-Balls BGA Package**

v **0.35µm 3.3V CMOS Technology**

2.2 FUNCTIONAL BLOCK DIAGRAM



***Multi-function pins**

KEN#/INV RAS[5:0]#/CS[5:0]# CAS[7:0]#/DQM[7:0]

PGNT4#/BM_REQ#

Figure 2.2-1 SiS5591/5592 Functional Block Diagram

3. PIN ASSIGNMENT

3.1 SiS5591 PIN ASSIGNMENT (TOP VIEW)

SiS5591 Pin Assignment (Top View-Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A			NC	MD1	MD35	MD5	MD40	MD9	MD11	MD13	MD15	MPD1	CAS4#	RAS5#	RAS1#	A
B		MD32	MD0	MD34	MD3	MD38	MD8	MD10	MD44	MD46	MPD4	SCAS#	CAS0#	RAS4#	RAS0#	B
C	NC	5VDD	MD33	MD2	MD36	MD6	MD41	MD43	MD12	MD14	MPD0	RAMWA#	CAS5#	RAS3#	SRAS#	C
D	SBA0	ST2	ST1	ST0	MD4	MD7	VSSG	VSSG	VSSG	MD39	MD42	MD47	CAS1#	RAS2#	MA0B	D
E	SB_STB	SBA3	SBA2	SBA1	MD37	NC	NC	NC	NC	NC	MD45	MPD5	VSSG	VSSG	DVDD	E
F	AGNT#	SBA7	SBA6	SBA5	SBA4								NC	NC	DVDD	F
G	AAD30	AAD31	PIPE#	VSSG	AREQ#											G
H	AAD27	AAD28	AAD29	VSSG	NC											H
J	AD_STB1	AAD25	AAD26	RBF#	NC											J
K	AAD21	AAD22	AAD23	AAD24	NC							OVDD3	OVDD3			K
L	AAD18	AAD19	AAD20	AC/BE3#	NC											L
M	VREF	VREFVSS	AC/BE2#	AAD16	AAD17					OVDD3		VSS	VSS	OVDD2	OVDD2	M
N	ADEVSEL#	ATRDY#	AIRDY#	VREFVDD	AFRAME#	NC				OVDD3		VSS	VSS	VSS	OVDD2	N
P	AAD15	AC/BE1#	ASTOP#	APAR	ASERR#	NC						VSS	VSS	VSS	VSS	P
R	AAD11	AAD12	AAD13	AAD14	DVDD	DVDD						OVDD2	OVDD2	VSS	VSS	R
T	AC/BE0#	AD_STB0	AAD8	AAD9	AAD10	NC						VSS	VSS	VSS	VSS	T
U	AAD3	AAD4	AAD5	AAD6	AAD7	NC				OVDD3		VSS	VSS	VSS	OVDD2	U
V	BM_REQ#	AAD0	AAD1	PHLDA#	AAD2					OVDD3		VSS	VSS	OVDD2	OVDD2	V
W	AGPCLK	PHOLD#	PREQ4#	TEST_PIN	PCIRST#											W
Y	PLLVSS	PLLVDD	VSSP	PGNT2#	PGNT0#							OVDD3	OVDD3			Y
AA	PREQ2#	PREQ1#	PREQ0#	VSSG	AD29											AA
AB	PGNT3#	PREQ3#	PGNT1#	AD20	C/BE3#											AB
AC	AD28	AD30	AD31	VSSG	AD16											AC
AD	AD23	AD24	AD25	AD26	AD27								DVDD	DVDD	DVDD	AD
AE	AD18	AD19	AD21	AD22	AD12	C/BE0#	PLOCK#	PAR	AD9	AD3	IDA8	IDA3	IIORA	IDSA2A	DVDD	AE
AF	IRDY#	FRAME#	C/BE2#	AD17	AD11	AD6	STOP#	AD13	AD7	IRQ14	IDA10	IDA1	IDACKA	IDECS0A	IDB6	AF
AG	NC	TRDY#	5VDD	C/BE1#	AD10	AD5	AD1	IDA7	IDA5	IDA12	IDA14	IDREQA	IIRQA	IDECS1A	IDB9	AG
AH		DEVSEL#	SERR#	AD15	AD8	AD4	AD0	IDA6	IDA4	IDA2	IDA0	IIOWA	IDSA1A	IDB7	IDB5	AH
AJ			NC	AD14	PCICLK	AD2	IRQ15	IDA9	IDA11	IDA13	IDA15	ICHRDYA	IDSA0A	IDB8	IDB10	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 3.1-0-1 SiS5591/5592 Pin Assignment (Left Side)

SiS5591 Pin Assignment (Top View-Right Side)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	MA0A	MA3	MA7	MA11	CAS6#	RAMWB#	MPD2	MD48	MD20	MD53	MD22	NC			A
B	MA1B	MA4	MA8	MA12	CAS2#	CKE	MPD7	MD16	MD18	MD21	5VDD	MD23	MD25		B
C	MA1A	MA5	MA10	MA13	CAS3#	MPD6	MPD3	MD49	MD51	MD54	MD55	MD56	MD26	NC	C
D	MA2	MA6	MA9	CAS7#	VSSG	VSSG	VSSG	MD17	MD19	MD57	MD29	MD28	MD60	MD27	D
E	NC	NC	NC	NC	NC	NC	NC	MD50	MD52	MD24	HD0	MD31	MD30	MD62	E
F	NC	NC								VSSG	MD58	HD5	HD3	HD1	F
G										MD59	HD10	HD9	HD7	HD6	G
H										MD63	MD61	HD13	HD14	HD12	H
J										HD4	HD2	HD17	HD16	HD18	J
K		OVDD3	OVDD3							HD11	HD8	HD19	HD21	HD20	K
L										HD22	HD15	HD25	HD26	HD23	L
M	VSS	VSS	VSS		OVDD3					HD28	HD24	HD29	HD30	HD27	M
N	VSS	VSS	VSS		OVDD3				DVDD	HD31	HD34	HD35	HD32	HD33	N
P	VSS	VSS	VSS						DVDD	HD39	HD42	HD38	HD36	HD37	P
R	VSS	OVDD2	OVDD2						DVDD	DVDD	HD41	HD44	HD46	HD40	R
T	VSS	VSS	VSS						DVDD	HD45	HD50	HD48	HD47	HD43	T
U	VSS	VSS	VSS		OVDD3				DVDD	HD49	HD53	HD51	HD52	CPUCLK	U
V	VSS	VSS	VSS		OVDD3					HD60	HD56	HD57	HD55	HD54	V
W										ADSC#	HD63	HD61	HD59	HD58	W
Y		OVDD3	OVDD3							TA2	TA7	BWE#	GWE#	HD62	Y
AA										BRDY#	M/IO#	CCS1#	ADV#	KOE#	AA
AB										EADS#	HLOCK#	TA5	TA6	TAGWE#	AB
AC										HBE4#	HBE1#	TA1	TA3	TA4	AC
AD	DVDD	DVDD								NA#	AHOLD	KEN#/INV	CACHE#	TA0	AD
AE	IDB4	IDB14	VSSG	IDECS0B	HA25	HA6	VSSG	HA20	HA4	HA9	D/C#	ADS#	SMIACT#	BOFF#	AE
AF	IDB11	IDB13	IIRQB	HA24	HA30	HA10	HA16	HBE6#	HA7	HA12	HBE2#	HBE0#	W/R#	HITM#	AF
AG	IDB3	IDB1	IDREQB	ICHRDYB	IDSA0B	HA23	HA22	HA28	HA5	HA13	HA17	HEB7#	HBE3#	NC	AG
AH	IDB12	IDB0	IIOWB	IDACKB	IDSA2B	HA21	HA26	HA29	HA8	HA15	HA18	HBE5#	5VDD		AH
AJ	IDB2	IDB15	IIORB	IDSA1B	IDECS1B	HA27	HA31	HA3	HA11	HA14	HA19	NC			AJ
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 3.1-0-2 SiS5591 Pin Assignment (Right Side)

3.2 SiS5592 PIN ASSIGNMENT (TOP VIEW)

SiS5592 Pin Assignment (Top View-Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A			NC	AD14	PCICLK	AD2	IRQ15	IDA9	IDA11	IDA13	IDA15	ICHRDYA	IDSA0A	IDB8	IDB10	A
B		DEVSEL#	SERR#	AD15	AD8	AD4	AD0	IDA6	IDA4	IDA2	IDA0	IIOWA#	IDSA1A	IDB7	IDB5	B
C	NC	TRDY#	5VDD	C/BE1#	AD10	AD5	AD1	IDA7	IDA5	IDA12	IDA14	IDREQA	IIRQA	IDECS1A#	IDB9	C
D	IRDY#	FRAME#	C/BE2#	AD17	AD11	AD6	STOP#	AD13	AD7	IRQ14	IDA10	IDA1	IDACKA#	IDECS0A#	IDB6	D
E	AD18	AD19	AD21	AD22	AD12	C/BE0#	PLOCK#	PAR	AD9	AD3	IDA8	IDA3	IIORA#	IDSA2A	DVDD	E
F	AD23	AD24	AD25	AD26	AD27								DVDD	DVDD	DVDD	F
G	AD28	AD30	AD31	VSSG	AD16											G
H	PGNT3#	PREQ3#	PGNT1#	AD20	C/BE3#											H
J	PREQ2#	PREQ1#	PREQ0#	VSSG	AD29											J
K	PLLVSS	PLLVDD	VSSP	PGNT2#	PGNT0#							OVDD3	OVDD3			K
L	AGPCLK	PHOLD#	PREQ4#	TEST_PIN	PCIRST#											L
M	REQ#/PGN	AAD0	AAD1	PHLDA#	AAD2					OVDD3		VSS	VSS	OVDD2	OVDD2	M
N	AAD3	AAD4	AAD5	AAD6	AAD7	NC				OVDD3		VSS	VSS	VSS	OVDD2	N
P	AC/BE0#	AD_STB0	AAD8	AAD9	AAD10	NC						VSS	VSS	VSS	VSS	P
R	AAD11	AAD12	AAD13	AAD14	DVDD	DVDD						OVDD2	OVDD2	VSS	VSS	R
T	AAD15	AC/BE1#	ASTOP#	APAR	ASERR#	NC						VSS	VSS	VSS	VSS	T
U	ADEVSEL#	ATRDY#	AIRDY#	VREFVDD	AFRAME#	NC				OVDD3		VSS	VSS	VSS	OVDD2	U
V	VREF	VREFVSS	AC/BE2#	AAD16	AAD17					OVDD3		VSS	VSS	OVDD2	OVDD2	V
W	AAD18	AAD19	AAD20	AC/BE3#	NC											W
Y	AAD21	AAD22	AAD23	AAD24	NC							OVDD3	OVDD3			Y
AA	AD_STB1	AAD25	AAD26	RBF#	NC											AA
AB	AAD27	AAD28	AAD29	VSSG	NC											AB
AC	AAD30	AAD31	PIPE#	VSSG	AREQ#											AC
AD	AGNT#	SBA7	SBA6	SBA5	SBA4								NC	NC	DVDD	AD
AE	SB_STB	SBA3	SBA2	SBA1	MD37	NC	NC	NC	NC	NC	MD45	MPD5	VSSG	VSSG	DVDD	AE
AF	SBA0	ST2	ST1	ST0	MD4	MD7	VSSG	VSSG	VSSG	MD39	MD42	MD47	CAS1#	RAS2#	MA0B	AF
AG	NC	5VDD	MD33	MD2	MD36	MD6	MD41	MD43	MD12	MD14	MPD0	RAMWA#	CAS5#	RAS3#	SRAS#	AG
AH		MD32	MD0	MD34	MD3	MD38	MD8	MD10	MD44	MD46	MPD4	SCAS#	CAS0#	RAS4#	RAS0#	AH
AJ			NC	MD1	MD35	MD5	MD40	MD9	MD11	MD13	MD15	MPD1	CAS4#	RAS5#	RAS1#	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 3.2-0-1 SiS5592 Pin Assignment (Left Side)

SiS5592 Pin Assignment (Top View-Right Side)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	IDB2	IDB15	IIORB#	IDSA1B	IDECS1B#	HA27	HA31	HA3	HA11	HA14	HA19	NC			A
B	IDB12	IDB0	IIOWB#	IDACKB#	IDSA2B	HA21	HA26	HA29	HA8	HA15	HA18	HBE5#	5VDD		B
C	IDB3	IDB1	IDREQB	ICHRDYB	IDSA0B	HA23	HA22	HA28	HA5	HA13	HA17	HEB7#	HBE3#	NC	C
D	IDB11	IDB13	IIRQB	HA24	HA30	HA10	HA16	HBE6#	HA7	HA12	HBE2#	HBE0#	W/R#	HITM#	D
E	IDB4	IDB14	VSSG	IDECS0B#	HA25	HA6	VSSG	HA20	HA4	HA9	D/C#	ADS#	SMIACT#	BOFF#	E
F	DVDD	DVDD								NA#	AHOLD	KEN#/INV	CACHE#	TA0	F
G										HBE4#	HBE1#	TA1	TA3	TA4	G
H										EADS#	HLOCK#	TA5	TA6	TAGWE#	H
J										BRDY#	M/IO#	CCS1#	ADV#	KOE#	J
K		OVDD3	OVDD3							TA2	TA7	BWE#	GWE#	HD62	K
L										ADSC#	HD63	HD61	HD59	HD58	L
M	VSS	VSS	VSS		OVDD3					HD60	HD56	HD57	HD55	HD54	M
N	VSS	VSS	VSS		OVDD3				DVDD	HD49	HD53	HD51	HD52	CPUCLK	N
P	VSS	VSS	VSS						DVDD	HD45	HD50	HD48	HD47	HD43	P
R	VSS	OVDD2	OVDD2						DVDD	DVDD	HD41	HD44	HD46	HD40	R
T	VSS	VSS	VSS						DVDD	HD39	HD42	HD38	HD36	HD37	T
U	VSS	VSS	VSS		OVDD3				DVDD	HD31	HD34	HD35	HD32	HD33	U
V	VSS	VSS	VSS		OVDD3					HD28	HD24	HD29	HD30	HD27	V
W										HD22	HD15	HD25	HD26	HD23	W
Y		OVDD3	OVDD3							HD11	HD8	HD19	HD21	HD20	Y
AA										HD4	HD2	HD17	HD16	HD18	AA
AB										MD63	MD61	HD13	HD14	HD12	AB
AC										MD59	HD10	HD9	HD7	HD6	AC
AD	NC	NC								VSSG	MD58	HD5	HD3	HD1	AD
AE	NC	NC	NC	NC	NC	NC	NC	MD50	MD52	MD24	HD0	MD31	MD30	MD62	AE
AF	MA2	MA6	MA9	CAS7#	VSSG	VSSG	VSSG	MD17	MD19	MD57	MD29	MD28	MD60	MD27	AF
AG	MA1A	MA5	MA10	MA13	CAS3#	MPD6	MPD3	MD49	MD51	MD54	MD55	MD56	MD26	NC	AG
AH	MA1B	MA4	MA8	MA12	CAS2#	CKE	MPD7	MD16	MD18	MD21	5VDD	MD23	MD25		AH
AJ	MA0A	MA3	MA7	MA11	CAS6#	RAMWB#	MPD2	MD48	MD20	MD53	MD22	NC			AJ
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 3.2-2 SiS5592 Pin Assignment (Right Side)

3.3 SiS5591/5592 ALPHABETICAL PIN LIST

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
5VDD	B26	AH26
5VDD	C2	AG2
5VDD	AG3	C3
5VDD	AH28	B28
AAD0	V2	M2
AAD1	V3	M3
AAD2	V5	M5
AAD3	U1	N1
AAD4	U2	N2
AAD5	U3	N3
AAD6	U4	N4
AAD7	U5	N5
AAD8	T3	P3
AAD9	T4	P4
AAD10	T5	P5
AAD11	R1	R1
AAD12	R2	R2
AAD13	R3	R3
AAD14	R4	R4
AAD15	P1	T1
AAD16	M4	V4
AAD17	M5	V5
AAD18	L1	W1
AAD19	L2	W2
AAD20	L3	W3
AAD21	K1	Y1
AAD22	K2	Y2
AAD23	K3	Y3
AAD24	K4	Y4
AAD25	J2	AA2
AAD26	J3	AA3
AAD27	H1	AB1
AAD28	H2	AB2
AAD29	H3	AB3
AAD30	G1	AC1
AAD31	G2	AC2
AC/BE0#	T1	P1
AC/BE1#	P2	T2
AC/BE2#	M3	V3
AC/BE3#	L4	W4
AD_STB0	T2	P2
AD_STB1	J1	AA1
AD00	AH7	B7
AD01	AG7	C7
AD02	AJ6	A6
AD03	AE10	E10
AD04	AH6	B6
AD05	AG6	C6
AD06	AF6	D6

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
AD07	AF9	D9
AD08	AH5	B5
AD09	AE9	E9
AD10	AG5	C5
AD11	AF5	D5
AD12	AE5	E5
AD13	AF8	D8
AD14	AJ4	A4
AD15	AH4	B4
AD16	AC5	G5
AD17	AF4	D4
AD18	AE1	E1
AD19	AE2	E2
AD20	AB4	H4
AD21	AE3	E3
AD22	AE4	E4
AD23	AD1	F1
AD24	AD2	F2
AD25	AD3	F3
AD26	AD4	F4
AD27	AD5	F5
AD28	AC1	G1
AD29	AA5	J5
AD30	AC2	G2
AD31	AC3	G3
ADEVSEL#	N1	U1
ADS#	AE27	E27
ADSC#	W25	L25
ADV#	AA28	J28
AFRAME#	N5	U5
AGNT#	F1	AD1
A.G.P.CLK	W1	L1
AHOLD	AD26	F26
AIRDY#	N3	U3
APAR	P4	T4
AREQ#	G5	AC5
ASERR#	P5	T5
ASTOP#	P3	T3
ATRDY#	N2	U2
BM_REQ#/	V1	M1
BOFF#	AE29	E29
BRDY#	AA25	J25
BWE#	Y27	K27
C/BE0#	AE6	E6
C/BE1#	AG4	C4
C/BE2#	AF3	D3
C/BE3#	AB5	H5
CACHE#	AD28	F28

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
CAS0#DQM	B13	AH13
CAS1#/DQM	D13	AF13
CAS2#/DQM2	B20	AH20
CAS3#/DQM3	C20	AG20
CAS4#/DQM4	A13	AJ13
CAS5#/DQM5	C13	AG13
CAS6#/DQM6	A20	AJ20
CAS7#/DQM7	D19	AF19
CCS1#	AA27	J27
CKE	B21	AH21
CPUCLK	U29	N29
D/C#	AE26	E26
DEVSEL#	AH2	B2
DVDD	E15	AE15
DVDD	F15	AD15
DVDD	N24	U24
DVDD	P24	T24
DVDD	R5	R5
DVDD	R6	R6
DVDD	R24	R24
DVDD	R25	R25
DVDD	T24	P24
DVDD	U24	N24
DVDD	AD13	F13
DVDD	AD14	F14
DVDD	AD15	F15
DVDD	AD16	F16
DVDD	AD17	F17
DVDD	AE15	E15
EADS#	AB25	H25
FRAME#	AF2	D2
GWE#	Y28	K28
HA3	AJ23	A23
HA4	AE24	E24
HA5	AG24	C24
HA6	AE21	E21
HA7	AF24	D24
HA8	AH24	B24
HA9	AE25	E25
HA10	AF21	D21
HA11	AJ24	A24
HA12	AF25	D25
HA13	AG25	C25
HA14	AJ25	A25
HA15	AH25	B25
HA16	AF22	D22
HA17	AG26	C26
HA18	AH26	B26
HA19	AJ26	A26
HA20	AE23	E23
HA21	AH21	B21

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
HA22	AG22	C22
HA23	AG21	C21
HA24	AF19	D19
HA25	AE20	E20
HA26	AH22	B22
HA27	AJ21	A21
HA28	AG23	C23
HA29	AH23	B23
HA30	AF20	D20
HA31	AJ22	A22
HBE0#	AF27	D27
HBE1#	AC26	G26
HBE2#	AF26	D26
HBE3#	AG28	C28
HBE4#	AC25	G25
HBE5#	AH27	B27
HBE6#	AF23	D23
HBE7#	AG27	C27
HD0	E26	AE26
HD1	F29	AD29
HD2	J26	AA26
HD3	F28	AD28
HD4	J25	AA25
HD5	F27	AD27
HD6	G29	AC29
HD7	G28	AC28
HD8	K26	Y26
HD9	G27	AC27
HD10	G26	AC26
HD11	K25	Y25
HD12	H29	AB29
HD13	H27	AB27
HD14	H28	AB28
HD15	L26	W26
HD16	J28	AA28
HD17	J27	AA27
HD18	J29	AA29
HD19	K27	Y27
HD20	K29	Y29
HD21	K28	Y28
HD22	L25	W25
HD23	L29	W29
HD24	M26	V26
HD25	L27	W27
HD26	L28	W28
HD27	L29	W29
HD28	M25	V25
HD29	M27	V27
HD30	M28	V28

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
HD31	N25	U25
HD32	N28	U28
HD33	N29	U29
HD34	N26	U26
HD35	N27	U27
HD36	P28	T28
HD37	P29	T29
HD38	P27	T27
HD39	P25	T25
HD40	R29	R29
HD41	R26	R26
HD42	P26	T26
HD43	T29	P29
HD44	R27	R27
HD45	T25	P25
HD46	R28	R28
HD47	T28	P28
HD48	T27	P27
HD49	U25	N25
HD50	T26	P26
HD51	U27	N27
HD52	U28	N28
HD53	U26	N26
HD54	V29	M29
HD55	V28	M28
HD56	V26	M26
HD57	V27	M27
HD58	W29	L29
HD59	W28	L28
HD60	V25	M25
HD61	W27	L27
HD62	Y29	K29
HD63	W26	L26
HITM#	AF29	D29
HLOCK#	AB26	H26
ICHRDYA	AJ12	A12
ICHRDYB	AG19	C19
IDACKA#	AF13	D13
IDACKB#	AH19	B19
IDA0	AH11	B11
IDA1	AF12	D12
IDA2	AH10	B10
IDA3	AE12	E12
IDA4	AH9	B9
IDA5	AG9	C9
IDA6	AH8	B8
IDA7	AG8	C8
IDA8	AE11	E11
IDA9	AJ8	A8

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
IDA10	AF11	D11
IDA11	AJ9	A9
IDA12	AG10	C10
IDA13	AJ10	A10
IDA14	AG11	C11
IDA15	AJ11	A11
IDB0	AH17	B17
IDB1	AG17	C17
IDB2	AJ16	A16
IDB3	AG16	C16
IDB4	AE16	E16
IDB5	AH15	B15
IDB6	AF15	D15
IDB7	AH14	B14
IDB8	AJ14	A14
IDB9	AG15	C15
IDB10	AJ15	A15
IDB11	AF16	D16
IDB12	AH16	B16
IDB13	AF17	D17
IDB14	AE17	E17
IDB15	AJ17	A17
IDECS0A#	AF14	D14
IDECS1A#	AG14	C14
IDECS0B#	AE19	E19
IDECS1B#	AJ20	A20
IDREQA#	AG12	C12
IDREQB#	AG18	C18
IDSA0A	AJ13	A13
IDSA1A	AH13	B13
IDSA2A	AE14	E14
IDSA0B	AG20	C20
IDSA1B	AJ19	A19
IDSA2B	AH20	B20
IIORA	AE13	E13
IIORB	AJ18	A18
IIOWA	AH12	B12
IIOWB	AH18	B18
IIRQA	AG13	C13
IIRQB	AF18	D18
IRDY#	AF1	D1
IRQ14	AF10	D10
IRQ15	AJ7	A7
KEN#/INV	AD27	F27
KOE#	AA29	J29
M/IO#	AA26	J26
MA0A	A16	AJ16
MA0B	D15	AF15
MA1A	C16	AG16

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
MA1B	B16	AH16
MA2	D16	AF16
MA3	A17	AJ17
MA4	B17	AH17
MA5	C17	AG17
MA6	D17	AF17
MA7	A18	AJ18
MA8	B18	AH18
MA9	D18	AF18
MA10	C18	AG18
MA11	A19	AJ19
MA12	B19	AH19
MA13	C19	AG19
MD0	B3	AH3
MD1	A4	AJ4
MD2	C4	AG4
MD3	B5	AH5
MD4	D5	AF5
MD5	A6	AJ6
MD6	C6	AG6
MD7	D6	AF6
MD8	B7	AH7
MD9	A8	AJ8
MD10	B8	AH8
MD11	A9	AJ9
MD12	C9	AG9
MD13	A10	AJ10
MD14	C10	AG10
MD15	A11	AJ11
MD16	B23	AH23
MD17	D23	AF23
MD18	B24	AH24
MD19	D24	AF24
MD20	A24	AJ24
MD21	B25	AH25
MD22	A26	AJ26
MD23	B27	AH27
MD24	E25	AE25
MD25	B28	AH28
MD26	C28	AG28
MD27	D29	AF29
MD28	D27	AF27
MD29	D26	AF26
MD30	E28	AE28
MD31	E27	AE27
MD32	B2	AH2
MD33	C3	AG3
MD34	B4	AH4
MD35	A5	AJ5

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
MD36	C5	AG5
MD37	E5	AE5
MD38	B6	AH6
MD39	D10	AF10
MD40	A7	AJ7
MD41	C7	AG7
MD42	D11	AF11
MD43	C8	AG8
MD44	B9	AH9
MD45	E11	AE11
MD46	B10	AH10
MD47	D12	AF12
MD48	A23	AJ23
MD49	C23	AG23
MD50	E23	AE23
MD51	C24	AG24
MD52	E24	AE24
MD53	A25	AJ25
MD54	C25	AG25
MD55	C26	AG26
MD56	C27	AG27
MD57	D25	AF25
MD58	F26	AD26
MD59	G25	AC25
MD60	D28	AF28
MD61	H26	AB26
MD62	E29	AE29
MD63	H25	AB25
MPD0	C11	AG11
MPD1	A12	AJ12
MPD2	A22	AJ22
MPD3	C22	AG22
MPD4	B11	AH11
MPD5	E12	AE12
MPD6	C21	AG21
MPD7	B22	AH22
NA#	AD25	F25
NC	A3	AJ3
NC	A27	AJ27
NC	C1	AG1
NC	C29	AG29
NC	E6	AE6
NC	E7	AE7
NC	E8	AE8
NC	E9	AE9
NC	E10	AE10
NC	E16	AE16
NC	E17	AE17
NC	E18	AE18

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
NC	E19	AE19
NC	E20	AE20
NC	E21	AE21
NC	E22	AE22
NC	F13	AD13
NC	F14	AD14
NC	F16	AD16
NC	F17	AD17
NC	H5	AB5
NC	J5	AA5
NC	K5	Y5
NC	L5	W5
NC	N6	U6
NC	P6	T6
NC	T6	P6
NC	U6	N6
NC	AG1	C1
NC	AG29	C29
NC	AJ3	A3
NC	AJ27	A27
OVDD2	M14	V14
OVDD2	M15	V15
OVDD2	N15	U15
OVDD2	U15	N15
OVDD2	R12	R12
OVDD2	R13	R13
OVDD2	R17	R17
OVDD2	R18	R18
OVDD2	V14	M14
OVDD2	V15	M15
OVDD3	K12	Y12
OVDD3	K13	Y13
OVDD3	K17	Y17
OVDD3	K18	Y18
OVDD3	M10	V10
OVDD3	M20	V20
OVDD3	N10	U10
OVDD3	N20	U20
OVDD3	U10	N10
OVDD3	U20	N20
OVDD3	V10	M10
OVDD3	V20	M20
OVDD3	Y12	K12
OVDD3	Y13	K13
OVDD3	Y17	K17
OVDD3	Y18	K18
PAR	AE8	E8
PCICLK	AJ5	A5
PCIRST#	W5	L5

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
PGNT0#	Y5	K5
PGNT1#	AB3	H3
PGNT2#	Y4	K4
PGNT3#	AB1	H1
PHLDA#	V4	M4
PHOLD#	W2	L2
PIPE#	G3	AC3
PLLVDD	Y2	K2
PLLVSS	Y1	K1
PLOCK#	AE7	E7
PREQ0#	AA3	J3
PREQ1#	AA2	J2
PREQ2#	AA1	J1
PREQ3#	AB2	H2
PREQ4#	W3	L3
RAMWA#	C12	AG12
RAMWB#	A21	AJ21
RAS0#/CS0#	B15	AH15
RAS1#/CS1#	A15	AJ15
RAS2#/CS2#	D14	AF14
RAS3#/CS3#	C14	AG14
RAS4#/CS4#	B14	AH14
RAS5#/CS5#	A14	AJ14
RBF#	J4	AA4
SBA0	D1	AF1
SBA1	E4	AE4
SBA2	E3	AE3
SBA3	E2	AE2
SBA4	F5	AD5
SBA5	F4	AD4
SBA6	F3	AD3
SBA7	F2	AD2
SB_STB	E1	AE1
SCAS#	B12	AH12
SERR#	AH3	B3
SMIACT#	AE28	E28
SRAS#	C15	AG15
STOP#	AF7	D7
ST0	D4	AF4
ST1	D3	AF3
ST2	D2	AF2
TAGWE#	AB29	H29
TA0	AD29	F29
TA1	AC27	G27
TA2	Y25	K25
TA3	AC28	G28
TA4	AC29	G29
TA5	AB27	H27
TA6	AB28	H28

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
TA7	Y26	K26
TEST_PIN#	W4	L4
TRDY#	AG2	C2
VREF	M1	V1
VREFVDD	N4	U4
VREFVSS	M2	V2
VSS	M12	V12
VSS	M13	V13
VSS	M16	V16
VSS	M17	V17
VSS	M18	V18
VSS	N12	U12
VSS	N13	U13
VSS	N14	U14
VSS	N16	U16
VSS	N17	U17
VSS	N18	U18
VSS	P12	T12
VSS	P13	T13
VSS	P14	T14
VSS	P15	T15
VSS	P16	T16
VSS	P17	T17
VSS	P18	T18
VSS	R14	R14
VSS	R15	R15
VSS	R16	R16
VSS	T12	P12
VSS	T13	P13
VSS	T14	P14
VSS	T15	P15
VSS	T16	P16
VSS	T17	P17
VSS	T18	P18

SIGNAL NAME	SiS5591 BALL NO.	SiS5592 BALL NO.
VSS	U12	N12
VSS	U13	N13
VSS	U14	N14
VSS	U16	N16
VSS	U17	N17
VSS	U18	N18
VSS	V12	M12
VSS	V13	M13
VSS	V16	M16
VSS	V17	M17
VSS	V18	M18
VSSG	D7	AF7
VSSG	D8	AF8
VSSG	D9	AF9
VSSG	D20	AF20
VSSG	D21	AF21
VSSG	D22	AF22
VSSG	E13	AE13
VSSG	E14	AE14
VSSG	F25	AD25
VSSG	G4	AC4
VSSG	AA4	J4
VSSG	AC4	G4
VSSG	AE18	E18
VSSG	AE22	E22
VSSP	Y3,	K3
W/R#	AF28	D28

4. PIN DESCRIPTIONS

4.1 SiS5591/5592 PIN DESCRIPTION

4.1.1 Host Bus Interface

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
U29	N29	CPUCLK	I	**Host Clock :** Primary clock input to drive the part.
AE27	E27	ADS#	I	**Address Status :** Address Status is driven by the CPU to indicate the start of a CPU bus cycle.
AA26	J26	M/IO#	I	**Memory I/O Command Indicator :** Memory I/O definition is an input to indicate an I/O cycle when low, or a memory cycle when high.
AE26	E26	D/C#	I	**Data/Code Command Indicator :** Data/Code is used to indicate whether the current cycle is a data or code access.
AF28	D28	W/R#	I	**Write/Read Command Indicator :** Write/Read from the CPU indicates whether the current cycle is a write or read access.
AA25	J25	BRDY#	O	**Burst Ready :** Burst Ready indicates that data presented are valid during a burst cycle.
AD28	F28	CACHE#	I	**Cacheable Indicator :** The Cache pin indicates an L1 internally cacheable read cycle or a burst write-back cycle. If this pin is driven inactive during a read cycle, the CPU will not cache the returned data, regardless of the state of the KEN# pin.
AD27	F27	KEN#/ INV	O	**Cache Enable/Invalidate :** This function as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN/INV is normally low. KEN#/INV will be driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read. KEN#/INV is driven high (low) during the EADS# assertion of a PCI master DRAM write (read) snoop cycle.
AD25	F25	NA#	O	**Next Address :** The SiS Chip always asserts NA# no matter the burst, or pipelined burst SRAMs are used. This signal is connected to CPU and indicate to CPU that it is ready to process a second cycle.

AE29	E29	BOFF#	O	**Back Off :** The SiS Chip asserts BOFF# to stop the current CPU cycle.
AD26	F26	AHOLD	O	**Address Hold :** The SiS Chip asserts AHOLD when a PCI master is performing a cycle to DRAM. AHOLD is held for the duration of PCI burst transfer. The SiS Chip negates AHOLD when the completion of PCI to DRAM read or write cycles complete and during PCI peer transfers.
AB26	H26	HLOCK#	I	**Host Lock :** When CPU asserts HLOCK# to indicate the current bus cycle is locked.
AB25	H25	EADS#	O	**External Address Strobe :** The EADS# is driven to indicate that a valid external address has been driven to the CPU address pins to be used for an inquire cycle.
AF29	D29	HITM#	I	**Hit Modified :** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of the CPU.
AE28	E28	SMIACT#	I	**System Management Interrupt Active :** The SMIACT# pin is used as the SMI acknowledgement input from the CPU to indicate that the SMI# is being acknowledged and the processor is operating in System Management Mode (SMM).
AG27,AF23, AH27,AC25, AG28,AF26, ,AC26,AF27	C27,D23, B27,G25, C28,D26, G26,D27	HBE[7:0]#	I	**Host Byte Enables :** CPU Byte Enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. HBE7# indicates that the most significant byte of the data bus is valid while HBE0# indicates that the least significant byte of the data bus is valid.
AJ22,AF20, AH23,AG23, AJ21,AH22, AE20,AF19, AG21,AG22, AH21,AE23, AJ26,AH26, AG26,AF22, AH25,AJ25, AG25,AF25, AJ24,AF21, AE25,AH24, AF24,AE21, AG24,AE24, AJ23	A22,D20, B23,C23, A21,B22, E20,D19, C21,C22, B21,E23, A26,B26, C26,D22, B25,A25, C25,D25, A24,D21, E25,B24, D24,E21, C24,E24, A23	HA[31:3]	I/O	**Host Address Bus :** The Host Address is driven by the CPU during CPU bus cycles. The SiS Chip forwards it to either the DRAM or the PCI bus depending on the address range. The address bus is driven by the SiS Chip during bus master cycles or Flushing L2 cycle.

W26,Y29, W27,V25, W28,W29, V27,V26, V28,V29, U26,U28, U27,T26, U25,T27, T28,R28, T25,R27, T29,P26, R26,R29 P25,P27, P29,P29, P28,N27, N26,N29, N28,N25, M28,M27, M25,L29, L28,L27, M26,L29, L25,K28, K29,K27, J29,J27, J28,L26, H28,H27, H29,K25, G26,G27, K26,G28, G29,F27, J25,F28, J26,F29, E26	L26,K29, L27,M25, L28,L29, M27,M26, M28,M29, N26,N28, N27,P26, N25,P27, P28,R28, P25,R27, P29,T26, R26,R29, T25,T27, T29,T29, T28,U27, U26,U29, U28,U25, V28,V27, V25,W29, W28,W27, V26,W29, W25,Y28, Y29,Y27, AA29,AA27, AA28,W26, AB28,AB27, AB29,Y25, AC26,AC27, Y26,AC28, AC29,AD27, AA25,AD28, AA26,AD29, AE26	HD[63:0]	I/O	**Host Data Bus :** The Host data is driven by the CPU during CPU write cycle. The Host data is driven by L2 in three conditions: One is the CPU reads cycle and it hits the L2 cache. The other is the CPU reads cycle but the data does not exist in L2 cache, and it needs to perform a write-back cycle before a burst line fill. Another is the flushing L2 cycle. When CPU reading data from DRAM, the Host data is driven by SiS5591/5592.

4.1.2 L2 Cache Controller

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
AA29	J29	KOE#	O	**Cache Output Enable :** Cache Output Enable for pipelined burst SRAM to enable data read.

AA27	J27	CCS1#	O	**Cache Chip Select :** A L2 cache consisting of burst SRAMs will power up, if necessary, and perform an access if this signal is asserted when ADSC# is asserted. A L2 cache consisting of burst SRAMs will power down if this signal is negated when ADSC# is asserted. When CCS1# is negated a L2 cache consisting of burst SRAMs ignores ADS#. If CCS1# is asserts when ADS# is asserted a L2 cache consisting burst SRAMs will power up, if necessary, and perform an access.
Y28	K28	GWE#	O	**Global-write Enable :** GWE# asserted causes a QWORD to be written into the L2 cache. It is used for L2 cache line fills.
Y27	K27	BWE#	O	**Byte-Write Enable :** When GWE#=1, the assertion of BWE# causes the byte lanes that are enabled via the HBE[7:0]# signals to be written into the L2 cache, if they are powered up.
W25	L25	ADSC#	O	**Cache Address Strobe :** Cache address strobe is for pipelined burst SRAM to load L2 cache address register from the SRAM address pins.
AA28	J28	ADV#	O	**Cache Address Advance :** Cache address advance is for pipelined burst SRAM to advance to the next data into the cache line.
AB29	H29	TAGWE#	O	**TAG RAM Write Enable Output :** When asserted, new state and/or new TAG address are written into the external tag RAM.
Y26, AB28, AB27,AC29, AC28,Y25, AC27,AD29	K26,H28, H27,G29, G28, K25, G27, F29	TA[7:0]	I/O	**TAG RAM Data Bus Lines :** The voltage level must be the same as DRAM voltage level.

4.1.3 DRAM Controller

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
C19,B19, A19,C18, D18,B18, A18,D17, C17,B17, A17,D16	AG19,AH19, AJ19,AG18, AF18,AH18, AJ18,AF17, AG17,AH17, AJ17,AF16	MA[13:2]	O	**Memory Address Lines 13-2:** Memory address 13-2 are the row and column addresses for DRAM.
C16	AG16	MA1A	O	**Memory Address Line 1A :** Two copies are provided for loading purposes.
B16	AH16	MA1B	O	**Memory Address Line 1B :** Two copies are provided for loading purposes.

A16	AJ16	MA0A	O	**Memory Address Line 0A :** Two copies are provided for loading purposes
D15	AF15	MA0B	O	**Memory Address Line 0B :** Two copies are provided for loading purposes.
H25,E29,H26, D28,G25,F26, D25,C27,C26, C25,A25,E24, C24,E23,C23, A23,D12,B10, E11,B9,C8, D11,C7,A7, D10,B6,E5, C5,A5,B4, C3,B2,E27, E28,D26,D27, D29,C28,B28, E25,B27,A26, B25,A24,D24, B24,D23,B23, A11,C10,A10, C9,A9,B8,A8, B7,D6,C6,A6, D5,B5,C4,A4, B3	AB25,AE29, AB26,AF28, AC25,AD26, AF25,AG27, AG26,AG25, AJ25,AE24, AG24,AE23, AG23,AJ23, AF12,AH10, AE11,AH9, AG8,AF11, AG7,AJ7, AF10,AH6, AE5,AG5, AJ5,AH4, AG3,AH2, AE27,AE28, AF26,AF27, AF29,AG28, AH28,AE25, AH27,AJ26, AH25,AJ24, AF24,AH24, AF23,AH23, AJ11,AG10, AJ10,AG9, AJ9,AH8, AJ8,AH7, AF6,AG6, AJ6,AF5, AH5,AG4, AJ4,AH3	MD[63:0]	I/O	**Memory Data Bus :** When write, it is driven by SiS5591/5592. When read, it is driven by DRAM medules.
A14,B14, C14,D14, A15,B15	AJ14,AH14, AG14,AF14, AJ15,AH15	RAS[5:0] #/CS[5:0]#	O	**RAS Address Strobe (EDO/FP):** DRAM Row address strobe 5-0 for DRAM banks 2-0. **Chip Select (SDRAM) :** These pins activate the SDRAM and accept any command when CS# signal is low.
D19,A20, C13,A13, C20,B20, D13,B13	AF19,AJ20, AG13,AJ13, AG20,AH20 ,AF13,AH13	CAS[7:0]#/ DQM[7:0]#	O	**DRAM Column address strobe (FPM/EDO) :** DRAM Column address strobe 7-0 for byte 7-0. **Input / Output Data Mask (SDRAM) :** SDRAM output enables during a read cycle and a byte mask during a write cycle.

C12, A21	AG12, AJ21	RAMWA# RAMWB#	O	**Memory Write :** RAM Write is an active low output signal to enable local DRAM writes. Two copies are provided for loading purposes.
C15	AG15	SRAS#	O	**SDRAM Row Address Strobe :** SDRAM latch row address on the positive edge of the clock with SRAS# low. This pin is driven to low by SiS5591/5592 when row access or prechange.
B12	AH12	SCAS#	O	**SDRAM Column Address Strobe :** SDRAM latches column address on the positive edge of the clock with SCAS# low. This pin is driven to low by SiS5591/5592 when column access.
B22,C21, E12,B11, C22,A22, A12, C11	AH22,AG21 ,AE12,AH11 ,AG22,AJ22, AJ12,AG11	MPD[7:0]	I/O	**Memory ECC/Parity Data Bus :** These signals carry memory ECC data or parity data during read/write to DRAM.
B21	AH21	CKE	O	**SDRAM Clock Enable :** While in ACPI S2 or S3 state, SiS5591/5592 can put the SDRAM in the self refresh mode by CKE signal. During power down mode, CKE must remain low by SiS5595.

4.1.4 PCI Interface

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
AJ5	A5	PCICLK	I	**PCI Clock :** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
AB5, AF3, AG4, AE6	H5, D3, C4, E6	C/BE[3:0]#	I/O	**PCI Bus Command and Byte Enables :** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.

AC3,AC2, AA5,AC1, AD5,AD4, AD3,AD2, AD1,AE4, AE3,AB4, AE2,AE1, AF4,AC5, AH4,AJ4, AF8,AE5, AF5,AG5, AE9,AH5, AF9,AF6, AG6,AH6, AE10,AJ6, AG7,AH7	G3,G2,J5,G1, F5,F4,F3,F2, F1,E4,E3,H4, E2,E1,D4,G5, B4,A4,D8,E5, D5,C5,E9,B5, D9,D6,C6,B6, E10,A6,C7,B7	AD[31:0]	I/O	**PCI Address /Data Bus :** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1. When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2. When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
AE8	E8	PAR	I/O	**Parity :** Parity is an even parity generated across AD[31:0] and C/BE[3:0]#.
AF2	D2	FRAME#	I/O	**Frame :** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
AF1	D1	IRDY#	I/O	**Initiator Ready :** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.
AG2	C2	TRDY#	I/O	**Target Ready :** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.
AF7	D7	STOP#	I/O	**Stop :** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.

AH2	B2	DEVSEL#	I/O	**Device Select :** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being access by a PCI master, PCI configuration registers or embedded controllers′ registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
AE7	E7	PLOCK#	I	**PCI Lock :** PCI Lock indicates an exclusive bus operation that may require multiple transactions to complete. When PLOCK# is sampled asserted at the beginning of a PCI cycle, the SiS Chip considers itself a locked resource and remains in the locked state until PLOCK# is sampled negated on a new PCI cycle.
W3,AB2, AA1,AA2, AA3	L3,H2, J1,J2, J3	PREQ[4:0]#	I	**PCI Bus Request :** PCI Bus Request is used to indicate to the PCI bus arbiter that an agent requires use of the PCI bus.
AB1,Y4, AB3, Y5	H1, K4, H3,K5	PGNT[3:0]#	O	**PCI Bus Grant :** PCI Bus Grant indicates to an agent that access to the PCI bus has been granted.
AH3	B3	SERR#	I	**System Error :** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the SiS Chip generates a non-maskable interrupt to the CPU.
V1	M1	BM_REQ#/ PGNT4#	O	**Multi-function pins :** It can be used as the PCI Bus Grant by programming the Register69h bit0 to 0 in Host to PCI bridge Configuration Space to assert PGNT4# to grant PCI access to SiS5591/5592. It can also be used to carry the following two information : 1) A.G.P. activity event to reload the system standby timer in the SiS5595, and 2)A.G.P./PCI/IDE bus master request event to exit from ACPI/C3 state. Upon power up, the clock after FRAME# is sampled asserted is defined as the slot containing the Bus master request event, the next clock containing the A.G.P. activity event, ...etc.
W5	L5	PCIRST#	I	**PCI Bus Reset :** The PCIRST# is used to reset the device on PCI bus. PCIRST# is driven low when PWRGD is sampled low and driven inactive about lms after PWRGD is sampled high.

W2	L2	PHOLD#	I	**Bus Hold :** PHOLD# is used to request the use of the PCI bus. PHOLD# is asserted on behalf of the ISA master, DMA devices, or USB devices. PHOLD# is eventually connected to the PCI system arbiter (normally located in SiS5591/5592).
V4	M4	PHLDA#	O	**Bus Hold Acknowledge :** The PCI system arbiter asserts this signal to acknowledge grant of the PCI bus access to the SiS5595.

4.1.5 PCI IDE Interface

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
AJ11,AG11, AJ10,AG10, AJ9,AF11, AJ8,AE11, AG8,AH8, AG9,AH9, AE12,AH10, AF12,AH11	A11,C11, A10,C10, A9,D11, A8,E11, C8,B8, C9,B9, E12,B10, D12,B11	IDA[15:0]	I/O	**IDE Channel_0 Data Bus :**
AJ17,AE17, AF17,AH16, AF16,AJ15, AG15,AJ14, AH14,AF15, AH15,AE16, AG16,AJ16, AG17,AH17	A17,E17,D17, B16,D16,A15, C15,A14,B14, D15,B15,E16, C16,A16,C17, B17	IDB[15:0]	I/O	**IDE Channel_1 Data Bus :**
AG14, AF14	C14, D14	IDECS[1:0]A#	O	**IDE Channel 0 Chip Select signals :**
AJ20, AE19	A20, E19	IDECS[1:0]B#	O	**IDE Channel 1 Chip Select signals :**
AE13,AJ18	E13,A18	IIOR[A:B]#	O	**IDE Channel 0/1 I/O Read Cycle Command :**
AH12,AH18	B12,B18	IIOW[A:B]#	O	**IDE Channel 0/1 I/O Write Cycle Command :**
AJ12, AG19	A12, C19	ICHRDYA ICHRDYB	I	**IDE Channel 0/1 I/O Channel Ready Signal :**
AG12, AG18	C12, C18	IDREQA# IDREQB#	I	**IDE Channel 0/1 DMA Request Signals :**
AF13, AH19	D13, B19	IDACKA# IDACKB#	O	**IDE Channel 0/1 DMA Acknowledge Signals :**
AG13, AF18,	C13, D18	IIRQ[A:B]	I	**IDE Channel 0/1 Interrupt Request Signals :** These are the synchronous interrupt request inputs from IDE device.
AJ7, AF10	A7, D10	IRQ[15:14]	O	**IDE channel 1/0 Interrupt Request Signals :** These are the synchronous interrupt request output to the SiS 5595 internal 8259 controller.

AE14,AH13, AJ13,	E14,B13, A13	IDSA[2:0]A	O	**IDE Channel 0 Address [2:0] :**
AH20, AJ19, AG20,	B20, A19, C20	IDSA[2:0]B	O	**IDE Channel 1 Address [2:0] :**

4.1.6 A.G.P. Interface

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
G3	AC3	PIPE#	I	**Pipelined Operation :** The A.G.P. master asserts PIPE# to inform the target to enqueue a full width request. The master always enqueues one request on each rising edge of A.G.P.CLK while PIPE# is asserted.
F2,F3,F4,F5, E2,E3,E4,	AD2,AD3, AD4,AD5, AE2,AE3, AE4,AF1	SBA[7:0]	I	**Sideband Address Port :** These signals provides an optional path for the A.G.P. master to pass the address and command to the target.
J4	AA4	RBF#	I	**Read Buffer Full :** A.G.P. bus master asserts the signal to tell the A.G.P. local arbiter not to initiate the return of any low priority read data since the A.G.P. master is not affordable to buffer it.
D2, D3, D4	AF2,AF3, AF4	ST[2:0]	O	**Status Bus :** Status bus passes the information to the A.G.P. master on what it may do. ST[2:0] Description 000 : Indicates that previously requested low priority read data is being return to the master. 001 : Indicates that previously requested high priority read data is being return to the master. 010 : Indicates that the master is to provide low priority write data for a previous enqueued write command. 011 : Indicates that the master is to provide high priority write data for a previous enqueued write command. 111 : Indicates that the master has been given permission to start a bus transaction.
J1	AA1	AD_STB1	IO	**AD bus Strobe 1 :** AD bus Strobe 1 provides timing for 2x transfer mode on the AD[31:16]. SiS5591/5592 drives this signals while it is providing data.
T2	P2	AD_STB0	I/O	**AD bus Strobe 0 :** AD bus strobe 0 provides timing for 2x transfer mode on the AD[15:0]. While SiS5591/5592 is presenting data on the A.G.P. interface, it drives AD_STB0.

E1	AE1	SB_STB	I	**Side Band Strobe :** Side Band Strobe provides timing for SiS5591/5592 to strobe SBA[7:0]
W1	L1	A.G.P.CLK	I	**A.G.P. Clock :** A.G.P. CLK provides timing for A.G.P. control signals.
N5	U5	AFRAME#	I/O	**Frame (Same as PCI) :** AFRAME# remains deserted by the external pull up resistor in the A.G.P. operation. AFRAME# behaves the same as FRAME# in the PCI bus during PCI operations on the A.G.P. interface.
N3	U3	AIRDY#	I/O	**A.G.P. IRDY# :** Assertion of AIRDY# indicates the A.G.P. master is ready to provide all write data for the current transaction. While in the A.G.P. read cycle, it indicates that the master is ready to transfer a subsequent block of data.
N2	U2	ATRDY#	I/O	**A.G.P. TRDY# :** Assertion of ATRDY# indicates that SiS5591/5592 is ready to provide read data for the entire transaction or is ready to transfer a block of data.
P3	T3	ASTOP#	I/O	**Stop (Same as PCI) :** ASTOP# is only used during PCI operation on the A.G.P. interface.
N1	U1	ADEVSEL#	I/O	**Device Select (Same as PCI) :** ADEVSEL# is only used during PCI operation on the A.G.P. interface.
P5	T5	ASERR#	I	**A.G.P. SERR# :** It is provided for the A.G.P. master to report any error.
G5	AC5	AREQ#	I	**Request :** A.G.P. master asserts this signal to request the access of the A.G.P. interface.
F1	AD1	AGNT#	O	**Grant :** SiS5591/5592 grants the A.G.P. port authority to the A.G.P. master to initiate a bus transaction. Together with ST[2:0], the assertion of AGNT# can also indicates that the master is the recipient of the previously requested read data, or that the master can provide write data for a previously enqueued write command.

G2,G1,H3, H2,H1,J3, J2,K4,K3, K2,K1,L3, L2,L1,M5, M4,P1,R4, R3,R2,R1, T5,T4,T3, U5,U4,U3, U2,U1,V5, V3,V2	AC2,AC1, AB3,AB2, AB1,AA3, AA2,Y4,Y3, Y2,Y1,W3, W2,W1,V5, V4,T1,R4, R3,R2,R1, P5,P4,P3, N5,N4,N3, N2,N1,M5, M3, M2	AAD[31:0]	I/O	**A.G.P./PCI Address/Data Bus :** Same as AD[31:0] on PCI interface.
L4, M3, P2, T1	W4, V3, T2, P1	AC/BE[3:0]#	I/O	**A.G.P./PCI Command/Bye Enables Bus :** Provides command information by the master, when requests are belong enqueued using PIPE#. Provides valid byte information during A.G.P. write transactions and is driven by the master. The target drives to "0000" during the return of A.G.P. real data. During PCI transaction, the meaning is same as C/BE[3:0]#.
P4	T4	APAR	I/O	**Parity :** APAR is only used during PCI operation on the A.G.P. bus.
M1	V1	VREF	I	**A.G.P. Reference Voltage :** This pin should be guarded by VREFVDD/ VREFVSS on the motherboard layout.
N4	U4	VREFVDD	I	**3.3V DC power signal for A.G.P. VREF.**
M2	V2	VREFVSS	I	**Ground signal for A.G.P. VREF.**

4.1.7 Power Pins

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
E15, F15, N24, P24, R5,R6,R24, R25, T24, U24, AD13, AD14, AD15, AD16, AD17, AE15	F15, G15, Q24, S5,S6,S24, S25, U24, W24, AE13,AE14, AE15,AE16, AE17, AF15,	DVDD	PWR	**+3.3V I/O PAD DC Power.**

M12,M13, M16,M17, M18, N12,N13, N14,N16, N17,N18, P12,P13, P14,P15, P16,P17, P18, R14,R15, R16, T12,T13, T14,T15, T16,T17, T18, U12,U13, U14,U16, U17,U18, V12,V13, V16,V17, V18	O12,O13, O16,O17, O18, P12,P13, P14,P16, P17,P18, Q12,Q13, Q14,Q15, Q16,Q17, Q18, S14,S15, S16, U12,U13, U14,U15, U16,U17, U18, W12,W13, W14,W16, W17,W18, X12,X13, X16,X17, X18,	VSS	PWR	**Ground signals for core logic.**
D7,D8,D9, D20,D21, D22, E13,E14, F25, G4, H4, AA4, AC4, AE18,AE22	E22, G4, J4, AB4, AC4, AD25, AE13,AE14, AF7,AF8, AF9,AF20, AF21, AF22	VSSG	PWR	**Ground signals for current return path.**
B26, C2, AG3, AH28	B28, C3, AG2, AH26	5VDD	PWR	**5V DC Power.**
Y1, Y2	K1, K2	PLLVDD PLLVSS	PWR	**Phase Lock Loop circuit power and ground.**
Y3,	K3,	VSSP	PWR	**Ground pin for PLL circuit guard ring.**

K12,K13, K17,K18, M10,M20, N10,N20, U10,U20, V10,V20, Y12,Y13, Y17,Y18	Z12,Z13, Z17,Z18, X10,X20, W10,W20, P10,P20, O10,O20, L12,L13, L17,L18	OVDD3	PWR	**3.3V DC Power.**
M14,M15, N15, R12,R13, R17,R18, U15, V14,V15	O14,O15, S12, S13, S17, S18, W15, X14,X15	OVDD2	PWR	**DC power pin connect to CPU Vccio.**

4.1.8 Misc. Pins

SiS5591 BALL NO.	SiS5592 BALL NO.	NAME	TYPE ATTR	DESCRIPTION
A3,A27, C1,C29, E[6:10], E[16:22], F13,F14, F16,F17, H5, J5, K5, L5, N6, P6, T6, U6, AG1,AG29, AJ3,AJ27	A3,A27, C1,C29, N6, P6, T6, U6, W5, Y5, AA5, AB5, AD13,AD14 ,AD16, AD17, AE6,AE7, AE8,AE9, AE10,AE16, AE17,AE18, AE19,AE20, AE21,AE22, AG1,AG29, AJ3,AJ27	NC	NC	**Not Connect**
W4	L4	TEST_PIN#	I	**Test Mode Select for NAND Tree function.** Ball connectivity test mode Pull-up : Disable Pull-down : Enable

5. HARDWARE TRAP

There are two pins in the SiS Chip are used for trapping purpose to identify the hardware configurations at the power-up stage. These pins should be defined as if pull-up resistors are used; and these pins should be if pull-down resistors are used. The following table is a summary of all the Hardware Trap pins in SiS Chip.

SiS5591 BALL NO.	SiS5592 BALL NO.	SYMBOL	DESCRIPTION
H25	AB25	MD63	**Internal DLL circuits for CPU clock and PCI clock to optimize timing Control** Pull-up : Disable Pull-down : Enable
E29	AE29	MD62	**Internal PLL circuit for APG clock to optimize timing Control** Pull-up : Disable Pull-down : Enable

Note: there are pull-down resistors on MD lines.

6. FUNCTIONAL DESCRIPTION

6.1 HOST INTERFACE

SiS5591/5592 is designed to support Socket7 CPU and Accelerated Graphic Port (A.G.P.) interface.

SiS5591/5592 supports the pipelined addressing mode of the CPU by issuing the next address signal, NA#. NA# is asserted except single read DRAM cycle.

SiS5591/5592 supports the CPU L1 write-back (WB) or write-through (WT) cache policies and the L2 WB cache policies. The L1 cache is snooped by the assertion of EADS# when the CPU is put in the HOLD state.

SiS5591/5592 issues AHOLD to the CPU in response to the assertion of PCI master requests. Once the AHOLD is asserted, SiS5591/5592 does not immediately assert PGNT[3:0]# until both the CPU to PCI posted write buffer and the memory write buffer are empty.

6.1.1 Host Interface Decoding Rules

The destination of CPU initiated cycle is decoded by the host interface. Memory cycles may be forwarded to DRAM controller, A.G.P. bus or PCI bus. I/O cycles are either forwarded to A.G.P. bus or PCI bus.

6.1.1.1 Memory Cycle

SiS5591/5592 determines whether a memory cycle's destination is system DRAM or not by checking DRAM bank registers, shadowing related registers, Graphics Window base address registers, Graphics Window size registers. For memory cycles which are not targeting system DRAM, the host interface further checks memory space enable register, memory base address register and memory limit address register, prefetchable memory base address register and prefetchable memory limit address register in the virtual PCI-to-PCI bridge to see if the destination is residing in A.G.P. bus or not. If the address locates within these ranges, the host interface signals A.G.P. Interface to forward the cycle to A.G.P. Otherwise, the cycle would be forwarded to PCI bus by PCI Interface.

The only exception for the above rule is mapping standard video buffer area (A0000h~BFFFFh). The mapping of this range is totally controlled by VGA enable bit of the PCI-to-PCI bridge control register residing in the virtual bridge (device 2). When the bit is enabled, all CPU initiated memory cycles in this range are forwarded to A.G.P. bus. When the bit is disabled, all CPU initiated memory cycles are forwarded to PCI bus.

6.1.1.2 I/O Cycle

I/O cycles are either forwarded to A.G.P. or PCI bus. Basically, SiS5591/5592 determines whether an I/O cycle is destining A.G.P. bus or not by checking I/O base address register and I/O limit address register in the virtual PCI-to-PCI bridge. If the address locates within the range, the host interface signals A.G.P. Interface to forward the cycle to A.G.P. bus. Otherwise, the cycle would be forwarded to PCI bus by PCI Interface.

The I/O address decoding is also affected by the bridge control register and bridge command register of the virtual PCI-to-PCI bridge (device 2). When VGA enable bit of the bridge control register is set to 1, all I/O accesses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3Dfh are forwarded to A.G.P. bus. When the bit is set to 0, I/O accesses with the address ranges are forwarded to PCI bus.

I/O address decoding for the addresses of A[9:0] = 3C6h, 3C8h and 3C9h is also affected by the VGA palette snoop enable bit of the bridge command register and the palette write cycle forwarding control register. When the palette write cycle forwarding control register is set to 1, I/O writes with these addresses are forwarding to one interface only (either A.G.P. or PCI Interface), and it is totally controlled by VGA enable bit. When the value of palette write cycle forwarding control register is 0, these I/O write cycles are always forwarding to PCI Interface and may optionally be forwarded to A.G.P. Interface, which is controlled by VGA palette snoop enable and VGA enable. Please refer to the register description for detail.

Host interface must take care of returning BRDY# for palette write when the cycle is forwarded both to PCI and A.G.P. bus. Host interface must wait until both PCI and A.G.P. device have finished the operation before returning BRDY# to CPU.

ISA enable bit of the bridge control register also affects I/O address decoding. When the ISA enable bit is 1, CPU initiated I/O cycles addressing the last 768 bytes in each 1Kbyte block will be forwarded to the PCI bus even the address is within the address range defined by the virtual bridge's I/O base and I/O limit registers.

I/O addresses CF9h (reset control register) and CF8h (configuration address register, only accepts double word access) are always forwarded to PCI bus. The decoding of I/O addresses in the range CFCh~CFFh (configuration data register) depends on the bus number defined configuration address register. If the bus number is equal to or greater than the secondary bus number register and is smaller or equal to the subordinate bus number register in the virtual PCI-to-PCI bridge, the cycle will be forwarded to A.G.P. bus. Otherwise, the cycle will be forwarded to PCI bus.

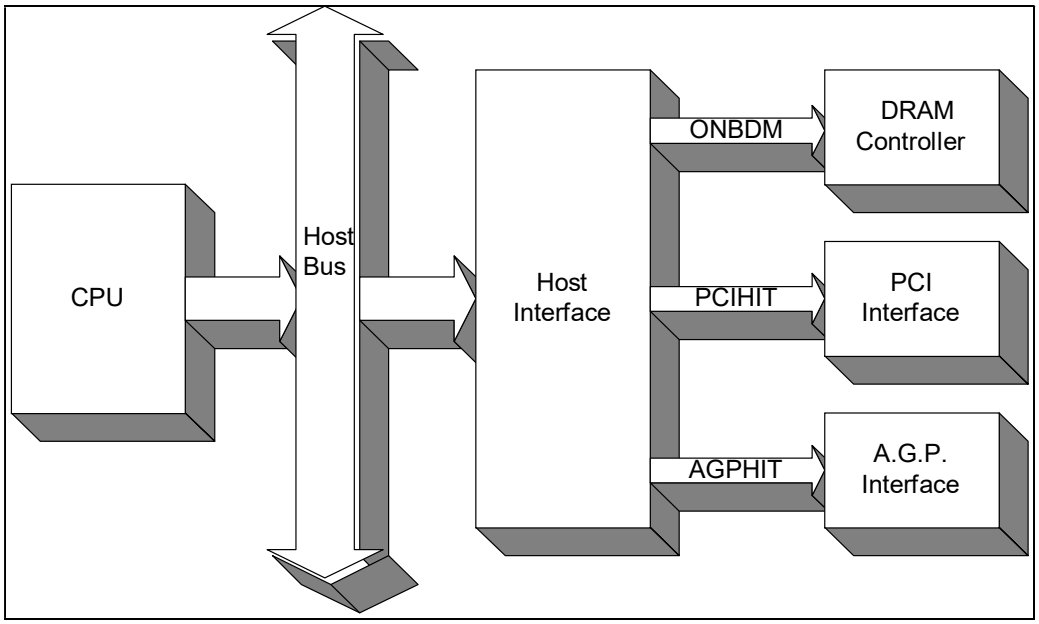


Figure 6.1-1 Block Diagram for Host Decoding

6.1.1.3 Other Cycles

Interrupt acknowledge cycles are always forwarded to PCI bus (PCI Interface intercepts the first cycle and forward the second cycle to PCI bus). The Write Back special cycle is handled by the host interface itself when the write back enable bit is set to 1 and L2 flushing mechanism control is set to 0. Otherwise, the Write Back special cycle will be passed to PCI Interface (PCI Interface does nothing except for return BRDY# to CPU).

6.1.1.4 Host Bus Arbitration

SiS5591/5592 may require the usage of host bus for some reasons. After L2 flushing command is accepted, host bus must be owned by SiS5591/5592 to flush modified lines in L2 cache into system DRAM. When a PCI master is accessing system memory, host bus must also be owned by SiS5591/5592 to snoop about CPU and to access L2 cache.

Host bus arbitration must be done among CPU, flushing L2 control circuit in Host Interface, PCI Interface and A.G.P. Interface. When SiS5591/5592 determined that itself needed the host bus, it asserts AHOLD or BOFF# to seize the host bus from the Pentium processor. If SiS5591/5592 requires only the host address bus, it asserts AHOLD. If SiS5591/5592 wants to seize the host data bus, it also asserts BOFF# in addition to the assertion of AHOLD.

PCI Interface and A.G.P. Interface asserts HOLD to Host Bus Arbiter in the Host Interface. After HLDA is returned, the respective block has totally control the host bus. It can snoop about the CPU cache and access L2 cache/DRAM. After HLDA is returned to PCI Interface or A.G.P. Interface. PCI Interface or A.G.P. Interface can own the host bus as long as it keeps HOLD asserted. Arbiter in PCI Interface or A.G.P. Interface will determine how long the HOLD should be lasted.

When flushing L2, the flushing L2 circuit will own the host bus until it finishes the flushing operation, if the L2 flushing priority timer enable register is set to 0. When the L2 flushing priority timer enable register is 1, the flushing L2 control circuit will remain the highest priority for a period of time defined by the FL2PT (L2 Flushing Priority Timer).

The host bus arbiter uses a rotating priority algorithm for solving the arbitration problem among PCI interface, A.G.P. interface and flushing L2 circuit. After returning the control of host bus to host interface, the priority of the respective module will be dropped to the lowest. Flushing L2 control circuit will be dropped to the lowest priority after the timer is expired. So, the cycles from PCI Interface or A.G.P. Interface can interrupt the flushing L2 operation to snoop about the CPU and access L2 cache/DRAM.

The priority structure is shown in Figure 6.1-2 Priority Structure and the block diagram for host bus arbitration is shown in 6.1. Please refer to 6.2 Cache Controller for more information about the operation of the flushing L2 circuit.

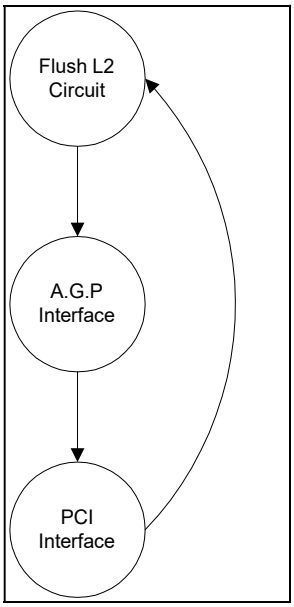


Figure 6.1-2 Priority Structure

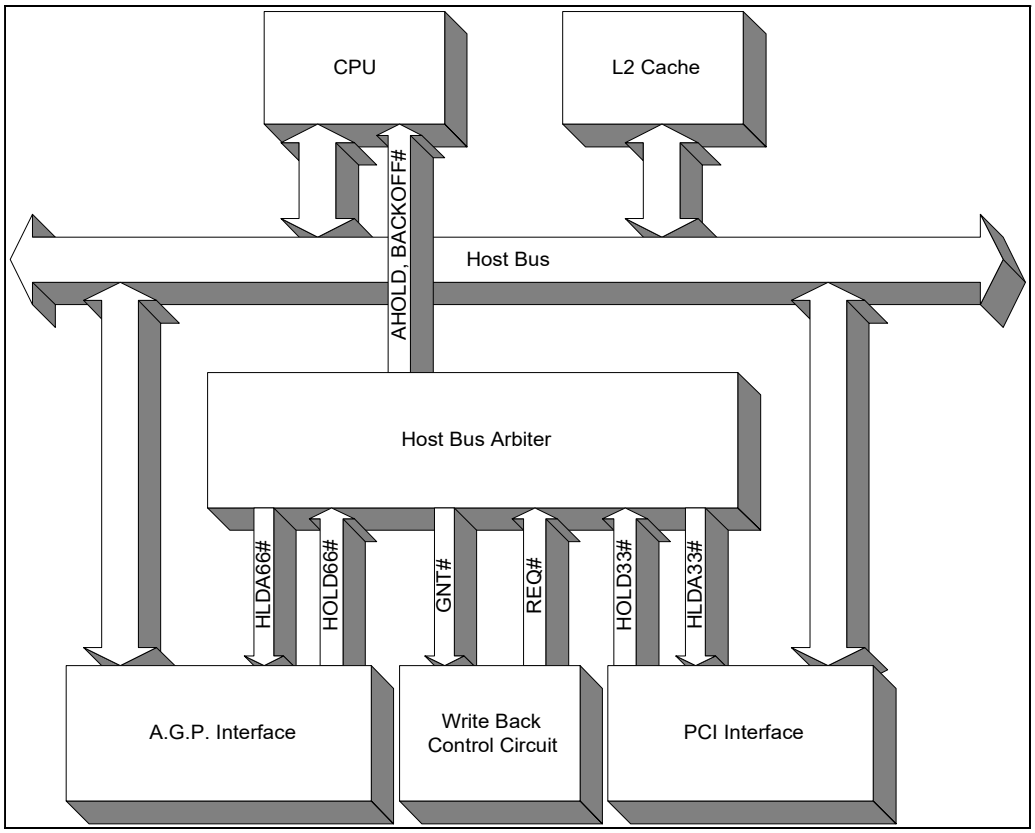


Figure 6.1-3 Arbitration of Host Bus

6.2 CACHE CONTROLLER

The built-in L2 Cache Controller uses a direct-mapped scheme, which can be configured as either in the write through or write back mode. Notice that the L2 Write-through mode is only supported during the cache sizing period. SiS5591/5592 supports 256K/512K/1M Bytes pipelined burst SRAM and the function of auto-sizing cache size.

SiS5591/5592 supports 7 or 8bits TAG address lines. TAG-7bits means that the 7 bits of TAG RAM are used for TAG address and another one bit is use as dirty bit. TAG-8bits means that all 8 bits of TAG RAM are used for TAG address and SiS5591/5592 inside provides the dirty bit. So, TAG-8bits may have larger cacheable size than TAG-7bits.

SiS5591/5592 also provide internal invalid bit for each cache line. If the invalid bit is set to 1, that means this corresponding cache line is invalid. It exists for A.G.P. bus to maintain data coherence between L2 cache and system DRAM. When L2 flushing command is accepted, SiS5591/5592 will flush the dirty lines into system DRAM and all of the L2 cache will be set to invalid.

Table 6.2-1 Supported Size of L2 Cache shows the cache sizes that are supported by the SiS5591/5592, with the corresponding TAG RAM sizes, and cacheable memory sizes of TAG-7/8bits. Table 6.2-2 SRAM TAG Address Mapping shows the TAG address mapping.

Table 6.2-1 Supported Size of L2 Cache

CACHE SIZE	TAG RAM	CACHEABLE SIZE OF TAG 7 BITS	CACHEABLE SIZE OF TAG 8 BITS
256K	8Kx8	32M	64M
512K	16Kx8	64M	128M
1M	32Kx8	128M	256M

Table 6.2-2 SRAM TAG Address Mapping

TAG-8BITS	256K	512K	1M
TA7	HA18	HA26	HA26
TA6	HA25	HA25	HA25
TA5	HA24	HA24	HA24
TA4	HA23	HA23	HA23
TA3	HA22	HA22	HA22
TA2	HA21	HA21	HA21
TA1	HA20	HA20	HA20
TA0	HA19	HA19	HA27

TAG-7BITS	256K	512K	1M
TA7	dirty bit	dirty bit	dirty bit
TA6	HA18	HA25	HA25
TA5	HA24	HA24	HA24
TA4	HA23	HA23	HA23
TA3	HA22	HA22	HA22
TA2	HA21	HA21	HA21
TA1	HA20	HA20	HA20
TA0	HA19	HA19	HA26

There are two mechanisms to trigger the flushing L2 operation, which are decided by L2 flushing mechanism control register. When triggered by write back special cycle, SiS5591/5592 only supports flushing all function. When triggered by configuration write register A0h, SiS5591/5592 also supports the flushing 4K function.

During the flushing operation, SiS5591/5592 will assert AHOLD to hold the CPU and drive the address to host address bus. If this cache line is dirty, SiS5591/5592 will read the data from L2 cache and write into system DRAM. In the same time, SiS5591/5592 cleans the dirty bit and sets this cache line to be invalid. If this cache line is not dirty, SiS5591/5592 will do nothing except setting this cache line to be invalid. After, these operation, it starts next address's scanning.

6.3 DRAM CONTROLLER

The SiS5591/5592 can support up to 768MBytes of DRAM and each bank could be single or double sided 72-bit (64-bit data and 8-bit ECC code) Fast Page Mode (FPM) DRAM, Extended Data Output (EDO) DRAM, and Synchronous DRAM (SDRAM). The SiS5591/5592 supports industry standard SIMM/DIMM modules. Six RAS#/CS# lines permit up to six rows (3 double sided banks) of DRAM, and mixing the different type of DRAM bank by bank is acceptable.

The installed EDO/FPM DRAM type can be 256K, 512k, 1M, 2M, 4M, 8M or 16M bit deep by n (n = 4, 8, 16,or 32) bit wide, and both symmetrical and asymmetrical addressing modes are supported. The installed SDRAM type can be 1M, 2M, 4M, 8M, 16M bit deep by n (n = 4, 8, 16,or 32) bit wide. The SiS5591/5592 DRAM Controller operates synchronously to the CPU clock.

6.3.1 DRAM Configuration

SiS5591/5592 supports three banks (double sided DRAM) of DRAM each 64/72-bit wide. The three banks may be configured in three banks of EDO/FPM SIMM, three banks of EDO/SDRAM DIMM or any other

combinations as required. Access to the banks are not interleaved and need not to be populated starting from row 0 or in consecutive sequence.

The SiS5591/5592 can support EDO, FPM and SDRAM. These different types of DRAM can be mixed for each bank, it must contain only one type of DRAM in each bank.

The basic configurations are shown as the following sections:

6.3.1.1 EDO/FPM DRAM Configuration (4 SIMM/6 SIMM):

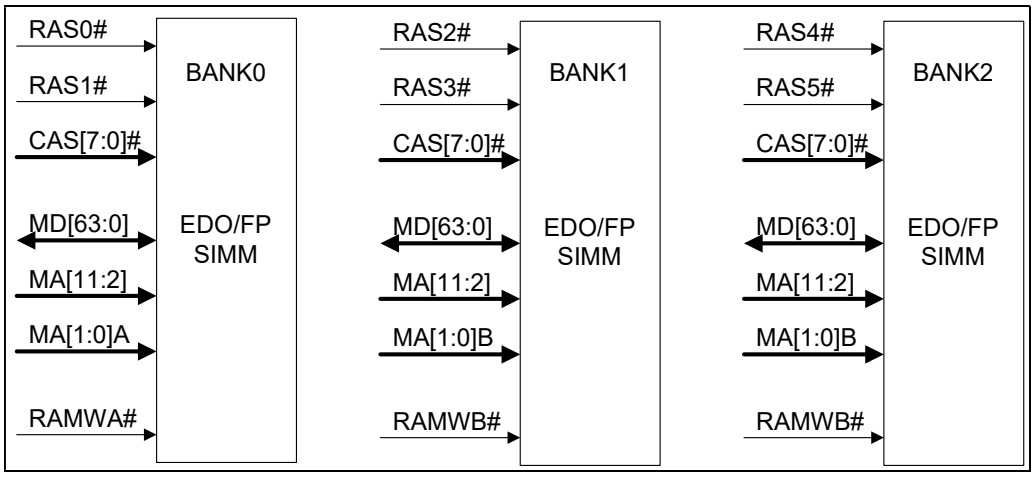


Figure 6.3-1 ED0/FPM DRAM Configuration

6.3.1.2 SDRAM Configuration (2 DIMM/3 DIMM):

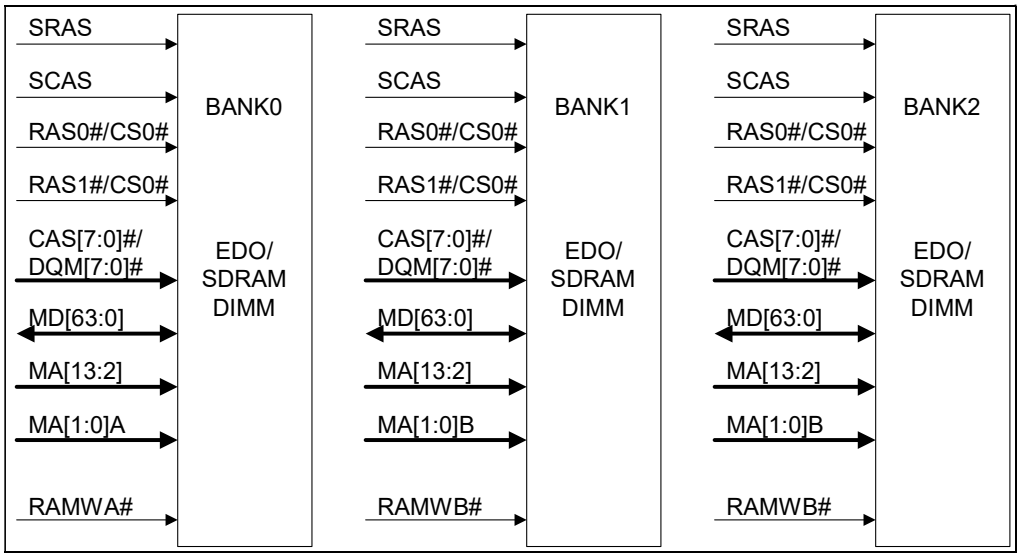


Figure 6.3-2 SDRAM Configuration

6.3.1.3 DRAM Type Mixed Configuration: EDO/FPM + SDRAM (4 SIMM + 2 DIMM)

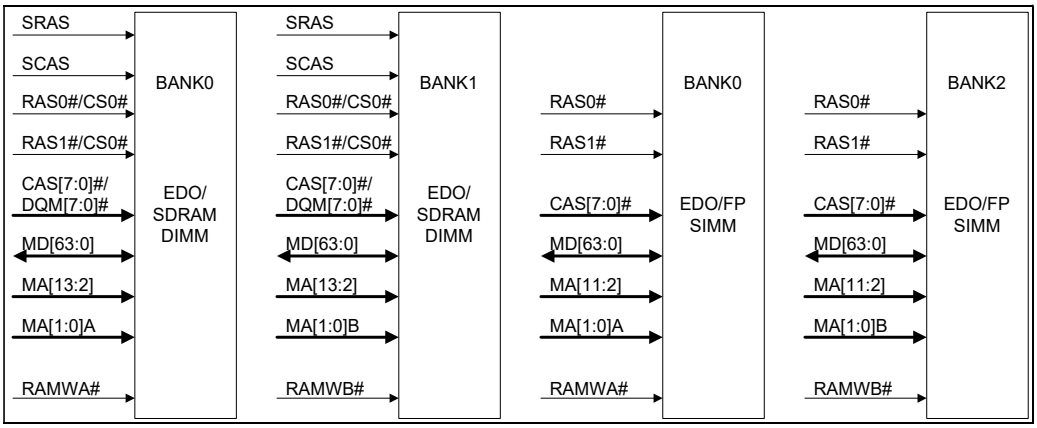


Figure 6.3-3 DRAM Type Mixed Configuration : ED0/FPM + SDRAM

Note:

1. SiS5591/5592 only support six rows (3 banks) DRAM.
2. It is recommended that board designer must follow DC characteristics of each type DRAM (SDRAM, EDO, FPM) to design the portion of DRAM in DRAM mode mixed configuration.

6.3.2 DRAM Scramble Table

The DRAM scramble table contains information for memory address mapping. These tables provide the translation between CPU host address and memory Row and Column address.

There are several memory address mapping: MA mapping for FPM/EDO DRAM, 2Bank and 4Bank mapping for SDRAM that SiS5591/5592 supports:

6.3.2.1 MA mapping table for FPM/EDO DRAM

Table 6.3-1 MA mapping table for FPM/EDO DRAM

TYPE			MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Symmetric	256K	R	X	X	X	14	13	12	20	19	18	17	16	15
	9x9	C	X	X	X	11	10	9	8	7	6	5	4	3
	1M	R	X	X	13	14	22	21	20	19	18	17	16	15
	10x10	C	X	X	12	11	10	9	8	7	6	5	4	3
	4M	R	X	14	24	23	22	21	20	19	18	17	16	15
	11x11	C	X	13	12	11	10	9	8	7	6	5	4	3

	16M	**R**	26	25	24	23	22	21	20	19	18	17	16	15
	12x12	**C**	14	13	12	11	10	9	8	7	6	5	4	3
Asymmetric	**512K**	**R**	X	X	12	14	13	21	20	19	18	17	16	15
	10x9	**C**	X	X	X	11	10	9	8	7	6	5	4	3
	1M	**R**	X	13	12	14	22	21	20	19	18	17	16	15
	11x9	**C**	X	X	X	11	10	9	8	7	6	5	4	3
	1M	**R**	14	13	12	11	22	21	20	19	18	17	16	15
	12x8	**C**	X	X	X	X	10	9	8	7	6	5	4	3
	2M	**R**	X	14	13	23	22	21	20	19	18	17	16	15
	11x10	**C**	X	X	12	11	10	9	8	7	6	5	4	3
	2M	**R**	14	13	12	23	22	21	20	19	18	17	16	15
	12x9	**C**	X	X	X	11	10	9	8	7	6	5	4	3
	4M	**R**	14	13	24	23	22	21	20	19	18	17	16	15
	12x10	**C**	X	X	12	11	10	9	8	7	6		4	3
	8M	**R**	14	25	24	23	22	21	20	19	18	17	16	15
	12x11	**C**	X	13	12	11	10	9	8	7	6	5	4	3

Note : "X" means do not care.

6.3.2.2 MA mapping table for SDRAM

Table 6.3-2 MA mapping table for SDRAM

TYPE			**MA13**	**MA12**	**MA11**	**MA10**	**MA9**	**MA8**	**MA7**	**MA6**	**MA5**	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**
2 Bank	**1M**	**R**	X	X	11	14	13	12	22	21	20	19	18	17	16	15
	1x11x8	**C**	X	X	11	X	X	X	10	9	8	7	6	5	4	3
	2M	**R**	X	X	12	14	13	23	22	21	20	19	18	17	16	15
	1x11x9	**C**	X	X	12	X	X	11	10	9	8	7	6	5	4	3

2 Bank	4M	R	X	X	13	14	24	23	22	21	20	19	18	17	16	15
	1x11x10	C	X	X	13	X	12	11	10	9	8	7	6	5	4	3
	4M	R	23	24	11	14	13	12	22	21	20	19	18	17	16	15
	1x13x8	C	X	X	11	X	X	X	10	9	8	7	6	5	4	3
	8M	R	24	25	12	14	13	23	22	21	20	19	18	17	16	15
	1x13x9	C	X	X	12	X	X	11	10	9	8	7	6	5	4	3
	16M	R	25	26	13	14	24	23	22	21	20	19	18	17	16	15
	1x13x10	C	X	X	13	X	12	11	10	9	8	7	6	5	4	3
4 Bank	2M	R	X	12	11	14	13	23	22	21	20	19	18	17	16	15
	2x11x8	C	X	12	11	X	X	X	10	9	8	7	6	5	4	3
	4M	R	24	12	11	14	13	23	22	21	20	19	18	17	16	15
	2x12x8	C	X	12	11	X	X	X	10	9	8	7	6	5	4	3
	8M	R	25	13	12	14	24	23	22	21	20	19	18	17	16	15
	2x12x9	C	X	13	12	X	X	11	10	9	8	7	6	5	4	3
	16M	R	26	14	13	25	24	23	22	221	20	19	18	17	16	15
	2x12x10	C	X	14	13	X	12	11	10	9	8	7	6	5	4	3

6.3.3 DRAM Auto-Detection

SiS5591/5592 supports three banks DRAM for SIMM/DIMM from bank0 to bank2. The DRAM detection sequence is a bank-based detection sequence, it is performed by the BIOS bank by bank and fulfill the DRAM configuration information into the corresponding DRAM configuration registers. The following steps will be described the DRAM detection sequence.

Step 1. To detect if there is any DRAM populated in bank N, SiS5591/5592 set this bank with maximum DRAM size, then write/read the same address with test pattern by the normal DRAM read/write timing and compare the data. If the read data is the same as the write pattern, then there exist DRAM in the bank N; otherwise, proceed the SDRAM detection from step 3.

Step 2. If the DRAM is detected in the bank N by step 1, SiS5591/5592 treat it as EDO or FPM DRAM. SiS5591/5592 first write test pattern into DRAM, then set register 59h bit 0 (EDO Test Mode) to be "1" in HOST-to-PCI bridge configuration space, then read the same DRAM location and compare with the test pattern. The EDO test bit will delay the data forward to CPU after 4096 CPU clock. If the CPU still

get the right data, then EDO mode DRAM is set to this row; otherwise, the FP mode DRAM is set. Go to step 8.

Step 3. If the DRAM is detected not populated in bank N by normal write/read procedure, SiS5591/5592 check if there is SDRAM exist in this bank or not. SiS5591/5592 first assume the DRAM mode is SDRAM (set bit [7:6] of register 60h/61h/62h to be "11" in HOST-to-PCI bridge configuration space, it depends on which bank is under detection), and then do the SDRAM initialization procedure from step 4 to step 6.

Step 4. Set register 5Ch bit 7 to be "1", this bit will drive a precharge command to SDRAM, then disable this bit (set to be "0").

Step 5. Set register 5Ch bit 6 to be "1", this bit will drive a "Mode Register Set" (MRS) command to SDRAM. When SDRAM receive MRS command, it will load the needed information (Toggle/Linear mode, CAS Latency) into SDRAM. After doing MRS, disable this bit (set to be "0").

Step 6. Set register 5Ch bit 5 to be "1" at least two times, then SDRAM will perform refresh cycle at least two times before the normal operation. Disable this bit (set to be "0").

Step 7. Write/Read the test pattern into SDRAM, then compare the data. If the data is correct, SDRAM is detected, and set bank N as SDRAM; otherwise, bank N is no DRAM populated.

Step 8. After DRAM mode is set, SiS5591/5592 do DRAM sizing by write/read test pattern based on the MA mapping table.

Step 9. Repeat from step 1 to step 8 to detect the other banks.

Note: The value of N is from 0 to 2.

The following will be shown the flow chart of DRAM Detection Sequence.

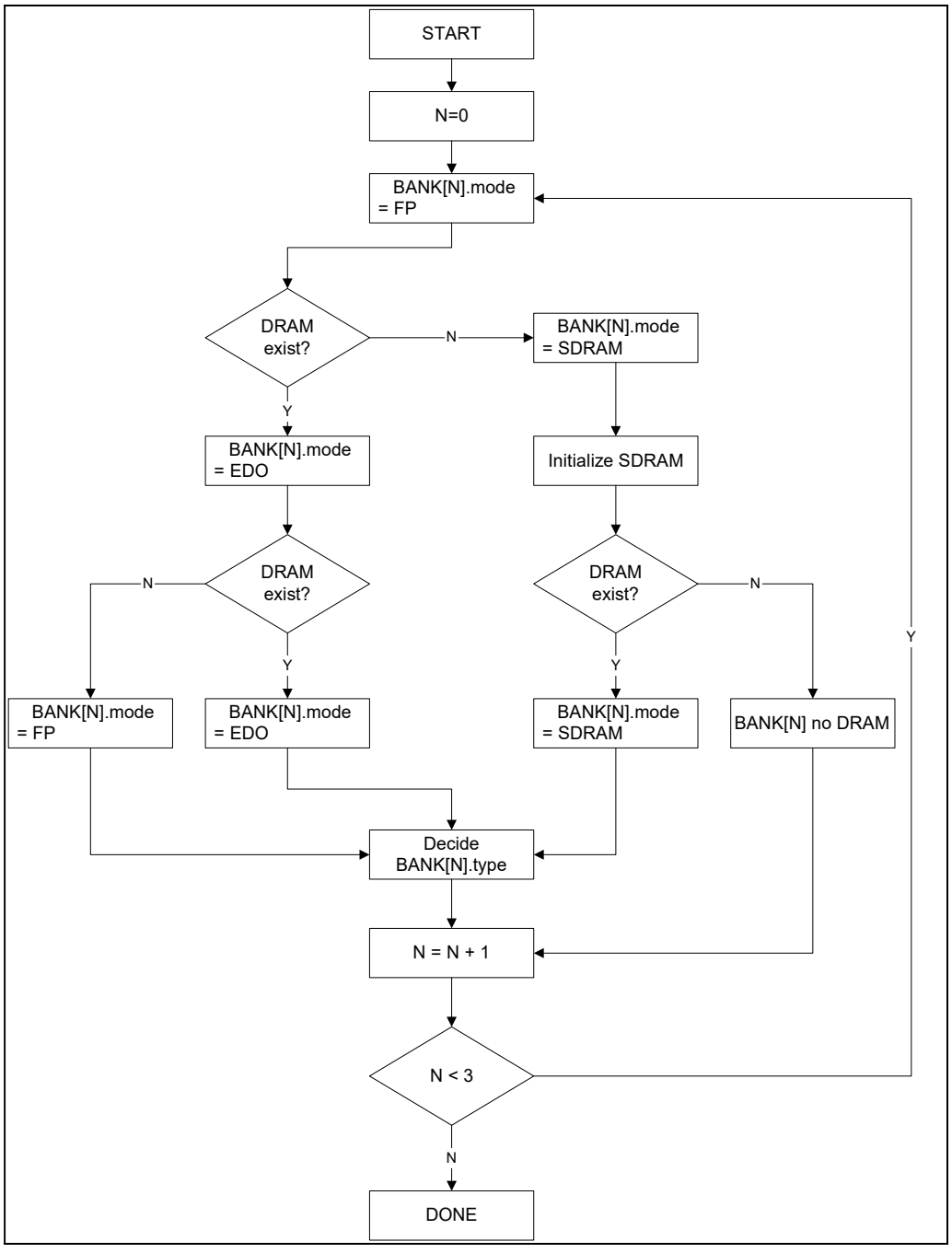


Figure 6.3-4 DRAM Detection Sequence

6.3.4 DRAM Performance

All the DRAM cycles are synchronous with the CPU clock. The following table shows the different possible speed settings that depend on different DRAM mode, RAS# setting, CAS# setting, and so forth.

Cycle Type	FP	EDO	SDRAM	
			CL=2	CL=3
Read Burst Rate	X-3-3-3	X-2-2-2	X-1-1-1	X-1-1-1
Read Lead off Time				
Page Hit	5	5	6	7
Row Start	$5+T_{RCD}$	$5+T_{RCD}$	$6+T_{RCD}$	$7+T_{RCD}$
Page Miss	$5+T_{RCD}+T_{RP}$	$5+T_{RCD}+T_{RP}$	$6+T_{RCD}+T_{RP}$	$7+T_{RCD}+T_{RP}$
Read Back-to-Back Page Hit				
Single	X-3-3…	X-3-3…	X-4-4…	X-5-5…
Burst	X-3-3-3-3-3-3-3…	X-2-2-2-2-2-2-2…	X-1-1-1-2-1-1-1…	X-1-1-1-3-1-1-1…
Write Burst Rate	3	2	1	1
Write Page Hit	3			
Write Row Start	$3+T_{RCD}$			
Write Page Miss	$3+T_{RCD}+T_{RP}$			

Note:

1. EDO CAS# width=1T, FP CAS# width=2T, CAS precharge time=1T.
2. T_{RCD} is RAS# to CAS# delay time that can be programmed to 3/4/5T
3. T_{RP} is RAS# prechagre time that can be programmed to 2/3/4/5T

6.3.5 Graphic Window Re-mapping

For support A.G.P. bus, SiS5591/5592 supports an address range, Graphic Window (GW), which is virtual, contiguous, programmable range and can be re-mapped by Graphic Address Re-mapping Table (GART) to non-contiguous pages of system memory. Graphic Window is defined by Graphic Window Base Address (GWBA) configuration register. The size of Graphic Window is allowed the selection of 4M, 8M, 16M, 32M, 64M, 128M and 256M. It is defined by Graphic Window Size Register.

When an access is addressing to the Graphic Window, the memory controller will firstly read the re-mapping relation from GART, then translate to the physical address and read the data from system memory.

Figure 6.3-5 Graphic Address Re-mapping Function shows the graphic address re-mapping function.

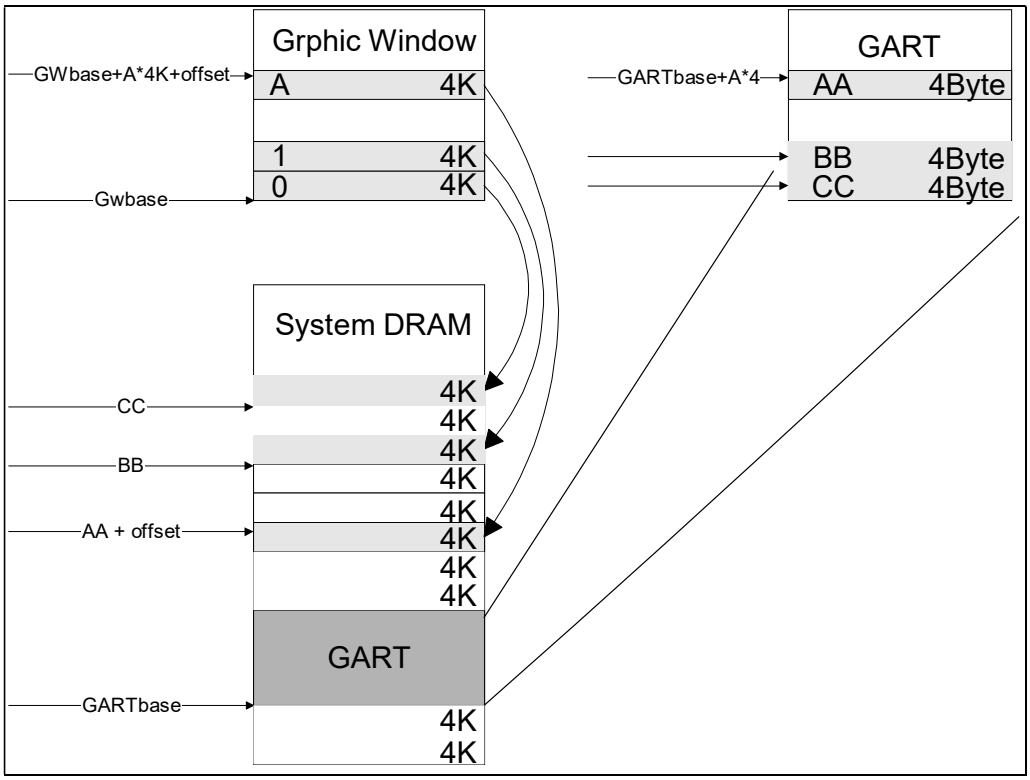


Figure 6.3-5 Graphic Address Re-mapping Function

In order to improve the performance of accessing Graphic Window, SiS5591/5592 builds a page table cache inside. The page table store re-mapping relations of the most frequently used pages. It is set-associated with 8 ways and each way has 2 entries. If the page table stores the re-mapping relation of one specific page, then access within this page will directly be translated to the physical address without looking up the GART and be read by the memory controller.

6.3.6 CPU to DRAM Posted Write FIFO

There is a built-in CPU to Memory posted write buffer with 8 QWord deep (CTMFF). All write accesses from CPU to DRAM will be buffered. For the CPU read miss / Line fill cycles, the write-back data from the second level cache will be buffered first, and right after the data had been written into the FIFO, CPU can performs the read operation by the memory controller starting to read data from DRAM. The buffered data are then written to DRAM whenever no any other read DRAM request comes. With this concurrent write back policy, many wait states are eliminated. If there comes a bunch of continuous DRAM write cycles, some ones will be pending if the CTMFF is full.

6.3.7 Arbiter

The arbiter is the interface between the DRAM interface and the masters that can access DRAM. In addition to pass or translate the information from outside to DRAM controller, arbiter is also responsible for which master has higher priority to access DRAM. The arbiter treats different DRAM access request as DRAM master, and that makes there be 9 masters which are trying to access DRAM by sending their request to the arbiter. After one of them get the grant from the arbiter, it owns DRAM bus and begins to do memory data transaction.

The masters are: CPU read request, 33MHZ PCI masters, 66MHZ PCI master, Posted write FIFO write request, AGP high read request, AGP high write request, AGP low read request, AGP low write request and Refresh request. The order of these masters shown above also stands for their priority to access memory.

6.3.8 Refresh cycle

Refresh functionality is provided. There are up to twelve deep refresh queues with two levels of refresh priority. SiS5591/5592 generates a new refresh request every 15.6 us, and the request will be served only when there is no other DRAM operation in progress or pending. If the request does not get service, it will be pushed into the refresh queue. When the queue is full, a high priority refresh request asserts and takes priority over all other DRAM requests.

During refresh operation, CAS[7:0]# will be asserted at the same time, and the RAS[5:0]# are asserted sequentially to minimize the power surge.

6.3.9 Data Integrity

SiS5591/5592 support ECC data integrity feature on the 64-bit DRAM interface. This feature provides single-error correction and double-error detection. After system reset, the DRAM controller is set in non-ECC mode. In this mode there is no provision for protecting the integrity of data within the DRAM. After the BIOS configuration procedure detects that all memory modules support 72-bit ECC mode operation, the DRAM controller can be set in ECC mode.

6.3.9.1 Initialization

When ECC is enabled, the whole DRAM modules must be first initialized by doing writes before the DRAM read operations to establish the correlation between 64-bit data and associated 8-bit ECC code which does not exist after power-on.

6.3.9.2 ECC Detection and Correction

During DRAM read operations, the full Qword of data and the associated ECC code are transferred simultaneously from DRAM to the SiS5591/5592. If there is a single-bit error in the 72-bit signals (64-bit data plus 8-bit code), the ECC mechanism will automatically recover the correct 64-bit data. Note that the recovered data is transferred to the requesting master (Host, PCI, or AGP interface), but the DRAM controller does not initiate a DRAM write cycle to fix the single-bit error in DRAM.

If the ECC mechanism detects a two-bit error, SiS5591/5592 can report this error by SERR# or record it on the Error Status Register optionally.

6.3.9.3 ECC Generation

During DRAM write operations, SiS5591/5592 automatically generates an 8-bit ECC code for the 64-bit data. If the requested write operation transfers single or multiple Qword of data, the ECC DRAM write can be completed without any overhead. If the write request only transfers less than 64 bits of data, the DRAM controller performs a read-merge-write operation.

6.4 PCI BRIDGE

The PCI bridge of SiS5591/5592 consists of three parts: PCI arbiter, PCI master bridge and PCI target bridge. The PCI arbiter controls the assignment of PCI bus ownership among all PCI masters. The PCI master bridge forwards the transactions from host bus. The PCI target bridge claims PCI cycles toward system memory or AGP bus as required by PCI master devices.

SiS5591/5592 is able to operate at both asynchronous and synchronous PCI clock with CPU and AGP clocks. Synchronous mode is provided for those synchronous systems to improve the overall system performance. The synchronous mode for PCI master bridge and PCI target bridge can be set separately.

6.4.1 PCI Arbiter

The main function of PCI arbiter takes charge of the PCI bus ownership assignment. This PCI arbiter supports at most 5 external PCI masters using standard PCI REQ#/GNT# mechanism and 1 PCI master using PHOLD#/PHLDA# mechanism. The master that uses PHOLD#/PHLDA mechanism is not pre-emptive. That means the master can own the bus as long as it wishes after it gains the control of PCI bus. The master that use PHOLD#/PHLDA# mechanism to access PCI bus is typically SiS5595 chip.

Arbitration Algorithm

PCI Masters (Agent 0~6, SIO) Requests

Figure6.4-1 Arbitration Tree shows the arbitration tree in arbiter design. Whenever a PCI cycle occurs, priority status will be changed. The initial priority for master 0-7 to own PCI bus is 4 -> 0->SIO->2->5->1->6->3->4...

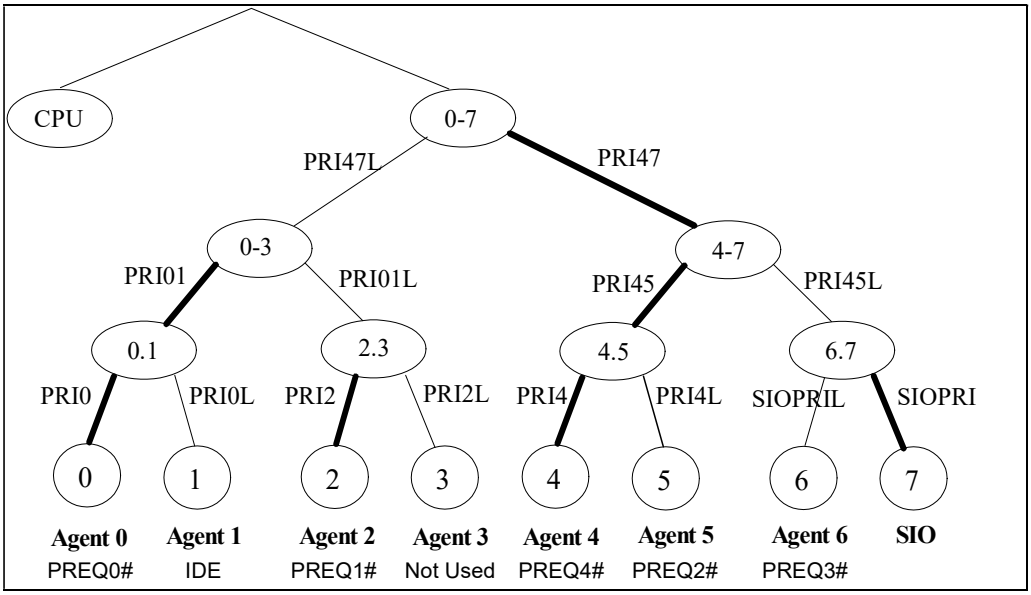


Figure 6.4-1 Arbitration Tree

NOTE: 1. "SIO" means the System I/O for PCI to ISA bridge (SiS5595).

2. The arbiter will treat PHOLD# as Agent SIO.

CPU Request

To avoid CPU being constantly held for a long time while PCI masters continuously deliver requests to the arbiter, SiS5591/5592 implemented a timer-based algorithm to reserve PCI bandwidth for CPU. Three timers, PCI Grant Timer (PGT)/ Master Latency Timer (MLT)/ CPU Idle Timer (CIT), are included in the host bridge for this purpose.

Whenever any PCI device owns the PCI bus other than host bridge, PCI grant timer (PGT) starts to count. After the timer is expired, the host bridge asserts its request signal to ask for gaining the control of PCI bus. Since the host bridge has the highest priority, PCI arbiter grants the bus to the host bridge as soon as possible after it receives the request from the host bridge.

Once the host bridge get a chance to start a transaction on PCI bus, its master latency timer (MLT) begins to count. After MLT is expired, the host bridge deasserts its request signal to inform the arbiter that the host bridge

no more needs the PCI bus. If there is any other PCI device that requests for the bus, arbiter grants the bus to the device and CPU is held again.

If there is no request from any PCI devices, the arbiter parks the bus on the host bridge. The ratio MLT/PGT approximately guarantees the minimum PCI bandwidth allocated to host bridge when CPU and PCI masters are contending for system resources, but it does not constrain CPU's highest utilization of PCI bus because of our bus parking policy.

To prevent the host bridge from capturing PCI bus too long while CPU actually has nothing to do at all, the third timer, CPU Idle Timer (CIT) is included in our design. CIT starts to count when the host bridge get a chance to start a transaction on PCI bus, but is reloaded with its initial value whenever the host bus leaves idle state. CIT actually keeps track on how long the CPU is in idle state. After CIT is expired, the host bridge deasserts its request signal just in the same manner as the case of MLT's expiration.

PGT is a 16-bit timer. MLT and CIT are both 8-bit timers. All of the initial values of the three timers are programmable and can be tuned according to the nature of the application. Although CIT & MLT are both 8-bit timers, the initial value of CIT is typically programmed much smaller than MLT.

Arbitration Parking

When no agent is currently using or requesting the bus, the arbiter will grant the bus ownership to the arbitration controller of SiS5591/5592.

PCI peer-to-peer access concurrent with CPU to L2/DRAM access

Although the PCI arbiter holds CPU in response to master requests, the PCI arbiter will release the CPU hold as soon as possible after it detects the cycle initiated by the master is not targeting system memory.

With this feature, a transaction initiated by a PCI master targeting a PCI target would not hold CPU. The CPU can still access L2 cache, system memory and PCI post-write buffers when PCI peer-to-peer activities are undergoing. With the enlarged 8 Dword deep PCI post-write buffers, it takes longer for CPU to halt while PCI peer-to-peer accesses are taking place.

6.4.2 PCI Master Bridge(PMR33)

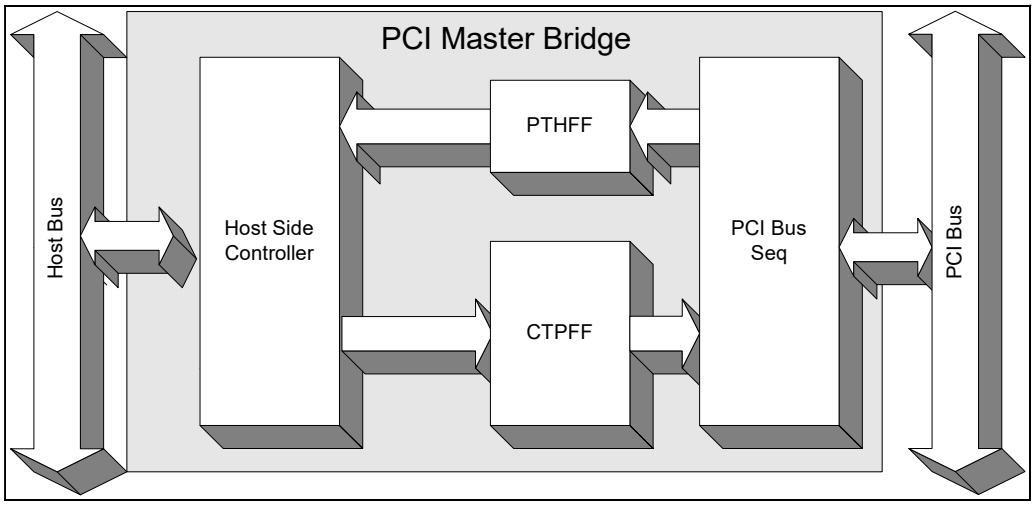


Figure 6.4-2 Block Diagram of PCI Master Bridge

The PCI master bridge forwards CPU cycles to the 33Mhz PCI bus. In the case of a 64-bit CPU request, the bridge takes the duty of read assembly and write disassembly control, A 8 level post-write buffer is implemented to improve the performance of CPU to PCI memory write and CPU to IDE data post write. Any non-posted write cycles forwarded to the PCI bus will be suspended until the post-write buffer is empty. For memory write cycles

toward PCI or I/O write cycles towards IDE data port, the address and data from host bus are pushed into the post write buffer if it is not full. The push rate for a double word is 3 CPU clocks. The pushed data are, at later time, written to the PCI bus. If the addresses of consecutive written data are in double word incremental sequence and they are targeting memory space, they will be transferred to the PCI bus in a burst manner.

The bridge provides a mechanism for converting standard I/O cycles on the CPU bus to configuration cycles on the PCI bus. Configuration Mechanism#1 in PCI Specification is used to do the cycle conversion.

The bridge is response for updating SiS5591/5592 internal configuration register. Care has to be done when updating GART base address register and Graphics Window size register since these two registers affect the mapping of system memory. The bridge will postpone the update of these two registers until all previously issued system memory write accesses are all retired from the DRAM post-write buffer.

The bridge always intercepts the first interrupt acknowledge cycle from CPU bus, and forwards the second interrupted acknowledge cycle onto the PCI bus.

PMR33 asserts BOFF# to CPU when its read cycle is retried by any PCI target. However, PMR33 would not assert BOFF# for retried memory write cycles or I/O write cycles. Instead PMR33 will re-initiate the retried cycles again and again until they are successfully transferred on PCI bus. The main reason for not asserting BOFF# to CPU for retried I/O write cycles is to secure correct palette snoop operation on A.G.P. If PMR33 asserts BOFF# to CPU for a retried palette write cycle, the cycle will be forwarded both to PCI bus and A.G.P., and this will result in incorrect palette updating behaviour on A.G.P.

The PCI arbiter parks the PCI bus to PMR when there are no requests from master. Typically, the bridge issues PCI cycles through bus parking mechanism. However PMR33 may also issue bus request to PCI arbiter when the CPU is held too long or when the PCI bus is occupied by PCI masters for a period of time. Three counters: PGT, MLT and CIT are included in PMR33 for managing bridge's bus request. Please reference PCI arbiter section for more information about the arbitration mechanism.

Since the system reset circuitry is moved to South Bridge (SiS5595) other than North Bridge itself. To have the correct response on CPU initiated special cycles, the PMR33 is responsible for transferring these cycles to South Bridge by way of PCI bus. For all special cycles, the PMR33 translates them into PCI Special Cycles with embedded information on AD bus following the encoding rule in Table 6.4-1 Special Bus Cycle Encoding Rule.

The bridge is designed to be able to handle asynchronous clock relationship between CPU and PCI. However, in order to enhance the performance of the bridge when PCI clock is lagging CPU clock by 2~4 ns, an optional synchronous mode is provided. The synchronous mode can on average save two extra CPU clocks for a single non-post cycle.

Table 6.4-1 Special Bus Cycle Encoding Rule

SPECIAL BUS CYCLE	AD[31:0]
Shutdown	00000000h
Flush (INVD, WBINVD instr.)	00000001h
Halt	00000002h
Write Back (WBINVD instr.)	00000003h
Flush Acknowledge (FLUSH# assertion)	00000004h
Branch Trace Message	00000005h
Stop Grant	00000012h

6.4.3 66Mhz PCI Master Bridge(PMR66)

The 66MHz PCI Master Bridge mainly forwards memory and I/O read/write cycles from host bus destining to AGP bus. To determine whether it is an AGP transaction or not, the decoding circuit of host interface refers to the Address Base and Address Limit in the configuration space of virtual PCI-to-PCI bridge (Bus 0, Device 2). However, PMR66 is responsible for generating configuration cycles for A.G.P. device.

Basically, the PMR66 owns the same function as PMR33 does, but they work with different bus segments. As a result, the mechanism of CPU Idle Timer on AGP (CITA), AGP Grant Timer (AGT) and CPU Latency Timer on

AGP (CLTA) provide a fair and efficient arbitration mechanism on AGP bus as CIT, PGT and MLT do on PCI bus. Except that, for memory cycles, the PMR66 is able to generate burst cycles. And, for memory write cycles, it is capable to translate them into post-write cycles based on two kinds of lead-off timing.

Since the operating frequency of AGP bus is higher than traditional 33Mhz PCI bus and even the same as host bus. Thereafter, the consuming of post-write cycles would be at a great rate and cause more non-burst transactions on AGP bus. To have good bus utilization and gain higher performance whenever CPU issues post-write cycles, the PMR66 will postpone the post-write cycles and try to wait for a period. Then, the PMR66 combines them into a single burst transaction if they have continuous addresses.

Beside, SiS5591/5592 allows PCI masters to write transactions of 33Mhz PCI bus toward AGP bus. Subsequently, additional data path from PSL33 is implemented to transfer such cycles for PCI masters as depicted in Figure6.4-3. Block diagram of 66Mhz PCI Master Bridge.

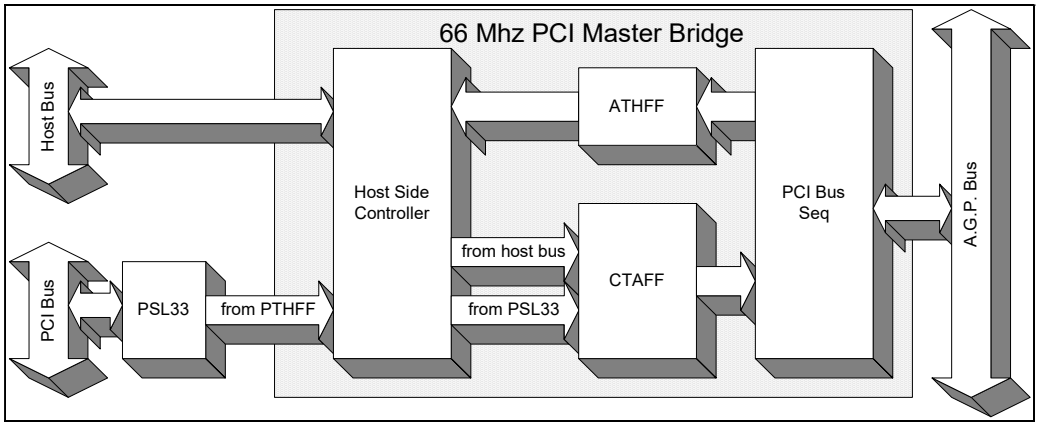


Figure 6.4-3 Block diagram of 66Mhz PCI Master Bridge

6.4.4 PCI Target Bridge(PSL33)

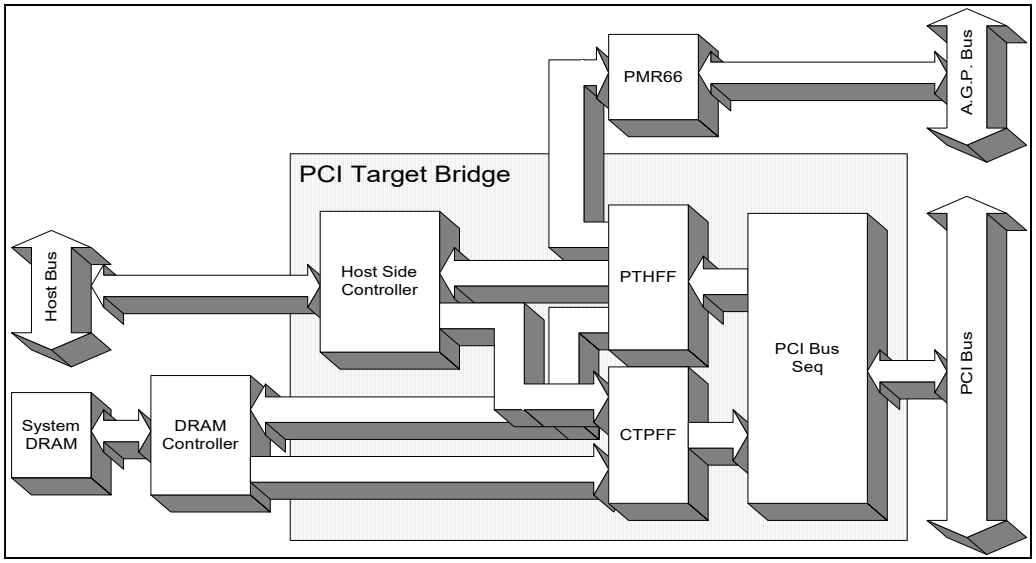


Figure 6.4-4 Block Diagram of PCI Target Bridge

While in the PCI Master write cycles, post-write is always performed. And function of Write Merge with CPU-to-DRAM post-write buffer is incorporated to eliminate the penalty of snooping write-back. On the other hand, prefetch is enabled for master read cycles by default, and such function could be disabled optionally. And, Direct-Read from CPU-to-DRAM post-write buffer is implemented to eliminate the overhead of snooping write-back also.

In addition to Write-Merge and Direct-Read, Snoop-Ahead also hides the overhead of inquiry cycles for master to main memory cycles. These key functions, Write-Merge, Direct-Read and Snoop-Ahead, achieve the purpose of zero-wait for PCI burst transfer.

The post-write and prefetch buffers are both 16 Double-Words deep FIFO.

A PCI master device may access system memory, a PCI target residing at 33Mhz PCI bus, or a PCI target residing at 66Mhz PCI bus(A.G.P.). When the destining target resides at 66Mhz PCI bus and the access is a memory write cycle, PSL33 first pushes the data into PTHFF and then CTAFF and the data will be consumed by PMR66 later. If a PCI master accesses memory located in Graphics Window, the DRAM controller will translate the address with GART table automatically and the translation is totally invisible to PCI target bridge.

6.4.4.1 Snooping Control

In order to maintain the cache consistency while PCI master accesses to main memory, SiS5591/5592 performs inquiry cycle to snoop L1 and L2 caches before PCI masters really read from or write to memory. For the purpose of snooping, AHOLD is asserted to force the Pentium-like processors to float its address bus as soon as PCI master requests the PCI bus. Such the host bus hold mechanism is completed by an AHOLD/BOFF# process and is depicted in the host interface. Since the inquiry cycle is the major penalty for PCI master cycles, SiS5591/5592 builds in a high performance snoop-ahead mechanism to incorporate the zero-wait requirement of PCI bus transactions.

The main idea of "Snoop-ahead" is to do memory operations and inquiry cycle simultaneously. For example, when transferring the L_n line of data, SiS5591/5592 also performs the L_{n+1} line of inquiry cycle in the mean while.

On the other hand, PCI Target Bridge may optionally skip the snooping process to enhance the lead-off time when PCI master initiating a memory cycle targeting the Graphics Window.

6.4.4.2 ECC Support

When ECC is enabled, SiS5591/5592 must distinguish partial write and perform read-merge-write operation.

Note that 8-bit ECC code is written along with the 64-bit data (entire Qword) into main memory. If a quantity of less than a Qword is written, PCI Target Bridge performs a single read operation in advance to fetch the original Qword data in DRAM. And then merges the read data with the write data to generate ECC code through ECC control unit.

6.4.4.3 Target Initiated Termination

In general, SiS5591/5592 is capable to complete all the requests to access main memory from PCI masters until master terminates the transaction actively. Sometimes, as SiS5591/5592 is unable to respond or is unable to burst, it will initiate to terminate bus transactions and STOP# will be issued by doing Retry or Disconnect.

6.4.4.4 Target Retry

SiS5591/5592 may operate Target Retry for one of two reasons:

1. Whenever a PCI master tries to access main memory and SiS5591/5592 is locked previously by another agent, Target Retry will be signalled.
2. Once SiS5591/5592 can not meet the requirement of target initial latency, Target Retry is used and no data is transferred.

6.4.4.5 Disconnect With Data

In some situations, such as the burst crosses a resource boundary or a resource conflict, SiS5591/5592 might be temporarily unable to continue bursting, and, therefore, SiS5591/5592 concludes an active termination.

1. SiS5591/5592 supports PCI burst transfers, the bursting length can be 256 bytes, 512 bytes, 1K bytes, 2K bytes, or 4K bytes. A burst will be terminated by doing Disconnect if the transfer goes across the programmed bursting length. In this way, at most 128 cache lines of data can be uninterruptedly transferred no matter what the status they are in L1 and L2. One reason for the constraint is that page miss may occur only once at the beginning of the entire bursting transaction since the maximum bursting length is always within the page size in any of the used DRAM.
2. If advanced snoop function is disabled, PCI transaction will not cross the cache boundary and also causes a Disconnect operation. Since the heavy overhead of inquiry cycles is not preventable, and SiS5591/5592 can not keep bursting transfer.

6.4.4.6 Disconnect Without Data

If Target Subsequent Latency timer expires, it causes SiS5591/5592 to assert STOP# by doing Disconnect operation.

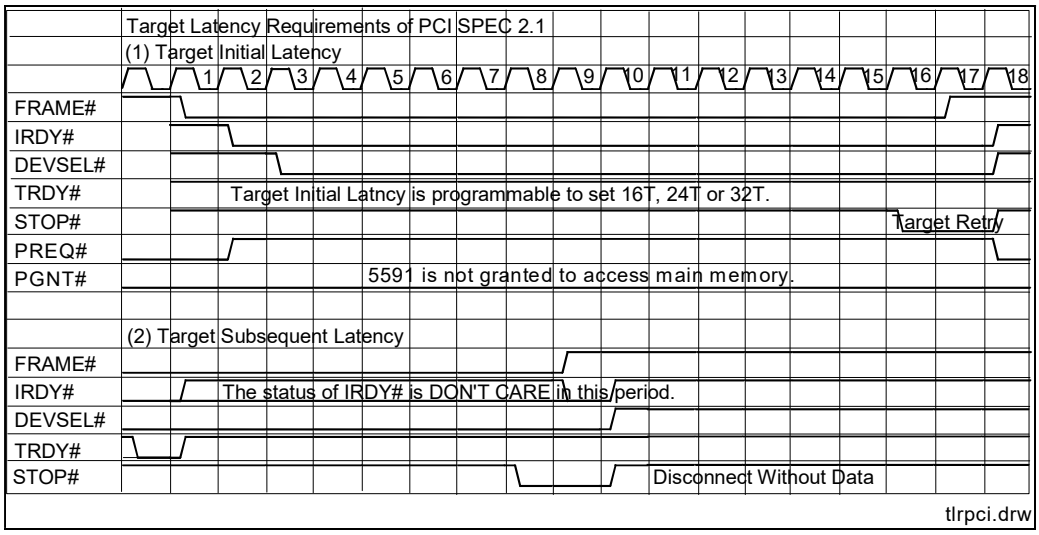


Figure 6.4-5 Disconnect without Data

6.4.4.7 DATA Flow

The major two data paths are PCI->PTHFF->DRAM and DRAM->CTPFF->PCI for PCI master write DRAM cycles and read DRAM cycles, respectively. For cache system, if an inquiry cycle hits Pipeline Burst SRAM, SiS5591/5592 would read from L2 directly, but write DRAM and L2 simultaneously.

Based on snooping result, there is additional data path that SiS5591/5592 should perform.

Table 6.4-2 Data Flow Based on Snooping Result

PCI Master Read Memory Cycle			
Result of Snoop			
Status of L1	Status of L2	Data Flow	Operation
	Miss or None	DRAM -> CTPFF -> PCI	Read DRAM
Miss or Unmodified	Hit and Not Dirty	DRAM -> CTPFF -> PCI	Read DRAM
	Hit and Dirty	L2 -> CTPFF -> PCI	Read L2
	Miss or None	L1 -> CTMFF & CTPFF	Direct Read
		CTPFF -> PCI	
Hit Modified	Hit, Dirty or Not	L1 -> L2 & CTPFF	Direct Read
		CTPFF -> PCI	

PCI Master Write Memory Cycle			
Result of Snoop			
Status of L1	Status of L2	Data Flow	PSL Operation
	Miss or None	PCI -> PTHFF -> DRAM	Write DRAM
Miss or Unmodified	Hit, Dirty or Not	PCI -> PTHFF -> L2&DRAM	Write DRAM&L2
	Miss or None	L1 -> CTMFF	
		PTHFF & CTMFF -> DRAM	Write Merge
Hit Modified	Hit, Dirty or Not	L1 -> L2	
		PCI -> PTHFF -> L2&DRAM	Write DRAM&L2

Note: CTPFF means CPU-to-PCI Posted Write Buffer.
CTMFF means CPU-to-Memory Posted Write Buffer
PTMFF means PCI-to-Memory Posted Write Buffer

In order to eliminate the penalty of partial write when ECC is enabled, PCI Target Bridge provides refined data paths for write cycle if internal dirty bit is used. The major difference is that PCI Target Bridge would only write L2 while an inquiry cycle hits L2. The table of data flow is as follows.

PCI Master Write Memory Cycle			
Result of Snoop			
Status of L1	Status of L2	Data Flow	PSL Operation
	Miss or None	PCI -> PTHFF -> DRAM	Write DRAM
Miss or Unmodified	Hit, Dirty or Not	PCI -> PTHFF -> L2&Set Dirty	Write L2 Only
	Miss or None	L1 -> CTMFF	
		PTHFF & CTMFF -> DRAM	Write Merge
Hit Modified	Hit, Dirty or Not	L1 -> L2	
		PCI -> PTHFF -> L2&Set Dirty	Write L2 Only

6.4.4.8 PCI Master Read/Write DRAM Cycle

If inquiry cycle hits neither L1 nor L2, SiS5591/5592 could perform prefetching/retiring operation and inquiry cycles simultaneously.

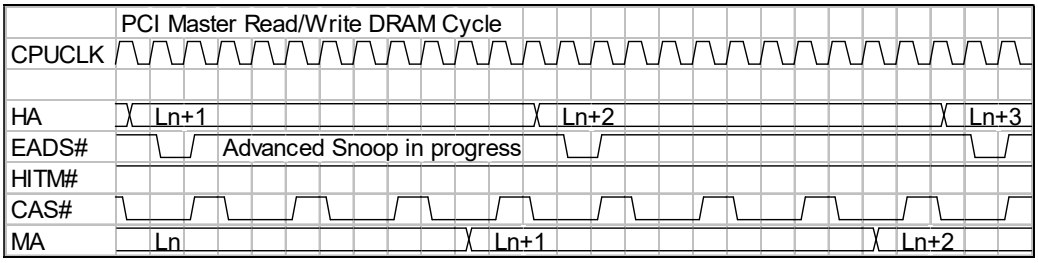
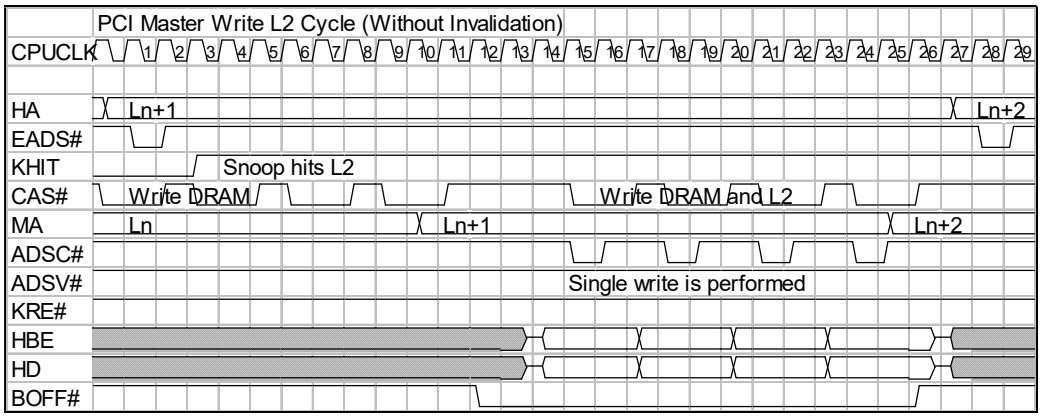


Figure 6.4-6 PCI Master Read/Write DRAM Cycle

6.4.4.9 PCI Master Write L2 and DRAM Cycles

(1) Without Invalidation

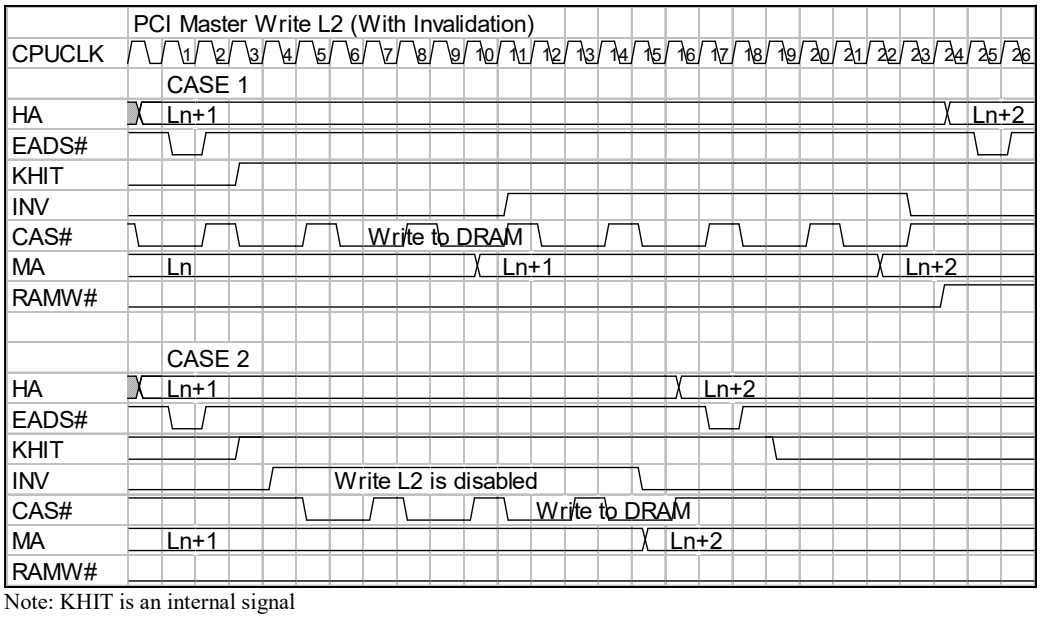
For the purpose of writing L2, PCI Target Bridge must drive the HBE and HD bus. Then, BOFF# is asserted to force CPU floats the host bus. And to retain the correct address on HA, advanced snoop is temporally suspended.



Note: KHIT is an internal signal.

Figure 6.4-7 PCI Master Write L2 and DRAM Cycles(Without Invalidation)

(2) With Invalidation



Note: KHIT is an internal signal

Figure 6.4-8 PCI Master Write L2 and DRAM Cycles (With Invalidation)

6.4.5 66Mhz PCI Target Bridge (PSL66)

PSL66 claims PCI transactions that are destining system memory or 33Mhz PCI bus. All memory write accesses with PCI protocol initiated by A.G.P. compliant master are claimed by PSL66.

For memory read cycles, PSL66 only claims transactions that are targeting system memory.

The system memory referred above includes main memory range and Graphics Window.

PSL66 would not respond to I/O, PCI configuration, Interrupt acknowledge and special cycles. If the A.G.P. compliant master generates any of these cycles, the cycle will be ended with master-abort.

PSL66 is responsible for maintaining data consistence between CPU cache, L2 cache and system DRAM. That means PSL66 should snoop CPU cache, retrieve data from L2 cache and update data to L2 cache.

When PSL66 is processing accesses toward system DRAM, it checks whether the CPU is held or not. If the CPU is not held, PSL66 generates hold request to host interface. Host interface responds to this hold signal by asserting HLDA66. After the HLDA is returned, PSL66 has totally control over the host bus and then the accesses can be continued.

PSL66 and PMR66 share the same FIFO (CTAFF and ATHFF). The usage of the shared FIFO is mutual exclusive. PSL66's operation toward system memory will be suspended until all PMR66's data are flushed out of CTAFF.

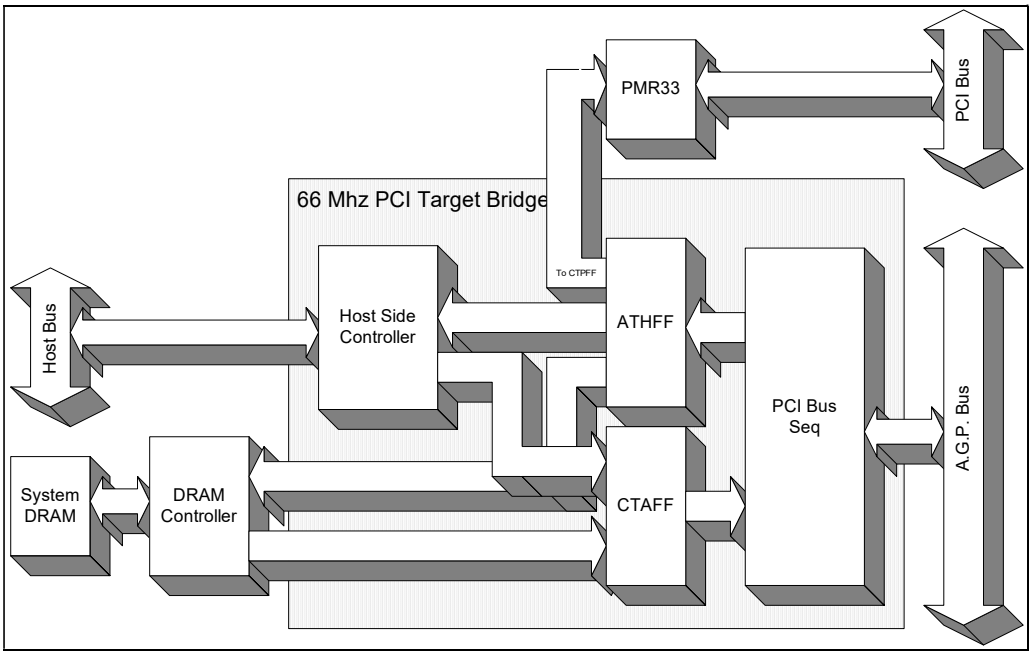


Figure 6.4-9 Block Diagram of 66Mhz PCI Target Bridge

In general, the functions of PSL66 are the same with the ones of PSL33. For further details of functional descriptions, make reference to the paragraph of PSL33.

6.5 A.G.P. COMPLIANT TARGET/HOST-TO-PCI66 BRIDGE

A.G.P. Compliant Target/Host-to-PCI66 Bridge is constituted by 4 blocks: A.G.P. arbiter, A.G.P. Target, PMR66 and PSL66. The A.G.P. arbiter coordinates the operation of A.G.P. Target, PMR66 and A.G.P. compliant master. The A.G.P. target is response for transferring data between A.G.P. bus and dram controller when the A.G.P. compliant target initiate bus transactions with A.G.P. protocol. PMR66 forward cycles from host bus or 33Mhz PCI bus to A.G.P. bus with PCI protocol. PSL66 claims PCI transactions which are destining to system memory.

6.5.1 Block Diagram

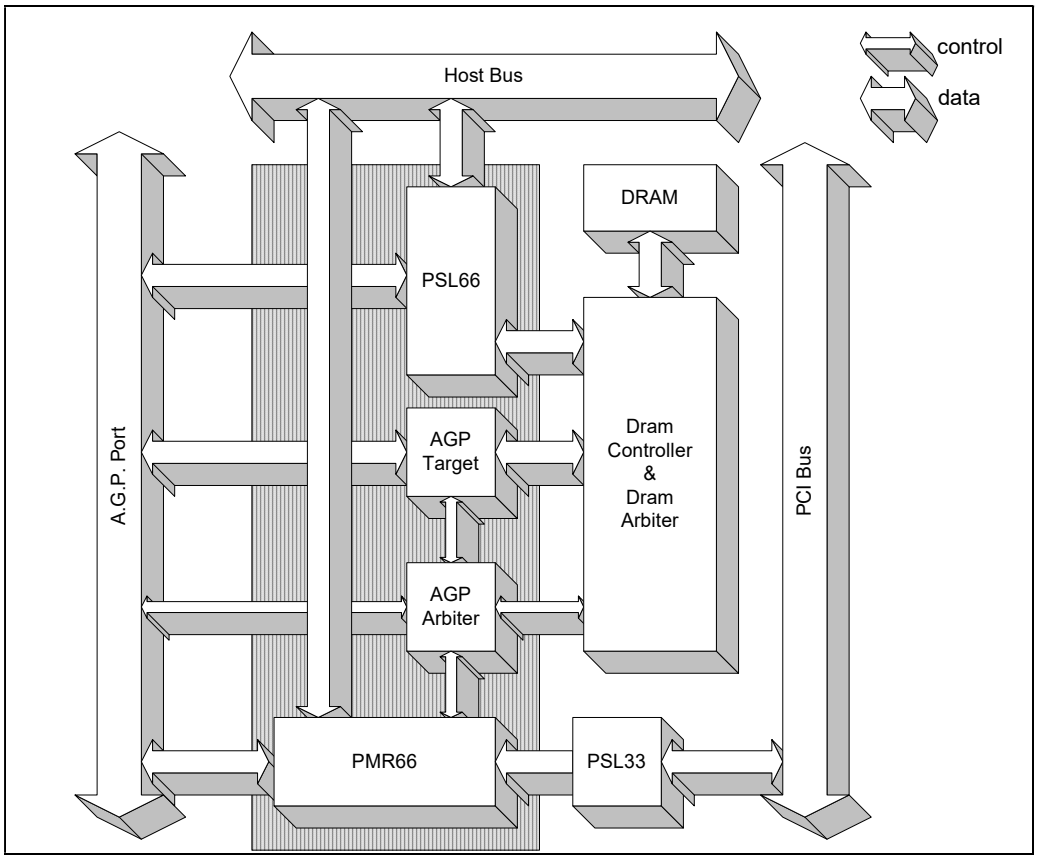


Figure 6.5-1 Block Diagram of AGP Compliant Target/Host-to-PCI66 Bridg

6.5.2 A.G.P. Arbiter

A.G.P. Arbiter serves several roles in the system. It allocates A.G.P. port among A.G.P. data transactions, CPU to A.G.P. transactions, A.G.P. compliant master initiated PCI transactions and A.G.P. data requests enqueued by PIPE#. It reserves a fair system bandwidth for CPU by a timer-based hold mechanism. It arranges the order of A.G.P. data transactions to be returned to A.G.P. compliant target to get better A.G.P. port utilization. It also adjusts the order of DRAM accesses among A.G.P. data transactions to minimize transaction latency and maximize DRAM throughput.

The allocation of A.G.P. port among various operations is done through the priority structure maintained by A.G.P. arbiter. The priority structure has three layers. High-priority data transactions are located in the first layer and they always have superior priority over other kinds of operations. The second layer contains PCI transactions and A.G.P. low priority data transactions. The third layer has two separate groups. The first group of the layer contains A.G.P. Master initiated PCI transactions and PMR66 initiated PCI transactions, and the other group contains low-priority read transactions and high-priority write transactions. The privilege of each layer(or group) is changed in rotational manner. Please refer register D4h, D5h, and D6h for more information about the priority rotation.

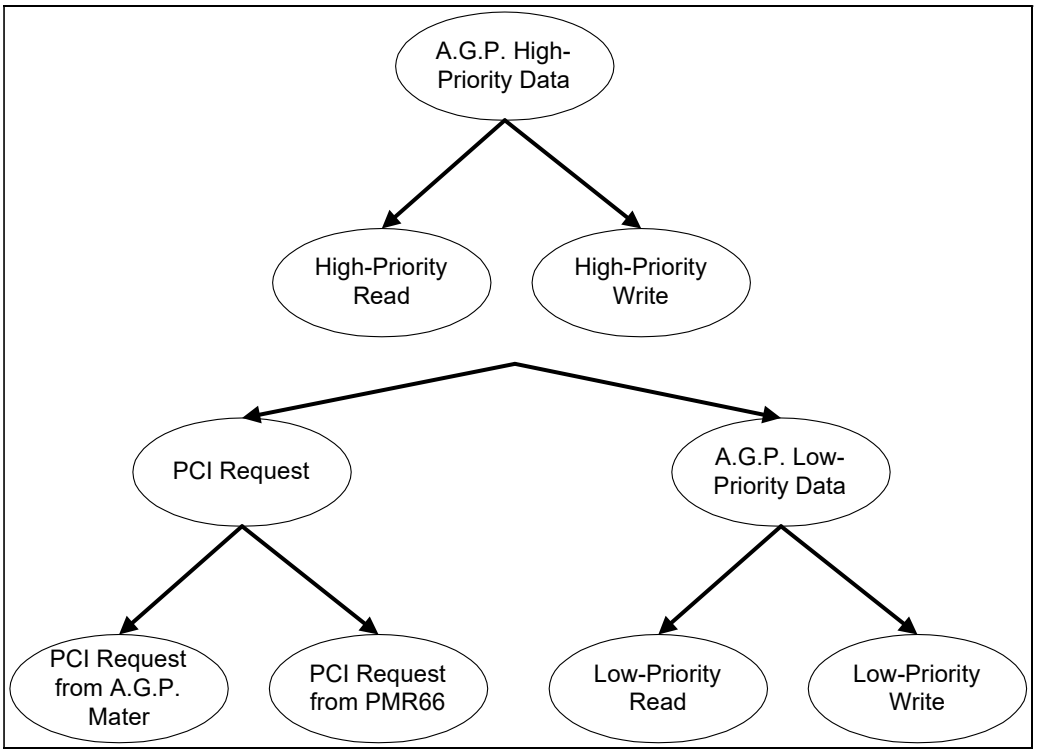


Figure 6.5-2 Priority Structure of A.G.P. Arbiter

To prevent CPU from being constantly held, a timer-based hold mechanism is used to provide CPU a fair system bandwidth. A.G.P. grant counter is decrease by one every clock when CPU is held by A.G.P. master. When the timer expired, A.G.P. arbiter forces the master to relinquish A.G.P. by removing its grant for PCI transactions. CPU latency timer and CPU idle timers are now used to guarantee the minimum system bandwidth for CPU and to prevent system from idling.

The maximum number of A.G.P. command requests that A.G.P. arbiter can manage is 32. The enqueued requests are managed in pipelined manner by A.G.P. arbiter and the A.G.P. arbiter may rearrange the order of these requests to get best system performance.

6.5.3 A.G.P. Compliant Target

The A.G.P. compliant target controls the data flow on A.G.P. port and does data transfer to and from DRAM controller. To prevent from inserting wait states on A.G.P. during low-priority data read transactions, a programmable threshold point is included in A.G.P. compliant target. A.G.P. compliant target requests A.G.P. arbiter for asserting low-priority read grant only when the read buffer of the A.G.P. compliant target contains more data items than the value defined by the threshold point.

6.6 POWER MANAGEMENT SUPPORT

To support power management feature of SiS5595, SiS5591/5592 reports all PCI masters′ activities and optionally reports activities on A.G.P. bus. SiS5591/5592 to SiS5595 via the pin BMREQ#. The information contained by BMREQ# can be classified into two categories. The first category is CPU operation and the second category is master operation. Each category occupies different time slot. If BMREQ# is reporting CPU operation

in this clock, then BMREQ# will report master operation in the next clock and vice versa. Configuration Register 69h of host bridge is used to define what kinds of operations should be reported.

SiS5591/5592 may also trap ACPI I/O port accesses to support ACPI S3 and S2 states and to disable system arbiter. Configuration register 6Ah is used to define the ACPI I/O space base address and SiS5591/5592 uses this register to trap the ACPI I/O port accesses.

6.7 BALL CONNECTIVITY TESTING

SiS Chip will provide a NAND chain Test Mode by TEST_PIN signal is pull low. In order to ensure the connections of balls to tracks of main board, SiS Chip provides a simple way to do connective measurements. Basically, an additional 2-input-NAND gate is added into the I/O buffer cells. And, one of inputs of NAND gate is connected to input pin of I/O buffer as test input port in test mode. To monitor the test result at test output port, the output of the NAND gate is connected to the other input of the next NAND gate. Such that, the test result could be propagated and it forms a NAND tree, as depicted in Figure6.7-1. To adapt to the scheme, all output buffers of SiS Chip are changed to bi-direction buffers to accept test signals.

6.7.1 Test Scheme

There are six NAND tree chains are provided by SiS Chip. Each NAND tree chain has several test-input pins and one output pin.

The following description is an example on 4-test-input pins to explain a NAND tree chain test scheme.

First of all, logic LOW is driven into TESTIN1 pin from track on main board. If logic HIGH could be observed at TESTOUT pin, it means that the connection of TESTIN1 pin to track is good, as shown in Figure6.7-2. To test TESTIN2 pin, TESTIN2 pin should be driven LOW also. And, TESTIN1 pin should be kept at logic HIGH, such that the test result could be passed to TESTOUT pin and so on. Although SiS Chip operates at 3.3V, all input buffers of SiS Chip are 5V-input tolerance. Hence, all test signal could go up to 5V.

6.7.2 Measurements

During test process, this scheme requires all test inputs to be driven simultaneously. To decrease the amount of test probes, SiS Chip divide pins into 6 branches. Meanwhile, some noise sensitive signals or analogue signals, i.e. RTC, and power signals, are excluded. The final number of test-input probes is limited to 78 and these six NAND trees are listed in Table 6.5-1 NAND Tree List on next page.

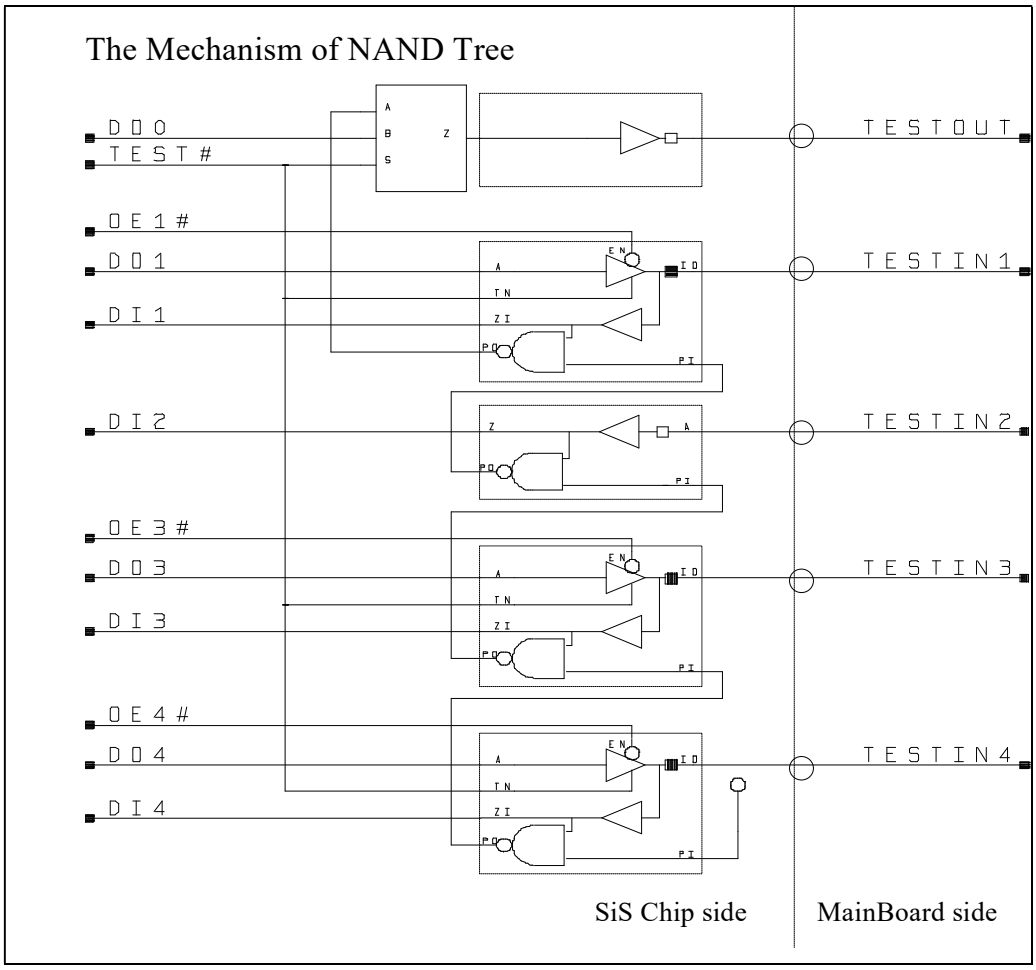


Figure 6.5-3The Mechanism of NAND Tree

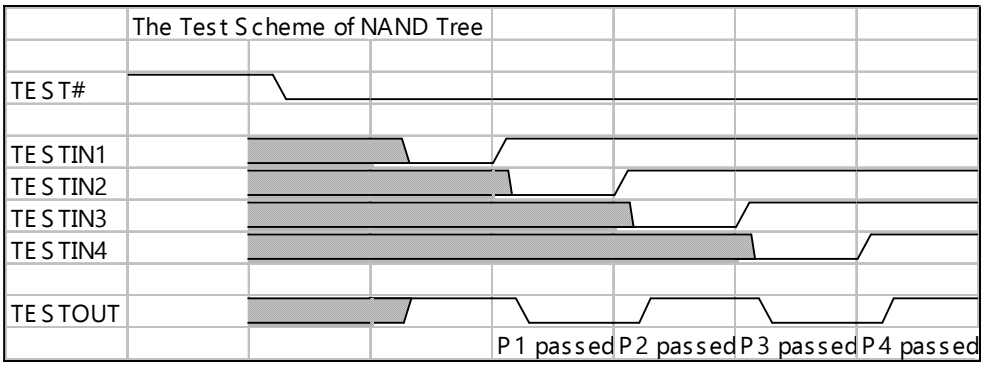


Figure 6.5-4 The Test Scheme of NAND Tree

Table 6.5-1 NAND Tree List for SiS5591/5592

TEST VECTORS	TEST INPUT BALL NAME LIST	TEST OUTPUT BALL NAME
NT1[1:61] (NAND Tree 1)	AAD0, AAD2, AAD1, AAD3, AAD4, AAD7, AAD5, AAD6, AC/BE0#, AD_STB0, AAD8, AAD9, AAD10, AAD11, AAD12, AAD13, AAD14, AAD15, AC/BE1#, ASERR#, ASTOP#, APAR, ADEVSEL#, ATRDY#, AIRDY#, AFRAME#, AC/BE2#, AAD18, AAD16, AAD19, AAD20, AAD17, AAD21, AAD22, AAD23, AC/BE3#, AD_STB1#, AAD25, AAD26, AAD27, AAD24, AAD28, AAD29, AAD30, AAD31, PIPE#, RBF#, AGNT#, SBA7, SBA6, SBA5, SBA4, SB_STB, SBA3, SBA2, SBA1, SBA0, ST2, ST1, ST0, AREQ#	PGNT4#
NT2[1:71] (NAND Tree 2)	IDA15, IDA0, IDA14, IDA1, IDA13, IDA2, IDA12, IDA3, IDA11, IDA4, IDA10, IDA5, IDA9, IDA6, IDA8, IDA7, IRQ15, IRQ14, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, C/BE0#, PCICLK, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, C/BE1#, PAR, SERR#, STOP#, PLOCK#, DEVSEL#, TRDY#, IRDY#, FRAME#, C/BE2#, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, C/BE3#, AD24, AD25, AD26, AD27, AD28, AD29, AD30, AD31, PREQ3#, PREQ2#, PREQ1#, PREQ0#, PCIRST#, A.G.P.CLK, PHOLD#, PREQ4#	PHLDA#
NT3[1:67] (NAND Tree 3)	HA20, HA19, HA18, HA17, HA16, HA14, HA15, HA13, HA12, HA9, HA10, HA11, HA8, HA5, HA6, HA7, HA4, HA3, HA30, HA29, HA28, HA31, HA25, HA26, HA22, HA27, HA24, HA21, HA23, IDECS1B#, IDECS0B#, IDSA2B, IDSA0B, IDSA1B, IIRQB, IDACKB, ICHRDYB, IIORB, IIOWB, IDRQB, IDB15, IDB0, IDB14, IDB1, IDB13, IDB2, IDB12, IDB3, IDB11, IDB4, IDB10, IDB5, IDB9, IDB6, IDB8, IDB7, IDECS1A#, IDECS0A#, IDSA2A, IDSA0A, IDSA1A, IIRQA, IDACKA#, ICHRDYA, IIORA#, IIOWA#, IDREQA#	PGNT0#
Nt4[1:67] (NAND Tree 4)	HD34, HD37, HD36, HD39, HD38, HD42, HD40, HD46, HD44, HD45, HD41, HD43, HD47, HD48, HD49, HD50, CPUCLK, HD52, HD51, HD53, HD54, HD55, HD56, HD57, HD58, HD59, HD60, HD61, HD62, HD63, GWE#, BWE#, KOE#, ADSC#, ADSV#, CCS1#, TAGWE#, TA7, TA6, TA5, TA4, TA3, TA2, TA1, TA0, M/IO#, CACHE#, KEN#, AHOLD#, BRDY#, NA#, BOFF#, SMIACT#, HLOCK#, ADS#, D/C#, HITM#, EADS#, W/R#, HBE0#, HBE1#, HBE2#, HBE3#, HBE4#, HBE5#, HBE6#, HBE7#	PGNT1#
NT5[1:70] (NAND Tree 5)	MPD6, MPD2, MPD7, MPD3, MD48, MD16, MD49, MD17, MD50, MD18, MD51, MD19, MD52, MD20, MD53, MD21, MD54, MD22, MD55, MD23, MD56, MD24, MD57, MD25, MD58, MD26, MD59, MD27, MD60, MD28, MD61, MD29, MD30, MD31, HD0, HD2, HD1, HD3, HD4, HD5, HD6, HD7, HD8, HD9, HD10, HD11, HD12, HD14, HD13, HD15, HD18, HD16, HD17, HD22, HD20, HD21, HD19, HD24, HD23, HD26, HD25, HD28, HD27, HD30, HD29,	PGNT2#

	HD31, HD33, HD32, HD35, MD63	
NT6[1:72] (NAND Tree 6)	MD32, MD0, MD33, MD1, MD34, MD2, MD35, MD3, MD36, MD4, MD37, MD5, MD38, MD6, MD39, MD7, MD40, MD8, MD41, MD9, MD42, MD10, MD43, MD11, MD44, MD12, MD45, MD13, MD46, MD14, MD47, MD15, MPD4, MPD0, MPD5, MPD1, SCAS#, RAMWA#, CAS4#, CAS0#, CAS5#, CAS1#, RAS5#, RAS4#, RAS3#, RAS2#, RAS1#, RAS0#, SRAS#, MA0B, MA0A, MA1B, MA1A, MA2, MA3, MA4, MA5, MA6, MA7, MA8, MA9, MA10, MA11, MA12, MA13, CAS6#, CAS2#, CAS7#, CAS3#, RAMWB#, CKE, MD62	PGNT3#

7. CONFIGURATION REGISTER

7.1 HOST-TO-PCI BRIDGE CONFIGURATION SPACE

7.1.1 Host-to-PCI Bridge Configuration Space Header

DEVICE	IDSEL	FUNCTION NUMBER
Host to PCI bridge	AD11	0000b

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	5591h	RO
04-05h	PCI Command Register	0005h	RO,R/W
06-07h	PCI Status Register	0210h	RO, R/W WC
08h	Revision ID	02h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	00h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	FFh	R/W
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10-13h	Graphic Window Base Address	00000000h	RO R/W
14-33h	Reserved		
34h	Capability Pointer	C0h	RO

7.1.2 Registers for Host, L2 Cache & DRAM

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
50h	NA# Control	00h	R/W
51h	L2 Cache Control Register 0	18h	R/W
52h	L2 Cache Control Register 1	00h	R/W
53h	Reserved		
54h	DRAM Controller Characteristics	00h	R/W
55h	DRAM Paging Control	0Eh	R/W
56h	Refresh Control	40h	R/W
57h	DRAM Control	00h	R/W
58h	DRAM Control	50h	R/W
59h	FP/EDO DRAM Control	00h	R/W
5Ah	FP/EDO DRAM Control	00h	R/W

5Bh	Reserved		
5Ch	SDRAM Initialisation Command	00h	R/W
5Dh	SDRAM Control	00h	R/W
5Eh	SDRAM Control	00h	R/W
5Fh	SDRAM Control	00h	R/W
60~62h	DRAM Type Registers of Bank 0/1/2	00h	R/W
63h	DRAM Status Register	FFh	R/W

7.1.3 Current Driving

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
64h	DRAM Signals Driving Current Control	00h	R/W
65h	PCI/A.G.P. Signals Driving Current Control	00h	R/W

7.1.4 Power Management

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
68h	SMRAM Access Control	00h	R/W
69h	System Event Monitor Control for Power Management	00h	R/W
6A~6Bh	ACPI I/O Base Address Register	0000h	R/W
6Ch	DRAM Self-Refresh Control for Power Management	00h	R/W

7.1.5 Shadow RAM & Non-cacheable Area

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
70~75h	Shadow RAM Register	00h	R/W
76h	BIOS Shadow Attribute	00h	R/W
77h	Non-cacheable Area Characteristics	00h	R/W
78~79h	Allocation of Non-cacheable area I	0000h	R/W
7A~7Bh	Allocation of Non-cacheable area II	0000h	R/W

7.1.6 Target Bridge to DRAM Characteristics

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
80h	Target Bridge to DRAM Characteristics	00h	R/W

7.1.7 33Mhz Host Bridge & PCI Arbiter

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
81h	PCI33 Target Bridge Characteristics	00h	R/W

82h	PCI33 Target Bridge Bus Characteristics	00h	R/W
83h	CPU to PCI33 Characteristics	00h	R/W
84~85h	PCI33 Grant Timer	FFFFh	R/W
86h	CPU Idle Timer for PCI	FFh	R/W
87h	CPU to PCI33 Characteristics and Arbitration option	00h	R/W
88~89h	Base Address of Frame Buffer Area for fast back-to-back Transaction	0000h	R/W
8A~8Bh	Size of Frame Buffer Area	0000h	R/W

7.1.8 DLL & PLL Control

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
8Ch	DLL Control	00h	R/W
8Dh	PLL Control	00h	R/W

7.1.9 GART and Page Table Cache Registers

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
90~93h	GART Base Address for 1-level Re-mapping	00000000h	R/W
94h	Graphic Window Control	00h	R/W
95~96h	Reserved		
97h	Page Table Cache Control	00h	R/W
98~9Bh	Page Table Cache Invalidation Control	00000000h	R/W
9C~9Fh	DIR Base Address for 2-level remapping	00000000h	R/W

7.1.10 Flush L2

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
A0~A3h	L2 Flushing Control	00000000h	R/W
A4h	L2 Flushing Function & DRAM Bandwidth Sharing Control	00h	R/W
A5h	L2 Flushing Priority Timer	00h	R/W

7.1.11 DRAM Priority Timer

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
A6~A7h	CPU-A.G.P. Privilege Timer	0000h	R/W
A8~A9h	PCI33-A.G.P. Privilege Timer	0000h	R/W
AA~ABh	PCI66-A.G.P. Privilege Timer	0000h	R/W

7.1.12 Error Control & Status

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
B0h	Error Reporting Control	00h	R/W
B2h	Error Status	00h	WC RO

7.1.13 A.G.P. and 66MHz Host Bridge

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
C0~C3h	A.G.P. Capability Identify Register	00100002h	RO
C4~C7h	A.G.P. Status Register	1F000203h	RO
C8~CBh	A.G.P. Command Register	00000000h	R/W
CC~D3h	Reserved		
D4h	A.G.P. Priority Rotation Timer	00h	R/W
D5h	Data Priority Timer	00h	R/W
D6h	Write Buffer Flush Counter & Data Transfer Counter	00h	R/W
D7h	CPU Idle Timer on A.G.P.	00h	R/W
D8~D9h	A.G.P. Grant Timer	0000h	R/W
DAh	CPU Latency Timer on A.G.P.	00h	R/W
DB~DFh	Reserved		
E0h	A.G.P. Compliant Target / Arbiter Control Register.	00h	R/W
E1h	PCI66 Target Bridge Characteristics	00h	R/W
E2h	PCI66 Target Bridge Characteristics	00h	R/W
E3h	CPU to PCI66 Bridge Characteristics	00h	R/W

7.1.14 Miscellaneous Control

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
EFh	Miscellaneous function	00h	R/W

7.2 DEVICE 2 (VIRTUAL PCI-TO-PCI BRIDGE)

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	0001h	RO
04-05h	PCI Command Register	0000h	RO R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	00h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	04h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO

0Dh	Master Latency timer	00h	RO
0Eh	Header Type	01h	RO
0Fh	BIST	00h	RO
19h	Secondary Bus Number	00h	R/W
1Ah	Subordinate Bus Number	00h	R/W
1Bh	Secondary Master Latency Timer	00h	R/W
1Ch	I/O Base	F0h	R/W RO
1Dh	I/O Limit	00h	R/W RO
1Eh	Secondary PCI-PCI Status	0000h	R/W RO
20~21h	Non-prefetchable Memory Base Address	FFF0h	R/W RO
22~23h	Non-prefetchable Memory Limit Address	0000h	R/W RO
24~25h	Prefetchable Memory Base Address	FFF0h	R/W RO
26~27h	Prefetchable Memory Limit Address	0000h	R/W RO
28~3Dh	Reserved		
3Eh	PCI to PCI Bridge Control	0000h	RW RO

7.3 PCI IDE DEVICE

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	5513h	RO
04-05h	PCI Command Register	0000h	RO R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	D0h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	01h	RO
0Bh	Base Class Code	01h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	00h	RO
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10h~13h	Primary Channel Command Block Base Address Register	00h	R/W
14h~17h	Primary Channel Control Block Base Address Register	00h	R/W

18h~1Bh	Secondary Channel Command Block Base Address Register	00h	R/W
1Ch~1Fh	Secondary Channel Control Block Base Address Register	00h	R/W
20h~23h	Bus Master IDE Control Register Base Address	00h	R/W
24h~2Bh	Reserved		
2Ch	Subsystem ID	00h	R/W
2Dh~2Fh	Reserved		
30h~33h	Expansion ROM Base Address	0000h	R/W
40h	IDE Primary Channel/Master Drive Data Recovery Time	00h	R/W
41h	IDE Primary Channel/Master Drive Data Active Time	00h	R/W
42h	IDE Primary Channel/Slave Drive Data Recovery Time	00h	R/W
43h	IDE Primary Channel/Slave Drive Data Active Time	00h	R/W
44h	IDE Secondary Channel/Master Drive Data Recovery Time	00h	R/W
45h	IDE Secondary Channel/Master Drive Data Active Time	00h	R/W
46h	IDE Secondary Channel/Slave Drive Data Recovery Time	00h	R/W
47h	IDE Secondary Channel/Slave Drive Data Active Time	00h	R/W
48h	IDE Command Recovery Time Control	00h	R/W
49h	IDE Command Active Time Control	00h	R/W
4Ah	IDE General Control Register 0	00h	R/W
4Bh	IDE General Control Register 1	00h	R/W
4Ch~4Dh	Prefetch Count of Primary Channel	FFFFh	R/W
4Eh~4Fh	Prefetch Count of Secondary Channel	FFFFh	R/W
50h~51h	IDE minimum accessed time register	0000h	R/W
52h	IDE Miscellaneous Control Register	00h	R/W

8. REGISTER DESCRIPTIONS

8.1 HOST BRIDGE REGISTERS (FUNCTION 0)

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 5591h

Access: Read Only

The device identifier is allocated as 5591h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0005h

Access: Read/Write, Read Only

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:10	RO	**Reserved**
9	R/W	**Fast Back-to-Back Enable** This bit controls whether or not the host bridge can do fast back-to-back transactions to different devices. Please note that even when this bit is disabled, the host bridge may still do fast back-to-back transactions if the host bridge can guarantee that the adjacent transactions are destining to the same device. The register that controls fast back-to-back transactions to the same agent is located in Register 83h of Host to PCI bridge configuration space. 0: Disable 1: Enable
8	R/W	**SERR# enable** This bit controls the SERR# driver. When this bit is disabled, SiS5591/5592 would not drive SERR# under any condition. When this bit is enabled, SiS5591/5592 may drive SERR# in responding to ECC error or the assertion of ASERR# on A.G.P. bus. 0: Disable 1: Enable
7:3	RO	**Reserved**
2	RO	**Bus Master** This bit is read-only and the default value is 1. That means you cannot disable bus master function of the host bridge.

1	R/W	**Memory Space** The bit controls the response to memory space accesses. When the bit is disabled, the host bridge neglect all accesses from PCI masters. 0: Disable 1: Enable
0	RO	**I/O Space** Default value is 1. The host bridge only respond to the addresses 0CF8h and 0CF9h in I/O space, and the I/O transaction must be generated by the host bridge itself.

Register 06h Status

Default Value: 0210h

Access: Read/Write, Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

BIT	ACCESS	DESCRIPTION
15	RO	**Detected Parity Error** This bit is always 0, SiS5591/5592 does not support parity checking on the PCI bus.
14	WC	**Signaled System Error** This bit is set whenever SiS5591/5592 drives SERR#. It is cleared by writing a 1 to it.
13	WC	**Received Master Abort** This bit is set by SiS5591/5592 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12	WC	**Received Target Abort.** This bit is set by SiS5591/5592 whenever it terminates a transaction with target abort. This bit is cleared by writing a 1 to it.
11	RO	**Signaled Target Abort** This bit is always 0 since SiS5591/5592 will never respond a transaction with target abort.
11:9	RO	**DEVSEL# Timing DEVT.** The two bits define the timing to assert DEVSEL#. SiS5591/5592 always asserts DEVSEL# within two clocks after the assertion of FRAME#. Default value is DEVT=01.
8	RO	**Reserved**
7:5	RO	**Reserved**
4	RO	**CAP_LIST Bit** The default value is 1 to indicate the configuration space of SiS5591/5592 implements new capability mechanism.
3:0	RO	**Reserved.**

Register 08h Revision ID

Default Value: 02h

Access: Read Only

The Revision ID is 02h for SiS 5591/5592 A2 stepping.

BIT	ACCESS	Description
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 00h

Access: Read Only

The Sub Class Code is 00h for host bridge.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h

Access: Read Only

The value of 06h in this field identifies a bridge device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

The value of this register is always 00h since the host bridge would not generate the Memory Write and Invalidate command.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: FFh

Access: Read/Write

The MLT is used in conjunction with PGT(Register 84h) and CIT(Register 86h) to provide a fair and efficient system arbitration mechanism. The value of MLT guarantees the minimum system bandwidth for CPU when both CPU and PCI masters are all craving for system resources(system memory or PCI bus).

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Master Latency Timer** Power-on default value is FFh but we recommend you to set its value to 20h. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

The value of 80h implies that SiS5591/5592 is a multiple function device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

The value is 00h since we do not support Build-in Self Test.

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 10h Graphic Window Base Address (GWBA)

Default Value: 00000000h

Access: Read/Write, Read Only

The register defines the starting address of the graphic window for A.G.P. Accessibility and effectiveness of this register is controlled by the Graphic Window Control Register(Register 94h).

BIT	ACCESS	DESCRIPTION										
31:22	R/W RO	**Define A[31:22] of Graphic window base address** The accessibility of this bits[31:22] are controlled by graphic window size(Bits[6:4], Register 94h).										
		Bit31	**Bit30**	**Bit29**	**Bit28**	**Bit27**	**Bit26**	**Bit25**	**Bit24**	**Bit23**	**Bit22**	**Size**
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	4M
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	8M
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	16M
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	32M
		R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	64M
		R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	128M
		R/W	R/W	R/W	R/W	0	0	0	0	0	0	256M
21:0	RO	**Reserved and read as zeroes.**										

8.1.1 Host/L2 Cache/DRAM Control Register

Register 34h Capability Pointer (CAPPTR)

Default Value: C0h

Access: Read Only

The value of C0h indicates that the A.G.P. standard register block is started from Register C0h.

BIT	ACCESS	Description
7:0	RO	**Capability Pointer** Pointer to the Start of A.G.P. standard register block.

Register 50h NA Control

Default Value: 00h

Access: Read/Write

The register controls when and how the core logic assert NA# to CPU for allowing address/data pipelining on the host bus.

BIT	ACCESS	DESCRIPTION
7	R/W	**NA# assert Control** When this bit is disabled, SiS5591/5592 would not assert NA# under any circumstance. When this bit is enabled, SiS5591/5592 asserts NA# for all burst read cycles and I/O cycles. However, I/O address 0CF8h and 0CFCh are the only exceptions and SiS5591/5592 would not asserts NA# for these I/O cycles. Bits[6:4] control how and when SiS5591/5592 asserts NA# if this bit is enabled. 0: Disable 1: Enable
6	R/W	**Memory Single Write Cycle NA#** Please note that the value of "0" means enable and "1" indicates disable for this bit. When this bit is enabled, SiS5591/5592 asserts NA# for all memory single write cycles regardless of the destination of the cycles. When this bit is disabled, SiS5591/5592 would not respond NA# to CPU for all single memory write cycles. This bit can only be enabled when the internal dirty SRAM is used. 0: Enable 1: Disable
5	R/W	**NA# Timing for L2 Cache-hit Burst Read Cycle** This bit controls when SiS5591/5592 asserts NA# for L2 cache-hit burst read cycles. When the bit is 0, SiS5591/5592 asserts NA# and the 1st BRDY# for the burst read cycle exactly at the same time. When the bit is 1, SiS5591/5592 asserts NA# one clock after the 1st BRDY# is returned to CPU. It is recommended to set this bit to 1 if there are two banks of PB SRAM in the system. 0: Normal 1: Delay 1 CPU clock
4	R/W	**NA# Timing for L2 Cache-miss Burst Read Cycle** Please note that this bit can be set to 1 only when the system adopts SDRAM and there is no other types of DRAM. This bit controls when SiS5591/5592 asserts NA# for L2 cache-miss burst read cycles. When the bit is 0, SiS5591/5592 asserts NA# and the 1st BRDY# for the burst read cycle exactly at the same time. When the bit is 1, SiS5591/5592 asserts NA# one clock before the 1st BRDY# is returned to CPU. 0: Slower 1: Faster
3:0	R/W	**Reserved**

Register 51h L2 Cache Control Register 0

Default Value: 18h

Access: Read/Write

L2 Cache Control register 0 and 1 define the configuration and characteristics of the L2 cache.

BIT	ACCESS	DESCRIPTION

7	R/W	**L2 Cache Enable** When no L2 exists, this bit should be programmed to 0. 0: Disable 1: Enable
6	R/W	**L2 internal invalid bit enable** When this bit is enabled, SiS5591/5592 uses not only the TAG address but also the internal invalid bit associated with the cache line to determine whether a memory cycle hits L2 cache. When the value of this enable bit is 1 and an internal invalid bit is also set to 1, the corresponding cache line will never cause a L2 cache-hit cycle. The initialization of the internal bits is done with cache by BIOS when system boots up. 0: Disable 1: Enable
5:4	R/W	**L2 Cache Size** The register specifies the L2 cache size of the system. **Bits[5:4]** **Size** 00 Reserved 01 256K (default) 10 512K 11 1M
3	R/W	**L2 Cache WT/WB Policy** The register specifies the coherence policy for L2 cache and system DRAM. It is recommended to set this to 0 when BIOS is sizing the L2 cache. 0: Write Through Mode 1: Write Back Mode (default)
2	R/W	**L2 Cache Burst Addressing mode** This bit specifies the addressing mode of CPU burst cycles. The linear mode is used for Cyrix CPU. 0: Toggle Mode 1: Linear Mode
1	R/W	**L2 Cache Tag Size Selection** This bit specifies the size of the TAG address. The value of "0" indicates 7-bit TAG address is used and the bit 7 of TAG address of each cache line is used to record whether the line has been modified or not(dirty bit). The value of "1" indicates 8-bit TAG address is used and internal dirty bit SRAM is served to record whether the corresponding line has been modified. The size of L2 cacheable memory space is also affected by this bit. The size of L2 cacheable memory space for 8-bit TAG is doubled in comparison with 7-bit TAG. 0: 7-bit Tag address 1: 8-bit Tag address
0	R/W	**L2 Cache Sizing Mode** SiS5591/5592 enters its L2 cache sizing mode when this bit is set to 1. In the sizing mode, TAG addresses are neglected and all accesses to system memory are treated as L2 cache hit cycles. This bit should be set to 0 after the L2 cache sizing procedure has finished. 0: Disable 1: Enable

Register 52h L2 Cache Control Register 1

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6	R/W	**Single Read Allocation (L2 Update) Control** When this bit is enabled, any memory single read cycle will cause the corresponding memory line to be updated to L2 cache. 0: Disable 1: Enable
5:2	R/W	**Reserved**
1	R/W	**SRAM Power Down Test Mode** This bit is for internal usage only, and must be programmed with 0. 0: Normal Mode 1: Test Mode
0	R/W	**Internal SRAM Test Mode** This bit is for internal usage only, and must be programmed with 0. 0: Normal Mode 1: Test Mode

Register 54h DRAM Controller Characteristics

Default Value: 00h

Access: Read/Write

The 8-bit register controls various advance features for DRAM controller and DRAM error reporting/handling functions.

BIT	ACCESS	DESCRIPTION
7	R/W	This bit should be programmed to 1.
6	R/W	This bit should be programmed to 1.
5	R/W	**Read FIFO Control** The read FIFO is used to provide a higher level of concurrent degree between host bus and DRAM bus. When the host bus is occupied by another operation and the operation must be done before an currently outstanding memory read cycle on the host bus but there is no strict order between these two operations on the DRAM bus or PCI bus, SiS5591/5592 may try to complete the memory cycle on the DRAM bus first and latch the result on the read FIFO. However, SiS5591/5592 would not try to complete the memory read cycle on the host bus until the preceding operation has been finished on the host bus. 0: Disable 1: Enable
4	R/W	**Reserved**
3	R/W	**ECC Support** When this bit is enabled, SiS5591/5592 corrects one-bit memory access error and optionally reports two-bit memory access error. When this bit is enabled, the error reporting control register(Register B0h bit0) determines whether two-bit memory error will be reported in error status register(Register B2h bit0). 0: Disable 1: Enable

2	R/W	**Parity Check Support** When this bit is enabled, SiS5591/5592 detects memory access parity error and optionally reports the error in error status register(Register B2h bit0). Whether or not the parity error should be reported in error status register is determined by the error reporting control register(Register B0h bit0). 0: Disable 1: Enable
1:0	R/W	**Reserved**

Register 55h DRAM Paging Control

Default Value: 0Eh

Access: Read/Write

This register controls the paging prediction options for various cycles. Please note that some bits' default values of this register are set to 1.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Starting Point of Paging Function** This register controls when to precharge RAS# after the DRAM cycle that its page miss option is enabled. **Bits[7:6]** **Delay** 00 1T 01 2T 10 4T 11 8T
5:4	R/W	**Reserved**
3	R/W	**Always Page Miss After Write DRAM Cycles** 0: Disable 1: Enable (default)
2	R/W	**Always Page Miss After Data Read DRAM Cycles** 0: Disable 1: Enable (default)
1	R/W	**Always Page Miss After Code Read DRAM Cycles** 0: Disable 1: Enable (default)
0	R/W	**Always Page Miss after Graphics Window Range Access** 0: Disable 1: Enable

Register 56h Refresh Control

Default Value: 40h

Access: Read/Write

This register controls the characteristics of DRAM refresh operation.

BIT	ACCESS	DESCRIPTION

7:6	R/W	**RAS# Pulse Width** This field controls the RAS# pulse width for refresh cycle **For EDO/FPM DRAM** |**For SDRAM** **Bits[7:6] Plus Width** | **Bits[7:6] Plus Width** 00 5T | 00 4T 01 6T(default) | 01 5T(default) 10 7T | 10 6T 11 8T | 11 7T
5:4	R/W	**Refresh Queue Depth** Bits[5:4] controls the depth of refresh queue. To minimize the performance penalty caused by refresh cycles, the concept of refresh queue is introduced. Refresh request is arbitrated with other DRAM request. If a refresh request does not get served, it enters the refresh queue. The priority of refresh request is promoted to highest when the refresh queue is full. **Bits[5:4] Depth** 00 0 01 4 10 8 11 12
3	R/W	**Refresh Cycle Time** This bit controls in how many clocks that SiS5591/5592 generates a new DRAM refresh request. 0: 1040 CPU Clocks (for low bus frequency) 1: 1300 CPU Clocks (for high bus frequency)
2:1	R/W	**Reserved**
0	R/W	**DRAM Refresh Test Mode** For internal test only, please program this bit with 0. 0: Normal Mode 1: Test Mode

Register 57h DRAM Control

Default Value: 00h

Access: Read/Write

This register controls lead-off time for DRAM read cycles and the timing of DRAM back-to-back read.

BIT	ACCESS	DESCRIPTION
7	R/W	**DRAM Read Lead-off Time Delay Control** 0: Normal 1: Slower 1T
6:5	R/W	**DRAM Read Command Timing Control** This bits control whether to delay the read command or not. It is used to meet the setup time of MA in high bus frequency, when necessary. **Bits[6:5] Meaning** 0X Zero wait state 10 One wait state 1T only when the second read accesses the Virtual graphic window 11 Always one wait state

4:0	R/W	**Reserved**

Register 58h DRAM Control

Default Value: 50h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**RAS Precharge time for SDRAM & EDO/FP DRAM** **Bits[7:6]** **Description** 00 2T 01 3T (default) 10 4T 11 5T
5:4	R/W	**RAS to CAS Delay for SDRAM & EDO/FP DRAM** **Bits[5:4]** **Description** 00 Reserved 01 3T (default) 10 4T 11 5T
3	R/W	**Read Cycle CAS# Pulse Width for EDO DRAM** 0: 2T 1: 1T
2	R/W	**Read Cycle CAS# Pulse Width for FP DRAM** 0: 2T 1: 1T
1	R/W	**Write Cycle CAS# Pulse Width for EDO DRAM** 0: 2T 1: 1T
0	R/W	**Write Cycle CAS# Pulse Width for FP DRAM** 0: 2T 1: 1T

Register 59h FP/EDO DRAM Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**CAS# Precharge Time for FP DRAM** **Bits[7:6]** **Description** 00 1T 01 1T during burst cycles, 2T for different cycles (1 wait state between cycles) 10 2T 11 Reserved

5:4	R/W	**CAS# Precharge Time for EDO DRAM** **Bits[5:4]** — **Description** 00 — 1T 01 — 1T during burst cycles, 2T for different cycles (1 wait state between cycles) 10 — 2T 11 — Reserved
3:1	R/W	**Reserved**
0	R/W	**EDO Test Mode** This bit is used by BIOS to detect whether the Dram is EDO type or not. When this bit is set, SiS5591/5592 will return Brdy# about 212 clocks later. If it is EDO type Dram, the data will still be valid on MD bus. If not, the data will disappear from MD bus. And the data returned to CPU will be wrong. After BIOS detecting, this bit should be programmed to 0. 0: Normal mode 1: Test mode

Register 5Ah FP/EDO DRAM Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	R/W	**Reserved**
3	R/W	**RAMW # Assertion Timing when Read Cycle Followed by Write Cycle** 0: Slower 1T 1: Normal
2:0	R/W	**MDLE Delay** These bits control the delay time of the latch signal MDLE, which keeps the data of MD Bus. Because FP DRAM and EDO DRAM are asynchronous devices, SiS5591/5592 uses a latch to prevent the data changing before next clock's rising edge. The value of delay time depends on the specification of Dram and the load of board. It is recommended to set MDLE delay to 3ns. **Bit[2:0]** — **Delay** 000 — No delay 001 — delay 1 ns 010 — delay 2 ns 011 — delay 3 ns 100 — delay 4 ns 101 — delay 5 ns 110 — delay 6 ns 111 — delay 7 ns

Register 5Bh Reserved.

Register 5Ch SDRAM Initialization Command

Default Value: 00h

Access: Read/Write

This register controls SDRAM initialization process. Writing this register may cause SiS5591/5592 to issue initialization command to SDRAM directly.

BIT	ACCESS	DESCRIPTION
7	R/W	**Precharge Command** Write 1 to this bit causes SiS5591/5592 to issue precharge command to SDRAM. This bit is automatically cleared after the precharge command completed.
6	R/W	**Mode Register Set Command** Write 1 to this bit causes SiS5591/5592 to issue mode setting command to SDRAM. This bit is automatically cleared after the command completed.
5	R/W	**SDRAM Refresh Command** Write 1 to this bit causes SiS5591/5592 to issue refresh command to SDRAM. This bit is automatically cleared after the command completed.
4	R/W	**SDRAM Initialization Mode Selection** This bit controls whether the command specified in Bits[7:5] of this register should be issued to one row only or to all rows. If the value of this bit is 0, the DRAM Status Register(Register 63h) controls which row the command should be issued to. 0: One Row 1: All Rows
3:0	R/W	**Reserved**

Register 5Dh SDRAM Command

Default Value: 00h

Access: Read/Write

BIT	ACCESS	Description
7	R/W	**SDRAM Fast Read Enable** Fast read is a function that SiS5591/5592 issues a SDRAM read command just when it samples a memory read ADS# from CPU and the SDRAM bunk is active. If it is a page-hit read cycle, SiS5591/5592 can return data 1T earlier than the normal case. If it is a page-miss cycle, SiS5591/5592 will precharge the SDRAM and newly start to read. 0: Disable 1: Enable
6	R/W	**Reserved**
5	R/W	**SDRAM Back-to-Back Read Timing** 0: 5-1-1-1-2-1-1-1 1: 5-1-1-1-1-1-1-1 Only for Non-cache systems, and Fast Read enabled (Register 5Dh [7]=1), and NA# 1T ahead BRDY# enabled (Register 50h[4]=1)
4	R/W	**SDRAM Write Retire Rate** 0: X-2-2-2 1: X-1-1-1
3	R/W	**CAS# Latency** 0: 2T 1: 3T

2	R/W	**Read Command Timing Control when Read Cycle Follows after Write Cycle** 0: Zero wait state 1: One wait state
1	R/W	**CS# Assertion Timing when Refresh Cycles** 0: Long pulse 1: 1T Pulse(Recommended)
0	R/W	**Reserved**

Register 5Eh SDRAM Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**SRAS#/SCAS#/RAMW# Timing** This bit controls when to assert and dessert SRAS#, SCAS# and RAMW#. When the bit is set to 1, these control signals are directly generated from internal combinational circuit. When the value of this bit is 0, these control signals passes through flip-flops first before driving to DRAM banks. It is recommended to set this bit to 1 to improve the setup time for these signals. 0: Slow 1: Fast(Recommended)
6	R/W	**SDRAM Optimal RAS Precharge Time Control** When the value of this bit is 1, SiS5591/5592 checks whether the consecutive cycles toward SDRAM are destining to the same row or not to optimize the RAS precharge time. If the cycles are destining to the same row, the minimum SRAS# precharge time for SDRAM must be met before issuing a row active command. However, if they are destining to the different row, the RAS precharge time is met automatically. So, row active command can be issued immediately. When this function is disabled, SiS5591/5592 does not use the information about the destinations of consecutive cycles to optimize RAS precharge time. There is no timing difference RAS regardless whether the cycles are destining to same or different row. 0: Disable 1: Enable
5	R/W	**Precharge Command Timing Control** 0: One wait state (Recommended) 1: Zero wait state
4:0	R/W	**Reserved**

Register 5Fh SDRAM Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

7:4	R/W	**DQM Timing Control** This field controls the timing of DQM. When the value of this field is 0000, DQM is driven by a flip-flop output signal. Otherwise, it is a combinational output. Various delay options are provided to ensure that DQM can meet SDRAM setup time and hold time specification when DQM is driven by combinational output. **Bits Description** — **Bits Description** 0000 : Flip-Flop output — 1000 : Delay 9ns 0001 : Delay 2ns — 1001 : Delay 10ns 0010 : Delay 3ns — 1010 : Delay 11ns 0011 : Delay 4ns — 1011 : Delay 12ns 0100 : Delay 5ns — 1100 : Delay 13ns 0101 : Delay 6ns — 1101 : Delay 14ns 0110 : Delay 7ns — 1110 : Delay 1ns 0111 : Delay 8ns — 1111 : No Delay
3:0	R/W	**CS# Timing Control** This field controls the timing of CS#. When the value of this field is 0000, CS# is driven by a flip-flop output signal. Otherwise, it is a combinational output. Various delay options are provided to ensure that CS# can meet SDRAM setup time and hold time specification when CS# is driven by combinational output. 0000 : Flip-Flop output — 1000 : Delay 9ns 0001 : Delay 2ns — 1001 : Delay 10ns 0010 : Delay 3ns — 1010 : Delay 11ns 0011 : Delay 4ns — 1011 : Delay 12ns 0100 : Delay 5ns — 1100 : Delay 13ns 0101 : Delay 6ns — 1101 : Delay 14ns 0110 : Delay 7ns — 1110 : Delay 1ns 0111 : Delay 8ns — 1111 : No Delay

Register 60/61/62h DRAM Type Registers of Bank 0/1/2

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**DRAM Mode Selection** **Bit [7:6]** — **DRAM Mode** 00 — FPM DRAM 01 — EDO DRAM 10 — Reserved 11 — SDRAM
5	R/W	**Double/Single Sided DRAM** 0: Single Sided 1: Double Sided
4	R/W	**Reserved**

3:0	R/W	**DRAM Type Selection** **For EDO/FPM DRAM**

Bit [3:0]		DRAM Type	
0000	256K	Symmetric	9x9
0001	1M	Symmetric	10x10
0010	4M	Symmetric	11x11
0011	16M	Symmetric	12x12
0100	1M	Asymmetric	12x8
0101	2M	Asymmetric	12x9
0110	4M	Asymmetric	12x10
0111	8M	Asymmetric	12x11
1000	512K	Asymmetric	10x9
1001	1M	Asymmetric	11x9
1010	2M	Asymmetric	11x10
Others	Reserved		

For SDRAM

Bit [3:0]		DRAM Type
0000	1M	12x8 (2-bank)
0001	4M	14x8 (2-bank)
0010	4M	14x8 (4-bank)
0011	Reserved	
0100	2M	12x9 (2-bank)
0101	8M	14x9 (2-bank)
0110	8M	14x9 (4-bank)
0111	Reserved	
1000	4M	12x10 (2-bank)
1001	16M	14x10 (2-bank)
1010	16M	14x10 (4-bank)
1011	Reserved	
1100	2M	13x8 (4-bank)
Others	Reserved	

Register 63h DRAM Status Register

Default Value: FFh

Access: Read/Write

This register is used to specify which DRAM banks are plugged with DRAM.

BIT	ACCESS	DESCRIPTION
7:3	R/W	**Reserved**
2	R/W	**DRAM Status for Bank2** 0: Absent 1: Installed (default)
1	R/W	**DRAM Status for Bank1** 0: Absent 1: Installed (default)

0	R/W	**DRAM Status for Bank0** 0: Absent 1: Installed (default)

Register 64h DRAM Signals Driving Current Control

Default Value: 00h

Access: Read/Write

This 8-bit register controls the buffer strengths of DRAM related signals.

BIT	ACCESS	DESCRIPTION
7	R/W	**RAS[5:0]# Current Rating** 0: 4mA 1: 8mA
6	R/W	**CAS[7:0]# Current Rating** 0: 12mA 1: 16mA
5	R/W	**MA[13:2] Current Rating** 0: 6mA 1: 16mA
4	R/W	**MA[1:0]A Current Rating** 0: 6mA 1: 16mA
3	R/W	**Selection of MA[1:0]B Current Rating** 0: 6mA 1: 16mA
2	R/W	**RAMWA# Current Rating** 0: 12mA 1: 16mA
1	R/W	**RAMWB# Current Rating** 0: 12mA 1: 16mA
0	R/W	**SRAS#/SCAS# Current Rating** 0: 12mA 1: 16mA

Register 65h PCI/A.G.P. Signals Driving Current Control

Default Value: 00h

Access: Read/Write

This 8-bit register controls the buffer strengths of the signals located on A.G.P. or PCI bus.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**Reserved**

3:2	R/W	**A.G.P. Current Rating** This field specifies the buffer strength of all signals on the A.G.P. **Bit[3:2]** **Buffer Strength** 00 3mA 01 2mA 10 2mA 11 4mA
1	R/W	**AD[31:0] Current Rating** This bit controls the buffer strength of AD[31:0] on PCI bus. 0: 4mA 1: 8mA
0	R/W	**PCI Control Signal Current Rating** This bit specifies the current rating of FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, C/BE[3:0]# and PGNT[3:0]#. 0: 4mA 1: 8mA

8.1.2 Legacy PMU Control Register

Register 68h SMRAM Access Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**SMRAM Area Re-mapping Control** This field controls how the address on the host bus is mapped to the system memory address when the SMRAM access control bit is enabled or CPU is in the system management mode. **Bits[7:6]** **Host Address** **System Memory Address** 00 E0000h~E7FFFh E0000h~E7FFFh 01 E0000h~E7FFFh A0000h~A7FFFh 10 E0000h~E7FFFh B0000h~B7FFFh 11 A0000h~AFFFFh A0000h~AFFFFh
5	R/W	**Reserved**
4	R/W	**SMRAM Access Control** When the bit is enabled, SMRAM area can be used even when SMIACT# is not asserted. If the bit is disabled, SMRAM area can only be accessed during the SMI handler. 0: Disable 1: Enable
3:0	R/W	**Reserved**

Register 69h System Event Monitor Control for Power Management

Default Value: 00h

Access: Read/Write

This register controls what kinds of events on A.G.P. bus should be reported to the SiS5595 through the pin

BM_REQ# for power management matter.

BIT	ACCESS	DESCRIPTION
7	R/W	**Monitoring A.G.P. I/O Access** When this bit is enabled, any I/O access from CPU to A.G.P. will be reported to the SiS 5595 via BM_REQ# if the address of the cycle is within the range of base address register. 0: Disable 1: Enable
6	R/W	**Monitoring A.G.P. Non-prefetchable Memory Access** When this bit is enabled, any memory access from CPU to A.G.P. non-prefetchable memory area will be reported to SiS 5595 via BM_REQ#. 0: Disable 1: Enable
5	R/W	**Monitoring A.G.P. Prefetchable Memory Access** When this bit is enabled, any memory access from CPU to A.G.P. prefetchable memory area will be reported to the south bridge via BM_REQ#. 0: Disable 1: Enable
4	R/W	**Monitoring VGA Compatible I/O Access toward A.G.P.** When this bit is enabled, any VGA compatible I/O access (3B0h ~ 3BBh, 3C0 ~ 3DFh) toward A.G.P. will be reported to the south bridge via BM_REQ#. 0: Disable 1: Enable
3	R/W	**Monitoring VGA Compatible Memory Access toward A.G.P.** When this bit is enabled, any VGA compatible memory access (A0000h ~ BFFFFh) toward A.G.P. will be reported to the south bridge via BM_REQ#. 0: Disable 1: Enable
2	R/W	**Monitoring A.G.P. Bus Master Activity** When this bit is enabled, any A.G.P. bus master activity will be reported to the south bridge via BM_REQ#. 0: Disable 1: Enable
1	R/W	**Reserved**
0	R/W	**Pin Definition Select for PGNT4# / BM_REQ#** PGNT4# and BM_REQ# which is used for reporting A.G.P. activity to the south bridge share exactly the same pin on SiS5591/5592. If this bit is set to 1, the pin is used as PGNT4#. If this is set to 0, the pin is used as BM_REQ#. 0: PGNT4# 1: BM_REQ#

Register 6Ah~6Bh ACPI I/O Space Base Address Register

Default Value: 00000000h

Access: Read/Write

The register specifies the ACPI I/O space base address, and SiS5591/5592 may monitor ACPI I/O accesses if the validity bit of this register is set to 1.

BIT	ACCESS	DESCRIPTION

15:5	R/W	**A[15:5] for ACPI I/O Space Base Address** This register provides A[15:5] for the start address of the ACPI I/O space.
4:1	R/W	**Reserved**
0	R/W	**Validity** If this bit is set to 1, the base address contained in Bit[15:5] is valid. Otherwise the base address defined in Bit[15:5] is ignored. 0: Invalid 1: Valid

Register 6Ch DRAM Self-Refresh Control for Power Management

Default Value: 00h

Access: Read/Write

This register controls in what degree that SiS5591/5592 support ACPI function and also controls the behavior of CKE.

BIT	ACCESS	DESCRIPTION
7	R/W	**ACPI S3 State Support** 0: Disable 1: Enable
6	R/W	**ACPI S2 State Support** 0: Disable 1: Enable
5	R/W	**CKE Output Enable Control** When this bit is enabled, SiS5591/5592 drives CKE. When this bit is disable, SiS5591/5592 floats its CKE output. 0: Disable 1: Enable
4	R/W	**CKE Selection** When the value of this bit is 1, SiS5591/5592 always drives CKE to low provided CKE Output Enable Control bit is enabled. When the value of this bit is 0, SiS5591/5592 drives CKE to low only when it entered self-refresh mode (S2 or S3 state and stop grant cycle issued). 0: Normal Mode 1: Force Low

3:0	R/W	**CKE Timing Control** This field controls the timing of CKE. When the value of this field is 0000, CKE is driven by a flip-flop output signal. Otherwise, it is a combinational output. Various delay options are provided to ensure that CKE can meet SDRAM setup time and hold time specification when CKE is driven by combinational output. **Bits Description** — **Bits Description** 0000 : Flip-Flop delay — 1000 : Delay 9ns 0001 : Delay 2ns — 1001 : Delay 10ns 0010 : Delay 3ns — 1010 : Delay 11ns 0011 : Delay 4ns — 1011 : Delay 12ns 0100 : Delay 5ns — 1100 : Delay 13ns 0101 : Delay 6ns — 1101 : Delay 14ns 0110 : Delay 7ns — 1110 : Delay 1ns 0111 : Delay 8ns — 1111 : No Delay

8.1.3 Shadow Ram & Non/Cacheable Area Control Register

Register 70h to register 76h define the attribute of the Shadow RAM from 640 KByte to 1 MByte. All of the registers 70h to 75h are defined as below, and each register defines the corresponding memory segment's attribute which are listed in the following table.

REGISTER	DEFINED RANGE	REGISTER	DEFINED RANGE
Register 70h bits 7:5	0C0000h-0C3FFFh	Register 73h bits 7:5	0D8000h-0DBFFFh
Register 70h bits 3:1	0C4000h-0C7FFFh	Register 73h bits 3:1	0DC000h-0DFFFFh
Register 71h bits 7:5	0C8000h-0CBFFFh	Register 74h bits 7:5	0E0000h-0E3FFFh
Register 71h bits 3:1	0CC000h-0CFFFFh	Register 74h bits 3:1	0E4000h-0E7FFFh
Register 72h bits 7:5	0D0000h-0D3FFFh	Register 75h bits 7:5	0E8000h-0EBFFFh
Register 72h bits 3:1	0D4000h-0D7FFFh	Register 75h bits 3:1	0EC000h-0EFFFFh

Register 70/ 71/ 72/ 73/ 74/ 75h Shadow RAM Registers

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Read enable**
6	R/W	**L1/L2 cacheable**
5	R/W	**Write enable**
4	R/W	**Reserved**
3	R/W	**Read enable**
2	R/W	**L1/L2 cacheable**
1	R/W	**Write enable**
0	R/W	**Reserved**

Register 76h Attribute of Shadow RAM for BIOS Area

Default Value: 00h

Access: Read/Write

The 8-bit register controls the access of shadow RAM on BIOS area (F0000h~FFFFFh). When a bit is enabled,

the type of the access defined by the bit is allowed.

BIT	ACCESS	DESCRIPTION
7	R/W	**Read Control** When this bit is enabled, any read access for BIOS shadow RAM area is forwarded to system memory. 0: Disable 1: Enable
6	R/W	**Cacheable Control** This bit controls the cacheability for BIOS shadow RAM area 0: Disable 1: Enable
5	R/W	**Write Control** When this bit is enabled, any write access for BIOS shadow RAM area is forwarded to system memory. 0: Disable 1: Enable
4	R/W	**Reserved**
3	R/W	**Shadow RAM enable for PCI access** When this bit is enabled, accesses from PCI masters toward shadow RAM area is allowed. 0: Disable 1: Enable
2:0	R/W	**Reserved**

Register 77h Characteristics of Non-cacheable Area

Default Value: 00h

Access: Read/Write

This register controls the characteristics of the non-cacheable areas defined in Register78h and Register 7Ah.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**Reserved**
3	R/W	**Location of Non-cacheable Area I** This bit specifies whether the non-cacheable area I is located on system memory or PCI bus. 0: System Memory 1: PCI Bus.
2	R/W	**Non-cacheable Area I Enable Control** This bit controls whether the address and size specified on Register 78h are valid or not. When the bit is enable, the range defined by Register 78h is non-cacheable. 0: Disable 1: Enable
1	R/W	**Location of Non-cacheable Area II** This bit specifies whether the non-cacheable area II is located on system memory or PCI bus. 0: System Memory 1: PCI Bus.

0	R/W	**Non-cacheable Area II Enable Control** This bit controls whether the address and size specified on Register 7Ah are valid or not. When the bit is enable, the range defined by Register 7Ah is non-cacheable. 0: Disable 1: Enable

Register 78h~79h Allocation of Non-Cacheable Area I

Default Value: 0000h

Access: Read/Write

This register defines the size and the base address of the first non-cacheable area.

BIT	ACCESS	DESCRIPTION
15:13	R/W	**Size of Non-cacheable Area I** **Bits[15:13]** **Size** 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of Non-cacheable Area I** This field specifies A[28:16] for the base address of the non-cacheable area I. The upper 3 bits of the base address are always regarded as zeros.

Register 7Ah~7Bh Allocation of Non-cacheable Area II

Default Value: 0000h

Access: Read/Write

This register defines the size and the base address of the second non-cacheable area.

BIT	ACCESS	DESCRIPTION
15:13	R/W	**Size of Non-cacheable Area II** **Bits [15:13]** **Size** 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of Non-cacheable Area II** This field specifies A[28:16] for the base address of the non-cacheable area II. The upper 3 bits of the base address are always regarded as zeros.

8.1.4 Target Bridge to DRAM Control Register

Register 80h Target Bridge to DRAM Characteristics

Default Value: 00h

Access: Read/Write

The 8-bit register controls the characteristics of PCI-to-DRAM bridge. Every bit of this register applies both to 33Mhz PCI bus and A.G.P.

BIT	ACCESS	DESCRIPTION
7:5	R/W	**Address Boundary Alignment for PCI Bursting** This field controls the alignment of address boundaries. For SiS5591/5592, a master-generated PCI burst cycle can never across any address boundary defined by this field. If a cycle is trying to across an address boundary for a memory burst transaction, SiS5591/5592 will terminate this transaction with disconnect immediately. **Bits[7:5]** — **Boundary Alignment** 000 — 256 Bytes 001 — 512 Bytes 010 — 1 KBytes 011 — 2 KBytes 100 — 4 KBytes Others — reserved
4	R/W	**DRAM Leadoff Time Control** This bit controls the leadoff time of the DRAM operations that are resulted from PCI master initiated cycles. 0: faster (default) 1: slower
3	R/W	**Synchronous DRAM Burst Read Control** This bit controls whether or not SiS5591/5592 generates burst read command to SDRAM for a PCI master generated burst read transaction on PCI bus. 0: Disable (default) 1: Enable
2	R/W	**Snooping Write-Back Cycle Byte Merge Control** This bit controls the speed of the merging process described below. It may results a CPU write-back cycle when SiS5591/5592 snoops L1 cache for a PCI transaction. SiS5591/5592 always tries to merge the data from the write back cycle and the data from the PCI transaction before it takes the write operation toward DRAM. 0: faster (default) 1: slower
1	R/W	**Page Table Cache Decoding Timing** This bit controls the decoding time of page table cache hit for a PCI transaction toward graphic window region. 0: 1 CPU clock 1: 2 CPU clock
0	R/W	**Graphic Window Region Snooping Control** This bit controls whether or not SiS5591/5592 generates snooping process to CPU for a PCI transaction which is toward graphic window region. 0: Snoop 1: No Snoop

8.1.5 PCI33 Bridge and PCI Arbiter Control Register

Register 81h PCI33 Target Bridge Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for 33MHz PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**Advanced Snoop Control for Write cycle** This bit controls whether or not the PCI33 target bridge does advanced snoop for write cycles. 0: Disable 1: Enable
6	R/W	**Advanced Snoop Control for Read Cycle** This bit controls whether or not the PCI33 target bridge does advanced snoop for read cycles. 0: Disable 1: Enable
5	R/W	**Synchronous Mode** This bit can only be set for the system that CPU clock leads 33Mhz PCI clock within 2ns to 6ns and the frequency of PCI clock is half of the one of CPU clock.. The synchronous mode can avoid the penalty caused by synchronization matters. 0: Disable 1: Enable
4:0	R/W	**Reserved**

Register 82h PCI33 Target Bridge Bus Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for 33Mhz PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**PCI Peer Concurrency** When this bit is enabled, CPU to L2/DRAM accesses are allowed to perform concurrently with PCI-to-PCI accesses. 0: Disable 1: Enable
6	R/W	**Prefetch Buffer Control** When this bit is set to 1, SiS5591/5592 asserts its first TRDY# for a transaction after it prefetched 1quadword of data from system memory. Otherwise, SiS5591/5592 asserts its first TRDY# after 2 quadwords are prefetched. 0: Assert TRDY# after prefetching 2 Qws 1: Assert TRDY# after prefetching 1 Qws

5	R/W	**Memory Write and Invalidate Control** When this bit is enable, SiS5591/5592 skips the snooping process to optimize the PCI memory write and invalidate command for PCI masters. When this bit is disable, SiS5591/5592 treats memory write and invalidate command as the same as memory write command. This bit can only be set if the cache line size defined by master devices is the multiple of 8 double words. 0: Disable 1: Enable
4	R/W	**Memory Read Command Prefetch Control** This bit controls whether or not SiS5591/5592 prefetch data for memory read command. Please note that Memory Read Multiple and Memory Read Line commands always do prefetch. The semantic of this bit is different to others. The value of 0 means enable for this bit. 0: Enable 1: Disable
3:2	R/W	**Initial Latency Control** This field controls the target initial latency of the PCI33 target bridge. If SiS5591/5592 is unable to assert TRDY# for a transaction within the target initial latency defined by this field, SiS5591/5592 asserts STOP# to retry this cycle. 01: Disable 01: 16 PCI Clocks 11: 24 PCI Clocks 11: 32 PCI Clocks
1	R/W	**Subsequent Latency Control** When this bit is enabled, SiS5591/5592 terminates a transaction with STOP# if it fails to assert TRDY# for the subsequent block within 8 clocks. 0: Disable 1: Enable
0	R/W	**Address Decoding Time Extension Control** This bit controls the decoding time for SiS5591/5592 to guarantee that a PCI transaction is destining to system memory. When this bit is set to 1, it takes one extra CPU clock for the decoding process to complete. It is recommended to disable this function to optimize PCI performance unless there is any master device violates the maximum AD valid delay time(11ns)

Register 83h CPU to PCI33 Characteristics

Default Value: 00h

Access: Read/Write

This register controls miscellaneous functions supported by the CPU-to-PCI33 bridge of SiS5591/5592. The setting of this register may affect PCI performance in various degree

BIT	ACCESS	DESCRIPTION
7:5	R/W	**Reserved**

5	R/W	**Non-Post Write Cycle Retry Behavior Control** When this bit is set to 1, retry from any kind of CPU to PCI write cycles does not back off CPU. Instead, SiS5591/5592 tries to issue the retried cycle again and again until it completes successfully on PCI bus. When this bit is set to 0, retry from any non-post CPU to PCI write cycle results in CPU back off. 0: Back off CPU 1: Continuous Retry
4	R/W	**Fast Back-to-Back to Same Agent Control.** This bit controls whether consecutive post-write cycles toward the same agent should use fast back-to-back timing or not. When this bit is enabled, SiS5591/5592 uses fast back-to-back timing for IDE consecutive data port write cycles and consecutive CPU to 33 MHz PCI frame buffer memory write cycles. The base address and the size of the frame buffer area are defined by Register 88h and Register 8Ah. Register 88h and Register 8Ah must be initialized before this control bit is enabled. 0: Disable 1: Enable
3	R/W	**Post Write Rate Control** This bit controls the amount of time from the assertion of ADS# to the assertion of BRDY# for CPU-to-PCI33 post write cycle under the best case. 0: 4 CPU clocks 1: 3 CPU clocks
2	R/W	**IDE Data Port Post Write Control** When this bit is enable, any I/O write cycle with address 170h or 1F0h is posted. 0: Disable 1: Enable
1	R/W	**Memory Burst Control** This bit controls whether or not the host bridge generates memory burst cycles. 0: Disable 1: Enable
0	R/W	**Memory Post Write Control** When this bit is enable, all CPU to PCI memory write cycles are posted. 0: Disable 1: Enable

Register 84h PCI33 Grant Timer

Default Value: FFFFh

Access: Read/Write

The timer is used to prevent PCI masters from seizing the PCI bus too long. When the timer expired, PCI arbiter forces the master that is currently occupying PCI bus to relinquish PCI bus by removing its grant.

BIT	ACCESS	DESCRIPTION
15:0	R/W	**PCI33 Grant Timer** The setting of this register should consider the overall system configuration and the value of MLT(Register 1Dh). For a system that has many PCI master devices, the value should be higher. For a system with fewer master devices, the value should be smaller. Typical value of this timer is 60h if MLT is set to 20h. Unit: PCI clock

Register 86h CPU Idle Timer for PCI

Default Value: FFh

Access: Read/Write

The timer is used to prevent CPU from idling too long while outstanding PCI requests cannot be served.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**CPU Idle Timer** Recommended value for this timer is 03h. Unit: PCI clock

Register 87h CPU to PCI33 Characteristics and Arbitration Option

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**CPU to PCI33 Bridge Synchronous Mode** This bit can only be set for the system that CPU clock leads 33Mhz PCI clock within 2ns to 6ns and the frequency of PCI clock is equal to half of the frequency of CPU clock. The synchronous mode can avoid the penalty caused by synchronization matters. 0: Disable 1: Enable
6	R/W	**CPU Involved Arbitration on PCI** PGT(Register 84h), CIT(Register 86h) and MLT(Register 0Dh) can only take effect when this bit is enable. When this bit is enable, SiS5591/5592 does not block CPU from operation longer than the period defined by PGT to serve PCI masters, and minimum access time for CPU is guaranteed by MLT. 0: Disable 1: Enable
5	R/W	**Minimum Latency from ADS# to FRAME#** This bit is effective only under synchronous mode. When this bit is enabled, SiS5591/5592 tries to minimize the delay from ADS# to FRAME# for non-post cycle. This function can save about 1 CPU clock for each non-post cycle in average. 0: Disable 1: Enable
4	R/W	**PCI Grant Timer Testing Mode** For internal usage only, please program this bit with 0. 0: Disable 1: Enable
3	R/W	**64-bit Access Retry Behavior Control** When the value of this bit is 0 and the second half non-post PCI cycle(or the second data phase) of a 64-bit access is retried by a PCI target, SiS5591/5592 tries to issue the second half cycle again and again until it completes successfully on PCI bus. When this bit is set to 1, retry for any non-post cycle issued by the host bridge results in the assertion of BACKOFF#. It is recommended to set this bit to 0. 0: Continue Retry 1: Back-Off CPU

2	R/W	**Lock Control** When this bit is enabled, a 64-bit memory read cycle from CPU toward 33Mhz PCI bus is converted into locked PCI memory read cycles. 0: Disable 1: Enable
1:0	R/W	**Reserved**

Register 88h Base Address of Frame Buffer Area

Default Value: 0000h

Access: Read/Write

This register defines the base address of the frame buffer area which is used for generating fast back-to-back cycles.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Frame Buffer Base Address** Bits[15:4] corresponding to A[31:20] of the base address. The frame buffer base address must be 1MByte aligned.
3:0	R/W	**Reserved**

Register 8Ah Size of Frame Buffer Area

Default Value: 0000h

Access: Read/Write

This register defines the size of the frame buffer area which is used for generating fast back-to-back cycles.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Size of the frame buffer area** **Bits[15:4]** **Size** 000000000000b 4GB 100000000000b 2GB 110000000000b 1GB 111000000000b 512MB 111100000000b 256MB 111110000000b 128MB 111111000000b 64MB 111111100000b 32MB 111111110000b 16MB 111111111000b 8MB 111111111100b 4MB 111111111110b 2MB 111111111111b 1MB
3:0	R/W	**Reserved**

8.1.6 CPU/PCI/A.G.P. Clocks DLL/CLL Control Register

Register 8Ch DLL Control

Default Value: 00h

Access: Read/Write

DLL is used to minimize the skew between internal and external clocks. This register controls the time period that DLL circuit locks the reference clock again. This register applies only to CPU clock and PCI clock.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**DLL Lock Period** This field controls the period that DLL adjusts the internal clock to the reference clock source. **Bit[7:6]** — **Period** 00 — 4T 01 — 8T 10 — 16T 11 — 32T T is the reference clock source for DLL.
5:0	R/W	**Reserved**

Register 8Dh PLL Control Register

Default Value: 00h

Access: Read/Write

PLL is used to minimize the skew between internal A.G.P. clock and external A.G.P. clock. It also adjusts the phase relationship between internal 133Mhz clock and A.G.P. clock.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**PLL Control** Only for internal usage, please do not program these bits.
3	R/W	**Reserved**
2:0	R/W	**Internal 133MHz clock delay** **Bits[2:0]** — **Delay** 000 — 0.0ns 001 — 0.5ns 010 — 1.0ns 011 — 1.5ns 100 — 2.0ns 101 — 2.5ns 110 — 3.0ns 111 — 3.5ns

8.1.7 A.G.P GART and Page Table Cache Control Register

Register 90h GART Base Address for 1-level Re-mapping

Default Value: 00000000h

Access: Read/Write

This register specifies the starting address of the 1-level Graphics Address Re-mapping Table. The Re-mapping table is resided in system memory and it translates graphic address into the system memory address.

BIT	ACCESS	DESCRIPTION

31:12	R/W	**A[31:12] for GART Base Address** This register provides the starting address of the 1-level Graphics Address Re-mapping Table which is always located in system memory. Please note that although there is no register that directly specifies the size of GART, the size of GART can still be known via graphic window size(Bits[6:4] of Register 94h) (Please note that the address provided via GART Base is 4KB aligned)
11:0	R/W	**Reserved**

Register 94h Graphic Window Control

Default Value: 00h

Access: Read/Write

This register specified the size of the graphic window and indicates that whether the Graphic Window Base Address Register and 1-level Re-mapping GART Base Address Register contain valid information or not.

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6:4	R/W	**Graphic Window Size** This field defines the size of the graphic window. The accessibility of GWBA register (Register 10h) is also controlled by this field. **Bits[6:4]** **Size** 000 4MByte 001 8MByte 010 16MByte 011 32MByte 100 64MByte 101 128MByte 110 256MByte 111 Reserved
3:2	R/W	**Reserved**
1	R/W	**Graphic Window Base Address Validity** The value of "1" for this bit indicates that the Graphic Window Base Address specified in GWBA Register(Register 10h) is valid. Otherwise, the address specified in GWBA Register is invalid. 0: Invalid 1: Valid
0	R/W	**1-level Re-mapping GART Base Address Validity** The value of "1" for this bit indicates that the 1-level Re-mapping GART Base Address specified in Register 90h is valid. Otherwise, the address specified in Register 90h is invalid. 0: Invalid 1: Valid

Register 97h Page Table Cache Control

Default Value: 00h

Access: Read/Write

Page Table Cache is used to speedup the address translation process from graphic address to system memory address. It stores recently used GART entries in the core logic to prevent traffics toward system memory during address translation process. This register controls the characteristic of the page table cache and the address

translation mechanism.

BIT	ACCESS	DESCRIPTION
7:3	R/W	**Reserved**
2	R/W	**Page Table Cache Invalidation Control** This bit controls in what mean that SiS5591/5592 avoids to use stalled page table cache. When the value of this bit is 0, SiS5591/5592 automatically detects write accesses toward all GART entries and it invalidates the entire page table cache immediately once it observed such an event. When the value of this bit is 1, aids from software must be provided to prevent SiS5591/5592 from using stalled page table cache entries. Mini-port driver must write Page Table Cache Invalidation Control Register(Register 98h) when new re-mapping information is updated to GART. 0: Detect writing GART entry 1: Write Configuration Register 98h
1	R/W	**Re-mapping Table Level Selection** This control bit specifies whether 1 or 2 level re-mapping mechanism is being used on the system. 0: 1-level Re-mapping 1: 2-level Re-mapping
0	R/W	**Page Table Cache Enable** When this bit is enabled, page table cache will be used for accelerating the address translation process. When this bit is disable, no GART entries are cached into the page table cache and any address translation is done after getting the GART entry by a memory read. 0: Disable 1: Enable

Register 98h Page Table Cache Invalidation Control

Default Value: 00000000h

Access: Read/Write

This register controls the invalidation of page table cache. The invalidation process can apply to only one entry or to the whole page table cache.

BIT	ACCESS	DESCRIPTION
31:12	R/W	**Graphic Window Memory Address** Bits[31:12] define A[31:12] of a specific page of 4K A.G.P. graphic window memory address. There is a certain GART entry to handle address translation of this specific 4K page.. If the GART entry is resided in the page table cache and the invalidation of the GART entry is controlled by bit0 of this register.
11:2	R/W	**Reserved**
1	R/W	**Invalidate All** Invalidate all page table cache entries when write 1 to this bit. This bit is cleared after the invalidation process completed.
0	R/W	**Invalidate Entry** Invalidate the corresponding page table cache entry specified in Bits[31:12] when write 1 to it. This bit is cleared after the invalidation process completed.

Register 9Ch DIR Base Address for 2-level Remapping

Default Value: 00000000h

Access: Read/Write

This register defines the starting address of the GART directory. When 2-level re-mapping mechanism is chosen for address translation, the re-mapping information is distributed into two levels. The first level GART directory determines which 4K GART table should be used for translation, and the second level GART contains the starting address of each 4K page.

GART directory always resides inside SiS5591/5592 and system software should allocate 128 bytes of memory space for it.

BIT	ACCESS	DESCRIPTION
31:7	R/W	**DIR Base Address** Bits[31:7] defines A[31:7] of the memory mapped base address for DIR Registers.
6:0	R/W	**Reserved**

8.1.8 Flush L2 Control Register

Register A0h L2 Flushing Control

Default Value: 00000000h

Access: Read/Write

This register controls the L2 flushing operation. The flush operation can apply to only one 4Kbyte page or to the entire L2 cache.

BIT	ACCESS	DESCRIPTION
31:12	R/W	**Page Address** Bits[31:12] define A[31:12] of the base address of the specific page to be flushed.
11:2	R/W	**Reserved**
1	R/W	**Flush All** Flush the entire L2 cache when writing 1 to it. This bit is cleared when the flushing operation completed.
0	R/W	**Flush Page** Flush only the cache lines that reside in the page defined by Bits[31:12] when writing 1 to it. This bit is cleared when the flushing operation completed.

Register A4h L2 Flushing Function & DRAM Bandwidth Sharing Control

Default Value: 00h

Access: Read/Write

This register specifies various L2 flushing characteristics and also contains the enable bit for DRAM bandwidth sharing function.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Reserved**

5	R/W	**DRAM Bus Bandwidth Allocation Timers Enable** DRAM bus bandwidth allocation timers include CAPT(Register A6h), P33APT(Register A8h), P66APT(Register AAh). These timers are meaningful to DRAM arbiter only when this control bit is enabled. When the bit is disabled, DRAM bus is always allocated according to the following priority: CPU > A.G.P. > PCI. 0:Disable 1:Enable
4	R/W	**Test Bit of L2 Flushing address counter** For IC tester only, please program this bit with 0. 0: Normal State 1: Test State
3	R/W	**Flush L2 with Invalidation** When this bit is enabled, the L2 flushing operation not only flushes L2 but also invalidates the cache line that it flushes. 0: Disable 1: Enable
2	R/W	**L2 Flushing Priority Timer Enable** If this bit is enable, the priority timer starts to decrease when the L2 flushing operation begins. L2 flushing operation has higher priority over PCI Master before the timer is expired. If this bit is disabled, L2 flushing always has higher priority than PCI Master. 0: Disable 1: Enable
1	R/W	**L2 Flushing Mechanism Control** When the value of this bit is 0, L2 flushing operation is triggered by write back special cycle from CPU. When the value of this bit is 1, L2 flushing operation is triggered by a write to L2 flushing control register(Register A0h). 0: Triggered by Write Back Special Cycle 1: Triggered by Register A0h Configuration Write
0	R/W	**L2 Flushing Function Control** When this control bit is disabled, SiS5591/5592 never generates L2 flushing operation. When this bit is enabled, SiS5591/5592 generates L2 flushing operation in response to write back special cycle or L2 flushing control register write according to the setting of bit 1 of this register. 0: Disable 1: Enable

Register A5h L2 Flushing Priority Timer(FL2PT)

Default Value: 00h

Access: Read/Write

The flush L2 priority timer is used to prevent from blocking the operation of PCI master for a long time. The larger the initial value for the priority timer, the higher bandwidth for L2 flushing operation is allocated.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Flush L2 Priority Timer** When L2 Flushing Priority Timer is enabled, this register provides the initial value of the register. Unit: CPU clock * 4

8.1.9 DRAM Priority Timer Control Register

Register A6h CPU-A.G.P. Privilege Timer (CAPT)

Default Value: 0000h

Access: Read/Write

SiS5591/5592 maintains the privilege of DRAM usage between CPU and A.G.P. When both CPU and A.G.P. master are craving for the resource of system memory, this set of timers provides the adjustment of DRAM bandwidth between these two agents. The operation of the set of timers is explained below.

If A.G.P. data transfer has higher privilege over CPU, A.G.P. high privilege timer decreases every clock when A.G.P. low priority data access toward system memory is undergoing. If CPU privilege is higher than A.G.P., CPU high privilege timer decreases every clock when CPU accesses system memory. The privilege relationship between A.G.P. and CPU is exchanged after the timer expired. CPU accesses do not affect any one of these two timers if CPU does not have higher privilege than A.G.P. In the same way, A.G.P. low priority accesses do not affect timers if A.G.P. device does not have higher privilege than CPU.

BIT	ACCESS	DESCRIPTION
15:8	R/W	**Initial Value for A.G.P. High Privilege Timer** The timer controls how long A.G.P. low priority data transfer has higher privilege over CPU for DRAM accesses. The recommended value for this register is 30h. Unit: CPU clock * 4
7:0	R/W	**Initial Value for CPU High Privilege Timer** The timer controls how long the CPU has higher privilege over A.G.P. low priority data transfer for DRAM accesses. The recommended value for this register is 80h. Unit: CPU clock * 4

Register A8h PCI33-A.G.P. Privilege Timer (P33APT)

Default Value: 0000h

Access: Read/Write

SiS5591/5592 maintains the privilege of DRAM usage between 33Mhz PCI bus and A.G.P. When masters on 33Mhz PCI bus and A.G.P. master are all craving for the resource of system memory, this set of timers provides the adjustment of DRAM bandwidth between them. The operation of the set of timers is explained below.

If A.G.P. data transfer has higher privilege over PCI33, A.G.P. high privilege timer decreases every clock when A.G.P. low priority data access toward system memory is undergoing. If PCI33 privilege is higher than A.G.P., PCI33 high privilege timer decreases every clock when the master on PCI33 bus accesses system memory. The privilege relationship between A.G.P. and PCI33 is exchanged after the timer expired. Accesses from any PCI33 master do not affect any one of these two timers if PCI33 does not have higher privilege than A.G.P. In the same way, A.G.P. low priority accesses do not affect timers if A.G.P. does not have higher privilege than PCI33.

BIT	ACCESS	DESCRIPTION
15:8	R/W	**Initial Value for A.G.P. High Privilege Timer** The timer controls how long A.G.P. low priority data transfer has higher privilege over the agents on 33Mhz PCI bus for DRAM accesses. The recommended value for this register is 30h. Unit: CPU clock * 4

7:0	R/W	**Initial Value for PCI33 High Privilege Timer** The timer controls how long the agents on 33Mhz PCI bus have higher privilege over A.G.P. low priority data transfer for DRAM accesses. The recommended value for this register is 20h. Unit: CPU clock * 4

Register AAh PCI66-A.G.P. Privilege Timer (P33APT)

Default Value: 0000h

Access: Read/Write

SiS5591/5592 maintains the privilege of DRAM usage between two kinds of A.G.P. accesses by PCI protocol and A.G.P. protocol. When both kinds of transactions are craving for the resource of system memory, this set of timers provides the adjustment of DRAM bandwidth between them. The operation of the set of timers is explained below.

If A.G.P. data transfer has higher privilege over PCI66, A.G.P. high privilege timer decreases every clock when A.G.P. low priority data access toward system memory is undergoing. If PCI66 privilege is higher than A.G.P., PCI66 high privilege timer decreases every clock when the master using PCI protocol to access system memory. The privilege relationship between A.G.P. and PCI66 is exchanged after the timer expired. PCI transactions from the master do not affect any one of these two timers if PCI66 does not have higher privilege than A.G.P. In the same way, A.G.P. low priority accesses do not affect timers if A.G.P. does not have higher privilege than PCI66.

BIT	ACCESS	DESCRIPTION
15:8	R/W	**Initial Value for A.G.P. Low Privilege Timer** The timer controls how long A.G.P. low priority data transfer has higher privilege over PCI transactions on A.G.P bus for DRAM accesses. The recommended value for this register is 30h. Unit: CPU clock * 4
7:0	R/W	**Initial Value for PCI66 High Privilege Timer** The timer controls how long the PCI transactions on A.G.P. bus have higher privilege over A.G.P. low priority data transfer for DRAM accesses. The recommended value for this register is 18h. Unit: CPU clock * 4

8.1.10 Error Control & Status Control Register

Register B0h Error Reporting Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**Reserved**
0	R/W	**Parity/ECC Error Reporting Control** When this bit is disabled, SiS5591/5592 neglects all system memory parity errors and 2-bit ECC errors. When this bit is enabled, SiS5591/5592 reports system memory parity errors and 2-bit ECC errors on Error Status Register (Register B2h). If the SERR# enable bit of command register (Register 04h) and this bit are both enabled, SiS5591/5592 also drives SERR# when parity or 2-bit ECC errors is detected on system memory. 0: Disable 1: Enable

Register B2h Error Status

Default Value: 00h

Access: Write Clear, Read Only

BIT	ACCESS	DESCRIPTION
7:1	RO	**Reserved**
0	WC	**Parity/ECC Error** When parity/ECC error reporting control bit of error control register (Register B2h) is enabled, SiS5591/5592 sets this bit to 1 when it detected parity of 2-bit ECC error on system memory. When the error reporting control bit is disabled, SiS5591/5592 would not set this bit under any condition. The bit is cleared by write a 1 to it. 0: No Parity/2-bit ECC Error Detected 1: Parity/2-bit ECC Error Detected

8.1.11 A.G.P. and 66 MHz Host Bridge Control Registers

Register C0h A.G.P. Capability Identify Register(ACAPID)

Default Value: 00100002h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:24	RO	**Reserved**
23:20	RO	**A.G.P revision Major** Default value is 0001b to indicate that SiS5591/5592 conforms to the major revision 1 of A.G.P. interface specification.
19:16	RO	**A.G.P revision Minor** Default value is 0000b to indicate that SiS5591/5592 conforms to the minor revision 0 of A.G.P. interface specification..
15:8	RO	**Next Capability** Default value is 00h to indicate the final item.
7:0	RO	**A.G.P. Capability ID** Default value is 02h to indicate the list item as pertaining to A.G.P. registers.

Register C4h A.G.P. Status Register

Default Value: 1F000203h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:24	RO	**RQ Field** The RQ field contains the maximum number of A.G.P. command requests SiS5591/5592 can manage. Default value is 1Fh to indicate that the maximum number of A.G.P. command requests SiS5591/5592 can manage is 32.
23:10	RO	**Reserved**
9	RO	**SBA** Default value is 1 to indicate that SiS5591/5592 supports side band addressing.
8:2	RO	**Reserved**

1:0	RO	**Data Rate** The RATE field indicates the data transfer rates supported by this devices. Default value is 11b to indicate SiS5591/5592 support both 1X and 2X mode.

Register C8h A.G.P. Command Register

Default Value: 00000000h

Access: Read Write

BIT	ACCESS	DESCRIPTION
31:10	R/W	**Reserved**
9	R/W	**SBA_ENABLE.** When set, the side band address mechanism is enabled.
8	R/W	**A.G.P._ENABLE.** Setting the bit allows the target to accept A.G.P. operations. When cleared, the target ignores incoming A.G.P. operations. Please note that the target must be enabled before the master.
7:2	R/W	**Reserved**
1:0	R/W	**Data Rate** One(and only one) bit in the DATA_RATE field must be set to indicate the desired data transfer rate. <Bit1: 1X, Bit1: 2X>. The same bit must be set on both master and target. The DATA_RATE field applies to AD and SBA buses. **Bits[1:0] — Data Rate** 00 — Reserved 01 — 1X mode 10 — 2X mode 11 — Reserved

Register D4h A.G.P. Priority Rotation Timer (APRT)

Default Value: 00h

Access: Read Write

This timer controls the amount of time that A.G.P. is granted to an master that is using PCI protocol when the master request is continuous asserted. The purpose of AMTT is to allow the master to perform multiple back-to-back transactions on A.G.P. and guarantees fair bandwidth sharing. The timer applies both to the host bridge and the A.G.P. master. When the A.G.P. master or the host bridge is granted to start PCI transactions on A.G.P., the timer loads its initial value from this register and starts to count. Before the expiration of the timer, the agent that own GNT# has the highest priority for subsequent arbitration process. After the timer is expired, the priority of the agent that own GNT# is dropped to the lowest.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for APRT Timer** Recommended value for APRT is 60h. Please note that although the default value of APRT is 0, it is necessary to set this register to a non-zero value before master operation is enabled on A.G.P. Unit: A.G.P. clock

Register D5h Data Priority Timer (DPT)

Default Value: 00h

Access: Read Write

DPT timer controls the minimum amount of time allocated to low priority data transaction. When SiS5591/5592

issues low priority grant(read and write), the timer is loaded with its initial value and starts to count. Before the timer is expired, low priority data transactions have higher precedence for bus usage than PCI transactions.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for DPT Timer** Recommended value for DPT is 60h. Please note that although the default value of DPT is 0, it is necessary to set this register to a non-zero value before A.G.P. is enabled. Unit: A.G.P. clock

Register D6h Write Buffer Flush Counter(WBFC) & Data Transfer Counter (DTC)

Default Value: 00h

Access: Read Write

WBFC counter controls the number of write transactions to be flushed into system memory after write buffer is full. DTC is used to balance read and write data transactions on A.G.P. and is also used to allow back-to-back data transactions.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**WBFC (Write Buffer Flush Counter)** To minimize transaction latency time, a read transaction has higher precedence for system memory usage than a write transaction. However, the privilege of system memory access is changed when the write buffer is full. A write transaction starts to have higher privilege over a read transaction for system memory access when the buffer is full. The privilege for DRAM accesses is changed back either when the number of transactions flushed into main memory equals to WBFC or when all transactions in the write buffer are flushed. The counter applies both to low and high priority transactions. The recommended value for WBFC is Ah. Please note that although the default value of WBFC is 0, it is necessary to set this register to a non-zero value before A.G.P. is enabled.
3:0	R/W	**DTC (Data Transfer Counter)** DTC controls the number of grants allocated for read and write data. SiS5591/5592 maintains the privilege on A.G.P. between write transaction and read transaction. When write transactions have higher privilege, DTC decreases by one every time A.G.P. is granted to a write transaction. When DTC expires, the privilege between read and write is exchanged. It also exhibits the same behavior when read transactions have higher privilege. DTC applies both to low and high priority transaction. The recommended value for DTC is Ah. Please note that although the default value of DTC is 0, it is necessary to set this register to a non-zero value before A.G.P. is enabled.

Register D7h CPU Idle Timer on A.G.P. (CITA)

Default Value: 00h

Access: Read Write

The timer is used to prevent CPU from idling too long while outstanding A.G.P. requests cannot be served.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for CPU Idle Timer on A.G.P.** The recommended value for CITA is 06h. Please note that although the default value of CITA is 0, it is necessary to set this register to a non-zero value before master operation is enabled on A.G.P. Unit: A.G.P. clock

Register D8h A.G.P. Grant Timer (AGT)

Default Value: 0000h

Access: Read Write

The timer is used to prevent the A.G.P. master from holding CPU too long. When the timer expire, SiS5591/5592 forces the master to relinquish A.G.P. by remove its grant for PCI transactions(i.e. GNT# asserted and ST[2:0]=111).

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Initial Value for A.G.P. Grant Timer** The setting of this register should consider the value of CLTA(Register DAh). Typical value of this timer is A0h if CLTA is set to 40h. Please note that although the default value of AGT is 0, it is necessary to set this register to a non-zero value before master operation is enabled on A.G.P. Unit: A.G.P. clock

Register DAh CPU Latency Timer on A.G.P. (CLTA)

Default Value: 00h

Access: Read Write

CLTA used in conjunction with AGT(Register D8h) and CITA(Register D7h) to provide a fair and efficient arbitration mechanism. The value of CLTA guarantees the minimum system bandwidth for CPU when the A.G.P. master continuous issues PCI transactions on A.G.P.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for CPU Latency Timer on A.G.P.** The recommend value for CLTA is 40h. Please note that although the default value of CLTA is 0, it is necessary to set this register to a non-zero value before master operation is enabled on A.G.P. Unit: A.G.P. clock

Register E0h A.G.P. Compliant Target/Arbiter Control Register (ACTACR)

Default Value: 00h

Access: Read/Write

The 8-bit register contains various options for A.G.P. compliant target and arbiter.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Read Buffer Threshold Point for Read GNT.** To prevent from inserting wait states on A.G.P. for read cycles, SiS5591/5592 may not assert low-priority read grant to A.G.P. master immediately after 1 block of the transaction is available in the low-priority read buffer. Instead, SiS5591/5592 does not assert low priority read grant until the read buffer contains more data items than the threshold value set by this field. Please note that this field affects the assertion of low-priority read grant only and has no effect on high-priority read grant. **Bits[7:6] Latency** 11 8 blocks 10 4 blocks 01 2 blocks 00 1 block

5	R/W	**Pipeline option for read grant.** This control bit only affects 1 Qword data transfer in 2X mode. 0: Fast 1: Slow
4	R/W	**A.G.P. Flush Option** 0: Flush only low priority write 1: Flush both high and low priority write
3	R/W	**Asserting GNT# for PIPE# or FRAME# without CPU Hold.** If this bit is disabled, SiS5591/5592 asserts GNT# for A.G.P. master to asserts PIPE# or FRAME# only when CPU is held. If this bit is disabled, SiS5591/5592 may assert GNT# for A.G.P. master to assert PIPE# or FRAME# even when CPU is not held. It is recommended that this bit should be set to 0 when a pure PCI device or an A.G.P. device that uses SBA is plugged on A.G.P. When a A.G.P. device that uses PIPE# to enqueue requests is plugged on the system, it is recommend to set this bit to 1. 0: Disable 1: Enable
2	R/W	**A.G.P. Counter Testing Mode.** For internal test only. Must be programmed with 0. 0: Normal Mode 1: Test Mode
1	R/W	**Synchronous Mode.** This bit can only be enabled when the frequency of A.G.P. clock and frequency of CPU clock are the same and the skew between these two clocks is within 2ns externally. 0: Disable 1: Enable
0	R/W	**TRDY# Delay for Data Transfer.** When the value of this bit is 0, TRDY# is asserted in the fastest timing for read data transfer. When the value of this bit is 1, the assertion of TRDY# for read data transfer is delayed 1 clock. 0: Minimum Delay 1: Maximum Delay

Register E1h PCI66 Target Bridge Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for 66Mhz PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**Advanced Snoop Control for Write cycle** This bit controls whether or not the PCI66 target bridge does advanced snoop for write cycles. 0: Disable 1: Enable

6	R/W	**Advanced Snoop Control for Read Cycle** This bit controls whether or not the PCI66 target bridge does advanced snoop for read cycles. 0: Disable 1: Enable
5	R/W	**Synchronous Mode** This bit can only be enabled when the frequency of A.G.P. clock and the frequency of CPU clock are the same and the skew between these two clocks is within 2ns externally. 0: Disable 1: Enable
4:0	R/W	**Reserved**

Register E2h PCI66 Target Bridge Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for 66Mhz PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6	R/W	**Prefetch Buffer Control** When this bit is set to 1, SiS5591/5592 asserts its first TRDY# for a transaction after it prefetched 1 QW of data from system memory. Otherwise, SiS5591/5592 asserts its first TRDY# after it 2 quad-words are prefetched. 0: Assert TRDY# after prefetching 2 Qws 1: Assert TRDY# after prefetching 1 Qws
5	R/W	**Memory Write and Invalidate Control** When this bit is enable, SiS5591/5592 skips the snooping process to optimise the PCI memory write and invalidate command for PCI masters. When this bit is disable, SiS5591/5592 treats memory write and invalidate command as the same as memory write command. This bit can only be set if the cache line size defined by master devices is the multiple of 8 DWs. 0: Disable 1: Enable
4	R/W	**Memory Read Command Prefetch Control** This bit controls whether or not SiS5591/5592 prefetch data for memory read command. Please note that Memory Read Multiple and Memory Read Line commands always do prefetch. The semantic of this bit is different to others. The value of 0 means enabled for this bit. 0: Enable 1: Disable

3:2	R/W	**Initial Latency Control** This field controls the target initial latency of the PCI66 target bridge. If SiS5591/5592 is unable to assert TRDY# for a transaction within the target initial latency defined by this field, SiS5591/5592 asserts STOP# to retry this cycle. 00: Disable 01: 16 A.G.P. Clocks 10: 24 A.G.P. Clocks 11: 32 A.G.P. Clocks
1	R/W	**Subsequent Latency Control** When this bit is enabled, SiS5591/5592 terminates a transaction with STOP# if it fails to assert TRDY# for the subsequent block within 8 clocks. 0: Disable 1: Enable
0	R/W	**Address Decoding Time Extension Control** This bit controls the decoding time for SiS5591/5592 to guarantee that a PCI transaction is destining to system memory. When this bit is set to 1, it takes one extra CPU clock for the decoding process to complete. It is recommended to disable this function to optimise PCI performance unless there is any master device violates the maximum AD valid delay time(6ns)

Register E3h CPU to PCI66 Bridge characteristics

Default Value: 00h

Access: Read/Write

This register controls miscellaneous functions supported by the CPU-to-PCI66 bridge of SiS5591/5592. The setting of this register may affect PCI performance in various degree

BIT	ACCESS	DESCRIPTION
7	R/W	**Non-Post Write Cycle Retry Behavior Control** When this bit is set to 1, retry from any kind of CPU to A.G.P. write cycles does not back off CPU. Instead, SiS5591/5592 tries to issue the retried cycle again and again until it completes successfully on A.G.P. When this bit is set to 0, retry from any non-post CPU to A.G.P. write cycle results in CPU back off. 0: Back off CPU 1: Continuous Retry
6	R/W	**Post Write Delayed Issuing** When this bit is enabled, SiS5591/5592 may not immediately issue a post-write cycle to A.G.P. even when the post-write buffer is not empty. Instead, SiS5591/5592 tries to wait a period of time for more data to arrive and then combining the post-write data into a single burst transaction if they have continuous addresses. 0: Disable 1: Enable

5	R/W	**64-bit Access Retry Behavior Control** When the value of this bit is 0 and the second half non-post cycle(or the second data phase) of a 64-bit access is retried by the A.G.P. device, SiS5591/5592 tries to issue the second half cycle again and again until it completes successfully on A.G.P. When this bit is set to 1, retry for any non-post cycle issued by the host bridge results in the assertion of BACKOFF#. It is recommended to set this bit to 0. 0: Continue Retry 1: Back-Off CPU
4	R/W	**Fast back-to-back Control** This bit controls whether consecutive post-write cycles use fast back-to-back timing or not. 0: Disable 1: Enable
3	R/W	**Post Write Rate Control** This bit controls the amount of time from the assertion of ADS# to the assertion of BRDY# for CPU-to-PCI66 post write cycle under the best case. 0: 4 CPU clocks 1: 3 CPU clocks
2	R/W	**CPU to PCI66 Bridge Synchronous Mode** This bit can only be enabled when the frequency of A.G.P. clock and the frequency of CPU clock are the same and the skew between these two clocks is within 2ns externally. 0: Disable 1: Enable
1	R/W	**Memory Burst Control** This bit controls whether or not the host bridge generates memory burst cycles. 0: Disable 1: Enable
0	R/W	**Memory Post Write Control** When this bit is enable, all CPU to PCI memory write cycles are posted. 0: Disable 1: Enable

Register EFh **Miscellaneous Function**

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**Reserved**

0	R/W	**Palette Write Cycle Forwarding Control** This bit combined with the VGA Enable in the bridge control register and VGA Palette Snoop Enable in the command register of the virtual PCI-to PCI bridge decide palette write cycles to be forwarded to PCI bus or A.G.P. When the value of this control bit is 1, palette write cycles are forwarded to one interface only(either A.G.P. or PCI bus), and the forwarding is totally controlled by VGA Enable bit. When the value of this control bit is 0, palette write cycles are always forwarded to PCI bus and may optionally be forwarded to A.G.P., which is controlled by VGA Palette Snoop Enable and VGA Enable. The detail is listed below.

Reg. EF Bit 0	VGA Enable	VGA Palette Snoop Enable	Forward to A.G.P.	Forward to PCI Bus
0	0	0		*
0	0	1	*	*
0	1	0	*	*
0	1	1	*	*
1	0	0		*
1	0	1		*
1	1	0	*	
1	1	1	*	

8.2 VIRTUAL PCI-TO-PCI BRIDGE REGISTERS (DEVICE 2)

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0001h

Access: Read Only

The device identifier is allocated as 0001h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 00h

Access: Read/Write, Read Only

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:10	RO	**Reserved**

<table>
<tr><td>9</td><td>R/W</td><td>Fast Back-to-Back Enable
Although this bit is implemented as R/W, it is effectively useless. The generation of fast back-to-back cycle is always controlled by the Fast back-to-back Control bit that resides in Register E3h of function 0, device0.</td></tr>
<tr><td>8</td><td>R/W</td><td>SERR# Enable
This bit and bit 1 of the bridge control register (offset 3Fh) control the forwarding of ASERR# on A.G.P. to SERR# on PCI bus. When both of these two bits are enabled, SiS5591/5592 asserts SERR# when it detects the assertion of ASERR# on A.G.P. When any one of these two bits is disabled, the assertion of ASERR# would not affect SERR#.
0: Disable
1: Enable</td></tr>
<tr><td>7:6</td><td>RO</td><td>Reserved</td></tr>
<tr><td>5</td><td>R/W</td><td>VGA Palette Snoop Enable :
Controls the behaviour in the case of CPU access destining to VGA compatible address. The bit affects the destinations of I/O writes issued by the CPU with address 3C6h, 3C8h, 3C9h. This bit, VGA enable in the bridge control register, and palette write cycle forwarding control (Reg. EF Bit0) decide the palette write cycle to forward to PCI bus or A.G.P.. The detail is listed below.
0: Disable
1: Enable
<table>
<tr><th>Reg. EF Bit 0</th><th>VGA Enable</th><th>VGA Palette Snoop Enable</th><th>Forward to A.G.P.</th><th>Forward to PCI Bus</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td></td><td>*</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>*</td><td>*</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*</td><td>*</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>*</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td>*</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td>*</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>*</td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>*</td><td></td></tr>
</table></td></tr>
<tr><td>4:3</td><td>RO</td><td>Reserved</td></tr>
<tr><td>2</td><td>R/W</td><td>Bus Master Enable
Controls the bridge response to PCI cycles on A.G.P. When this bit is disabled, the bridge does not response to any transaction on A.G.P.
0: Disable
1: Enable</td></tr>
<tr><td>1</td><td>R/W</td><td>Memory Space Enable
Controls the forwarding of memory accesses from CPU to A.G.P. When the bit is disabled, the bridge would not forward any memory accesses to A.G.P. When the bit is enabled, the bridge forwards CPU memory cycles toward A.G.P. according to standard PCI-to-PCI bridge forwarding rule.
0: Disable
1: Enable</td></tr>
</table>

0	R/W	**I/O Space Enable** Controls the forwarding of I/O accesses from CPU to A.G.P. When the bit is disabled, the bridge would not forward any I/O accesses to A.G.P. bus. When the bit is enabled, the bridge forwards CPU I/O cycles toward A.G.P. bus according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable

Register 06h Status

Default Value: 00h

Access: Read Only

This register is reserved since the status information of the primary bus is stored in the status register of Device 0.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 00h

Access: Read Only

The Revision ID is 00h for our first Revision.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 04h

Access: Read Only

The Sub Class Code is 04h for PCI-to-PCI bridge.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h

Access: Read Only

The value of 06h in this field identifies a bridge device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

The value of this register is always 00h since the host bridge would not generate the Memory Write and Invalidate command.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Master Latency Timer**

Register 0Eh Header Type

Default Value: 01h

Access: Read Only

The value of 01h identifies PCI-to-PCI bridge header is being used.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

The value is 00h since we do not support Build-in Self Test.

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 19h Secondary Bus Number (SBUSN)

Default Value: 00h

Access: Read/Write

This register identifies the bus number assigned to the second bus side of the virtual" PCI-to-PCI Bridge. This field is programmed by the PCI configuration software to allow mapping of configuration cycles to A.G.P..

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Secondary Bus Number**

Register 1Ah Subordinate Bus Number (SUBUSN)

Default Value: 00h

Access: Read/Write

This register is used to record the number of the highest numbered PCI bus that is behind A.G.P.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Subordinate Bus Number**

Register 1Bh Secondary Master Latency Timer (SMLT)

Default Value: 00h

Access: Read/Write, Read Only

This register adheres to the definition of the Latency Timer in the PCI Local Bus Specification but applies only to

A.G.P. interface.

BIT	ACCESS	DESCRIPTION
7:3	R/W	**Secondary Master Latency Timer** Default value is 00h. Unit: 8 * A.G.P clock
2:0	RO	**Reserved**

Register 1Ch I/O Base

Default Value: F0h

Access: Read/Write, Read Only

The I/O Base register defines the bottom address of an address range that is used by SiS5591/5592 to determine when to forward I/O transactions from CPU to A.G.P.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**I/O Address Base A[15:12]** Bits[7:4] control the CPU to A.G.P. I/O access. SiS5591/5592 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. IO_BASE ≤ address ≤ IO_LIMIT
3:0	RO	**Reserved**

Register 1Dh I/O Limit

Default Value: 00h

Access: Read/Write, Read Only

The I/O Limit register defines the top address of an address range that is used by SiS5591/5592 to determine when to forward I/O transactions from CPU to A.G.P.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**I/O Address Limit A[15:12]** Bits[7:4] control the CPU to A.G.P. I/O access. SiS5591/5592 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. IO_BASE ≤ address ≤ IO_LIMIT
3:0	RO	**Reserved**

Register 1Eh Secondary PCI-PCI Status (SSTS)

Default Value: 0000h

Access: Read/Write, Read Only

The Secondary Status register is similar in function and bit definition to the Status register of device 0 function 0 of SiS5591/5592.

BIT	ACCESS	DESCRIPTION
15	RO	**Reserved**
14	WC	**Receiver System Error.** This bit is set when ASERR# assertion is detected on A.G.P. This bit can be cleared by writing a 1 to it.
13	WC	**Receiver Master Abort** When 5591/5592 terminates a cycle on A.G.P. with master abort, this bit is set to 1. This bit can be cleared by writing a 1 to it.

12	WC	**Receiver Target Abort** When a 5591/5592 initiated cycle on A.G.P. is terminated with a target abort, this bit is set to 1. This bit can be cleared by writing a 1 to it.
11:0	RO	**Reserved**

Register 20h Non-prefetchable Memory Base Address (MBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the bottom address of a non-prefetchable memory address range that is used by SiS5591/5592 to determine when to forward memory transactions from CPU to A.G.P.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. SiS5591/5592 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. MBASE ≤ address ≤ MLIMIT
3:0	RO	**Reserved**

Register 22h Non-prefetchable Memory Limit Address (MLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a non-prefetchable memory address range that is used by SiS5591/5592 to determine when to forward memory transactions from CPU to A.G.P.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. 5591/5592 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. MBASE ≤ address ≤ MLIMIT
3:0	RO	**Reserved**

Register 24h Prefetchable Memory Base Address (PMBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the bottom address of a prefetchable memory address range that is used by SiS5591/5592 to determine when to forward memory transactions from CPU to A.G.P.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. 5591/5592 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. PMBASE ≤ address ≤ PMLIMIT
3:0	RO	**Reserved**

Register 26h Prefetchable Memory Limit Address (PMLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a prefetchable memory address range that is used by SiS5591/5592 to determine when to forward memory transactions from CPU to A.G.P.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. 5591/5592 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. PMBASE ≤ address ≤ PMLIMIT
3:0	RO	**Reserved**

Register 3Eh PCI to PCI Bridge Control (BCTRL)

Default Value: 0000h

Access: Read/Write, Read Only

The Bridge Control register provides control extensions to the Command register.

BIT	ACCESS	DESCRIPTION
15:4	RO	**Reserved.**
3	R/W	**VGA Enable** The bit controls the forwarding of transactions initiated by CPU. When the bit is enabled, 5591/5592 forwards CPU-initiated cycles with the following address to A.G.P. ● Memory Address: 0A0000h ~ 0BFFFFh ● I/O Address: 3B0h ~ 3BBh, 3C0 ~ 3DFh 0 : Disable 1 : Enable
2	R/W	**ISA Enable** When this bit is enabled, IO transactions addressing the last 768 bytes in each 1KB block will be forwarded to primary PCI bus even if the address are within the range defined by the IOBASE and IOLIMIT. 0 : Disable 1 : Enable
1	R/W	**System Error Enable** This bit and bit 8 of the bridge command register (offset 3Fh) control the forwarding of ASERR# on A.G.P. to SERR# on PCI bus. When both of these two bits are enabled, SiS5591/5592 asserts SERR# when it detects the assertion of ASERR# on A.G.P. When any one of these two bits is disabled, the assertion of ASERR# would not affect SERR#. 0: Disable 1: Enable
0	RO	**Reserved**

8.3 PCI IDE CONFIGURATION SPACE REGISTER

DEVICE	IDSEL	FUNCTION NUMBER
IDE	AD11	0001b

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 5513h

Access: Read Only

The device identifier is allocated as 5513h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0000h

Access: Read/Write, Read Only

The Command register provides coarse control over a device ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:8	RO	**Reserved**
7:3	RO	**Reserved**
2	RO	**Bus Master** When set, the Bus master function is enabled. It is disabled by default.
1	R/W	**Memory Space** The bit controls the response to memory space accesses. This bit should be programmed as "0".
0	RO	**IO Space** When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocatable ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. This bit is zero(disabled) on reset.

Register 06h Status

Default Value: 0000h

Access: Read/Write, Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved** These bits are hardware to zero.
13	WC	**Master Abort Asserted** This bit is set when a PCI bus master IDE transaction is terminated by master abort. While this bit is set, IDE will issue an interrupt request. This bit can be cleared by writing a 1 to it.

12	WC	**Received Target Abort** The bit is set whenever PCI bus master IDE transaction is terminated with target abort.
11	RO	**Signaled Target Abort** The bit will be asserted when IDE terminates a transaction with target abort.
11:9	RO	**DEVSEL# Timing DEVT.** These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in fast timing, and thus the two bits are hardwired to 0 per PCI Spec.
8	R/W	**Reserved, Read as "0".**
7:0	RO	**Reserved** Default value is 00h

Register 08h Revision ID

Default Value: D0h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7	RO	**Master IDE Device** This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function.
6:4	RO	**Reserved**
3	RO	**Secondary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0"the mode is fixed and is determined by the value of bit 2. This bit should be programmed as '1' during the BIOS boot up procedures.
2	RO	**Secondary IDE Operating Mode** This bit defines the mode that the secondary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.
1	RO	**Primary IDE Programmable Indicator** When the bit is programmed as '1', it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as '0', the mode is fixed and is determined by the value of bit 0. This bit should be programmed as '1' during the BIOS boot up procedures.
0	RO	**Primary IDE Operating Mode** This bit defines the mode that the primary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.

Register 0Ah Sub Class Code

Default Value: 01h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 01h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Latency Timer

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Latency Timer** The default value is 0. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 10h~13h Primary Channel Command Block Base Address Register

Register 14h~17h Primary Channel Control Block Base Address Register

Register 18h~1Bh Secondary Channel Command Block Base Address Register

Register 1Ch~1Fh Secondary Channel Control Block Base Address Register

In the native mode, above four registers define the IDE base address for each of the two IDE devices in both the primary and secondary channels respectively. In the compatible mode, the four registers can still be programmed and read out, but it does not affect the IDE address decoding.

Register 20h~23h Bus Master IDE Control Register Base Address

OFFSET REGISTER	REGISTER ACCESS
00H	**Bus Master IDE Command Register (Primary)**
01H	**Reserved**
02H	**Bus Master IDE Status Register(Primary)**
03H	**Reserved**
04-07H	**Bus Master IDE PRD (*) Table Pointer (Primary)**
08H	**Bus Master IDE Command Register (Secondary)**
09H	**Reserved**
0AH	**Bus Master IDE Status Register (Secondary)**
0BH	**Reserved**
0C-0FH	**Bus Master IDE PRD (*) Table Pointer (Secondary)**

*PRD: Physical Region Descriptor

Register 24h~2Bh Reserved

Default Value: 00h
Access: RO

Register 2C~2Dh Subsystem Vendor ID

Default Value: 0000h
Access: Read/Write
This register can be written once and is used to identify vendor of the subsystem.

Register 2Eh~2Fh Subsystem Vendor ID

Default Value: 0000h
Access: Read/Write
This register can be written once and is used to identify subsystem ID.

Register 30h~33h Expansion ROM Base Address

Default Value: 00000000h
Access: Read/Write

Register 40h IDE Primary Channel/Master Drive Data Recovery Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode The test mode recovery and active timer counter.

6	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode The test mode of prefetch byte counter.
5:4	R/W	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 41h IDE Primary Channel/Master Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:5	R/W	**Ultra DMA/33 cycle time Select** 00: Reserved 01: Cycle time of 2 PCI clocks for data out 10: Cycle time of 3 PCI clocks for data out 11: Cycle time of 4 PCI clocks for data out
4:3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 42h IDE Primary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**

3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 43h IDE Primary Channel/Slave Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:5	R/W	**Ultra DMA/33 cycle time Select** 00: Reserved 01: Cycle time of 2 PCI clocks for data out 10: Cycle time of 3 PCI clocks for data out 11: Cycle time of 4 PCI clocks for data out
4:3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 44h IDE Secondary Channel/Master Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 45h IDE Secondary Channel/Master Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:5	R/W	**Ultra DMA/33 cycle time Select** 00: Reserved 01: Cycle time of 2 PCI clocks for data out 10: Cycle time of 3 PCI clocks for data out 11: Cycle time of 4 PCI clocks for data out
4:3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 46h IDE Secondary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 47h IDE Secondary Channel/Slave Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:5	R/W	**Ultra DMA/33 cycle time Select** 00: Reserved 01: Cycle time of 2 PCI clocks for data out 10: Cycle time of 3 PCI clocks for data out 11: Cycle time of 4 PCI clocks for data out
4:3	RO	**Reserved**

2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 48h IDE Command Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 49h IDE Command Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 4Ah IDE General Control Register 0

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Bus Master generates PCI burst cycles Control** 0: Disable 1: Enable
6	R/W	**Test Mode for internal use only** 0: Test Mode 1: Normal Mode The test mode of PCI FRAME signal: 1 flip-flop output 0 combination output.
5	R/W	**Fast post-write control** 0: Disabled 1: Enabled (Recommended)

4	R/W	**Test Mode for internal use only** 0: Normal Mode 1: Test Mode When this bit is set 1, the IRQ of HD drive would pass direct to 8259. On the others hand, IDE would gate IRQ until IDE FIFO is empty under ab-normal operation.
3	R/W	**Bus Master requests PCI bus ownership timing control** 0: PCI Request asserted when FIFO is 75% full during prefetch cycles. 1: PCI Request asserted when FIFO is 50% full during prefetch cycles. The default value is '0'.
2	R/W	**IDE Channel 1 Enable Bit** 0: Disabled (default) 1: Enabled
1	R/W	**IDE Channel 0 Enable Bit** 0: Disabled (default) 1: Enabled
0	R/W	**Reserved**

Register 4Bh IDE General Control register 1

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Enable Postwrite of the Slave Drive in Channel 1.** 0: Disabled. (default) 1: Enabled.
6	R/W	**Enable Postwrite of the Master Drive in Channel 1.** 0: Disabled. (default) 1: Enabled
5	R/W	**Enable Postwrite of the Slave Drive in Channel 0.** 0: Disabled. (default) 1: Enabled.
4	R/W	**Enable Postwrite of the Master Drive in Channel 0.** 0: Disabled. (default) 1: Enabled.
3	R/W	**Enable Prefetch of the Slave Drive in Channel 1.** 0: Disabled. (default) 1: Enabled.
2	R/W	**Enable Prefetch of the Master Drive in Channel 1.** 0: Disabled. (default) 1: Enabled.
1	R/W	**Enable Prefetch of the Slave Drive in Channel 0.** 0: Disabled. (default) 1: Enabled.

0	R/W	**Enable Prefetch of the Master Drive in Channel 0.** 0: Disabled. (default) 1: Enabled.

(Following two 16-bit wide registers define the prefetching length of each IDE channel respectively.)

Register 4Ch~4DhPrefetch Count of Primary Channel

Default Value: FFFFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Prefetch Count of Primary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 4Eh~4Fh Prefetch Count of Secondary Channel

Default Value: FFFFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Prefetch Count of Secondary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 50h~51h Reserved

Register 52h IDE Miscellaneous Control Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3	R/W	**IDE Command Timing Select** 0: The recovery and active time programmed in register 48h-49h will be applied to command cycles for all IDE devices 1: The recovery and active time programmed in register 40h-47h will be applied to command cycles for their associated IDE devices.
2	R/W	**Control of IDE Programmable Indicator register(09 bit 1 and 3)** 0: IDE register 09 bit 1 and 3 would be read as "0". 1: IDE register 09 bit 1 and 3 would be programmable.
1	R/W	**Test Mode for internal use only** 0 : Normal Mode 1 : Test Mode If this bit is set 1, IDE would reset IDE FIFO pointer when 8 bit command is forward to HDs driver. This bit would work on the condition that the transferring byte count of OS is not equal to the byte count received by HDs driver.
0	R/W	**IDE FIFO Size Select** 0: 32 Bytes FIFO 1: 64 Bytes FIFO(Recommended)

8.3.1 Offset Registers for PCI Bus Master IDE Control Registers

The PCI Bus master IDE Registers use 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE control register Base Address in the PCI IDE Configuration space. The base address is also defined in Register 20h~23h of PCI IDE configuration space.

Register 00h Bus Master Primary IDE Command Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Reserved. Return 0 on reads.**
6:5	R/W	**Read or Write Control.** This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.
4:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS Chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 01h Reserved

Register 02h Bus Master Primary IDE Status Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.
0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 03h Reserved

Register 04h~07h Bus Master Primary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

***PRD: Physical Region Descriptor**

Register 08h Bus Master Secondary IDE Command Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved. Return 0 on reads.**
3	R/W	**Read or Write Control.** This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.
2:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 09h Reserved

Register 0Ah Bus Master Secondary IDE Status Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers**.**
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.

1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.
0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 0Bh Reserved

Register 0Ch~0Fh Bus Master Secondary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

*PRD: Physical Region Descriptor

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN.	MAX.	UNIT
Ambient operation temperature	0	70	°C
Storage temperature	-40	125	°C
Input voltage	-0.3	Vcc+0.3	V
Output voltage	-0.5	3.3	V

NOTE:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

9.2 DC CHARACTERISTICS

9.2.1 DC Characteristics of Host, DRAM, PCI and IDE Interface

Ta= 0 - 700 C, Gnd= 0V, Vcc5= 5V+5%, Vcc=3.3V+5%

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{DD}+0.3	V	
V_{OL}	Output Low Voltage		0.4	V	
V_{OH}	Output High Voltage	2.4		V	
I_{OL1}	Output Low Current	6, 16		mA	Note 2, 7
I_{OH1}	Output High Current	-6, -16		mA	Note 2, 7
I_{OL2}	Output Low Current	12, 16		mA	Note 3, 7
I_{OH2}	Output High Current	-12, -16		mA	Note 3, 7
I_{OL3}	Output Low Current	4, 8		mA	Note 4, 7
I_{OH3}	Output High Current	-4, -8		mA	Note 4, 7
I_{OL4}	Output Low Current	4		mA	Note 5
I_{OH4}	Output High Current	-4		mA	Note 5
I_{IH}	Input High Leakage Current		-10	µA	
I_{IL}	Input Low Leakage Current		+10	µA	
C_{IN1}	Input Capacitance		12	pF	Fc=1 MHz
C_{OUT}	Output Capacitance		12	pF	Fc=1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	Fc=1 MHz

1. IOL1 and IOH1 are applicable to the following signals: MA[13:2], MA[1:0]A, MA[1:0]B.
2. OL2 and IOH2 are applicable to the following signals: CAS[7:0]#, RAMW#A/B, SRAS#, SCAS#.
3. IOL3 and IOH3 are applicable to the following signals: AD[31:0], C/BE[3:0]#, PGNT[4:0]#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, PHLDA#, PAR, RAS[5:0]# and IDE interface signals.
4. IOL4 and IOH4 are applicable to the following signals: KRE#, HA[31:3], EADS#, NA#, BRDY#, KEN#, A20M#, BOFF#, MD[63:0], HD[63:0], HBE[7:0]#, ADSC#, ADSV# and AHOLD.
5. The driving current is programmed. Please refer to register description.

9.2.2 DC Characteristics of A.G.P. Interface

Ta= 0 - 700 C, Gnd= 0V, Vcc5= 5V+5%, Vcc=3.3V+5%

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{DD}	I/O Supply Voltage	3.0	3.6	V	
V_{REF}	Input Reference Voltage	$0.39V_{DD}$	$0.41V_{DD}$	V	
V_{IL1}	Input Low Voltage for 1X Signaling	-0.5	$0.3V_{DD}$	V	
V_{IH1}	Input High Voltage for 1X Signaling	$0.5V_{DD}$	V_{DD}+0.5	V	
V_{IL2}	Input Low Voltage for 2X Signaling		V_{REF}-0.2	V	
V_{IH2}	Input High Voltage for 2X Signaling	V_{REF}+0.2		V	
V_{OL}	Output Low Voltage		$0.1V_{DD}$	V	
V_{OH}	Output High Voltage	$0.9V_{DD}$		V	
I_{REF}	V_{REF} Pin Input Current		+10	mA	
I_{OL}	Output Low Current	2, 3, 4		mA	Note 1
I_{OH}	Output High Current	-2, -3, -4		mA	Note 1
I_{IH}	Input High Leakage Current		70	μA	
I_{IL}	Input Low Leakage Current		±10	μA	
C_{IN}	Input Capacitance		8	pF	
C_{OUT}	Output Capacitance		12	pF	
ΔC_{IN}	Strobe to Data Pin Capacitance Delta	-1	2	pF	

Note:

1. The driving current is programmed. Please refer to register description.

9.3 AC CHARACTERISTICS

9.3.1 Host Signals AC Characteristics

Symbol	Parameter	MIN (ns)	MAX (ns)	CL (pf)
T1	BRDY# Active delay from CPUCLK	4.29	7.60	50
T2	BRDY# Inactive delay from CPUCLK	4.55	7.90	50
T3	KEN# Active delay from CPUCLK	4.42	7.65	50
T4	KEN# Inactive delay from CPUCLK	4.68	7.93	50
T5	NA# Active delay from CPUCLK	4.32	7.53	50
T6	NA# Inactive delay from CPUCLK	4.62	7.75	50
T7	BOFF# Active delay from CPUCLK	3.99	6.81	50
T8	BOFF# Inactive delay from CPUCLK	4.00	7.09	50
T9	AHOLD Active delay from CPUCLK	4.61	7.86	50
T10	AHOLD Inactive delay from CPUCLK	4.31	7.58	50
T11	EADS# Active delay from CPUCLK	4.32	7.66	50
T12	EADS# Inactive delay from CPUCLK	4.59	7.84	50
T13	KOE# Active delay from CPUCLK	4.10	7.26	50
T14	KOE# Inactive delay from CPUCLK	4.31	7.55	50
T15	CS1# Active delay from CPUCLK	4.06	7.03	50
T16	CS1# Inactive delay from CPUCLK	4.30	7.33	50

T17	BWE# Active delay from CPUCLK	4.11	7.29	50
T18	BWE# Inactive delay from CPUCLK	4.33	7.58	50
T19	GWE# Active delay from CPUCLK	4.14	7.16	50
T20	GWE# Inactive delay from CPUCLK	4.24	7.47	50
T21	ADSC# Low Valid delay from CPUCLK	4.24	7.33	50
T22	ADSC# High Valid delay from CPUCLK	4.45	7.62	50
T23	ADV# Low Valid delay from CPUCLK	4.18	7.23	50
T24	ADV# High Valid delay from CPUCLK	4.28	7.52	50
T25	TAGWE# Active delay from CPUCLK	4.10	6.98	50
T26	TAGWE# Inactive delay from CPUCLK	4.31	7.28	50
T27	TA[7:0] delay from TAGWE#	5.00	5.00	50
T28	HA[27:18] delay form CPUCLK Note (1) when flush L2	7.42	13.96	50
T29	HA[31:3] delay from CPUCLK Note (1) when snoop L1	9.42	17.14	50
T30	RFIFO data to HD[63:0] delay from CPUCLK	5.47	9.78	50
T31	MD[63:0] to HD[63:0] delay (EDO/FP)	7.92	9.3	50
T32	MD[63:0] to HD from CPUCLK (SDRAM)	5.94	9.9	50

Note :

1. When flush L2 or snoop L1, HA is driven at least one clock before it is sampled by others.

9.3.2 33MHz PCI Interface AC Characteristics

Symbol	Parameter	MIN (ns)	MAX (ns)	CL (pf)
T_{VAL}	CLK to AD[31:0] Valid Delay	2	11	
T_{VAL}	CLK to CBE[3:0] Valid Delay	2	11	
T_{VAL}	CLK to FRAME# Valid Delay	2	11	
T_{VAL}	CLK to IRDY# Valid Delay	2	11	
T_{VAL}	CLK to TRDY# Valid Delay	2	11	
T_{VAL}	CLK to DEVSEL# Valid Delay	2	11	
T_{VAL}	CLK to STOP# Valid Delay	2	11	
T_{VAL}	CLK to PAR Valid Delay	2	11	
T_{VAL}	CLK to SERR# Valid Delay	2	11	
$T_{VAL(PTP)}$	CLK to PGNT[4:0]# Valid Delay	2	12	
$T_{VAL(PTP)}$	CLK to PHLDA# Valid Delay	2	12	
T_{ON}	Float to Active Delay	2		
T_{OFF}	Active to Float Delay		28	
T_{SU}	AD[31:0] Set up Time to CLK	7		
T_{SU}	CBE[3:0] Set up Time to CLK	7		
T_{SU}	FRAME# Set up Time to CLK	7		
T_{SU}	IRDY# Set up Time to CLK	7		

T_{SU}	TRDY# Set up Time to CLK	7		
T_{SU}	DEVSEL# Set up Time to CLK	7		
T_{SU}	STOP# Set up Time to CLK	7		
$T_{SU(PTP)}$	PREQ[4:0]# Set up Time to CLK	12		
$T_{SU(PTP)}$	PHOLD# Set up Time to CLK	12		

9.3.3 Interface AC Characteristics for 1X Signals

Symbol	Parameter	MIN (ns)	MAX (ns)	CL (pf)
T_{CYC}	CLK Cycle Time	15	30	
T_{HIGH}	CLK High Time	6		
T_{LOW}	CLK Low Time	6		
T_{VALD}	CLK to AAD[31:0] Valid Delay	1.0	6.0	
T_{VALD}	CLK to ACBE[3:0] Valid Delay	1.0	6.0	
T_{VALC}	CLK to AFRAME# Valid Delay	1.0	5.5	
T_{VALC}	CLK to AIRDY# Valid Delay	1.0	5.5	
T_{VALC}	CLK to ATRDY# Valid Delay	1.0	5.5	
T_{VALC}	CLK to ADEVSEL# Valid Delay	1.0	5.5	
T_{VALC}	CLK to ASTOP# Valid Delay	1.0	5.5	
T_{VALC}	CLK to APAR Valid Delay	1.0	5.5	
T_{VALC}	CLK to AGNT# Valid Delay	1.0	5.5	
T_{VALC}	CLK to ST[2:0] Valid Delay	1.0	5.5	
T_{ON}	Float to Active Delay	1.0	6.0	
T_{OFF}	Active to Float Delay	1.0	14.0	
T_{SUD}	AAD[31:0] Set up Time to CLK	5.5		
T_{SUD}	ACBE[3:0] Set up Time to CLK	5.5		
T_{SUD}	ASBA[7:0] Set up Time to CLK	5.5		
T_{SUC}	PIPE# Set up Time to CLK	6.0		
T_{SUC}	AFRAME# Set up Time to CLK	6.0		
T_{SUC}	AIRDY# Set up Time to CLK	6.0		
T_{SUC}	ATRDY# Set up Time to CLK	6.0		
T_{SUC}	ADEVSEL# Set up Time to CLK	6.0		
T_{SUC}	ASTOP# Set up Time to CLK	6.0		
T_{SUC}	RBF# Set up Time to CLK	6.0		
T_{SUC}	SERR# Set up Time to CLK	6.0		
T_{SUC}	AREQ# Set up Time to CLK	6.0		

9.3.4 Interface AC Characteristics for 2X Signals

Symbol	Parameter	MIN (ns)	MAX (ns)	CL (pf)
T_{TSF}	CLK to Transmit Strobe Falling	2.0	12.0	

T_{TSR}	CLK to Transmit Strobe Rising		20.0	
T_{DVB}	Data Valid before Strobe	1.7		
T_{DVA}	Data Valid after Strobe	1.7		
T_{OND}	Float to Active Delay	-1.0	9.0	
T_{OFFD}	Active to Float Delay	1.0	12.0	
T_{ONS}	Strobe Active to Strobe Falling Edge Setup	6.0	10.0	
T_{OFFS}	Strobe Rising Edge to Strobe Float Delay	6.0	10.0	
T_{RSSU}	Receive Strobe Setup Time to CLK	6.0		
T_{RSH}	Receive Strobe Hold Time from CLK	1.0		
T_{DSU}	Data to Strobe Setup Time	1.0		
T_{DH}	Strobe to Data Hold Time	1.0		

9.3.5 DRAM Signals AC Characteristics

		SDRAM		EDO/FP		SDRAM		EDO/FP	
Symbol	Parameter	BST (ns)	CL (pf)	BST (ns)	CL (pf)	WST (ns)	CL (pf)	WST (ns)	CL (pf)
T33	RAS[5:0]# Active delay from CPUCLK	3.39	40	3.68	55	7.55	85	9.16	175
T34	RAS[5:0]# Inactive delay from CPUCLK	3.42	40	3.69	55	7.43	85	9.36	175
T35	CAS[7:0]# Active delay from CPUCLK	3.73	40	3.83	40	8.57	100	8.67	100
T36	CAS[7:0]# Inactive delay from CPUCLK	3.84	40	3.94	40	8.44	100	8.54	100
T37	SRAS# Active delay from CPUCLK Note (3)	7.35	40			12.58	360		
T38	SRAS# Inactive delay from CPUCLK	3.02	40			5.62	360		
T39	SCAS# Active delay from CPUCLK Note (3)	7.06	40			13.06	360		
T40	SCAS# Inactive delay from CPUCLK	3.17	40			5.84	360		
T41	MD[63:0] delay from CPUCLK	4.30	40	4.39	40	8.19	60	8.41	60
T42	RAMW# Active delay from CPUCLK Note (3)	5.77	40	4.00	55	15.49	245	13.92	320
T43	RAMW# Inactive delay from CPUCLK	3.99	40	4.26	55	12.76	245	14.78	320
T44	MA[1:0] Low Valid delay from CPUCLK		40	3.94	55		245	14.22	320
T45	MA[1:0] High Valid delay from CPUCLK		40	3.95	55		245	14.90	320
T46	HA[31:3] to MA[13:0] delay	6.23	40	6.24	55	19.66	355	26.02	605
T47	MA[13:0] delay from CPUCLK Note (4) for GART address translation (page table cache miss)	8.46	40	8.83	55	21.54	355	27.59	605
T48	MA[13:0] delay from CPUCLK Note (4) for Graphic window address translation (page table cache hit)	8.41	40	8.80	55	21.50	355	27.60	605
T49	WFIFO address to MA[13:0] delay from CPUCLK Note (5) (starting to write)	6.64	40	9.74	55	19.31	355	29.02	605
T50	WFIFO address to MA[13:0] delay from CPUCLK Note (5) (between back to back single write)	5.72	40	8.60	55	17.37	355	27.67	605
T51	CKE# Active delay from CPUCLK	6.63	40			13.86	360		
T52	CKE# Inactive delay from CPUCLK	9.20	40			14.93	360		

Note:

1. All above measurement are got with driving current of DRAM control signals programmed as below.

RAS[5:0]#	8mA, (Strong)
CAS[7:0]#	12mA, (Weak)
MA[13:2]	6mA, (Weak)
MA[1:0]A	6mA, (Weak)
MA[1:0]B	6mA, (Weak)
RAMWA#	12mA, (Weak)
RAMWB#	12mA, (Weak)
SRAS#/SCAS#	12mA. (Weak)

2. "Best Case" is measured with min. DRAM loading, while "Worst Case" is measured with max. DRAM loading.

3. In SDRAM, " SRAS#, SCAS#, and RAMW# are combined with their pre-state. In such an approach, SRAS#, SCAS#, and RAMW# are asserted almost one clock before the assertion of CS#. For instance, in 66Mhz system, SRAS# = 7.35~12.58 ns would present 17.42~22.65 ns setup time for the SRAS# signal, in deed, without considering damping effect.

4. In T46~T50, MA is driven at least one clock before issuing DRAM commands. This loose timing for fight time, setup time, and damping effect.

10. THERMAL ANALYSIS

10.1 CHIP THERMAL ANALYSIS WITHOUT HEAT SINK

Room Temp. = 22°C (No flow)
Location of thermal probe: centre of the chip
Result:

Temp.(°C)	28.9	37.4	47.5	57.2	67.5	77.4
Consumed Power (Watt)	0.38	0.85	1.39	1.99	2.65	3.37

Power (Watt)
The formula of the characteristics line is
Temp.=16.284x + 23.804 * Power (°C)

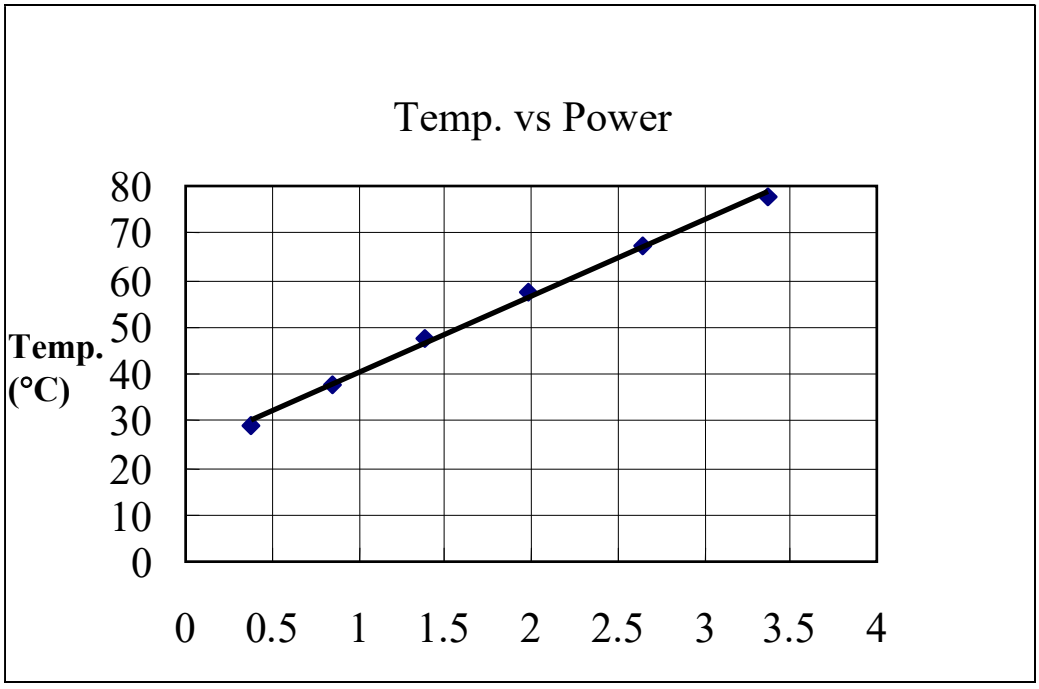


Figure 10.1-1 Temp. VS Power

10.2 CHIP THERMAL ANALYSIS WITH HEAT SINK

Room Temp. = 23°C (No flow)
Location of thermal probe: centre of the chip
Result:

Temp.(°C)	24.3	29.1	34	38.9	43.6	48.4
Consumed Power (Watt)	0.38	0.85	1.39	2.0	2.65	3.35

Power (Watt)
The formula of the characteristics line is
Temp.=8.0553x + 22.126 * Power (°C)

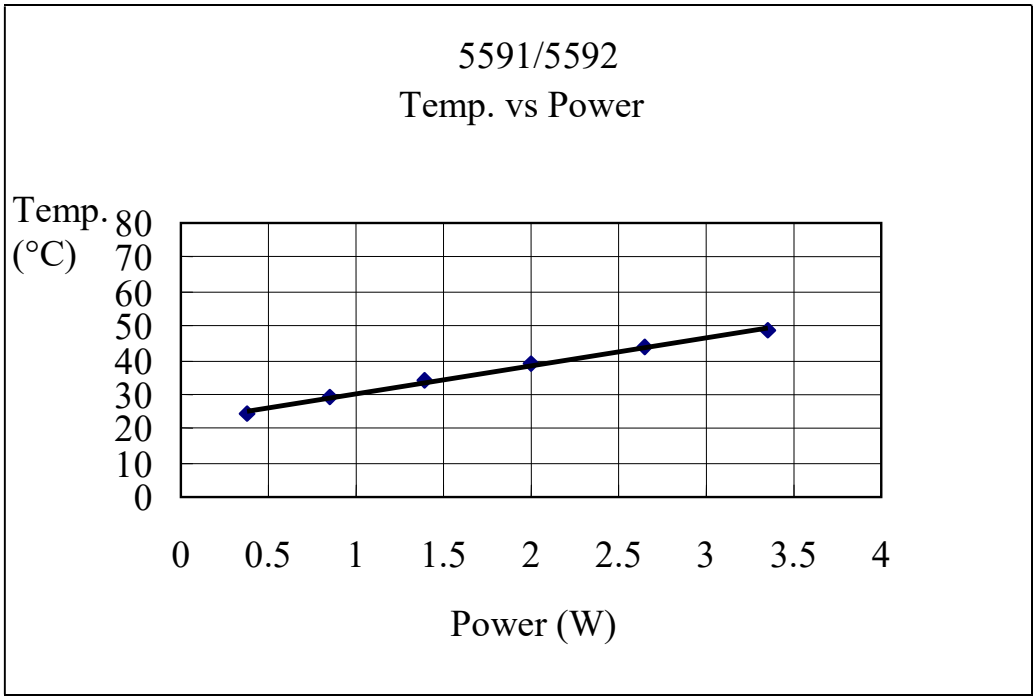
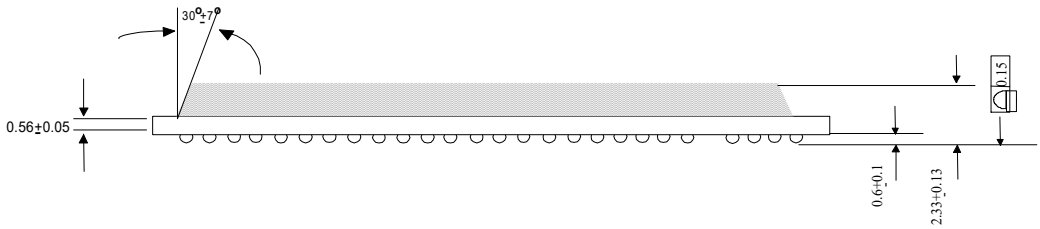


Figure 10.2-1 Temp. VS Power

11. MECHANICAL DIMENSION (TOP VIEW)

11.1 SiS5591/5592 (553 BGA)

(Unit: mm)



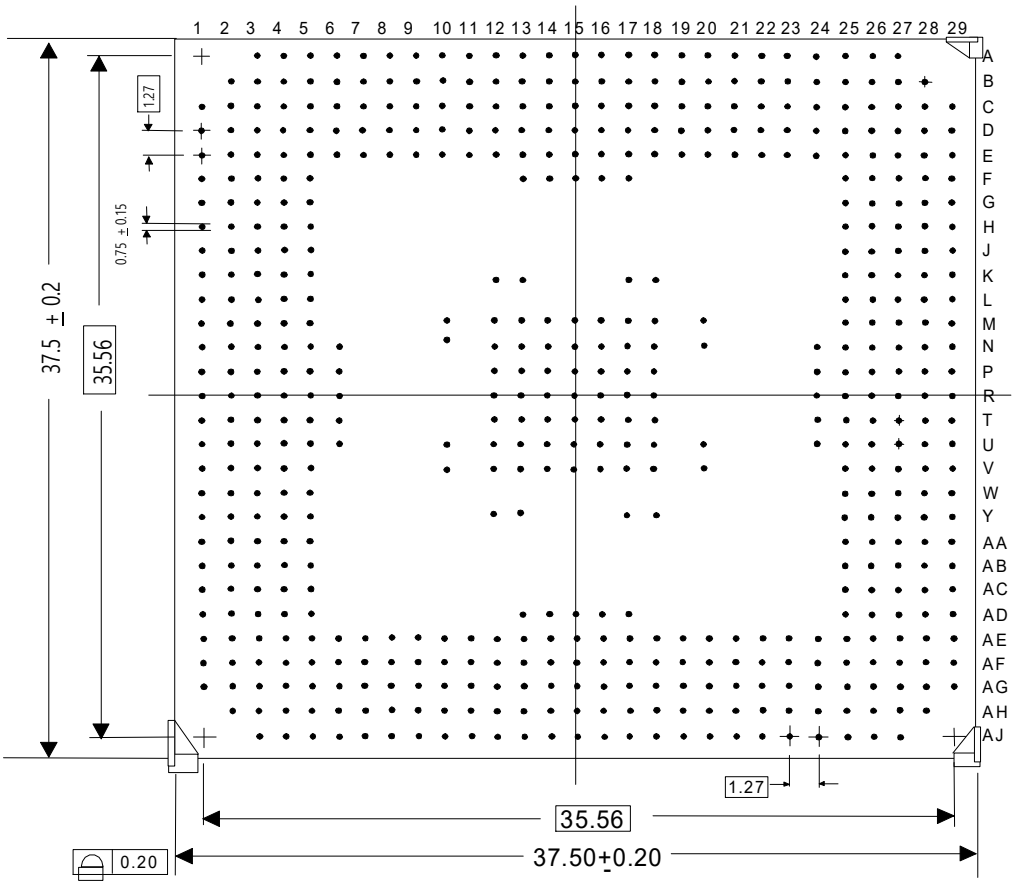


Figure 11.1-1 553 BGA

12. COPYRIGHT NOTICE

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