82340SX ISA CHIP SET

- Two Chip ISA (Industry Standard Architecture) Chip Set Capable of Use in 386™ SX-Based Systems Up to 20 MHz
- Both Chips are 160 Quad Flatpacks, 1.0- and 1.5-Micron CMOS
- Memory Control of One to Four Banks of 16-Bit DRAM Using 256k, 1M, or 4M Components Allowing 32 Mbytes on System Board
- Page Mode DRAM Operation on Any Number of Banks
- Two/Four-Way Interleaving or Direct Access on System Board Memory
- Programmable Option for Block or Word Interleave
- Programmable DRAM Timing Parameters
- Remap Option Allows Logical Reordering of System Board DRAM Banks
- System Board Refresh Optionally Decoupled from Slot Bus Refresh
- Staggered Refresh Minimizes Power Supply Load Variations
- Built-In "Sleep" Mode Features, Including Use of Slow Refresh DRAMs in Power Critical Operations
- EMS Hardware Supports Full LIM EMS 4.0 Spec over Entire 32 Mbyte Memory Map with Backfill to 256k—Includes Two Sets of 36 Mapping Registers Each
- Shadow RAM Support in 16k Increments over Entire 640k to 1M range
- Support for 387™ SX Numerical Coprocessors
- Software Coprocessor Reset can be Disabled
- Internal Switching and Programmable CLK2 Support for Slow and "Turbo" Modes
- Programmable Drive on DRAM and Slot Bus Interface Signals Allows Direct Drive Tailored to System Size
- Asynchronous or Synchronous Slot Bus Operation with Programmable bus Clock Divider
- Bus "Quiet" Mode Assures that Slot Bus Signal Lines are Driven Only During Slot Accesses
- Integrated Peripheral Functions:
  - Two 82C37A DMA Controllers
  - Two 82C59A Interrupt Controllers
  - One 82C54 Timer
  - One 146818 Real Time Clock
- Supports 8- or 16-Bit Wide BIOS ROMs
- I/O Decode Programmable for 10- or 16-Bit Addresses
- Separate Parity Generators/Checkers for High Speed Operation
- Designed for Systems with Up to 12 MHz Backplane Operation
- Three-State Control Pins Added for Board Level Testability
- Compatible with Lotus 1-2-3* Version 3.0 in 1M Systems

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*Lotus 1-2-3® is a registered trademark of Lotus Development Corporation.

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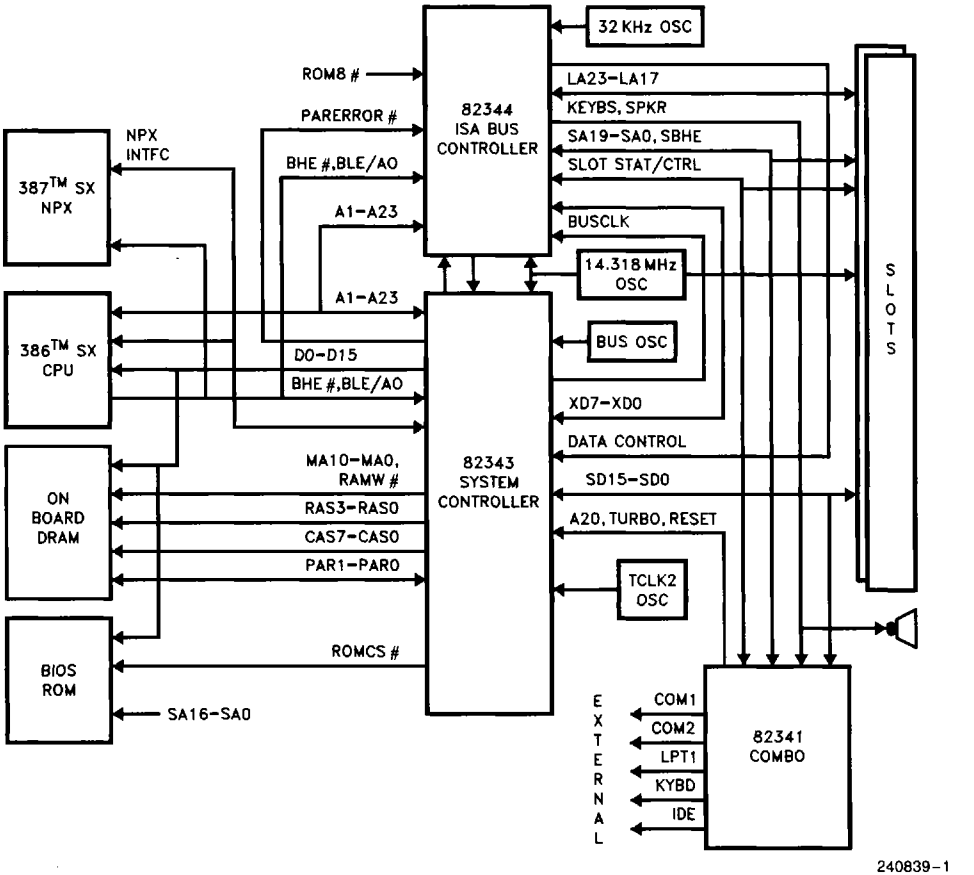
Block Diagram



8-bit ROM is on XD bus