Pentium/P54C PCI/ISA Chipset for Notebook

SiS 5101/5102/5103

Preliminary

Rev. 2.0

November 30, 1995

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1. SiS5101/5102/5103 OVERVIEW

A whole set of the SiS5101, 5102 and 5103 provides fully integrated support for the Pentium PCI/ISA Notebook system. The chipset is a low power portable solution which includes all of the smart power management technology. The chipset supports EDO DRAM, Pipelined Burst SRAM by using a high performance system.

The SiS5101 PCI Cache Memory Controller (PCMC) integrates the bridges that control the interfaces between CPU, PCI, CACHE and Memory. It converts host address and control signals to PCI cycles or CACHE/main memory cycles. It can also convert PCI master cycle to access cache and main memory.

The SiS5102 PCI Local Data Buffer (PLDB) provides the control of paths for the data to and from CPU, DRAM and PCI bus. It has built-in 4QW CPU to memory post write buffer, 4DW CPU to PCI post write buffer, 1QW PCI to memory post write buffer, 1QW memory to CPU read buffer and 1QW memory to PCI read buffer to increase the performance.

The SiS5103 System I/O and PMU (SIOP) are the system I/O controller with PCI to ISA bridge. The internal smart power management controller can be used to achieve the maximum power saving for the CPU and system. The leakage control is supported in all three chips.

With the SiS5101, SiS5102, and SiS5103 chipset, only 7TTLs are required to implement a Pentium Notebook system. Figure 1.1 shows the system block diagram.

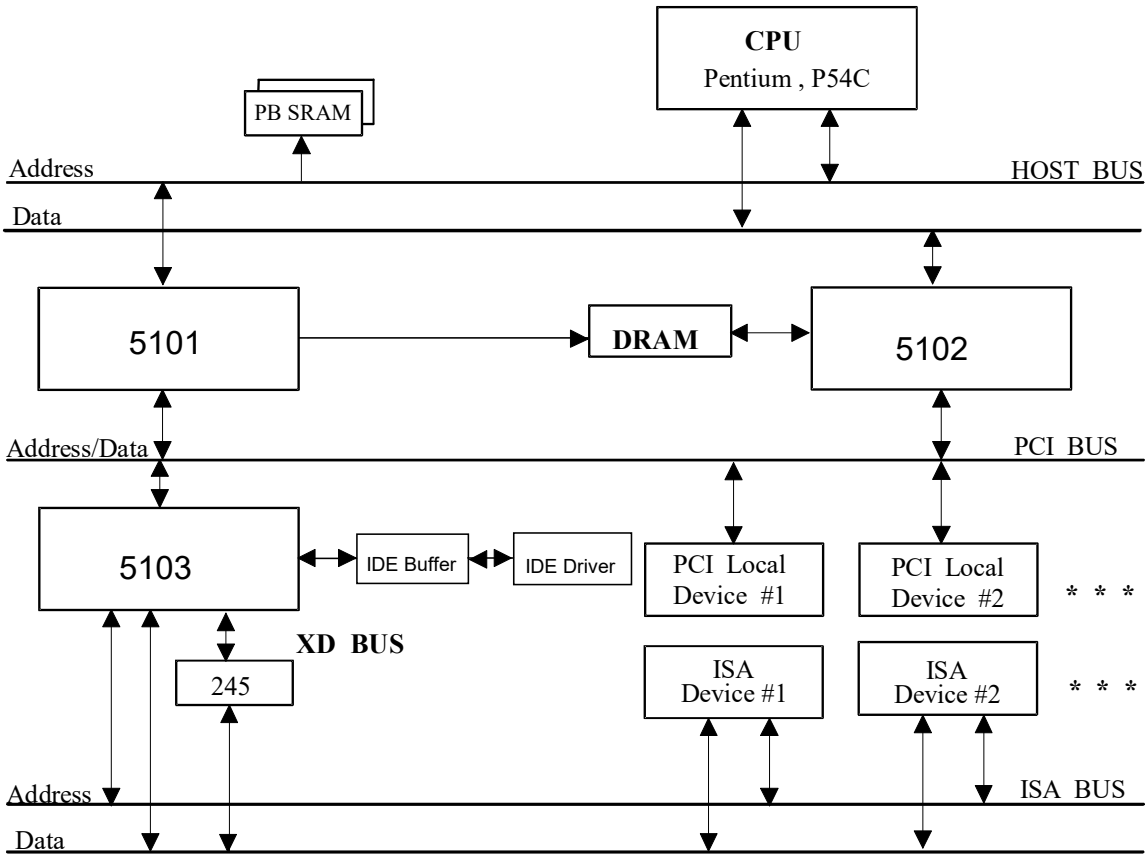


Figure 1.1 5101/5102/5103 System Block Diagram

2. SiS5101

2.1 Features

- **Supports Pentium Processor up to 120MHz**
- **Supports K5 and M1 CPU Processor**
- **Integrated Second Level (L2) Cache Controller**
  - Write Through and Write Back Cache Modes
  - 8 bits or 7 bits Tag with Direct Mapped Organization
  - Supports Standard and Pipelined Burst SRAMs
  - Supports SRAM Standby Mode
  - Supports 64 KBytes to 2 MBytes Cache Sizes
  - Cache Read/Write Cycle of 3-2-2-2 or 4-2-2-2 Using Standard SRAMs at 66 MHz
  - Cache Read/Write Cycle of 3-1-1-1 Using Pipelined Burst SRAMs at 66 MHz
- **Integrated DRAM Controller**
  - Supports 4 Banks of SIMMs up to 256 MBytes of Cacheable Main Memory
  - Supports " Table- Free " DRAM Configuration
  - Concurrent Write Back
  - CAS#-before-RAS# Transparent DRAM Refresh
  - Supports 256K/512K/1M/2M/4M/8M/16M xN 70ns Fast Page Mode and EDO DRAM
  - The Fastest Burst Cycle Speed for FP and EDO are 6-3-3-3 and 6-2-2-2 respectively
  - Programmable CAS# driving Current
  - Programmable DRAM Speed
  - Supports Slow Refresh
- **Two Programmable Non-Cacheable Regions**
- **Supports Synchronous and Asynchronous PCI Clock**
- **Supports SMI/SMM Mode**
- **Supports CPU Stop Clock**
- **Provides High Performance PCI Arbiter**
  - Supports Four PCI Masters
  - Supports Rotating Priority Mechanism
  - Hidden Arbitration Scheme Minimizes Arbitration Overhead
- **Integrated PCI Bridge**
  - Translates the CPU Cycles into the PCI Bus Cycles
  - Provides CPU-to-PCI Read Assembly and Write Disassembly Mechanism
  - Translates Sequential CPU-to-PCI Memory Write Cycles into PCI Burst Cycles
  - PCI Burst Write in the Pace of X-2-2-2-....
  - PCI Burst Read L2 Cache in X-2-2-2-....
  - PCI Burst Read DRAM in X-3-2-3-2-....
  - Cache Snoop Filters Ensure Data Coherency and Minimize Snoop Frequency
  - Meet PCI Specification Buffer Strength
- **Supports Leakage Control**
- **Supports Suspend to Memory**
- **208-Pin PQFP/TQFP Package**
- **0.6µm CMOS Technology**

2.2 SiS5101 Functional Block Diagram

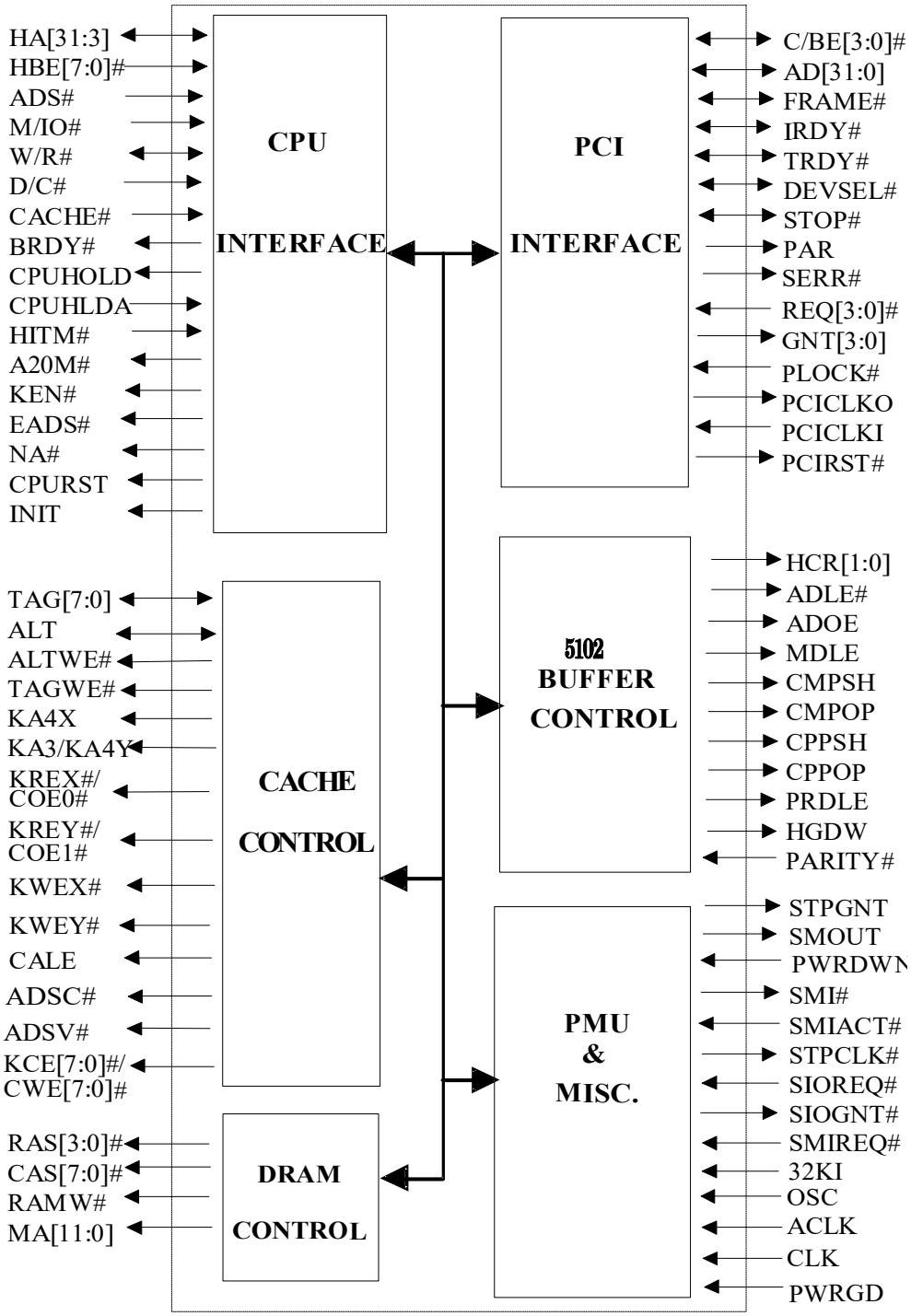


Figure 2.1 SiS5101 Functional Block Diagram

2.3 SiS5101 General Description

The SiS5101(PCMC) bridges the host bus and the PCI local bus. The SiS5101 (PCMC) monitors each cycle initiated by the CPU, and forwards it to the PCI bus if the CPU cycle is not the local memory cycle. For the CPU or the PCI bus to the local memory cycles, the built-in Cache and DRAM Controller assume control to the secondary cache, DRAMs, and the SiS5102 (PLDB). The SiS5101 (PCMC) also guides the SiS5102 (PLDB) for correct data flow. All of the Notebook Power Management Unit (PMU) functions are provided.

2.4 CPU Interface

The SiS5101 is designed to support Pentium/P54C CPU host interface at 50/60/66MHz. The host data bus and the DRAM bus are 64-bit wide.

The SiS5101 supports the pipelined addressing mode of the Pentium/P54C CPU by issuing the next address signal, NA#. NA# is only generated in two cases:
a) burst read L2 cache or DRAM
b) single read DRAM.

The PCMC supports the CPU L1 write back(WB) or write through(WT) cache and the PCMC L2 WB or WT cache. The L1 cache is snooped by the assertion of EADS# when the CPU is put in the HOLD state. The PCMC issues CPUHOLD to the Pentium/P54C CPU in response to the assertion of PCI master requests(REQ[3:0]#, and SIOREQ#). Upon receiving the CPUHLDA from the CPU, it does not immediately assert GNT[3:0]# or SIOGNT# until both the CPU to PCI posted write buffer and the Memory write buffer are empty. During inquire cycles, the CPUHOLD may be negated temporarily to allow the CPU to write back the inquired hit modified line to L2 or DRAM.

2.5 Cache Controller

The built-in L2 Cache Controller uses a direct-mapped, bank-interleaved/non-interleaved scheme, which can be configured as either in the write through or write back mode. Both standard and Pipelined Burst/ Burst SRAMs are supported.

Table 1 shows the cache sizes that are supported by the SiS5101, with the corresponding TAG RAM sizes, data RAM sizes, and cacheable memory sizes. Tables 2 and 3 summarize the performance and options when either the standard SRAMs or the Burst SRAMs are used.

Table 1

Cache Size	Data RAM	Tag RAM	Alter RAM	Cacheable Size	Interleaved
64K	8Kx8x8	2Kx8	2Kx1	16M	No
128K	8Kx8x16	4Kx8	4Kx1	32M	Yes
256K	32Kx8x8	8Kx8	8Kx1	64M	No
512K	32Kx8x16	16Kx8	16Kx1	128M	Yes
512K	64Kx8x8	16Kx8	16Kx1	128M	No
1M	128Kx8x8	32Kx8	32Kx1	256M	No
1M	64Kx8x16	32Kx8	32Kx1	256M	Yes
2M	128Kx8x16	64Kx8	64Kx1	512M	Yes

The PCMC also provides an alternative to save the dirty SRAM chip. This is accomplished by sharing the alter bit with tag address bits in the same 8-bit wide TAG RAM. System uses this implementation supports 7 tag address bits and 1 dirty bit. By doing so, the cacheable local memory sizes are reduced to half of the original sizes as indicated in Table 1.

In reality, the L2 Cacheable DRAM Size is determined by:
1) Max. L2 Cacheable Size as described in table 1.
2) Non-Cacheable Area defined in register 57h, 58h, 59h and 5Ah and
3) C, D, E, F Segment Cachability defined in register 53h, 54h, 55h, and 56h.

But, the L1 Cacheable size is only determined by 2), 3), and the maximum DRAM size, i.e., 256M bytes. Thus, the cycles with address ranging over the L2 Cacheable Size but within the 256M bytes can also be cacheable to L1. The behavior of KEN# is ruled by the L1 Cacheability. Note that only code of C, D, E, F segment is cacheable to L1/L2, and the data portion of C, D, E, F segment is not cacheable to L1/L2.

Table 2 Pipelined Burst SRAM Speed Setting

Cycle type	75 MHz	66,60 MHz	50MHz
Burst read	3/4-1-1-1	3/**4**-1-1-1	3/**4**-1-1-1
Burst write	3/4-1-1-1	3/**4**-1-1-1	3/**4**-1-1-1
Single read	4	3/**4**	3/**4**
Single write	4	3/**4**	3/**4**

Note :
1: The burst SRAM speed for 66/60MHz is 9 ns. For 50MHz, it is 12ns.
2: **X**-Y-Y-Y is the recommended setting.

Table 3 Asynchronous SRAM speed setting (apply to read and write cycle)

	75MHz		66MHz		60MHz		50MHz	
cache configuration	Tag	Data	Tag	Data	Tag	Data	Tag	Data
3-1-1-1 interleave	---	---	---	---	---	---	15ns	15ns
3-1-1-1 non-interleave	---	---	---	---	---	---	---	---
3-2-2-2 interleave	12ns	15ns	15ns	15ns	15ns	15ns	20ns	20ns
3-2-2-2 non-interleave	12ns	15ns	15ns	15ns	15ns	15ns	20ns	20ns
3-3-3-3 interleave	12ns	15ns	15ns	15ns	15ns	15ns	20ns	20ns
3-3-3-3 non-interleave	12ns	15ns	15ns	15ns	15ns	15ns	20ns	20ns
4-1-1-1 interleave	15ns	12ns	15ns	12ns	15ns	12ns	20ns	15ns
4-1-1-1 non-interleave	---	---	---	---	---	---	---	---
4-2-2-2 interleave	15ns	15ns	15ns	15ns	20ns	20ns	20ns	20ns
4-2-2-2 non-interleave	15ns	15ns	15ns	15ns	20ns	20ns	20ns	20ns
4-3-3-3 interleave	15ns	20ns	15ns	20ns	20ns	20ns	20ns	20ns
4-3-3-3 non-interleave	15ns	20ns	15ns	20ns	20ns	20ns	20ns	20ns
5-1-1-1 interleave	20ns	12ns	20ns	12ns	20ns	12ns	20ns	15ns
5-1-1-1 non-interleave	---	---	---	---	---	---	---	---
5-2-2-2 interleave	20ns	15ns	20ns	15ns	20ns	20ns	20ns	20ns
5-2-2-2 non-interleave	20ns	15ns	20ns	15ns	20ns	20ns	20ns	20ns
5-3-3-3 interleave	20ns	20ns	20ns	20ns	20ns	20ns	20ns	20ns
5-3-3-3 non-interleave	20ns	20ns	20ns	20ns	20ns	20ns	20ns	20ns

2.6 DRAM Controller

The 5101 can support 4 rows of DRAM, and memory size from 2 MBytes up to 256 MBytes. Each populated bank could be single or double sided 64 bits FP DRAM or EDO (Extended Data Output) DRAM. It is also permissible to mix FP DRAM bank and EDO DRAM bank without any order. The installed DRAM type can be 256K x 36, 512K x 36, 1M x 36, 2M x 36, 4M x 36, 8Mx36 or 16M x 36 SIMMs.

DBR 3~0 (DRAM Boundary Register 73h~70h) are used to configure the total amount of memory. In DBR 3~0, bit 7~0 corresponds to host address 28~21. Contents in these registers reflect the boundary address, that means the value programmed to the last DBR will be the DRAM size in the system.

DBR0 (Reg. 70) = Total amount of memory in Bank 0
DBR1 (Reg. 71) = Total amount of memory in Bank 0 + Bank 1
DBR2 (Reg. 72) = Total amount of memory in Bank 0 + Bank 1 + Bank 2
DBR3 (Reg. 73) = Total amount of memory in Bank 0 + ...+ Bank 3

The following two examples show how the DBR registers be used to determine the memory size.

Example 1:
The system memory is populated as 2 banks of single-sided 1M x 36 DRAM, which are located at Bank 1 and 3. This yields 16 M Bytes DRAM totally. The DBR registers are programmed as follows:

```
DBR0 = 00h   ; empty                    ; 0 M Byte totally
DBR1 = 04h   ; 8 M Bytes for Bank 1     ; 8 M Bytes totally
DBR2 = 04h   ; empty                    ; 8 M Bytes totally
DBR3 = 08h   ; 8 M Bytes for Bank 3     ; 16 M Bytes totally
```

Example 2:
The system memory is populated as 4 banks of single-sided 16 M x 36 DRAM, which are located from Bank 0 to 3. This yields 256 M Byte DRAM totally. The DBR registers are programmed as follows:

```
DBR0 = 40h   DBR 8 bit 0 = 0   ; 128 M Bytes for Bank 0   ; 128 M Bytes totally
DBR1 = 80h   DBR 8 bit 1 = 0   ; 128 M Bytes for Bank 1   ; 256 M Bytes totally
DBR2 = 80h   DBR 8 bit 2 = 0   ; 0 M Bytes for Bank 2     ; 256 M Bytes totally
DBR3 = 80h   DBR 8 bit 3 = 0   ; 0 M Bytes for Bank 3     ; 256 M Bytes totally
```

The 12-bit multiplexed row/column address MA[11:0] allows the PCMC to support 256K, 1M, 4M, and 16M 70ns fast page mode DRAMs. Table 4 shows the different memory address mapping for different DRAM Configuration.

Table 4. MA Generation Table

Body Type	256K		512K		1M		2M	
MA	CAS	RAS	CAS	RAS	CAS	RAS	CAS	RAS
MA0	A3	A12	A3	A12	A3	A22	A3	A22
MA1	A4	A13	A4	A13	A4	A24	A4	A24
MA2	A5	A14	A5	A14	A5	A14	A5	A26
MA3	A6	A15	A6	A15	A6	A15	A6	A15
MA4	A7	A16	A7	A16	A7	A16	A7	A16
MA5	A8	A17	A8	A17	A8	A17	A8	A17
MA6	A9	A18	A9	A18	A9	A18	A9	A18
MA7	A10	A19	A10	A19	A10	A19	A10	A19
MA8	A11	A20	A11	A20	A11	A20	A11	A20
MA9	NA	NA	NA	A21	A12	A21	A12	A21
MA10	NA	NA	NA	NA	NA	NA	NA	A23
MA11	NA	NA	NA	NA	NA	NA	NA	NA

Body Type	4M		8M		16M	
MA	CAS	RAS	CAS	RAS	CAS	RAS
MA0	A3	A22	A3	A22	A3	A22
MA1	A4	A24	A4	A24	A4	A24
MA2	A5	A14	A5	A14	A5	A26
MA3	A6	A15	A6	A15	A6	A15
MA4	A7	A16	A7	A16	A7	A16
MA5	A8	A17	A8	A17	A8	A17
MA6	A9	A18	A9	A18	A9	A18
MA7	A10	A19	A10	A19	A10	A19
MA8	A11	A20	A11	A20	A11	A20
MA9	A12	A21	A12	A21	A12	A21
MA10	A13	A23	A13	A23	A13	A23
MA11	NA	NA	NA	A25	A14	A25

To improve the CPU write DRAMs performance, there is a one level built-in CPU-to-Memory posted write buffer with 4 QWs deep (CTMPB). All the single writes and the burst writes are buffered. In the CPU read miss/line fill cycle, the write-back data from the L2 cache are also buffered into the CTMPB. At the same time, the PCMC starts reading from the DRAMs. The buffered data are written to the DRAMs when the read cycle completes. With this concurrent write back policy, many wait states are eliminated. However, any other cycle targeting the DRAMs will be suspended until the CTMPB is empty.

Table 5 outlines the read and write DRAM cycle performance based on 70ns DRAMs.
Table 6. shows the corresponding request address bits used in column address and row address for the DRAM.

Table 5 DRAM Performance

Cycle type	75MHz	66,60 MHz	50MHz	DRAM Type
read(page hit/row miss/page miss)	**7/10/13-4-4-4** 7/10/13-4-4-4 7/10/13-3-3-3 7/10/13-3-3-3	**6/9/12-3-3-3** 7/10/13-4-4-4 6/9/12-2-2-2 7/10/13-2-2-2	**6/9/12-3-3-3** 7/10/13-4-4-4 6/9/12-2-2-2 7/10/13-2-2-2	standard page mode standard page mode EDO EDO
posted write (CPU-> Buffer)	**3/4/5-2-2-2** 3/4/5-2-2-2 3/4/5-3-3-3	**3/4/5-1-1-1** 3/4/5-2-2-2 3/4/5-3-3-3	**3/4/5-1-1-1** 3/4/5-2-2-2 3/4/5-3-3-3	standard page mode, EDO standard page mode, EDO standard page mode, EDO
write retire rate (Buffer->DRAM)	**3**/4/5 3	**3**/4/5 2	**3**/4/5 2	standard page mode EDO

Note:
1: **X-Y-Y-Y** is the recommended setting.

Table 6 DRAM speed setting based on 70ns DRAMs (apply to read and write cycle)

	Register	75MHz	66MHz	60MHz	50MHz
read CAS pulse width	50h bit 7-6	2T	2T	2T	2T
write CAS pulse width	50h bit 5	2T	2T	2T	2T
CAS precharge time 1	53h bit 7	1T/2T	1T/2T	1T/2T	1T
RAS precharge time	7Ah bit 1	3T	3T	3T	3T
RAS to CAS delay time	53h bit 2	3T	3T	3T	3T
refresh RAS active time	52h bit 0	5T	5T	5T	4T
DRAM write push to CAS delay	5Bh bit 3	1T	1T	1T	1T
EDO DRAM CAS pulse width 2	7Ch bit 1	1T/2T	1T/2T	1T/2T	1T
EDO DRAM CAS precharge time 2	7Ch bit 0	1T/2T	1T/2T	1T/2T	1T

Note:
1. The burst DRAM read hit cycle is 6-3-3-3 when the CAS precharge time is 1T. If the CAS precharge time is 2T, the burst DRAM read hit cycle is increased to 7-4-4-4.
2. When EDO type DRAMs are installed and register 7Ch bits[1:0] are set to "11" (1T), the burst DRAM read hit cycle is 6-2-2-2. The standard Fast Page mode DRAM timing is applied, if register 7Ch bits[1:0] are set to "00". In fact, 5101 can detect the EDO type DRAM and applies optimal timing automatically.

Table 7 gives the corresponding register settings of EDO and Fast Page DRAMs. Table 8 shows the corresponding register settings of standard and pipelined burst SRAM.

Table 7 DRAM Speed Setting on Related Registers

Register	EDO	FPG 6-3-3-3
50 [7:6]	XX	00, 01, 10 4T, 3T, 2T
50 [5]	X	0, 1 3T, 2T
52 [0]	X	X
53 [7]	X	1 1T
53 [2]	X	X
53 [1]	X	X
5B [3]	X	X
78 [7:6]	11 7-2-2-2	00, 10
78 [5:4]	11 7-2-2-2	00, 10
7A [1]	X	X
7C [1]	1 1T	X
7C [0]	1 1T	X

Table 8 SRAM Speed Setting on Related Registers

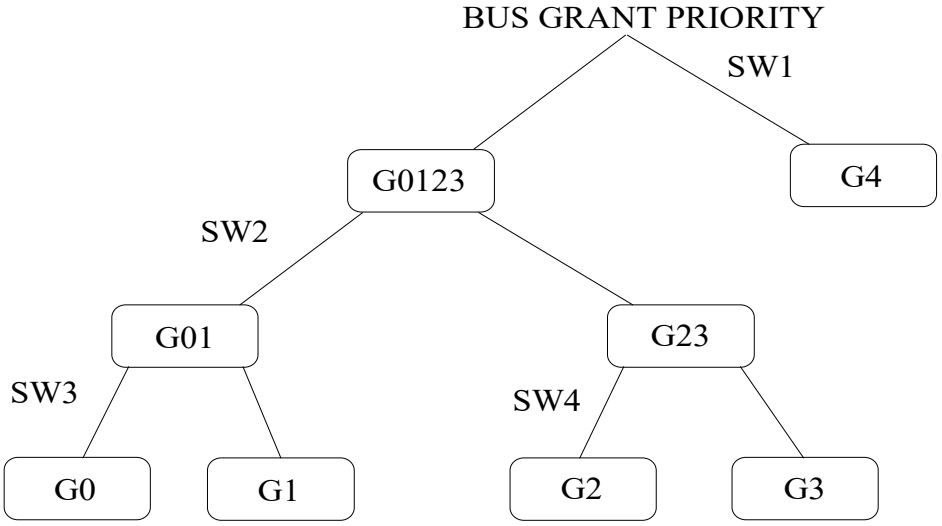
Register	Standard	Pipeline/Burst
52 [7:6]	01 4-X-X-X	01
52 [5:4]	10 2T	X1 1T
7F [7:6]	00	01, 10
7C [2]	X	0
7C [1]	X	X
7C [0]	X	0 2T

2.7 PCI Arbiter

The SiS5101 contains a high performance hidden arbitration scheme that allows efficient bus sharing among five PCI Masters and the CPU. Note that one PCI master is reserved for the PSIO chip. The SiS5101 employs the priority rotation scheme that is done at two different layers. The first layer is shared between PSIO and four PCI Masters as a group. The second layer consists of four PCI masters with equal priority. Arbitration is done at both layers. The winner of arbitration among the four PCI masters arbitrates the PCI bus against PSIO.

Fair rotation scheme applies only at layer level. The arbitration scheme assures that ISA master or DMA channels (represented by PSIO) access the bus with minimal latency. The PSIO is given a high level of priority to assure compatibility with traditional ISA expansion boards that require short bus latency. This implementation together with PCI Programmable Bursting Address Counter guarantees ISA device will not be starved during PCI master long bursting cycle. For example, When the maximum bursting length is 512 bytes, the maximum arbitration latency for PSIO, and PCI master is about 12us, and 40us respectively. The following two figures detail the rotation arbitration structure and its corresponding timing diagram.

Rotation Arbitration Scheme:



Notation:
SW1: is the switch for path from node G4 or G0123 to BUS GRANT PRIORITY
SW2: is the switch for path from node G01 or G23 to node G0123
SW3: is the switch for path from node G0 or G1 to node G01
SW4: is the switch for path from node G2 or G3 to node G23
G01, G23, G0123: are intermediate nodes
G4: is the bus request from PSIO
G0, G1, G2, G3: are the bus requests from PCI device 0, device 1, device 2, device 3 respectively.

Initial Path Parking:
SW1 : BUS GRANT PRIORITY-G4
SW2 : G0123-G01
SW3 : G01-G0
SW4 : G23-G2Rule of Rotating Priority for Bus Arbitration:

- BUS GRANT PRIORITY will choose a path whenever it encounters an optional path.
- PCI bus will be granted as Daisy Chain
- Path switches will be toggled from BUS GRANT PRIORITY to any request node (G4, G0, G1, G2, G3) if any of them have been utilized

Example:
Initial Priority:G4, G01, G0, G2

1. PSIO(G4) Request Bus
   SIOGNT# is asserted
   SW1 is toggled to G0123 (since it has been utilized)
   Priority change to G0, G1, G2, G3, G4

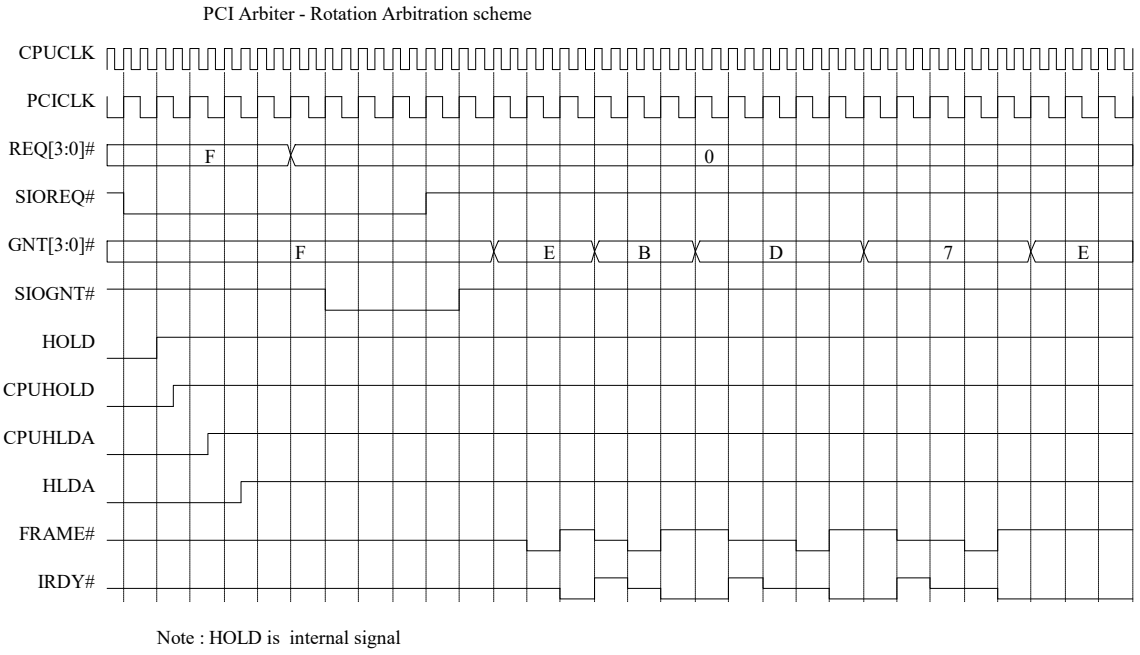
2. PSIO, REQ3, REQ2, REQ1, REQ0 are requesting bus
   GNT0# is asserted
   SW1, SW2 and SW3 are toggled to G4, G23 and G1 respectively (since they have been utilized)
   Priority change to G4, G2, G3, G1, G0

3. REQ3, REQ2, REQ1, REQ0 are active
   GNT2# is asserted
   SW2, SW4 are toggled to G01 and G3 respectively (since they have been utilized)
   Priority change to G4, G1, G0, G3, G2

4. REQ3, REQ2, REQ1, REQ0 are active
   GNT1# is asserted
   SW2, SW3 are toggled to G23 and G0 respectively (since they have been utilized)
   Priority change to G4, G3, G2, G0, G1

5. REQ3, REQ2, REQ1, REQ0 are active
   GNT3# is asserted
   SW2, SW4 are toggled to G01 and G2 respectively (since they have been utilized)
   Priority change to G4, G0, G1, G2, G3

6. During 3-5 if there is a request comes from PSIO, the Arbiter will grant bus to PSIO.



Note : HOLD is internal signal

A PCI master can burst so long as the target can source/sink the data, and no other agent requests the bus. However, PCI specifies two mechanisms that cap a master's tenure in the presence of other requests, so that predictable bus acquisition latency can be achieved. One is the Master Latency Timer(LT) that is not implemented into the PCMC, the other is the Target Initiated Termination. In the SiS5101, a Programmable Bursting Address Counter(PBAC) is implemented to disconnect the PCI master during the long bursting cycle. In this way, high throughput is maintained, and the bus latency is still kept reasonably small. Note that the bursting length is naturally applied to PCI master to local memory accessing. When PCI master accesses non-local memory target, the master and target should together have the responsibility of maintaining reasonable latency, but not the system arbiter does.

The PCI arbiter asserts only one GNT# at any time. The 5101 has also implemented a time-out counter to prevent faulty device hugging the bus. If the PCI bus is granted to a PCI device and the bus is currently idle, 16 PCI clocks is the limitation that device should assert FRAME# during the period of time. If time-out occurs, the arbiter will mask request line, therefore desserts GNT#. When this happens, all PCI devices start arbitration again. Note that PSIO is free to this constraint.

The 5101 PCI master will also mask the PSIO request to the arbiter if the PCI LOCK# is asserted to keep ISA master or DMA channels target latency within specification. The 5101 PCI arbiter is also allowed to force system back to CPU each time after SIOREQ# is serviced. This function is disabled by default, and can be enabled by set bit 7 of register 6F in the PCMC Configuration space.

2.8 PCI Bridge

2.8.1 PCI Master Controller

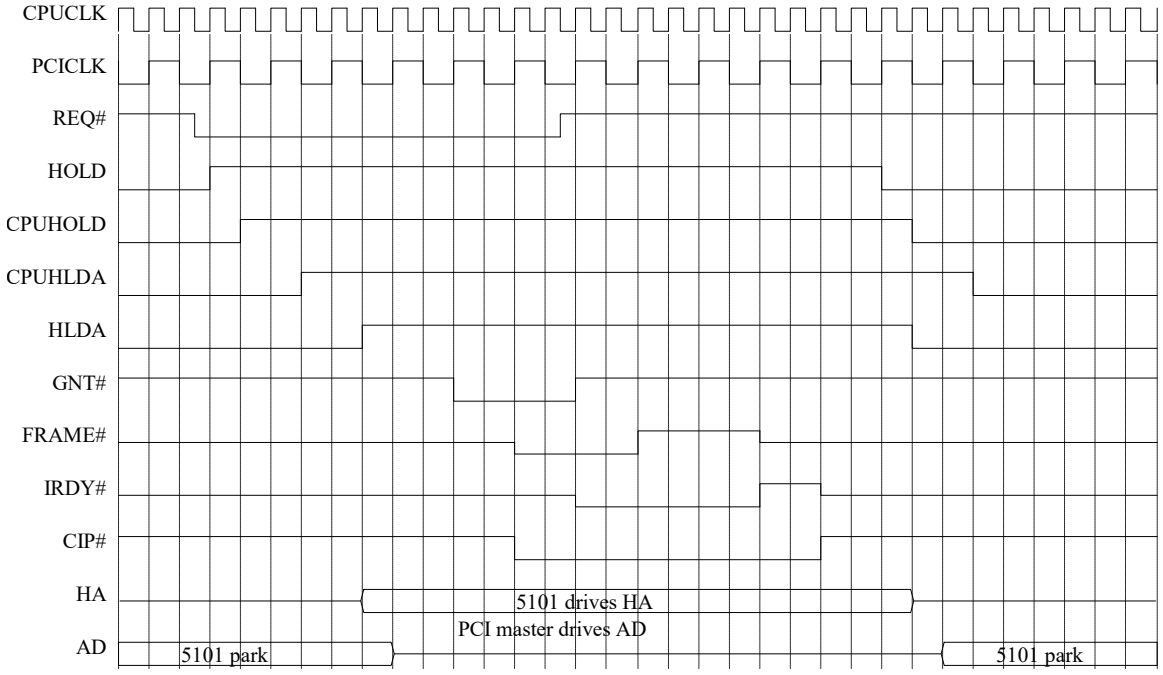
The PCI Master Controller forwards the CPU cycles not targeting the local memory to the PCI bus. In the case of a 64-bit CPU request or a misaligned 32-bit CPU request, the PCMC assumes the read assembly and write disassembly control. A 4 level posted write buffer (CTPPB) is implemented to improve the CPU to PCI memory write performance. Except for on-board memory write cycles, any cycles forwarded to the PCI bus will be suspended until the CTPPB is empty. For PCI bus memory write cycles, the CPU data are pushed into the CTPPB if it is not full. The pushed data are, at later time, written to the PCI bus. If the consecutive written data are in DW incremental sequence, they will be transferred to the PCI bus in a burst manner. The burst transfer rate is always X-2-2-2-... until 128 DWs are exhausted.

The PCI master interface can read data from or write data to the PCI bus at the utmost speed of 1 wait state. This is due to the fact that the PCMC drives the PCI bus address and the PLDB drives the PCI bus data. That necessitates a turn around cycle between the address and the data phases.

The PCMC provides a mechanism for converting standard I/O cycles on the CPU bus to Configuration cycles on the PCI bus. Configuration Mechanism #1 in PCI Specification 2.0 page 61 is used to do the cycle conversion.
The PCMC always intercepts the first interrupt acknowledge cycle from CPU bus, and forwards the second interrupt acknowledge cycle onto the PCI bus.

2.8.2 PCI Slave Controller

The SiS5101 operates as a slave on the PCI bus whenever a PCI master requests an access to the SiS5101 resource such as Cache, DRAM and the SiS5101 Internal registers. Note that the internal registers can only be accessed by the SiS5101 itself when in CPU cycle.
In the SiS5100 PCI/ISA system, the CPU is placed in HOLD state before granting the PCI bus to a PCI master. The following figure shows the behavior of CPUHOLD/CPUHLDA in response to PCI masters requests. Only linear ordered PCI cycles are supported by the PCMC PCI slave interface.



Note : HOLD,CIP# (current in progress) are internal signal

A PCI master to the local memory access is not conducted until the snoop cycle has completed.
The snoop cycle is used to inquire the first level cache to maintain coherency between first level and second level caches and main memory.

Snoop cycles are performed by driving the PCI master address onto the CPU bus and asserting EADS#. Depending on the status of HITM# two clocks after the assertion of EADS#, PCMC conducts the PCI master cycles as table 8 outlines.

A snoop filter is implemented to prevent the need of multiple inquires to the same line if the line was inquired previously. To support snoop filter, a Snoop Address Latch (SAL) and a Line Comparator are implemented. The line comparator is used to determine if the New Address (NA) is the same as the content of the SAL. If it is not, the NA is loaded into the SAL, and a snoop cycle is issued. In addition, a Valid bit in association with the SAL is used to ensure the snoop filtering is effective only when HLDA is asserted. The simplified filter algorithm is:

Table 9

PCI Master Read Cycle		
L1	L2	Data Transfer
Miss (or Unmodified)	Miss	Data transfer from DRAM to PCI
Miss (or Unmodified)	Hit (Dirty or !Dirty)	Data transfer from L2 to PCI
HitM	Miss	Data is first written back from L1 to DRAM. Then, PCI master gets data from DRAM.
HitM	Hit (Dirty or !Dirty)	Data is first written back from L1 to L2. Then, PCI master gets data from L2. The line is marked dirty in the L2.
PCI Master write Cycle		
L1	L2	Data Transfer
Miss (or Unmodified)	Miss	Data transfer from PCI to DRAM
Miss (or Unmodified)	Hit (Dirty or !Dirty)	Data transfer from PCI to DRAM and L2. The Dirty bit is not changed.
HitM	Miss	Data is first written back from L1 to DRAM. Then, PCI master writes data to DRAM.
HitM	Hit (Dirty or !Dirty)	Data is first written back from L1 to L2. Then, PCI master writes data to L2 and DRAM. The Line is marked dirty in the L2.

1) Write Back Mode

a) if NA=SAL in a PCI master write cycle, the PCMC only issues EADS#. It does not wait for the status of HITM#.

b) if NA=SAL in a PCI master read cycle, no snoop cycle nor EADS# is issued.

c) if NA≠SAL in a PCI master cycle, the PCMC issues a snoop cycle by EADS#, and then monitors the status of HITM#.

d) During a burst transaction, the PCMC automatically generates a snoop cycle when the address advances across a new line.

2) Write Through Mode

In the following two cases, the PCMC only generates EADS#. It ignores the logic of HITM#.

a) if NA=SAL in a PCI master write cycle, and

b) During a burst transaction, the address advances across a new line.

In the SiS5100, the INV signal of P54C should be connected to W/R# that is driven by the SiS5101 in the PCI master cycle. In this way, the SiS5101 can invalidate the line that is currently inquired via the assertion of EADS# in the PCI master write cycles.

The PCMC slave interface supports PCI burst transfers. A burst transfer will be disconnected (retry) if the transfer goes across the 512 bytes(or 1 KBytes selected by Register 5Dh, bit 5) address boundary. This is due to the fact that the address generator, to support the burst transfer, can only address 512 or 1K bytes. In this way, at most 32 cache lines can be uninterruptedly transferred if they are in I, S, or E state in the L1 cache.

Another reason for the constraint is that page miss may occur only once during the entire bursting transaction since the maximum bursting length is always within the page size in any of the used DRAM .

The PCI master writes are buffered in the one QW deep PCI to Memory posted write buffer (PTMPB). The PCMC always packs an aligned QW PCI write data into the write buffer, and then retires it into the DRAM array or the L2 cache. The PCI master write performance, to the utmost, is X-2-2-2- ...
The PCI master reads are through a QW read buffer with which the burst transfers can perform in the pace of X-2-2-2-... (from the L2 cache), or X-3-2-3-2-... (from the DRAMs).
Concurrent refresh will still be performed when CPU is put into Hold state. If the DRAM is idle, refresh can be conducted at any time. If refresh request occurs at the same time that a PCI master wants to access DRAM, an arbitration scheme is employed to resolve the conflict. The refresh request may thus get service while the PCI master accessing is suspended until refresh cycle is completed. Although refresh may win the DRAM bus, at most one refresh cycle may be conducted for each individual PCI transaction, i.e. for each Frame# initiating. On the other hand, refresh may be also deferred until the DRAM is idle. In SiS5100 system, the refresh may be postponed for no more than 24 us in the worst case when a PCI master is reading the whole 32 lines through one burst transaction.

2.8.3 PCI Bus Speed Setting

The following settings apply to all system environment, even though the system is running at 66MHz while the PCI bus is running at 33MHz.

Table 10 PCI bus setting

	Register	Setting	Unit
latency from ADS# to monitor local memory status	5Ch bit 7	2T	CPUCLK
CAS# pulse width in PCI master write cycle	5Ch bit 4	1T	PCICLK
latency from the disarming of "full" to the assertion of BRDY# for the pending CPU to PCI write cycle	5Ch bit 3	1T	CPUCLK
latency from reading L2/DRAM to the assertion of TRDY# in PCI master read cycles	5Dh bit 4	1T	PCICLK
latency from packing one Qword into PTMPB to the assertion of CAS#(or KWE#)	5Dh bit 3	1T	PCICLK
latency from TRDY# to BRDY# in CPU read/write PCI slave cycles	5Dh bit 2	2T	CPUCLK

2.8.4 Shadow Register

In order to support "suspend to HDD" function, all necessary shadow registers are implemented into 5103. For more detailed information, please refer to "5103 Register Description".

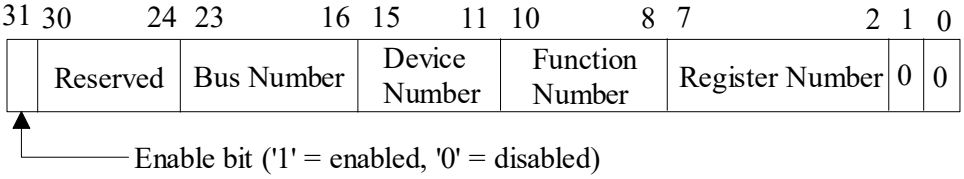
2.9 SiS5101 Configuration Registers

There are two sets of registers in the PCMC, I/O mapped registers and the PCI configuration space registers.

2.9.1 I/O Mapped Registers

The SiS5101 uses PCI configuration space access mechanism #1. This mechanism defines two registers, CONFIG_ADDRESS(CF8h) register and CONFIG_DATA(CFCh) register. Both CONFIG_ADDRESS and CONFIG_DATA are read/write registers, and the length is DWORD. The mechanism is to write a value into CONFIG_ADDRESS first, then read or write to CONFIG_DATA. The write to CONFIG_ADDRESS specifies the PCI bus, device on that bus, and the configuration register in that device being accessed. The read or write to CONFIG_DATA will cause the host bridge to translate the CONFIG_ADDRESS value to the requested configuration cycle.

The definition of CONFIG_ADDRESS register is described below:
Register 0CF8h CONFIG_ADDRESS Register



Bit 31 is an enable flag for determining if the accesses to CONFIG_DATA should be translated to configuration cycles on the PCI bus.

Bits 30:24 Reserved, read only, and must return 0's when read.

Bits 23:16 Choose a specific PCI bus in the system.

Bits 15:11 Choose a specific device on the bus.

Bits 10:8 Choose a specific function in a device.

Bits 7:2 Choose a DWORD in the device's configuration space.

Bits 1:0 read only and must return 0's when read.

A full Dword I/O write to address 0CF8h, the host bridge will load the data into CONFIG_ADDRESS register. Also, a full DWord I/O read to 0CF8h, the host bridge gets the data from CONFIG_ADDRESS register. Any non-Dword writes or reads to 0CF8h are treated as normal PCI I/O cycles. When the host bridge of SiS5101 sees an I/O access that falls inside the Dword beginning at CONFIG_DATA address, it checks the enable bit of the CONFIG_ADDRESS register. If bit 31 of CONFIG_ADDRESS register is 1, the I/O cycle is translated into a configuration cycle.

There are two types of configuration cycle determined by bus number. If the Bus Number is zero, the configuration cycle will be Type 0. If the Bus Number is non-zero, the configuration cycle will be Type 1.

For type 0 configuration cycle, AD[1:0] is driven to "00" during the address phase of the cycle. The host bridge decodes the device number of CONFIG_ADDRESS to assert only one "1" on the AD[31:11] and copies bits[10:2] of CONFIG_ADDRESS to AD[10:2] directly. For instance, when accessing the configuration registers of SiS5101, because SiS5101 is considered device 0 on bus 0, AD11 will be high, and bits[10:2] of CONFIG_ADDRESS are copied to AD[10:2] directly. Never use AD11 as the IDSEL line for any other PCI target device since it is reserved for PCMC. The SiS5101 responds to configuration by asserting DEVSEL#. For type 1 configuration cycle, AD[1:0] is driven to "01" and bits[31:2] of CONFIG_ADDRESS are copied to AD[31:2] directly during the address phase of the cycle. The byte-enables for the data phase of both types 0 and type 1 configuration cycles are copied from the HBE[7:4]# directly.

The following programming sequences is an example of writing register 51h in PCMC and of reading register 5Ch, 5Dh, 5Eh and 5Fh in PCMC.

write 51h:

```
MOV     EAX, 80000050h
OUT     0CF8h, EAX
MOV     AL, DATA
OUT     0CFDh, AL
```

read 5Ch, 5Dh, 5Eh and 5Fh:

```
MOV     EAX, 8000005Ch
OUT     0CF8h, EAX
IN      0CFCh
```

Register 0CF9h Turbo and Reset Control Register

Bits 7:5 Reserved

Bit 4 INIT Enable

When this bit is set to 1 ,the PCMC drives INIT during software reset. When this bit is cleared to 0, the PCMC drives CPURST during software reset, and INIT is inactive.

Bit 3 CPU BIST Enable.

When this bit is set to 1 and bit 4 as well as bit 1 are enabled, a subsequent initiation of the CPU hard reset through bit 2 of this register enables the Built In Self Test(BIST) mode of the CPU. The PCMC also drives the INIT during the hard reset.

Bit 2 **Reset CPU.**

There are two types of resets to the CPU: a hard reset using the CPURST signal and a soft reset using the INIT signal. If bit 1 of this register is set to 1 and bit 2 transitions from 0 to 1, the PCMC initiates a hard reset. A hard reset through this register thus requires two write operations to this register: the first write operation writes a 1 to bit 1 and a 0 to bit 2. The second write operation writes a 1 to bit 1 and a 1 to bit 2. When bit 1 of this register is 0 and bit 2 transitions from 0 to 1, the PCMC initiates a soft reset. The sequence to initiate a soft reset through this register is identical to that of a hard reset except a 0 is written to bit 1 in the first write operation.

Bit 1 **Enable System Hard Reset.**

When this bit is set to 1 and bit 2 transitions from 0 to 1, the PCMC initiates a hard reset to the CPU . When this bit is 0 and bit 2 transitions from 0 to 1, the PCMC initiates a soft reset to the CPU.

Bit 0 **Select Turbo /DeTurbo Mode**

There are two ways to enter Deturbo mode. One is through software; another is hardware.

- Software Deturbo: Set Reg. 5Bh bit 1 to 1, Reg. 65h bit 3 to 1, Reg. 78h bit 2 to 0 and pull GNT#3 high, then set Reg. CF9h bit 0 to 1.
- Hardware Deturbo: Set Reg. 5Bh bit 1 to 1, Reg. 65h bit 3 to 1, Reg. 78h bit 2 to 0 and pull GNT#3 high, then press deturbo switch.

2.9.2 PCI Configuration Space Mapped Registers

Register 00h Vendor ID - low byte

Bits 7:0 39h

Register 01h Vendor ID - high byte

Bits 7:0 10h

Register 02h Device ID - low byte

Bits 7:0 06h

Register 03h Device ID - high byte

Bits 7:0 04h

Register 04h Command - low byte

Bit 7 **Reserved**

Bit 6 **Respond to parity.**

This bit is always 0 since the PCMC does not support parity checking on the PCI bus

Bits 5:4 **Reserved**

Bit 3 **Enable special cycle.**

This bit is always 0 since the PCMC does not issue special cycle.

Bit 2 **Enable bus master.**

This bit is always 1, allowing the PCMC to serve as a PCI bus master.

Bit 1 **Enable response to memory access.**

0: Disables PCI master's accesses to local memory

1: Enables PCI master's accesses to local memory

Bit 0 **Enable response to I/O access.**

This bit is always 0 since the PCMC does not respond to any PCI I/O cycles. The PCMC only responds to CPU initiated I/O cycles.

Register 05h Command - high byte

Bits 7:0 **Reserved**

Register 06h Status - low byte

Bits 7:0 **Reserved**

Register 07h Status - high byte

Bit 7 **Detected parity error.**

This bit is always 0 since the PCMC does not support parity checking on the PCI bus.

Bit 6 **Signaled system error.**

This bit is set when the PCMC asserts SERR#. This bit is cleared by writing a 1 to it.

Bit 5 **Received master abort.**

This bit is set by the PCMC whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.

Bit 4 **Received target abort.**

This bit is set when a CPU to PCI transaction is terminated with target abort. This bit is cleared by writing a 1 to it.

Bit 3 **Signaled target abort.**

This bit is always 0 since the PCMC will not terminate a transaction with target abort.

Bits 2:1 **DEVSEL# Timing DEVT.**

The two bits define the timing to assert DEVSEL#. The PCMC asserts the DEVSEL# signal within three clocks after the assertion of FRAME#. The default value is DEVT=10. In fact, the PCMC always asserts DEVSEL# in medium timing except in CPU writes to I/O port 64h or 60h.

Bit 0 **Reserved**

Register 08h Revision Identification.

Bits 7:0 **00h.**

Register 0B~09h Class Code

Bits 23:0 **060000h**

Register 50h

Bits 7:6 **DRAM Read CAS Pulse Width**

00 : 4T

01 : 3T

10 : 2T

11 : Reserved

Bit 5 **DRAM Write CAS Pulse Width**

0 : 3T

1 : 2T

Bit 4 **Reserved**

Bit 3 **Reserved**

Bit 2 **Cache Toggle /Linear burst mode selection**

0: Toggle mode

1: Linear burst mode

Bits 1:0 DRAM type selection

00: 256k x N and 512K x N

01: 1M x N and 2M x N

10: 4M x N and 8M x N

11: 16M x N

Register 51h

Bit 7 L2 Cache Exist or not

0 : Not Exist

1 : Exist

Bit 6 L2 Cache Enable

0 : Disable

1 : Enable

Bit 5 Pipeline Burst SRAM / Burst SRAM Test Mode

0:Normal Mode

1:Test Mode

Like EDO test mode,BIOS writes a data into L2 cache,and then reads the data from cache at the same address.If BIOS can read the right data from cache by the end of T2,Burst SRAMs are detected, otherwise L2 cache is not Burst SRAM type.

The test-mode bit is set by BIOS before L2 cache auto-detection process.During the test mode,all the memory cycles are treated as L2 hit,and BRDY# is always asserted at the clock immediately after the asserted ADS#.

Bit 4 L2 Cache WT/WB Policy

0 : Write-Through mode

1 : Write-Back mode

Bits 3:1 L2 Cache Size

000 : 64KB

001 : 128KB

010 : 256KB

011 : 512KB

100 : 1MB

101 : 2MB

11x : Reserved

Bit 0 **CPU L1 Cache Write-Back Enable**

0 : Disable

1 : Enable

Register 52h

Bits 7:6 **Standard SRAM Cache speed (Read/Write)**

00 : 5-x-x-x Slower

01 : 4-x-x-x Faster

10 : 3-x-x-x Fastest

11 : Reserved

Bits 5:4 **Standard SRAM burst Timing.**

00 : 3T

x1 : 1T

10 : 2T

Note:It is recommended that set the Burst Timing to 1T for Pipelined Burst SRAM or Burst SRAM.

Bit 3 **Cache Interleave Enable**

0 : Disable

1 : Enable

Bit 2 **Burst SRAM Cache Burst Cycle**

0 : 4-x-x-x

1 : 3-x-x-x

Bit 1 **Cache Sizing Enable**

0: Normal Operation

1: Always Cache hit to enable Cache Sizing for BIOS

Bit 0 **Refresh RAS Active time**

0 : 6T

1 : 5T

Register 53h

Bit 7 **DRAM CAS precharge time**

0 : 2T

1 : 1T

Bit 6 **Shadow RAM Read Enable**

0 : Disable

1 : Enable

When this bit is enabled, the F segment is shadowed by default. Before shadowing, BIOS should not turn on the bit so that reading F segment is always forwarded to PCI bus.

Bit 5 **Shadow RAM Write Protection Enable**

0 : Disable

1 : Enable

After porting the shadowed segment into DRAM, this bit can be set so that the corresponding shadowed segment is not writable. Under such circumstances, the cycle which intends to write the segment is treated as non-local memory cycle, and is forwarded to PCI bus.

Bit 4 **Shadow RAM Enable for PCI Master Accesses**

0 : Disable

1 : Enable

Bit 3 **F0000h - FFFFFh Shadow RAM Cacheable**

0 : Non-Cacheable

1 : Cacheable

Note that only code is cacheable to L2/L1 when this bit is set.

Bit 2 **RAS to CAS delay time**

0 : 4T

1 : 3T

Bit 1 **RAS precharge time**

0 : 5T

1 : 4T

Bit 0 **Enable host to CTMPB push rate to be X-1-1-1**

0 : Enable

1 : Disable.

When this bit is disabled, the push rate is defined by bit [5:4] of register 52h.

Register 54h E Segment Setting

Bit 7 **E0000h - E3FFFh Shadow RAM Enable**

Bit 6 **E4000h - E7FFFh Shadow RAM Enable**

Bit 5 **E8000h - EBFFFh Shadow RAM Enable**

Bit 4 **EC000h - EFFFFh Shadow RAM Enable**

Bit 3 **E0000h - E3FFFh Shadow RAM Cacheable**

Bit 2 **E4000h - E7FFFh Shadow RAM Cacheable**

Bit 1 **E8000h - EBFFFh Shadow RAM Cacheable**

Bit 0 **EC000h - EFFFFh Shadow RAM Cacheable**

Register 55h D Segment Setting

Bit 7 **D0000h - D3FFFh Shadow RAM Enable**

Bit 6 **D4000h - D7FFFh Shadow RAM Enable**

Bit 5 **D8000h - DBFFFh Shadow RAM Enable**

Bit 4 **DC000h - DFFFFh Shadow RAM Enable**

Bit 3 **D0000h - D3FFFh Shadow RAM Cacheable**

Bit 2 **D4000h - D7FFFh Shadow RAM Cacheable**

Bit 1 **D8000h - DBFFFh Shadow RAM Cacheable**

Bit 0 **DC000h - DFFFFh Shadow RAM Cacheable**

Register 56h C Segment Setting

Bit 7 **C0000h - C3FFFh Shadow RAM Enable**

Bit 6 **C4000h - C7FFFh Shadow RAM Enable**

Bit 5 **C8000h - CBFFFh Shadow RAM Enable**

Bit 4 **CC000h - CFFFFh Shadow RAM Enable**

Bit 3 **C0000h - C3FFFh Shadow RAM Cacheable**

Bit 2 **C4000h - C7FFFh Shadow RAM Cacheable**

Bit 1 **C8000h - CBFFFh Shadow RAM Cacheable**

Bit 0 **CC000h - CFFFFh Shadow RAM Cacheable**

Register 57h

Bit 7 **Allocation of Non-cacheable Area #1**

0 : Local DRAM

1 : AT Bus. The local DRAM is disabled.

Bit 6 **Non-cacheable Area #1 Enable**

0 : Disable

1 : Enable

Bits 5:3 **Size of Non-Cacheable Area #1 (within 128 MBytes)**

000 : 64KB

001 : 128KB

010 : 256KB

011 : 512KB

100 : 1MB

101 : 2MB

110 : 4MB

111 : 8MB

Bits 2:0 **A26 ~ A24 of Non-Cacheable Area #1 (within 128MBytes)**

Register 58h

Bits 7:0 **A23 ~ A16 of Non-Cacheable Area #1 (within 128MBytes)**

Register 59h

Bit 7 **Allocation of Non-cacheable Area #2**

0 : Local DRAM

1 : AT Bus. The local DRAM is disabled.

Bit 6 **Non-cacheable Area #2 Enable**

0 : Disable

1 : Enable

Bits 5:3 **Size of Non-Cacheable Area #2 (within 128MBytes)**

000 : 64KB

001 : 128KB

010 : 256KB

011 : 512KB

100 : 1MB

101 : 2MB

110 : 4MB

111 : 8MB

Bits 2:0 A26 ~ A24 of Non-Cacheable Area #2 (within 128MBytes)

Register 5Ah

Bits 7:0 A23 ~ A16 of Non-Cacheable Area #2 (within 128MBytes)

Register 5Bh

Bit 7 Fast Gate A20 Emulation Enable

0 : Disable

1 : Enable

The sequence to generate A20M# is: write D1h to I/O port 64h followed by I/O write to port 60h with data 00h. When this bit is enabled, the SiS5101 responds the cycle by asserting DEVSEL# in slowest timing. Otherwise, the cycle is subtractively decoded by SiS 5103, and then is passed to 8042 on the ISA bus.

Bit 6 Fast Reset Emulation Enable

0 : Disable

1 : Enable

The Fast reset command is I/O write to port 64h with data 1111XXX0b.

After the command is issued, the assertion of INIT or CPURST is delayed by 2us or 6us which can be programmed in bit 5, and is held for 25 CPUCLK.

Bit 5 Fast Reset Latency Control

0 : 2us

1 : 6us

Bit 4 Slow Refresh Enable (1:4)

0 : Normal Refresh

1 : Slow Refresh

Bit 3 DRAM Write Push to CAS delay

0 : 2T

1 : 1T

Bit 2:1 Reserved

Bit 0 CAS Driving Current Control Bit 0 (Please refer to Reg. 5Eh Bit 0 for details)

Register 5Ch

Bit 7 **Latency from ADS# to Monitor Local Memory Status**

0 : 3T

1 : 2T

Depending on the setting of this bit, the PCI master bridge in the SiS5101 may monitor the local memory status from the inside local memory decoder either by the end of T2 or T3. If the CPU initiates a PCI cycle, it is determined to be converted to PCI side from this point. Specifically, BRDY# is always returned to CPU one CPUCLK later if the CTPPB is not full, for post memory write cycles. Thus, this bit also affects the CPU to PCI Post write speed. When it is set to 0, the Post write rate is 5T for each double word. When it is set to 1, the rate is 4T per double word. For a Qword PCI memory write, the post write rate is 7T(bit7=1), or 8T(bit7=0).

Bit 6 **Enable Refresh Cycle when CPU is hold**

0 : Disable

1 : Enable

Bit 5 **Enable Snoop Filter**

0 : Disable

1 : Enable

Bit 4 **CAS# Pulse Width in PCI master write cycle**

0 : 1T

1 : 2T

Bit 3 **Latency from the disarming of "Full" to the assertion of BRDY# for the pending CPU to PCI write cycle**

0 : 1T

1 : 2T

Bit 2 **Selection of KWE# synchronization**

0 : KWE# is synchronized with ACLK (Recommended)

1 : KWE# is synchronized with CPUCLK

Bit 1 **L2 Tag Length**

0 : 8 bits

1 : 7 bits

Bit 0

0: Enable parity error detection (default value)

1: Disable parity error detection

Register 5Dh PCI Control Register

Bits 7:6 PCI Clock Frequency Selection

00 : PCICLK=CPUCLK/2

01 : PCICLK=CPUCLK/1.5

10 : Reserved

11 : PCICLK=14MHz

Bit 5 Maximum Burstable Address Range in PCI master cycles

0 : 512 Bytes

1 : 1 KBytes

This bit defines the maximum bursting length for each FRAME# asserting.

Bit 4 Latency from Reading L2/DRAM to the assertion of TRDY# in PCI master read cycles

0 : 1T

1 : 2T

Bit 3 Latency from Packing one Qword into PTMPB to the assertion of CAS#(or KWE#)

0 : 1T

1 : 2T

This latency is reserved for the Post write data propagating onto MD bus, and also for the parity generation so that minimum set up time for MD data to CAS# will not be violated.

Bit 2 Latency from TRDY# to BRDY# in CPU read/write PCI slave cycles

0 : 2 CPUCLKs

1 : 3 CPUCLKs

Bit 1 CPU-to-PCI burst memory write Enable

0 : Disable

1 : Enable

Bit 0 CPU-to-PCI post memory write Enable

0 : Disable

1 : Enable

Register 5Eh

Bits 7:1 Reserved

Bit 0 **CAS Driving Current Control Bit 1**

Register 5B bit 0 and 5E bit 0 are used to control CAS driving current.

Register 5B bit 0	Register 5E bit 0	Minimum Current
0	0	8mA (default)
1	0	4mA
0	1	12mA
1	1	8mA

Register 5Fh Reserved

Register 60h

Bit 7:3 **Reserved**

Bit 2 **Pin 138 Input Function**

0: Disable
1: Enable

Bit 1:0 **Reserved**

Register 61h Reserved

Register 62h Reserved

Register 63h Reserved

Register 64h SMRAM mapping address.

Bits 7:0 **Correspond to Host address A[27:20].**

This register together with register 65h define SMRAM location. SMRAM location can either be set to a non-shadow, non-cacheable location by selecting E segment as defined in register 65h or be implemented through logical address remap scheme. Logical address remap is done through comparing the upper 11 bits of access address with the address bits defined in register 64h and 65h. If addresses are compared equal and SRAM area selection has been set to either A or B segment, then access is remapped into an A or B segment access. The SMRAM mapping address should be set up by BIOS during the POST process and the SMI service routine is also moved into the SMRAM area during this process. When the system is in the SMM mode or the SMRAM access control bit is enabled, any access to SMRAM area will be redirected as defined by these two registers.

Note: The SMRAM mapping address defines 1MB granularity and the logical address must not set to the first 1MB memory area.

Register 65h

Bits 7:5 SMRAM area selection

000 : E0000h-E7FFFh

100 : A0000h-A7FFFh

010 : A0000h-AFFFFh

110 : B0000h-B7FFFh

001 : B0000h-BFFFFh

others : reserved

The SMRAM area is non-cacheable, and non-shadowed.

E0000h-E7FFFh is a physical and logical address space. The other selections can be used to relocate the SMRAM from the pre-defined area (as defined in registers 64h and 65h) during SMM.

Bit 4 SMRAM access control

1: When set, the SMRAM area can be used. This bit can be set whenever it is necessary to access the SMRAM area. It is cleared after the access is finished.

0: The SMRAM area can only be accessed during the SMI handler.

Bit 3 Reserved

Bits 2:0 Bits 2-0 correspond to Host Address A[30:28].

Register 66h

Bits 7:1 Reserved

Bit 0 CPU reset for Suspend Wakeup enable

0 : Disable

1 : Enable

Register 67h

Bits 7:0

Bits 7:0 define the programmable 10-bit I/O port address bits A[9:2].

Register 68h

Bits 7:2 Reserved

Bit 1 Pin 138 SMI Function

0 : Disable

1 : Enable

Bit 0 **Reserved**

Register 69h **Reserved**

Register 6Ah **Reserved**

Register 6Bh **Reserved**

Register 6Ch **Reserved**

Register 6Dh **Reserved**

Register 6Eh **Reserved**

Register 6Fh

Bit 7 **Return Bus to CPU after SIOREQ# is Serviced**

0 : Disable

1 : Enable

Bits 6:0 **Reserved**

Register 70h ~ 73h **DRAM Boundary**

Each register records the accumulated DRAM size including the present and previous banks.

Bits 7:0 **DRAM Bank Boundary Address A[28:21]**

00h: 0Mbyte

01h: 2Mbyte

02h: 4Mbyte

04h: 8Mbyte

Note: Please refer to "2.6 DRAM Controller" for detailed information.

Register 74h~77h Reserved

Register 78h

Bits 7:6 **EDO BRDY# Timing Selection**

00,10: no EDO DRAM

01: BRDY# Sync. 1T timing (For 6-2-2-2)

11: BRDY# Sync. 2T timing (For 7-2-2-2)

Bits 5:4 EDO MDLE to 5102 Timing Selection

00,10: no EDO DRAM

01: MDLE type 1 timing (For 6-2-2-2)

11: MDLE type 2 timing (For 7-2-2-2)

Bit 3 Reserved

Bit 2 Reserved

Bit 1 Reserved

Bit 0 Reserved

Register 79h Reserved

Register 7Ah

Bit 7 M1 SMAC access

It must be set whenever the M1 CCR1 bit 2 is set and cleared if CCR1 bit 3 is cleared.

Bit 6 M1 MMAC access

If set, access to address within SMM space is conducted to main memory instead of SMM area. It must be set whenever the M1 CCR1 bit 3 is set and cleared if CCR1 bit 3 is cleared.

In the M1's specification, the SMIACT will be de-asserted when MMAC is set and re-asserted after it is cleared. This allows the SMI service routine to access normal memory area instead of SMM memory area.

Bit 5 M1 CPU

It should be set if the current CPU is M1.

Bits 4:3 Reserved

Bit 2 Reserved

Bit 1 RAS Precharge Time

0: Depend on the setting of register 53h bit 1

1: 3T

Bit 0 Reserved And Should be Written With 1

Register 7Bh

Bit 7 **AD[31:0] output current selection**

0: 50mA/2.2V (default value)

1: 95mA/2.2V

Bit 6 **FRAME#, IRDY#, TRDY#, DEVSEL#, C/BE[3:0]# output current selection**

0: 50mA/2.2V (default value)

1: 95mA/2.2V

Bit 5 **GNT[3:0]#, PAR, SERR# output current selection**

0: 50mA/2.2V (default value)

1: 95mA/2.2V

Bits 4:0 **Reserved**

Register 7Ch

Bits 7:2 **Reserved**

Bit 1 **Access EDO DRAM CAS# Precharge Time**

0: 2T

1: 1T

Bit 0 **Access EDO DRAM CAS# Pulse Width**

0: 2T

1: 1T

Note: It is recommended that set the CAS# pulse width to be 2T and pre-charge time to be 1T.

Register 7Eh

Bits 7:4 **Reserved**

Bit 3 **Setting Bank 3 Standard/EDO type DRAM**

0: Standard DRAM

1: EDO type DRAM

Bit 2 **Setting Bank 2 Standard/EDO type DRAM**

0: Standard DRAM

1: EDO type DRAM

Bit 1 **Setting Bank 1 Standard/EDO type DRAM**

0: Standard DRAM

1: EDO type DRAM

Bit 0 **Setting Bank 0 Standard/EDO type DRAM**

0: Standard DRAM

1: EDO type DRAM

Register 7Fh

Bits 7:6 **SRAM Type**

00:Standard SRAM

01:Burst SRAM

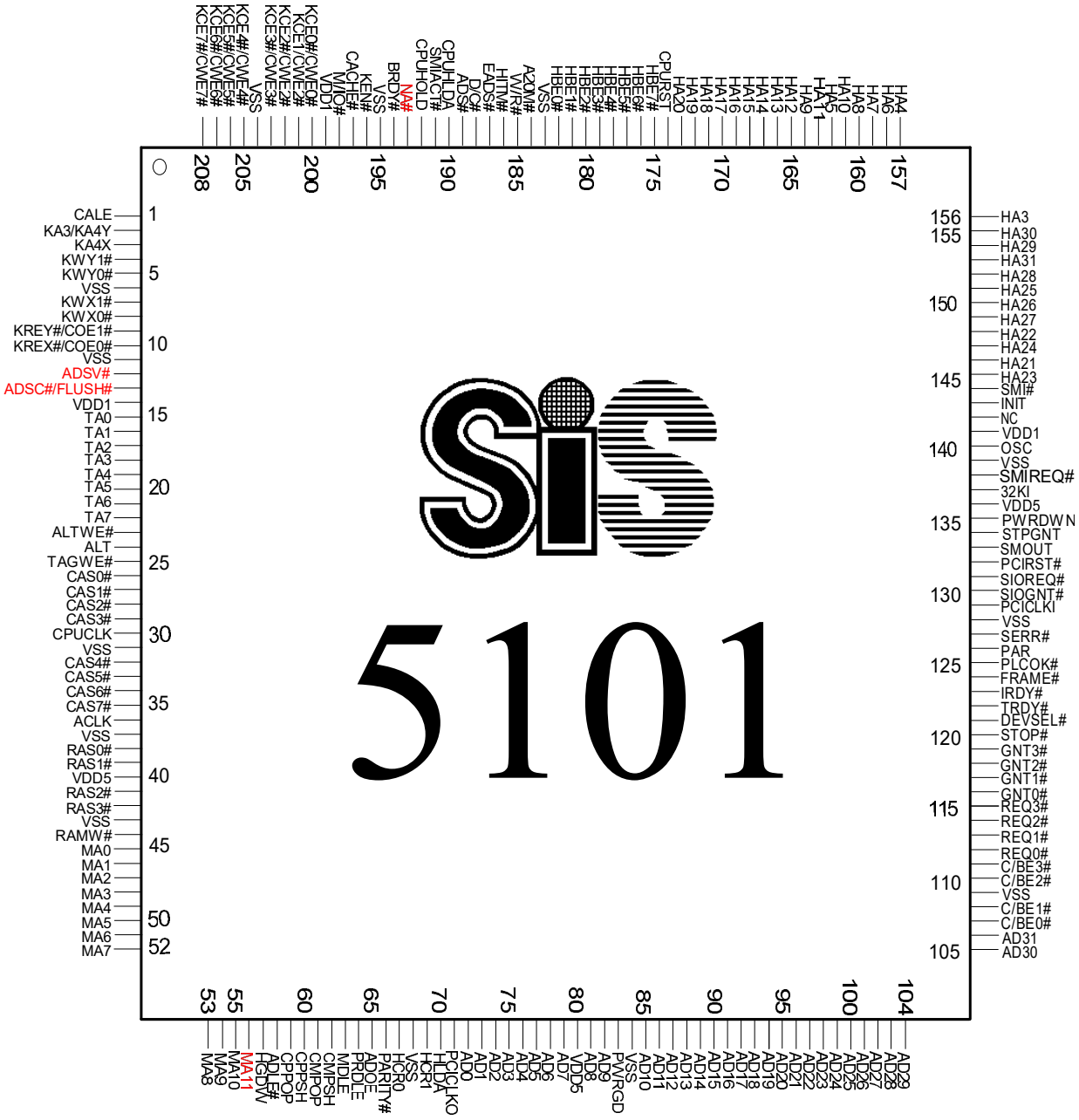
10:Pipeline Burst SRAM

11:Reserved

Bits 5:0 **Reserved**

2.10 Pin Assignment and Description

2.10.1 SiS5101 Pin Assignment



2.10.2 SiS5101 Pin Listing

1 =CALE	B	53=MA8	A	105=AD30	A	157=HA4	B
2=KA3/KA4Y	B	54=MA9	A	106=AD31	A	158=HA6	B
3=KA4X	B	55=MA10	A	107=C/BE0#	A	159=HA7	B
4=KWY1#	B	56=MA11	A	108=C/BE1#	A	160=HA8	B
5=KWY0#	B	57=HGDW	A	109=VSS		161=HA10	B
6=VSS	B	58=ADLE#	A	110=C/BE2#	A	162=HA5	B
7=KWX1#	B	59=CPPOP	A	111=C/BE3#	A	163=HA11	B
8=KWX0#	B	60=CPPSH	A	112=REQ0#	A	164=HA9	B
9=KREY#/COE1#	B	61=CMPOP	A	113=REQ1#	A	165=HA12	B
10=KREX#/COE0#	B	62=CMPSH	A	114=REQ2#	A	166=HA13	B
11=VSS		63=MDLE	A	115=REQ3#	A	167=HA14	B
12=ADSV#	B	64=PRDLE	A	116=GNT0#	A	168=HA15	B
13=ADSC#/FLUSH#	B	65=ADOE	A	117=GNT1#	A	169=HA16	B
14=VDD1	B	66=PARITY#	A	118=GNT2#	A	170=HA17	B
15=TA0	A	67=HCR0	A	119=GNT3#	A	171=HA18	B
16=TA1	A	68=VSS		120=STOP#	A	172=HA19	B
17=TA2	A	69=HCR1	A	121=DEVSEL#	A	173=HA20	B
18=TA3	A	70=HLDA	A	122=TRDY#	A	174=CPURST	B
19=TA4	A	71=PCICLKO	A	123=IRDY#	A	175=HBE7#	B
20=TA5	A	72=AD0	A	124=FRAME#	A	176=HBE6#	B
21=TA6	A	73=AD1	A	125=PLOCK#	A	177=HBE5#	B
22=TA7	A	74=AD2	A	126=PAR	A	178=HBE4#	B
23=ALTWE#	A	75=AD3	A	127=SERR#	A	179=HBE3#	B
24=ALT	A	76=AD4	A	128=VSS		180=HBE2#	B
25=TAGWE#	A	77=AD5	A	129=PCICLKI	A	181=HBE1#	B
26=CAS0#	A	78=AD6	A	130=SIOGNT#	A	182=HBE0#	B
27=CAS1#	A	79=AD7	A	131=SIOREQ#	A	183=VSS	
28=CAS2#	A	80=VDD5	A	132=PCIRST#	A	184=A20M#	B
29=CAS3#	A	81=AD8	A	133=SMOUT	A	185=W/R#	B
30=CPUCLK	A	82=AD9	A	134=STPGNT	A	186=HITM#	B
31=VSS		83=PWRGD	A	135=PWRDWN	A	187=EADS#	B
32=CAS4#	A	84=VSS		136=VDD5	A	188=D/C#	B
33=CAS5#	A	85=AD10	A	137=32KI	A	189=ADS#	B
34=CAS6#	A	86=AD11	A	138=SMIREQ#	A	190=CPUHLDA	B
35=CAS7#	A	87=AD12	A	139=VSS		191=SMIACT#	B
36=ACLK	A	88=AD13	A	140=OSC	A	192=CPUHOLD	B
37=VSS		89=AD14	A	141=VDD1	B	193=NA#	B
38=RAS0#	A	90=AD15	A	142=NC	A	194=BRDY#	B
39=RAS1#	A	91=AD16	A	143=INIT	B	195=VSS	
40=VDD5	A	92=AD17	A	144=SMI#	B	196=KEN#	B
41=RAS2#	A	93=AD18	A	145=HA23	B	197=CACHE#	B
42=RAS3#	A	94=AD19	A	146=HA21	B	198=M/IO#	B
43=VSS		95=AD20	A	147=HA24	B	199=VDD1	B
44=RAMW#	A	96=AD21	A	148=HA22	B	200=KCE0#/CWE0#	B
45=MA0	A	97=AD22	A	149=HA27	B	201=KCE1#/CWE1#	B
46=MA1	A	98=AD23	A	150=HA26	B	202=KCE2#/CWE2#	B
47=MA2	A	99=AD24	A	151=HA25	B	203=KCE3#/CWE3#	B
48=MA3	A	100=AD25	A	152=HA28	B	204=VSS	
49=MA4	A	101=AD26	A	153=HA31	B	205=KCE4#/CWE4#	B
50=MA5	A	102=AD27	A	154=HA29	B	206=KCE5#/CWE5#	B
51=MA6	A	103=AD28	A	155=HA30	B	207=KCE6#/CWE6#	B
52=MA7	A	104=AD29	A	156=HA3	B	208=KCE7#/CWE7#	B

Remark : "A"=Power Group A, "B"=Power Group B

SiS5101 Suspend State

L:Output Force Low , IH:Chipset Internal Gate to High,
OT:Output Tri-State, X:Users don't need to take care of anything.

1 =CALE	L	53=MA8	L	105=AD30	L	157=HA4	L
2=KA3/KA4Y	L	54=MA9	L	106=AD31	L	158=HA6	L
3=KA4X	L	55=MA10	L	107=C/BE0#	L	159=HA7	L
4=KWY1#	L	56=MA11	L	108=C/BE1#	L	160=HA8	L
5=KWY0#	L	57=HGDW	L	109=VSS		161=HA10	L
6=VSS		58=ADLE#	L	110=C/BE2#	L	162=HA5	L
7=KWX1#	L	59=CPPOP	L	111=C/BE3#	L	163=HA11	L
8=KWX0#	L	60=CPPSH	L	112=REQ0#	IH	164=HA9	L
9=KREY#/COE1#	L	61=CMPOP	L	113=REQ1#	IH	165=HA12	L
10=KREX#/COE0#	L	62=CMPSH	L	114=REQ2#	IH	166=HA13	L
11=VSS		63=MDLE	L	115=REQ3#	IH	167=HA14	L
12=ADSV#	L	64=PRDLE	L	116=GNT0#	L	168=HA15	L
13=ADSC#/FLUSH#	L	65=ADOE	L	117=GNT1#	L	169=HA16	L
14=VDD1	L	66=PARITY#	L/IH	118=GNT2#	L	170=HA17	L
15=TA0	L	67=HCR0	AL	119=GNT3#	L	171=HA18	L
16=TA1	L	68=VSS		120=STOP#	L/IH	172=HA19	L
17=TA2	L	69=HCR1	L	121=DEVSEL#	L/IH	173=HA20	L
18=TA3	L	70=HLDA	L	122=TRDY#	L/IH	174=CPURST	L
19=TA4	L	71=PCICLKO	L	123=IRDY#	L/IH	175=HBE7#	X
20=TA5	L	72=AD0	L	124=FRAME#	L/IH	176=HBE6#	X
21=TA6	L	73=AD1	L	125=PLOCK#	IH	177=HBE5#	X
22=TA7	L	74=AD2	L	126=PAR	L	178=HBE4#	X
23=ALTWE#	L	75=AD3	L	127=SERR#	L	179=HBE3#	X
24=ALT	L	76=AD4	L	128=VSS		180=HBE2#	X
25=TAGWE#	L	77=AD5	L	129=PCICLKI	X	181=HBE1#	X
26=CAS0#	X	78=AD6	L	130=SIOGNT#	X	182=HBE0#	X
27=CAS1#	X	79=AD7	L	131=SIOREQ#	X	183=VSS	
28=CAS2#	X	80=VDD5		132=PCIRST#	L	184=A20M#	L
29=CAS3#	X	81=AD8	L	133=SMOUT	L	185=W/R#	L
30=CPUCLK	X	82=AD9	L	134=STPGNT	X	186=HITM#	IH
31=VSS		83=PWRGD	X	135=PWRDWN	X	187=EADS#	L
32=CAS4#	X	84=VSS		136=VDD5		188=D/C#	X
33=CAS5#	X	85=AD10	L	137=32KI	X	189=ADS#	IH
34=CAS6#	X	86=AD11	L	138=SMIREQ#	IH	190=CPUHLDA	IL
35=CAS7#	X	87=AD12	L	139=VSS		191=SMIACT#	IH
36=ACLK	X	88=AD13	L	140=OSC	X	192=CPUHOLD	L
37=VSS		89=AD14	L	141=VDD1		193=NA#	L
38=RAS0#	X	90=AD15	L	142=NC	X	194=BRDY#	L
39=RAS1#	X	91=AD16	L	143=INIT	L	195=VSS	
40=VDD5	X	92=AD17	L	144=SMI#	L	196=KEN#	L
41=RAS2#	X	93=AD18	L	145=HA23	L	197=CACHE#	IH
42=RAS3#	X	94=AD19	L	146=HA21	L	198=M/IO#	X
43=VSS		95=AD20	L	147=HA24	L	199=VDD1	
44=RAMW#	L	96=AD21	L	148=HA22	L	200=KCE0#/CWE0#	L
45=MA0	L	97=AD22	L	149=HA27	L	201=KCE1#/CWE1#	L
46=MA1	L	98=AD23	L	150=HA26	L	202=KCE2#/CWE2#	L
47=MA2	L	99=AD24	L	151=HA25	L	203=KCE3#/CWE3#	L
48=MA3	L	100=AD25	L	152=HA28	L	204=VSS	
49=MA4	L	101=AD26	L	153=HA31	L	205=KCE4#/CWE4#	L
50=MA5	L	102=AD27	L	154=HA29	L	206=KCE5#/CWE5#	L
51=MA6	L	103=AD28	L	155=HA30	L	207=KCE6#/CWE6#	L
52=MA7	L	104=AD29	L	156=HA3	L	208=KCE7#/CWE7#	L

SiS5101 Output & I/O Signal States During Hard Reset

L: Low , H: High, Z: Tri-State , X: Don't Care

1 =CALE	H	53=MA8	H	105=AD30	H	157=HA4	Z
2=KA3/KA4Y	H	54=MA9	H	106=AD31	H	158=HA6	Z
3=KA4X	H	55=MA10	H	107=C/BE0#	H	159=HA7	Z
4=KWY1#	H	56=MA11	H	108=C/BE1#	H	160=HA8	Z
5=KWY0#	H	57=HGDW	H	109=VSS		161=HA10	Z
6=VSS		58=ADLE#	H	110=C/BE2#	H	162=HA5	Z
7=KWX1#	H	59=CPPOP	L	111=C/BE3#	H	163=HA11	Z
8=KWX0#	H	60=CPPSH	L	112=REQ0#		164=HA9	Z
9=KREY#/COE1#	H	61=CMPOP	L	113=REQ1#		165=HA12	Z
10=KREX#/COE0#	H	62=CMPSH	L	114=REQ2#		166=HA13	Z
11=VSS		63=MDLE	L	115=REQ3#		167=HA14	Z
12=ADSV#	X	64=PRDLE	L	116=GNT0#	H	168=HA15	Z
13=ADSC#/FLUSH#	X	65=ADOE	L	117=GNT1#	H	169=HA16	Z
14=VDD1		66=PARITY#		118=GNT2#	H	170=HA17	Z
15=TA0	Z	67=HCR0	L	119=GNT3#	H	171=HA18	Z
16=TA1	Z	68=VSS		120=STOP#	Z	172=HA19	Z
17=TA2	Z	69=HCR1	L	121=DEVSEL#	Z	173=HA20	Z
18=TA3	Z	70=HLDA	L	122=TRDY#	Z	174=CPURST	H
19=TA4	Z	71=PCICLKO	X	123=IRDY#	Z	175=HBE7#	
20=TA5	Z	72=AD0	H	124=FRAME#	Z	176=HBE6#	
21=TA6	Z	73=AD1	H	125=PLOCK#	Z	177=HBE5#	
22=TA7	Z	74=AD2	H	126=PAR	L	178=HBE4#	
23=ALTWE#	H	75=AD3	H	127=SERR#	Z	179=HBE3#	
24=ALT	Z	76=AD4	H	128=VSS		180=HBE2#	
25=TAGWE#	H	77=AD5	H	129=PCICLKI		181=HBE1#	
26=CAS0#	H	78=AD6	H	130=SIOGNT#	H	182=HBE0#	
27=CAS1#	H	79=AD7	H	131=SIOREQ#		183=VSS	
28=CAS2#	H	80=VDD5		132=PCIRST#	H	184=A20M#	H
29=CAS3#	H	81=AD8	H	133=SMOUT	X	185=W/R#	Z
30=CPUCLK		82=AD9	H	134=STPGNT	X	186=HITM#	
31=VSS		83=PWRGD		135=PWRDWN		187=EADS#	H
32=CAS4#	H	84=VSS		136=VDD5		188=D/C#	
33=CAS5#	H	85=AD10	H	137=32KI		189=ADS#	
34=CAS6#	H	86=AD11	H	138=SMIREQ#		190=CPUHLDA	
35=CAS7#	H	87=AD12	H	139=VSS		191=SMIACT#	
36=ACLK		88=AD13	H	140=OSC		192=CPUHOLD	L
37=VSS		89=AD14	H	141=VDD1		193=NA#	H
38=RAS0#	H	90=AD15	H	142=NC		194=BRDY#	L
39=RAS1#	H	91=AD16	H	143=INIT	L	195=VSS	
40=VDD5		92=AD17	H	144=SMI#	H	196=KEN#	L
41=RAS2#	H	93=AD18	H	145=HA23	Z	197=CACHE#	
42=RAS3#	H	94=AD19	H	146=HA21	Z	198=M/IO#	
43=VSS		95=AD20	H	147=HA24	Z	199=VDD1	
44=RAMW#	H	96=AD21	H	148=HA22	Z	200=KCE0#/CWE0#	H
45=MA0	H	97=AD22	H	149=HA27	Z	201=KCE1#/CWE1#	H
46=MA1	H	98=AD23	H	150=HA26	Z	202=KCE2#/CWE2#	H
47=MA2	H	99=AD24	H	151=HA25	Z	203=KCE3#/CWE3#	H
48=MA3	H	100=AD25	H	152=HA28	Z	204=VSS	
49=MA4	H	101=AD26	H	153=HA31	Z	205=KCE4#/CWE4#	H
50=MA5	H	102=AD27	H	154=HA29	Z	206=KCE5#/CWE5#	H
51=MA6	H	103=AD28	H	155=HA30	Z	207=KCE6#/CWE6#	H
52=MA7	H	104=AD29	H	156=HA3	Z	208=KCE7#/CWE7#	H

2.10.3 SiS5101 Pin Description

Host Interface

Pin No.	Symbol	Type	Function
145-173	HA[31:3]	I/O	The CPU Address is driven by the CPU during CPU bus cycles. The 5101 forwards it to either the DRAM or the PCI bus depending on the address range. The address bus is driven by the 5101 during bus master cycles.
175-182	HBE[7:0]#	I	CPU Byte Enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. HBE7# indicates that the most significant byte of the data bus is valid while HBE0# indicates that the least significant byte of the data bus is valid.
189	ADS#	I	Address Status is driven by the CPU to indicate the start of a CPU bus cycle.
198	M/IO#	I	Memory I/O definition is an input to indicate an I/O cycle when low, or a memory cycle when high.
185	W/R#	I/O	Write/Read from the CPU indicates whether the current cycle is a write or read access. It is an output during the PCI master cycles.
188	D/C#	I	Data/Code is used to indicate whether the current cycle is a data or code access.
194	BRDY#	O	Burst Ready indicates that data presented are valid during a burst cycle.
192	CPUHOLD	O	CPU Hold Request is used to request the control of the CPU bus. CPUHLDA will be asserted by the CPU after completing the current bus cycle.
190	CPUHLDA	I	CPU Hold Acknowledge comes from the CPU in response to a CPUHOLD request. It is active high and remains driven during bus hold period. CPUHLDA indicates that the CPU has given the bus to another bus master.
186	HITM#	I	Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of the CPU.
184	A20M#	O	A20 Mask is the fast A20GATE output to the CPU. It remains high during power up and CPU reset period. It forces A20 to go low when active.

196	KEN#	O	The CPU Cache Enable pin is used when the current cycle is cacheable to the L1 cache of the CPU. It is an active low signal asserted by the 5101 during cacheable cycles.
197	CACHE#	I	The Cache pin indicates an internally cacheable read cycle or a burst write-back cycle. If this pin is driven inactive during a read cycle, the CPU will not cache the returned data, regardless of the state of the KEN# pin.
187	EADS#	O	The EADS# is driven to indicate that a valid external address has been driven to the CPU address pins to be used for an inquire cycle.
174	CPURST	O	Reset CPU is an active high output to reset the CPU.
143	INIT	O	The Initialization output forces the CPU to begin execution in a known state. The CPU state after INIT is the same as the state after CPURST except that the internal caches, model specific registers, and floating point registers retain the values they had prior to INIT.
144	SMI#	O	System Management Interrupt is used to indicate the occurrence of system management events. It is connected directly to the CPU SMI# input.
191	SMIACT#	I	The SMIACT# pin is used as the SMI acknowledgment input from the CPU to indicate that the SMI is being acknowledged and the processor is operating in System Management Mode(SMM).

Cache & DRAM Interface

Pin No.	Symbol	Type	Function
22-15	TA[7:0]	I/O	TAG RAM data bus lines.
24	ALT	I/O	The ALT bit indicates the particular line in the 2nd level cache contains modified data.
3	KA4X	O	Cache address bit 4 for even bank in an interleaved cache configuration..
2	KA3/KA4Y	O	Cache address bit 4 for odd bank, or Cache address bit 3 in non-interleaved mode.
10	KREX#/COE0#	O	Cache Read Enable for even bank of standard SRAM, or Cache Output Enable for burst SRAM.

9	KREY#/COE1#	O	Cache Read Enable for odd bank of standard SRAM, or Cache Output Enable for burst SRAM. When used as COE1#, it is a copy of COE0# for loading consideration.
8,7	KWX0/1#	O	Cache Write Enable for standard SRAM, even bank.
5,4	KWY0/1#	O	Cache Write Enable for standard SRAM, odd bank.
23	ALTWE#	O	The ALTWE# is the write strobe to the ALT RAM. This signal is active low when cache read miss or cache write hit occurs. It is used to update the ALT bit.
25	TAGWE#	O	TAG RAM write enable output.
208-205 203-200	KCE[7:0]# / CWE[7:0]#	O	Cache Enable pins for standard SRAM indicate that the corresponding byte is accessed. Cache Write Enable pins for burst SRAM to allow cache data RAM update on a byte-by-byte basis.
1	CALE	O	The CALE controls the external latch between the host address lines and the cache address lines. When high, it allows the CPU address lines to propagate through external latches and onto cache address lines. When low, it is used to latch cache address lines.
42,41 39,38	RAS[3:0]#	O	The RAS[3:0]# are used to latch the row address on the MA bus. Each RAS[3:0]# corresponds to one DRAM row.
35-32 29-26	CAS[7:0]#	O	The CAS[7:0]# are used to latch the column address on the MA bus. Each CAS[7:0]# corresponds to one byte of the eight-byte wide array.
44	RAMW#	O	RAM Write is an active low output signal to enable local DRAM writes.
55-45	MA[10:0]	O	The MA[10:0] provide the row and column address to the DRAM.

PCI Interface

Pin No.	Symbol	Type	Function
111,110 108,107	C/BE[3:0]#	I/O	PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the 5101 is a PCI bus master and inputs when it is a PCI slave.

106-85 82,81 79-72	AD[31:0]	I/O	PCI Address /Data Bus *In address phase:* 1. When the 5101 is a PCI bus master, AD[31:0] are output signals. 2. When the 5101 is a PCI target, AD[31:0] are input signals. *In data phase:* 1. When the 5101 is a bus master of a memory read/write cycle, AD[31:0] are floating. 2. When the 5101 is a bus master of a configuration or an I/O cycle, AD[31:0] are input signals in a read cycle, and output signals in a write cycle. 3. When the 5101 is a target of a memory read/write cycle, AD[31:0] are floating. 4. When the 5101 is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
124	FRAME#	I/O	FRAME# is an output when the 5101 is a PCI bus master. The 5101 drives FRAME# to indicate the beginning and duration of an access. When the 5101 is a PCI slave, FRAME# is an input signal.
123	IRDY#	I/O	IRDY# is an output when the 5101 is a PCI bus master .The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the 5101 is a PCI slave, IRDY# is an input.
126	PAR	O	Parity is an even parity generated across AD[31:0] and C/BE[3:0]#.
122	TRDY#	I/O	TRDY# is an output when the 5101 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the 5101 is a PCI master, it is an input.

121	DEVSEL#	I/O	The 5101 drives DEVSEL# based on the DRAM address range being accessed by a PCI bus master or if the current configuration cycle is to the 5501. As an input it indicates if any device has responded to current PCI bus cycle initiated by the 5101.
120	STOP#	I/O	STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.
127	SERR#	O	System error is an open drain output for reporting errors.
115-112	REQ[3:0]#	I	PCI Bus Request is used to indicate to the PCI bus arbiter that an agent requires use of the PCI bus.
119-116	GNT[3:0]#	O	PCI Bus Grant indicates to an agent that access to the PCI bus has been granted.
125	PLOCK#	I	PCI Lock indicates an exclusive bus operation that may require multiple transactions to complete. When PLOCK# is sampled asserted at the beginning of a PCI cycle, the 5101 considers itself a locked resource and remains in the locked state until PLOCK# is sampled negated on a new PCI cycle.
71	PCICLKO	O	The PCICLKO provides the clock for the 5101/5102/5103 and PCI devices of the system.
129	PCICLKI	I	The PCICLKI input provides the fundamental timing and the internal operating frequency for the 5101. It runs at the same frequency and skew of the PCI local bus. It should be generated from the PCICLKO signal through a clock distribution buffer.
132	PCIRST#	O	The PCI Reset forces the PCI devices to a known state.

Data Buffer Control Interface

Pin No.	Symbol	Type	Function
69,67	HCR[1:0]	O	Host Data Bus Controls. These signals are driven by the 5101 and are used to control the 5102 HD[63:0] bus. They are defined as: 00: 5102 floats HD bus 01: 5102 drives FFFFFFFF to HD bus 10: 5102 drives data from AD bus to HD bus 11: 5102 drives data from MD bus to HD bus

58	ADLE#	O	AD Bus Data Latch Enable. This signal has the following functions: 1.Latch HD or MD data into the PCI read buffer (PRMB) 2.Latch AD data into CPU read PCI buffer on the rising edge of PCICLKI. 3.Latch AD data into PCI posted write buffer (PTMPB) on the rising edge of PCICLKI.
65	ADOE	O	AD Bus Output Enable. This signal is used to enable the 5102 to drive PCI AD bus. It is asserted in CPU writes PCI or PCI master reads local memory cycles.
63	MDLE	O	Memory Data Read Latch Enable. This signal latches the data on the MD bus when negated.
60	CPPSH	O	Push CPU to PCI Posted Write Data into the 5102. The data on the HD bus is latched into the 5102 CPU to PCI Posted Write Buffer on CPPSH rising edge. The edge also increases the write pointer to the next available loading entry in the buffer.
59	CPPOP	O	On the rising edge of CPPOP, the read pointer is changed to address the next available reading location.
62	CMPSH	O	When this signal is asserted, the data on the HD bus is written into the CPU to memory posted write buffer (CTMPB) on the rising edge of CPUCLK, and the write pointer is also changed to address the next available location.
61	CMPOP	O	Pop CPU to Memory Posted Write Buffer Data. When this signal is asserted, the read pointer of the CPU to Memory Posted Write Buffer is increased on the rising edge of CPUCLK.
64	PRDLE	O	This signal latches the current output entry in the CPU to PCI Posted Write Buffer into the prelatch in the 5102. The output of the prelatch is driven onto the PCI AD bus. In a PCI master cycle, PRDLE is asserted when PCI master is reading data from the secondary cache, or when PCI master is writing data to the local memory.

57	HGDW	O	High Double Word Indicator. The signal is driven high when: (1) a high DW from the HD bus is written into CPU to PCI Posted Write Buffer, (2) the CPU reads a high DW from PCI bus, (3) PCI master writes a high DW to local memory, (4) PCI master reads a high DW from local memory.
66	PARITY#	I	Parity Bit, from the 5102.
193	NA#	O	Next Address is driven for one clock to the CPU to indicate that the memory system is ready to accept a new bus cycle. Although the data transfer for the current cycle has not yet completed, the CPU may drive a internally pending cycle out to the address bus two clocks after NA# is asserted.
56	MA11	O	The MA11 provides the row and column address to the DRAM.
12	ADSV#	O	Cache Advance is driven to burst SRAM to advance the internal two-bit address counter to the next address of burst sequence.
13	ADSC#	O	Cache Address Strobe Control causes the burst SRAM to latch the cache address.

Others

Pin No.	Symbol	Type	Function
70	HLDA	O	Hold Acknowledge.
133	SMOUT	O	System Management Output control pin. It is used to control peripheral's power, clock...etc.
131	SIOREQ#	I	SIO Request from the 5103 to request the PCI bus.
130	SIOGNT#	O	SIO Grant. When asserted, SIOGNT# indicates that the PCI arbiter has granted use of the bus to the 5103.
138	SMIREQ#	I	The signal come form 5103 for SMI request
137	32KI	I	32KI is the Suspend clock source of the 32KHz oscillator
134	STPGNT	O	Default status during initialization, Power on state: Low; Power good state: Low When 5101 receives stop grant state from CPU , the signal will activate Hi to inform 5103 , that the following cycle is in stop grant state.
135	PWRDWN	I	Switch to 32KHz , When the signal is active , all 5101 internal clock will switch to 32KHz.

140	OSC	I	OSC is a clock input for the timer and the DMA controller. It is 14.318MHz and is generated by an external oscillator.
36	ACLK	I	Advanced CPU clock should lead the CPUCLK by 3 to 7 ns to provide the clock for the 5101 internal cache control logic.
30	CPUCLK	I	CPU clock input runs at the frequency and skew equal to those of the CPU clock.
83	PWRGD	I	Power Good is a power on reset and push button reset input.
142	NC		
40,80,136	VDD5		For Power Group A
14,141 199	VDD1		For Power Group B
6,11,31,37 43,68,84 109,128 139,183 195,204	VSS		Ground

2.11 Electrical Characteristics

2.11.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{O}C
Storage temperature	-40	125	^{O}C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V
Power Dissipation		1	W

Note:
Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

2.11.2 DC Characteristics

TA = 0 - 85 ^{O}C, VSS = 0V , VDD5=5V$\pm$5%, VDD1=3.3V$\pm$5% or 5V$\pm$5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL1}	Input low voltage	-0.3	0.8	V	*Note 1*, VDD1
V_{IH1}	Input High Voltage	2.2	VDD3+0.3V	V	*Note 1*
V_{IL2}	Input low voltage	-0.3	0.8	V	*Note 2*
V_{IH2}	Input high voltage	2.2	VDD+0.3	V	*Note 2*
V_{T1-}	Schmitt Trigger Threshod Voltage Falling Edge	1.6		V	*Note 3*
V_{T1+}	Schmitt Trigger Threshold Voltage Rising Edge		3.2	V	*Note 3*
V_{H1}	Hysteresis Voltage	0.3	1.2	V	*Note 3*
V_{OL1}	Output Low Voltage		0.45	V	*Note 4*
V_{OH1}	Output High Voltage	2.4		V	*Note 4*
V_{OL2}	Output Low Voltage		0.4	V	*Note 5*
V_{OH2}	Output High Voltage	2.0	VDD3	V	*Note 5*
I_{OL1}	Output Low Current	4		mA	*Note 6*
I_{OH1}	Output High Current	4		mA	*Note 6*
I_{OL2}	Output Low Current	6		mA	*Note 7*
I_{OH2}	Output High Current	6		mA	*Note 7*
I_{OL3}	Output Low Current	8		mA	*Note 8*
I_{OH3}	Output High Current	8		mA	*Note 8*
I_{OL4}	Output Low Current	16		mA	*Note 9*
I_{OH4}	Output High Current	16		mA	*Note 9*
I_{OL5}	Output Low Current	4		mA	*Note 10*
I_{OH5}	Output High Current	1		mA	*Note 10*, *Note 11*
I_{IH}	Input Leakage Current		+10	mA	
I_{IL}	Input Leakage Current		-10	mA	
C_{IN}	Input Capacitance		12	pF	Fc=1 Mhz

C_{OUT}	Output Capacitance		12	pF	Fc=1 Mhz
$C_{I/O}$	I/O Capacitance		12	pF	Fc=1 Mhz
I_{CC3}	Power Supply Current of VDD1		40	mA	3.3V, 66MHz

Note:

1. V_{IL1} and V_{IH1} apply to the following signals: HA[31:3], W/R#, HBE[7:0]#, HITM#, D/C#, ADS#, CPUHLDA, SMIACT#, CACHE#, M/IO#
2. V_{IL2} and V_{IH2} apply to the following signals: TA[7:0], ALT, CPUCLK, ACLK, PARITY#, AD[31:0], C/BE[3:0]#, REQ[3:0]#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, LOCK#, PCICLKI, SIOGNT#, SIOREQ#, OSC
3. V_{T1-},V_{T1+} and V_{H1} apply to PWRGD
4. V_{OL1} and V_{OH1} apply to the following signals: TA[7:0], ALTWE#, ALT, TAGWE#, CAS[7:0]#, RAS[3:0]#, RAMW#, MA11, MA[10:0], HGDW, ADLE#, CPPOP, CPPSH, CMPOP, CMPSH, MDLE, PRDLE, ADOE, HCR[1:0], HLDA, PCICLKO, AD[31:0], GNT[3:0]#, STOP#, DEVSEL#, TRDY#, FRAME#, PAR, SERR#, PCIRST#, SMOUT
5. V_{OL2} and V_{OH2} apply to the following signals: CALE, KA4Y, KA4X, KWY[1:0]#, KWX[1:0]#, KREX#, KREY#, ADSC#/FLUSH#, ADSV#, STPCLK#, INIT, SMI#, HA[31:3], CPURST, W/R#, A20M#, EADS#, CPUHOLD, NA#, BRDY#, KEN#, KCE[7:0]#
6. I_{OL1} and I_{OH1} apply to the following signals: TA[7:0], ALTWE#, ALT, TAGWE#, RAMW#, MA11, MA[10:0], HGDW, ADLE#, CPPOP, CPPSH, CMPOP, CMPSH, MDLE, PRDLE, ADOE, HCR[1:0], HLDA, PCICLKO, AD[31:0], C/BE[3:0]#, GNT[3:0]#, PAR, SERR#, PCIRST#, SMOUT,
7. I_{OL2} and I_{OH2} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#.
8. I_{OL3} and I_{OH3} apply to the following signals: CAS[7:0]#
9. I_{OL4} and I_{OH4} apply to the following signals: KA4X, KA4Y, KWY[1:0]#, KWX[1:0]#, ADSV#, ADSC#/FLUSH#, RAS[3:0]#
10. I_{OL5} and I_{OH5} apply to the following signals: CALE, KREY#, KREX#, STPCLK#, INIT, SMI#, HA[31:3], W/R#, EADS#, CPUHOLD, NA#, BRDY#, KEN#, KCE[7:0]#, CPURST, A20M#
11. I_{OH5} is 1mA in 3.3 system, when in 5V system, the I_{OH4} is 4mA.
12. The driving current of CAS# and some PCI bus signals are programmable. Please refer to Register Description.

2.11.3 AC Characteristics

Symbol	Parameter	Typ	Max	Unit	CL
T1	BRDY# Active delay from CPUCLK	8	12	ns	35pf
T2	BRDY# Inactive delay from CPUCLK	6	9	ns	35pf
T3	KEN# Active delay from CPUCLK	7	11	ns	35pf
T4	KEN# Inactive delay from CPUCLK	5	8	ns	35pf
T5	NA# Active delay from CPUCLK	8	12	ns	35pf
T6	NA# Inactive delay from CPUCLK	6	9	ns	35pf
T7	EADS# Active delay from CPUCLK	8	12	ns	35pf
T8	EADS# Inactive delay from CPUCLK	6	9	ns	35pf
T9	CPUHOLD Active delay from CPUCLK	8	12	ns	35pf
T10	CPUHOLD Inactive delay from CPUCLK	6	9	ns	35pf
T11	CPURST Inactive delay from CPUCLK	7	11	ns	35pf
T12	CPURST High Pulse Width	25		cpuclk	35pf
T13	KREX#, KREY# Active delay from ACLK	9	13	ns	100pf
T14	KREX#, KREY# Inactive delay from ACLK	6	9	ns	100pf
T15	KWX[0:1]#, KWY[0:1]# Active delay from ACLK	8	12	ns	100pf
T16	KWX[0:1]#, KWY[0:1]# Inactive delay from ACLK	6	9	ns	100pf
T17	KWX[0:1]#, KWY[0:1]# Active delay from CPUCLK	8	12	ns	100pf
T18	KWX[0:1]#, KWY[0:1]# Inactive delay from CPUCLK	6	9	ns	100pf
T19	KCE[7:0]# Active delay from ADS# falling edge	7	12	ns	35pf
T20	KCE[7:0]# Inactive delay from CPUCLK	7	12	ns	35pf
T21	MDLE High Active delay from CPUCLK	5	8	ns	35pf
T22	MDLE High Inactive delay from CPUCLK	7	11	ns	35pf
T23	KA4X,KA4Y Low Valid delay from ACLK	7	11	ns	100pf
T24	KA4X,KA4Y High Valid delay from ACLK	6	9	ns	100pf
T25	KA4X,KA4Y Low Valid delay from CPUCLK In Update Cycle & Write cycle	7	11	ns	100pf
T26	KA4X,KA4Y High Valid delay from CPUCLK In Update Cycle & Write cycle	6	9	ns	100pf
T27	Tag Output Valid delay from CPUCLK In Update Cycle	14	23	ns	35pf
T28	RAS[3:0]# Active delay from CPUCLK	12	18	ns	250pf
T29	RAS[3:0]# Inactive delay from CPUCLK	9	14	ns	250pf
T30	CAS[7:0]# Active delay from CPUCLK	11	16	ns	120pf
T31	CAS[7:0]# Inactive delay from CPUCLK	8	12	ns	120pf
T32	MA[11:0] Low Valid delay from CPUCLK	12	18	ns	35pf

T33	MA[11:0] High Valid delay from CPUCLK	11	16	ns	35pf
T34	MA[11:0] Propagation delay from A[27:3]	8	12	ns	35pf
T35	ALT Output Valid delay from CPUCLK	10	15	ns	35pf
T36	ALTWE#, TAGWE# Active delay from CPUCLK	9	14	ns	35pf
T37	ALTWE#, TAGWE# Inactive delay from CPUCLK	9	14	ns	35pf
T38	A20M# Active delay from CPUCLK	9	14	ns	35pf
T39	A20M# Inactive delay from CPUCLK	8	12	ns	35pf
T40	AD[31:0], C/BE[3:0]# Output valid delay from PCICLKI	10	15	ns	50pf
T41	PRDLE Active delay from PCICLKI	9	14	ns	35pf
T42	DEVSEL#, FRAME#,IRDY#,STOP#,TRDY# Active delay from PCICLKI	10	15	ns	50pf
T43	DEVSEL#, FRAME#, IRDY#, STOP#, TRDY# Inactive delay from PCICLKI	9	14	ns	50pf
T44	GNT[3:0]#, PAR, SERR#, SIOGNT#, STPCLK# Active delay from PCICLKI	10	15	ns	50pf
T45	GNT[3:0]#, PAR, SERR#, SIOGNT#, STPCLK# Inactive delay from PCICLKI	10	15	ns	50pf
T46	HA[31:3] Drive Output Valid delay from PCICLKI	12	18	ns	50pf
T47	HCR[1:0], HGDW Active delay from CPUCLK	7	11	ns	35pf
T48	HLDA Active delay from CPUCLK	8	12	ns	35pf
T49	HLDA Inactive delay from CPUCLK	7	11	ns	35pf
T50	INIT# Active delay from CPUCLK	7	11	ns	35pf
T51	INIT# Inactive delay from CPUCLK	6	9	ns	35pf
T52	MDLE Active delay from CPUCLK	7	11	ns	35pf
T53	MDLE Inactive delay from CPUCLK	6	9	ns	35pf
T54	PCICLKO,PCIRST Active delay from CPUCLK	8	12	ns	50pf
T55	RAMW# Active delay from CPUCLK	11	16	ns	35pf
T56	RAMW# Inactive delay from CPUCLK	8	12	ns	35pf
T57	SMOUT Active delay from CPUCLK	10	15	ns	50pf
T58	ADSC# Active delay from CPUCLK	7	11	ns	90pf
T59	ADSC# Inactive delay from CPUCLK	6	9	ns	90pf
T60	ADSV# Active delay from CPUCLK	7	11	ns	150pf
T61	ADSV# Inactive delay from CPUCLK	6	9	ns	150pf
T62	CPPSH Active delay from CPUCLK	4	6	ns	35pf
T63	CPPOP Active delay from PCICLK	8	12	ns	35pf
T64	CPPSH Inactive delay from CPUCLK	7	11	ns	35pf
T65	CPPOP Inactive delay from PCICLK	10	15	ns	35pf

T66	ADOE Active delay from PCICLK	6	9	ns	35pf
T67	ADOE Inactive delay from PCICLK	6	9	ns	35pf
T68	ADLE# Active delay from PCICLK	6	9	ns	35pf
T69	ADLE# Inactive delay from PCICLK	6	9	ns	35pf
T70	PCICLKO high time (Divided by 2)	15.2		ns	50pf
T71	PCICLKO low time (Divided by 2)	12.6		ns	50pf
T72	PCICLKO high time (Divided by 1.5)	12.5		ns	50pf
T73	PCICLKO low time (Divided by 1.5)	15.8		ns	50pf
T74	PCICLKO rise time (Divided by 2)	1.16		ns	50pf
T75	PCICLKO fall time (Divided by 2)	0.66		ns	50pf
T76	PCICLKO rise time (Divided by 1.5)	1.06		ns	50pf
T77	PCICLKO fall time (Divided by 1.5)	0.9		ns	50pf
T78	HCR[1:0] fall time to CPUCLK rising	4.5		ns	35pf
T79	HCR[1:0] rise time to CPUCLK rising	3.7		ns	35pf
T80	CALE# Active delay from CPUCLK	8	12	ns	35pf
T81	CALE# Inactive delay from CPUCLK	6	9	ns	35pf
T82	SMI# rise time to CPUCLK rising	7.8	10	ns	35pf
T83	SMI# fall time to CPUCLK rising	7.8	10	ns	35pf

2.11.4 AC Timing Diagram

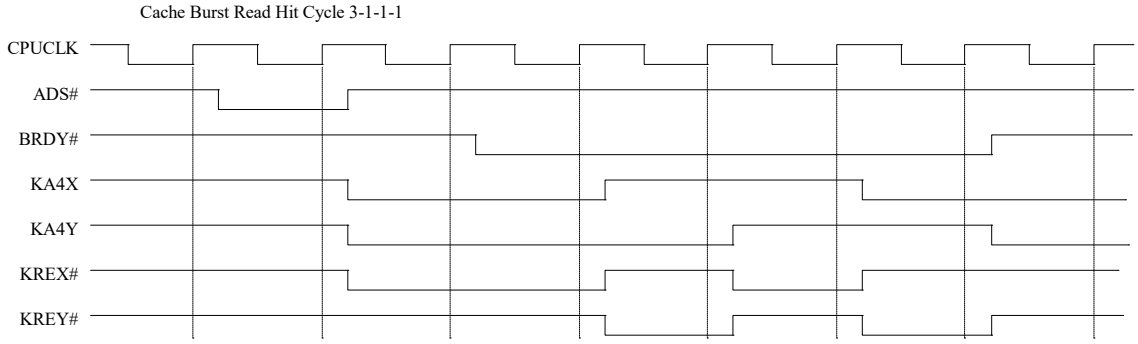


Figure 2.2

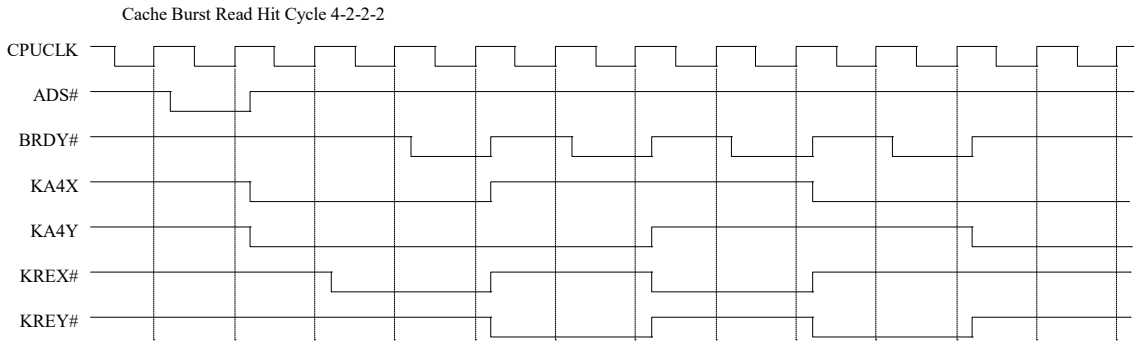


Figure 2.3

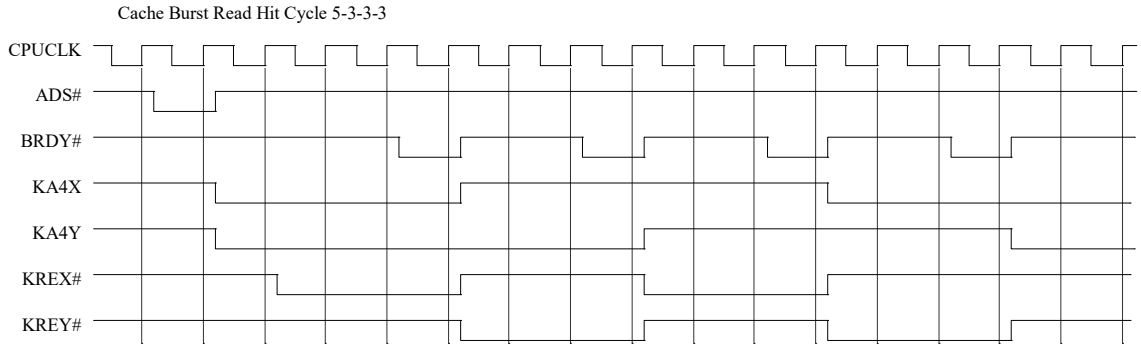


Figure 2.4

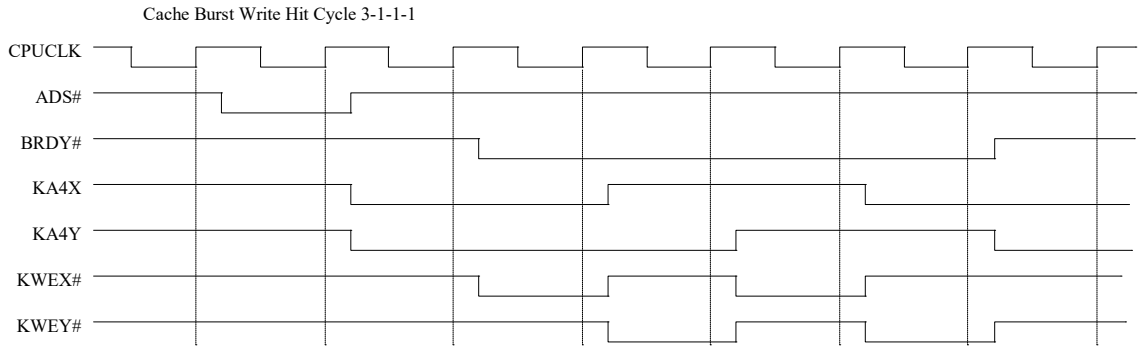


Figure 2.5

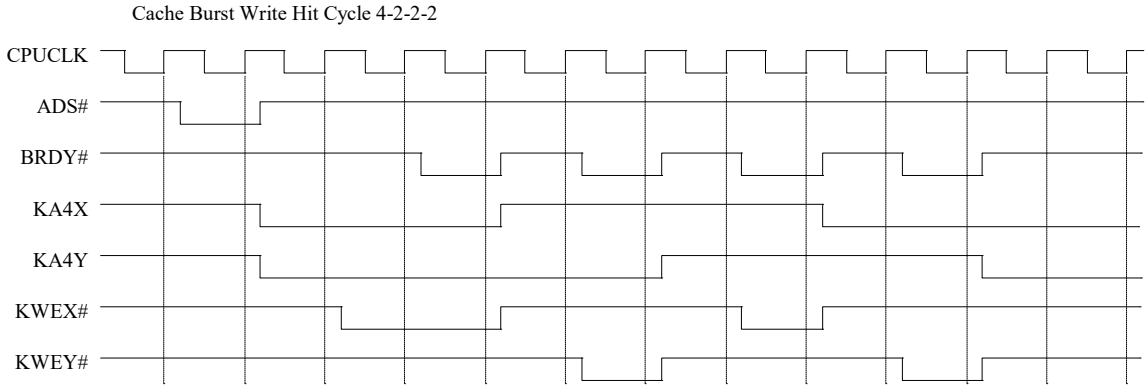


Figure 2.6

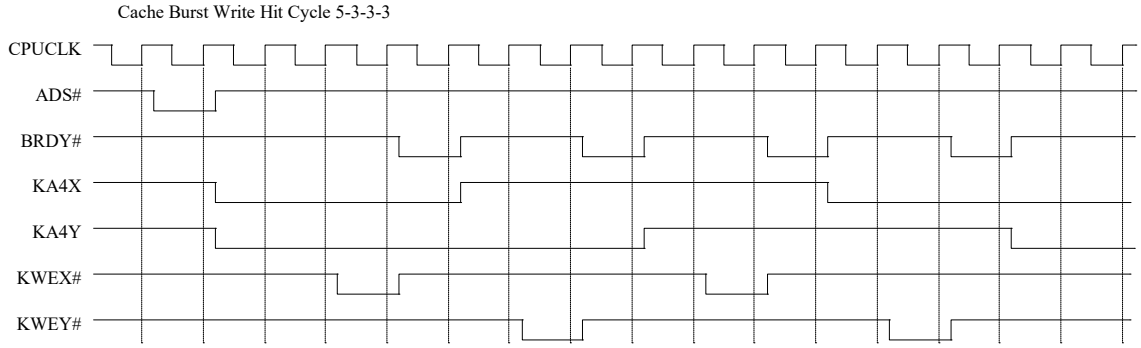


Figure 2.7

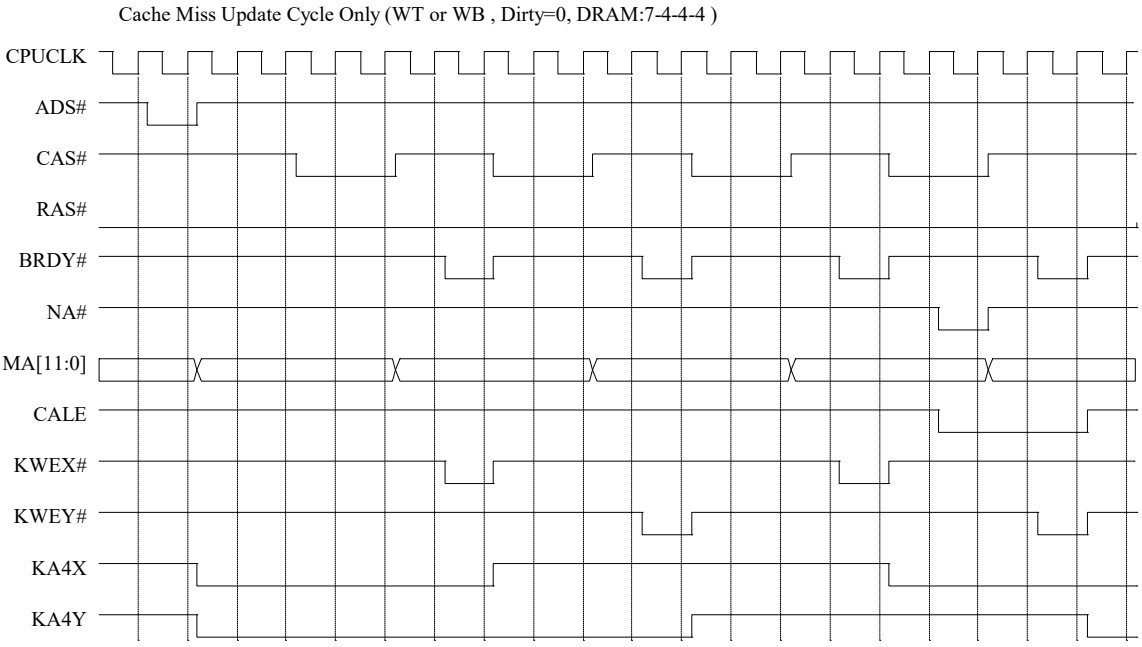


Figure 2.8

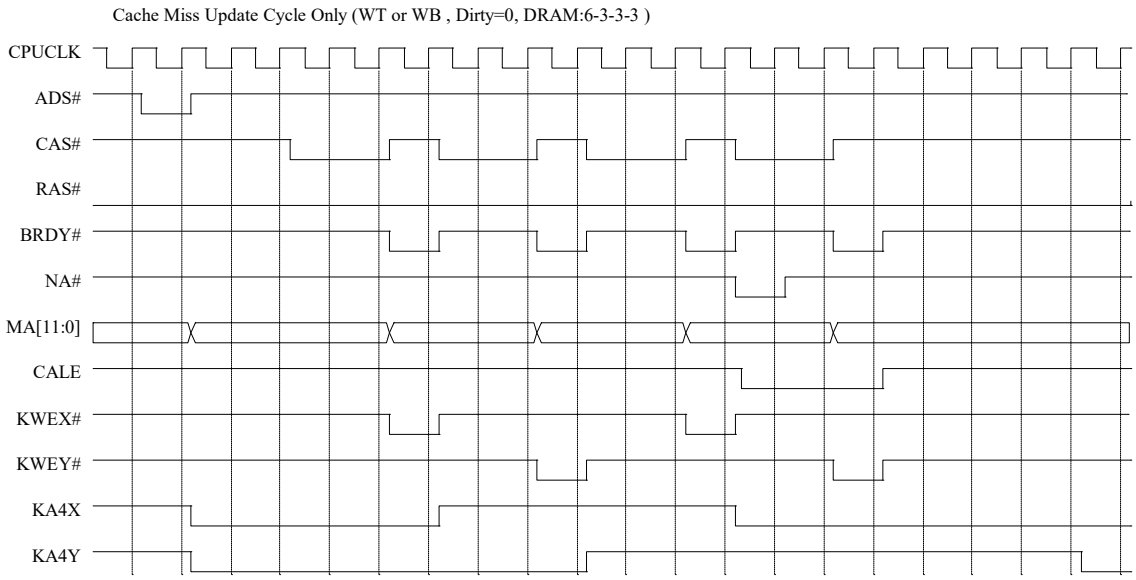


Figure 2.9

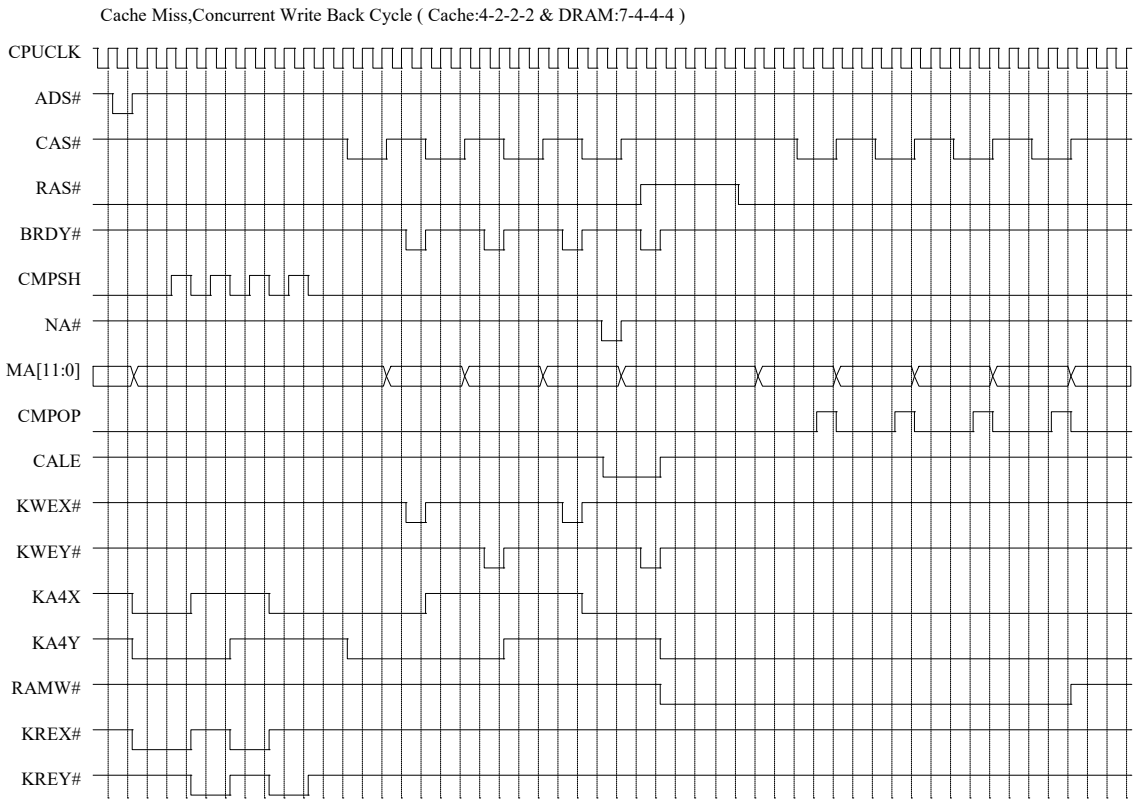


Figure 2.10

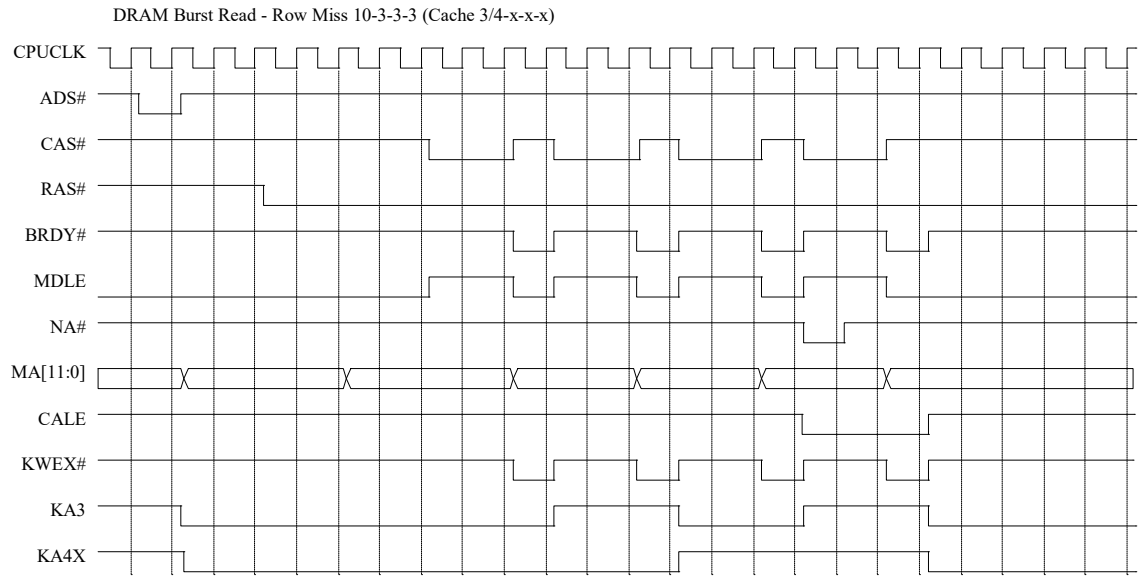


Figure 2.11

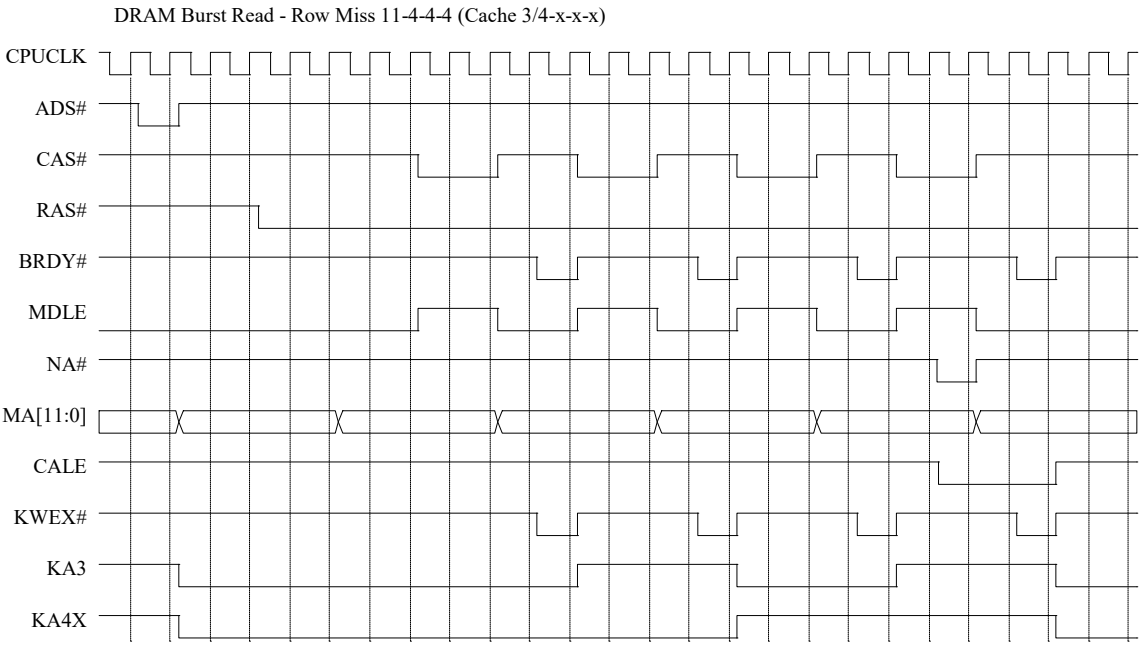


Figure 2.12

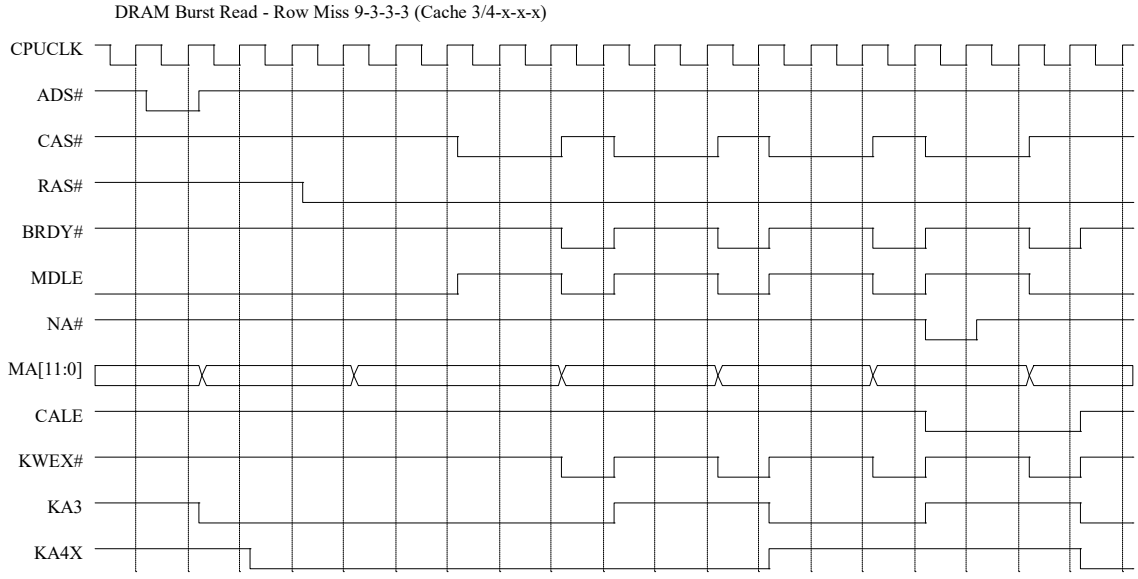


Figure 2.13

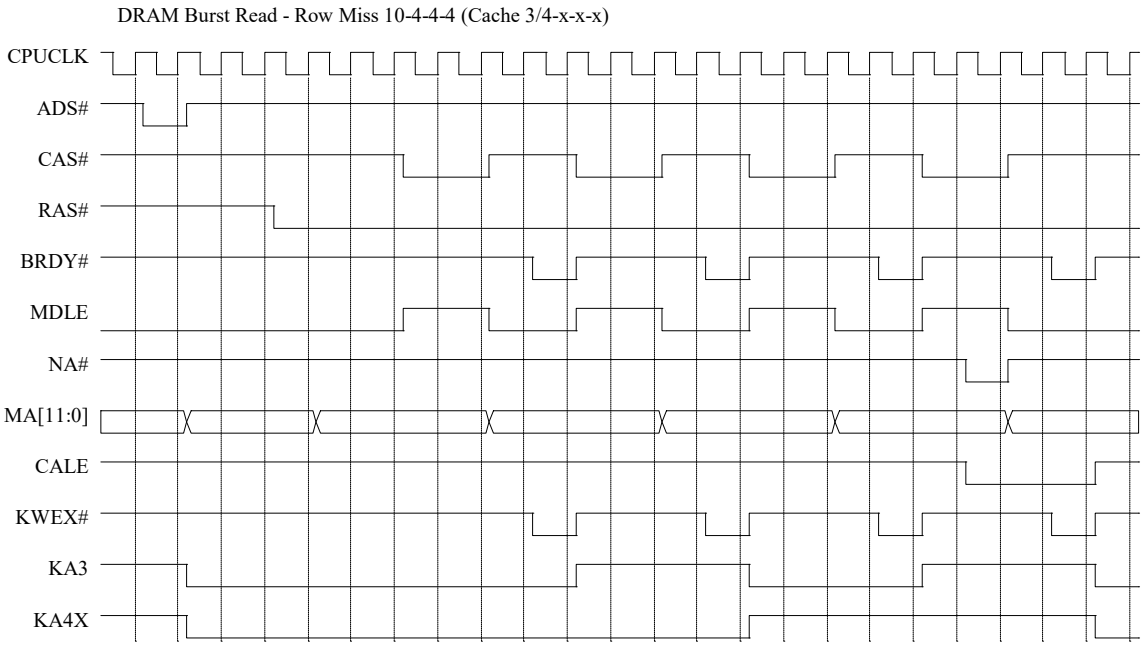


Figure 2.14

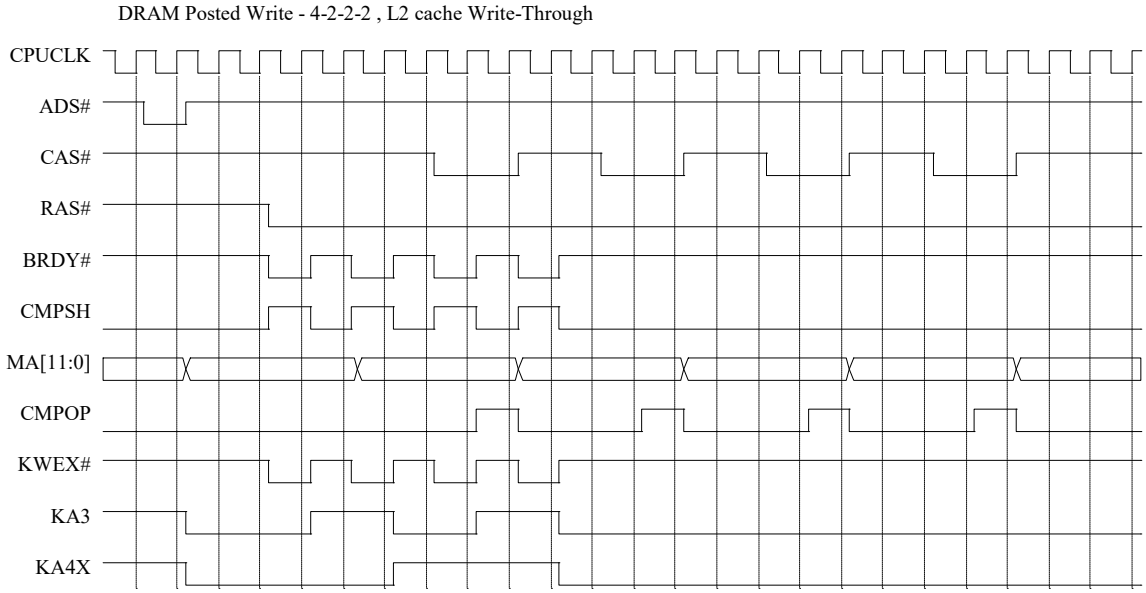


Figure 2.15

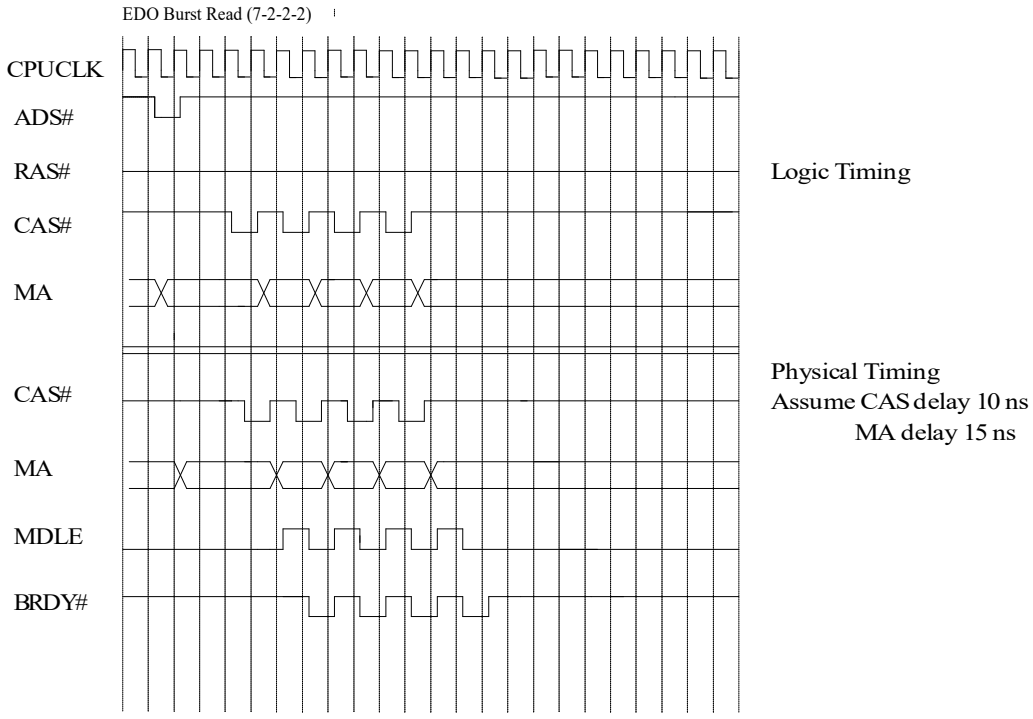


Figure 2.16

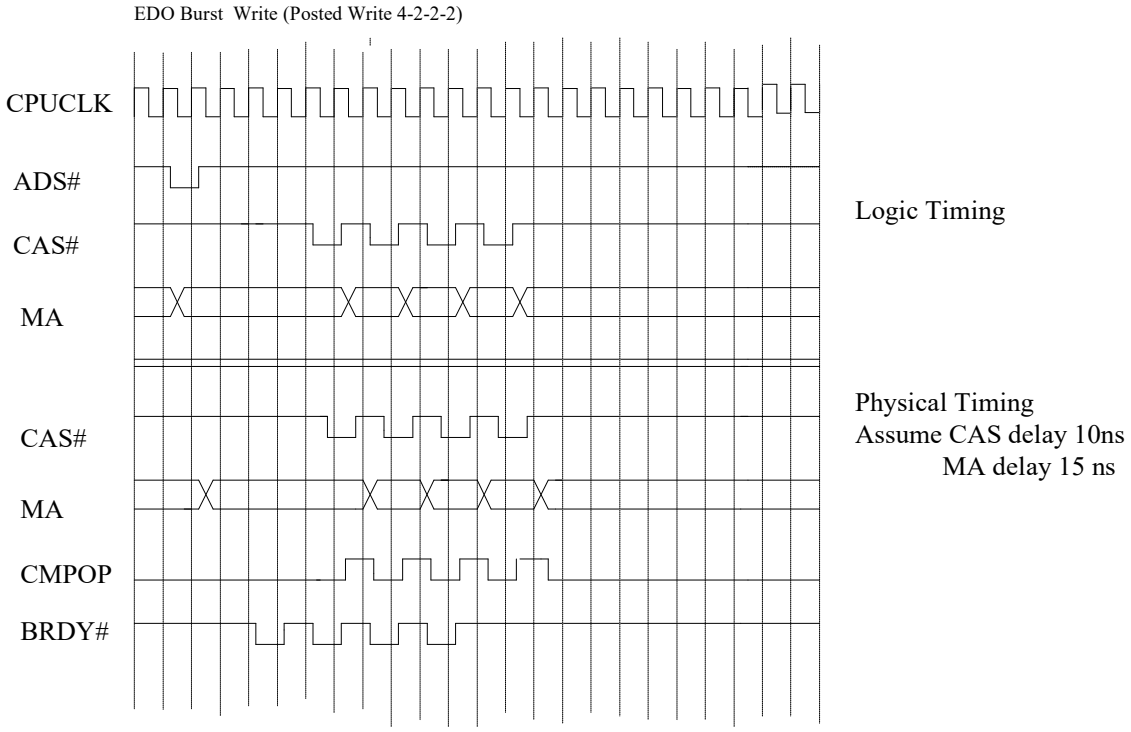


Figure 2.17

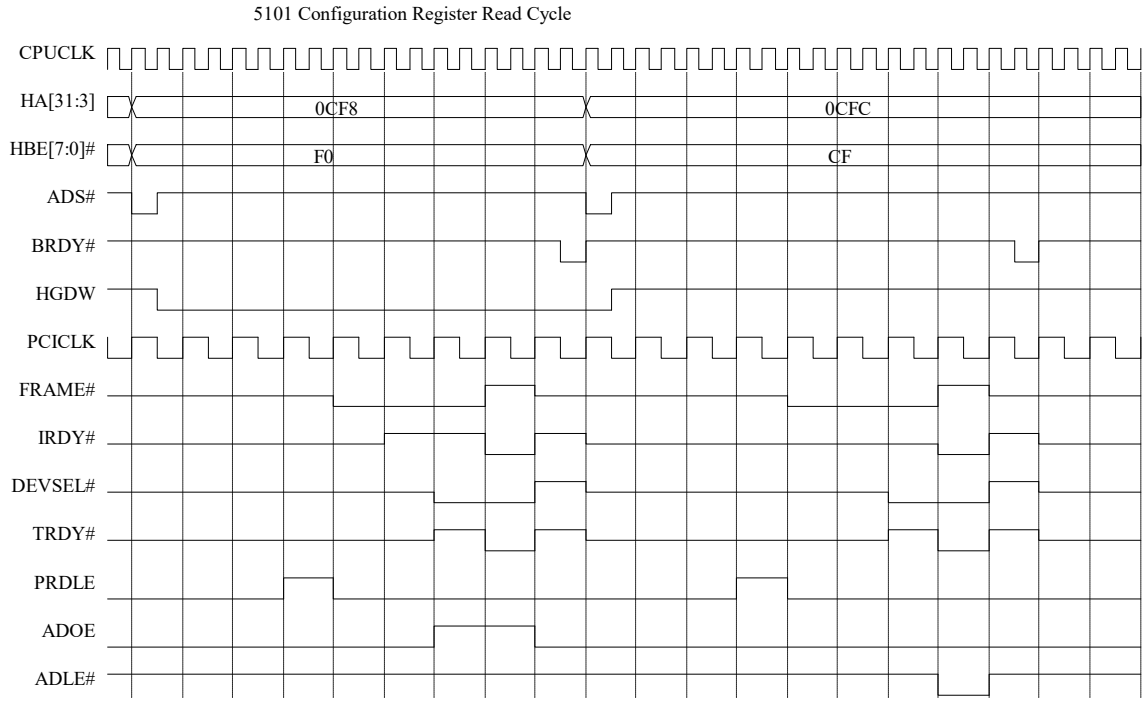


Figure 2.18

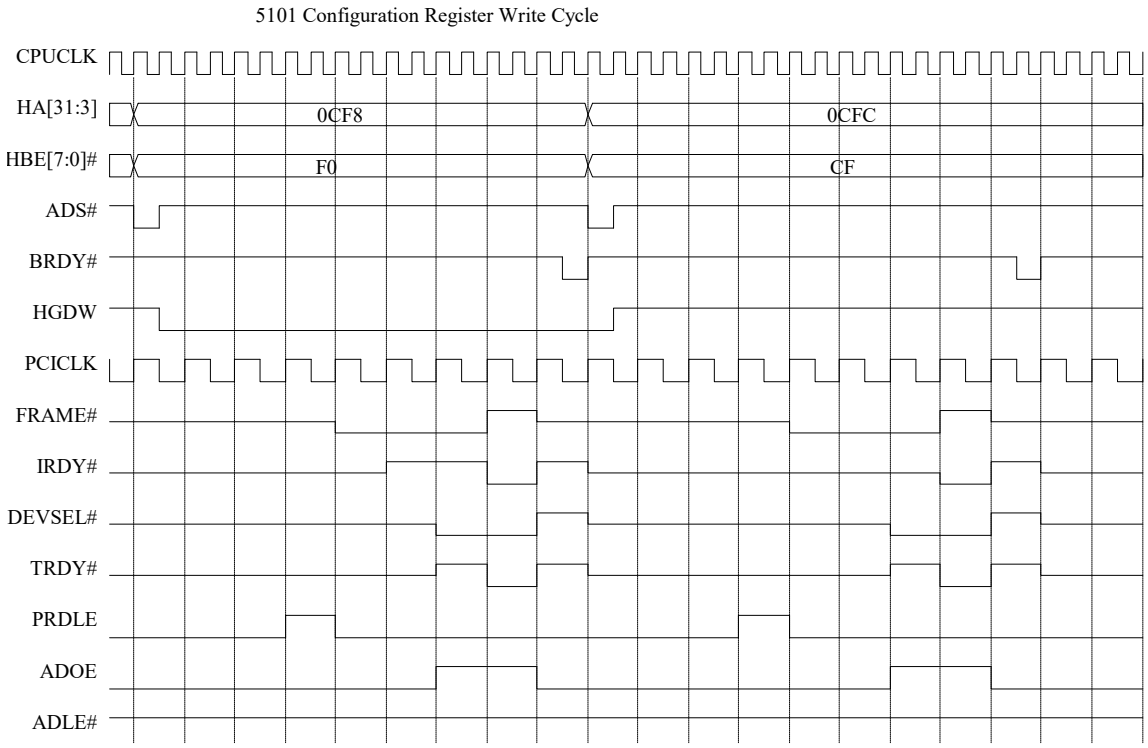

5101 Configuration Register Write Cycle
CPUCLK
HA[31:3]
0CF8
0CFC
HBE[7:0]#
F0
CF
ADS#
BRDY#
HGDW
PCICLK
FRAME#
IRDY#
DEVSEL#
TRDY#
PRDLE
ADOE
ADLE#

Figure 2.19

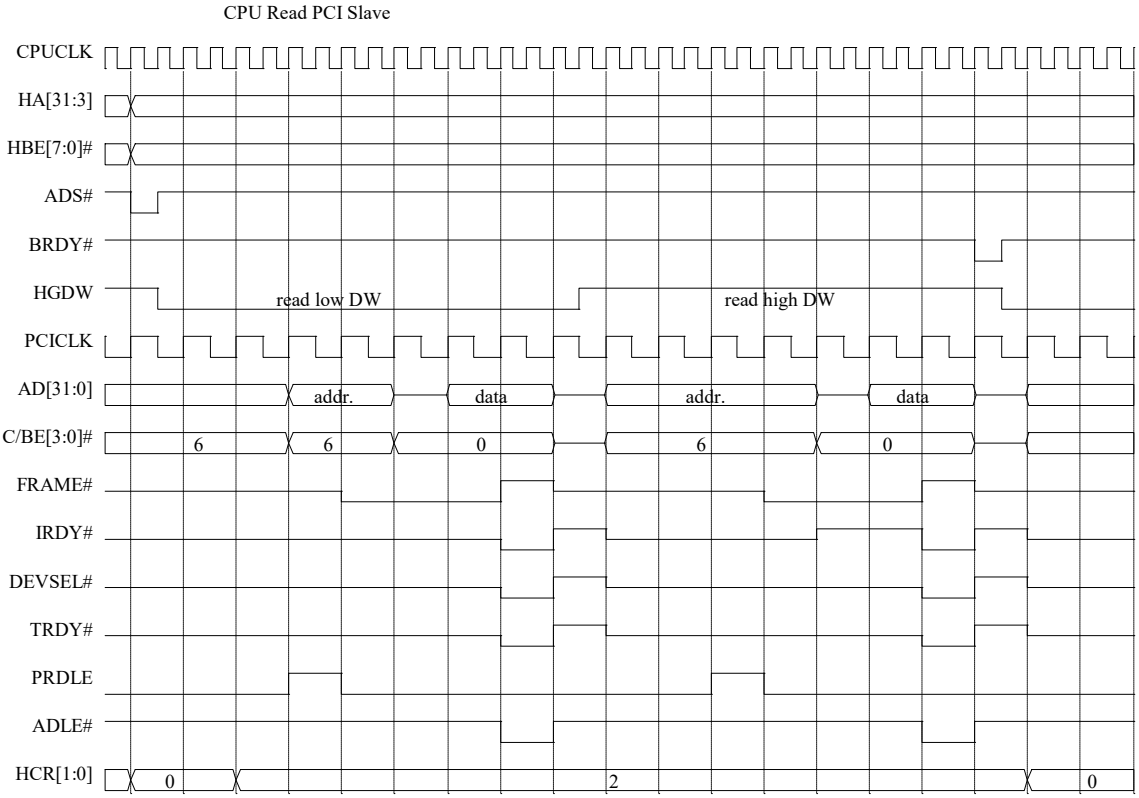

CPU Read PCI Slave
CPUCLK
HA[31:3]
HBE[7:0]#
ADS#
BRDY#
HGDW
read low DW
read high DW
PCICLK
AD[31:0]
addr.
data
addr.
data
C/BE[3:0]#
6
6
0
6
0
FRAME#
IRDY#
DEVSEL#
TRDY#
PRDLE
ADLE#
HCR[1:0]
0
2
0

Figure 2.20

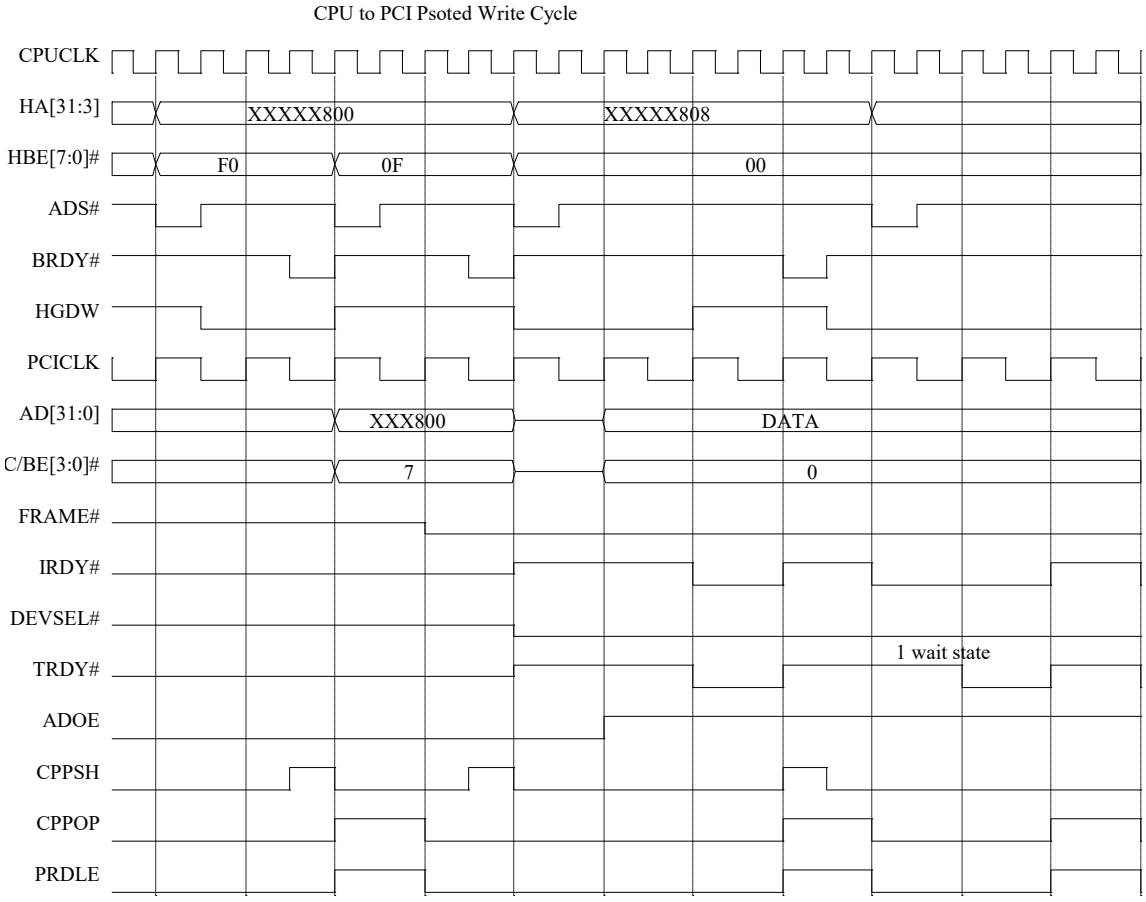


Figure 2.21

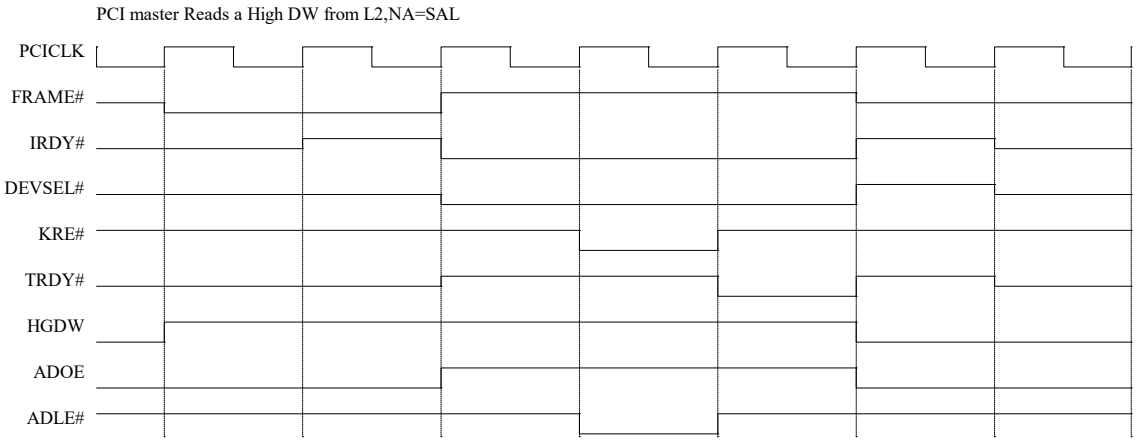


Figure 2.22

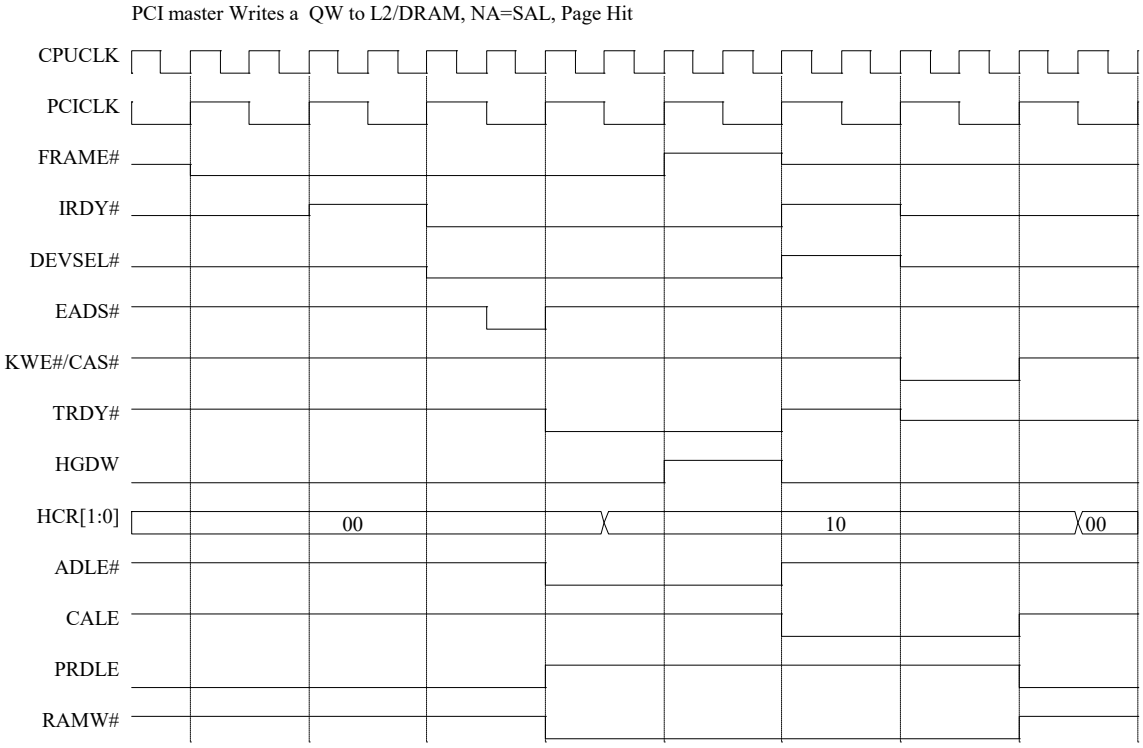

PCI master Writes a QW to L2/DRAM, NA=SAL, Page Hit
CPUCLK
PCICLK
FRAME#
IRDY#
DEVSEL#
EADS#
KWE#/CAS#
TRDY#
HGDW
HCR[1:0]
00
10
00
ADLE#
CALE
PRDLE
RAMW#

Figure 2.23

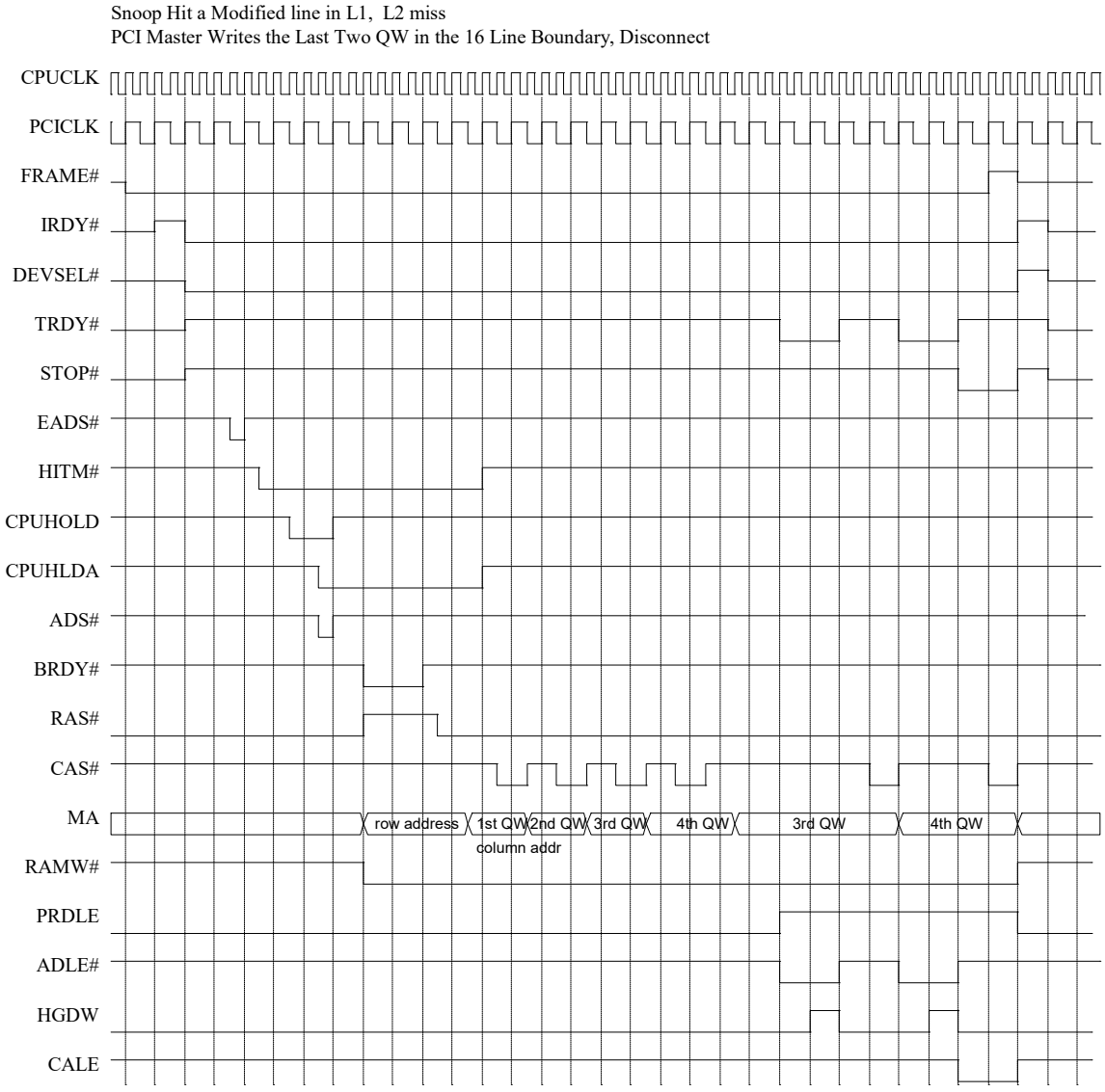

Snoop Hit a Modified line in L1, L2 miss
PCI Master Writes the Last Two QW in the 16 Line Boundary, Disconnect
CPUCLK
PCICLK
FRAME#
IRDY#
DEVSEL#
TRDY#
STOP#
EADS#
HITM#
CPUHOLD
CPUHLDA
ADS#
BRDY#
RAS#
CAS#
MA
RAMW#
PRDLE
ADLE#
HGDW
CALE
row address
column addr
1st QW
2nd QW
3rd QW
4th QW
3rd QW
4th QW

Figure 2.24

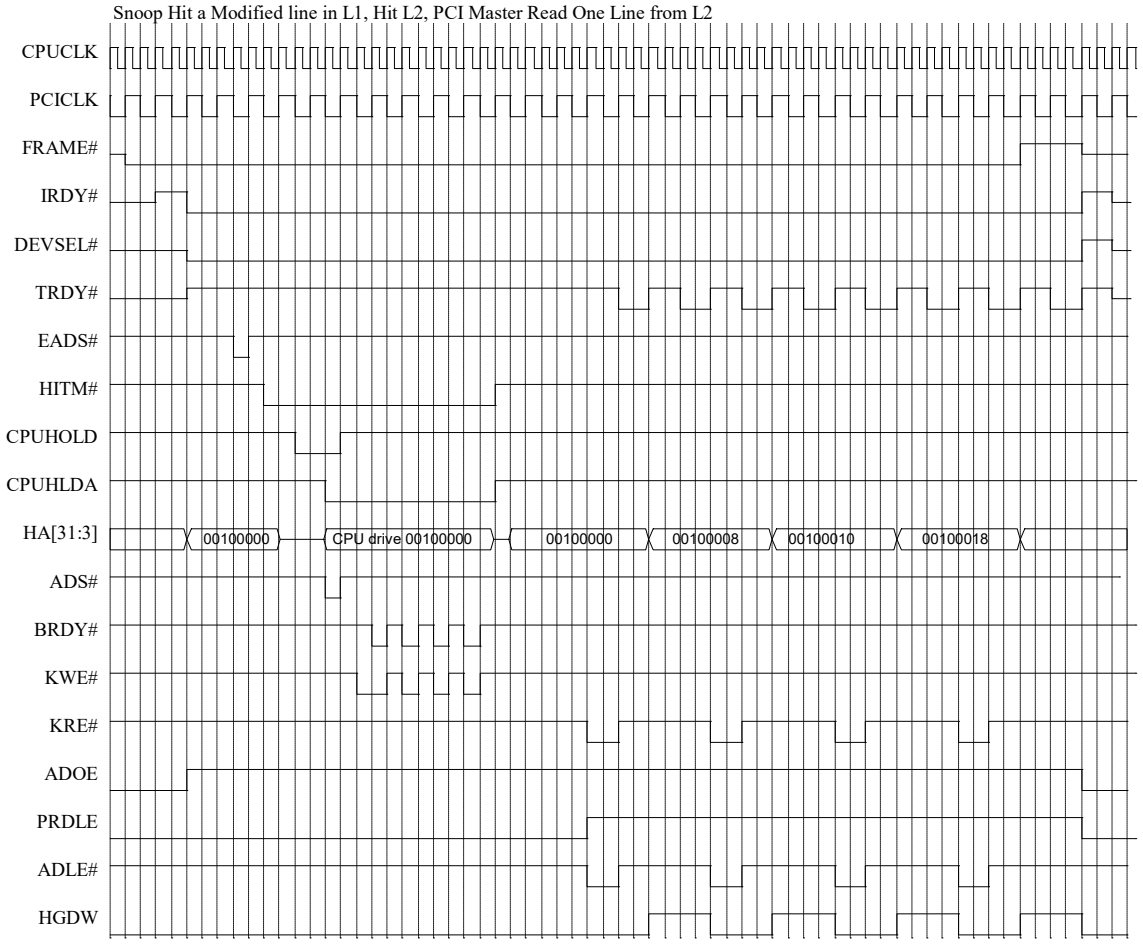


Figure 2.25

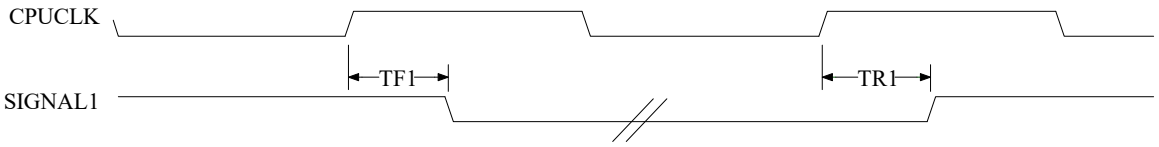


Figure 2.26

TF1 = T1, T3, T5, T7, T10, T11, T17, T22, T23, T25, T27, T28, T30, T32, T36, T38, T49, T50, T53, T55, T58, T60, T64, T78, T80, T83

TR1 = T2, T4, T6, T8, T9, T18, T20, T21, T24, T26, T27, T29, T31, T33, T35, T37, T39, T47, T48, T51, T52, T54, T56, T57, T59, T61, T62, T79, T81, T82

SIGNAL1 = BRDY#, KEN#, NA#, EADS#, CPUHOLD, CPURST, KWX[0:1]#, KWY[0:1]#, KCE[7:0]#, MDLE, CALE, KA4X, KA4Y, TA[7:0], RAS[3:0]#, CAS[7:0]#, MA[11:0], ALT, ALTWE#, TAGWE#, A20M#, HLDA, INIT#, PCICLKO, PCIRST, RAMW#, SMOUT, ADSC#, ADSV#, GNT[3:0]#, PAR, SERR#, SIOGNT#, STPCLK#, CPPSH

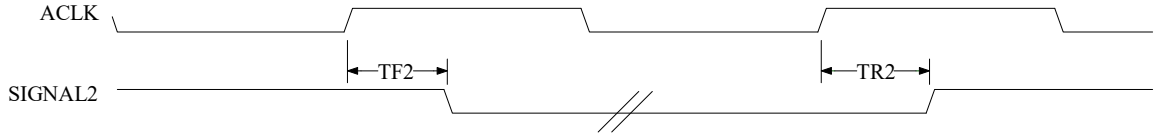


Figure 2.27

TF2 = T13, T15, T23
TR2 = T14, T16, T24
SIGNAL2 = KREX#, KREY#, KWX[0:1]#, KWY[0:1]#, KA4X, KA4Y

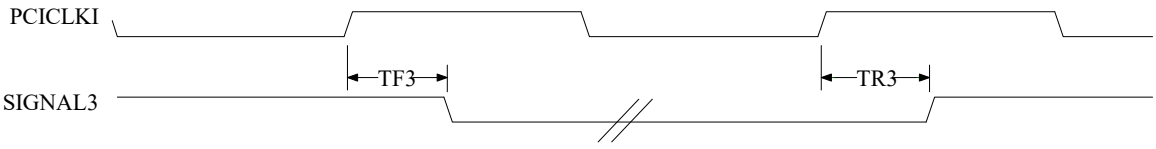


Figure 2.28

TF3 = T40, T41,T42, T46, T44, T65, T67, T68
TR3 = T40, T41, T43, T46, T45, T63, T66, T69
SIGNAL3 = AD[31:0], C/BE[3:0], ADLE#, ADOE, PRDLE, DEVSEL#, FRAME#, IRDY#,STOP#, TRDY#, HA[31:3], CPPOP, ADOE, ADLE

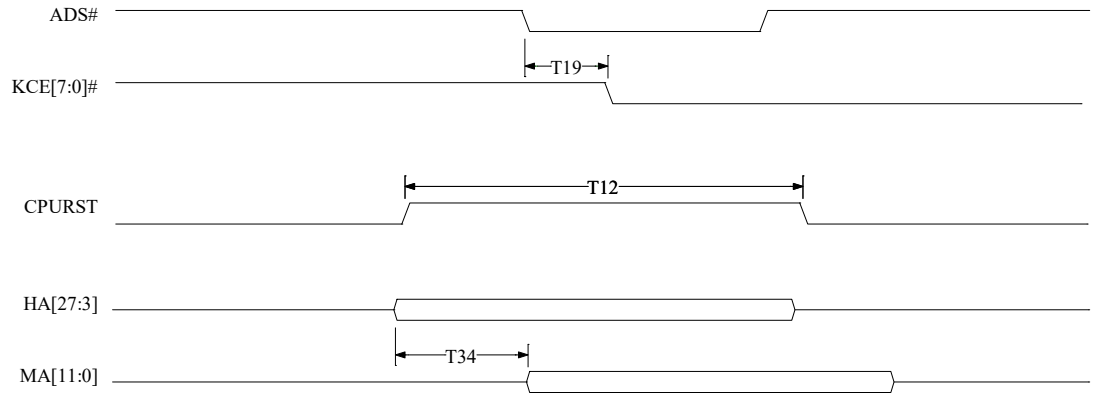


Figure 2.29

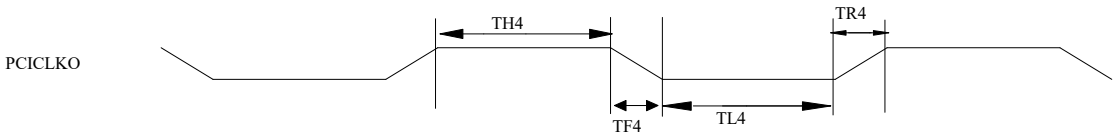


Figure 2.30

TH4 = T70,T72
TL4 = T71, T73
TR4 = T74, T76
TF4 = T75, T77

3. SiS5102

3.1 Features

- **Supports Full 64-bit Pentium Processor Data Bus**
- **Provides a 64-bit Interface to DRAM Memory**
- **Provides a 32-bit Interface to PCI**
- **Three Integrated Posted Write Buffers and Two Read Buffers Increase System Performance**
  - 1 level CPU-to-Memory Posted Write Buffer (CTMPB) with 4 QuadWords (QWs) Deep.
  - 4 level CPU-to-PCI Posted Write Buffer (CTPPB) with 4 DoubleWords (DWs) Deep.
  - 1 level PCI-to-Memory Posted Write Buffer (PTMPB) with 1 QW Deep.
  - 1 level Memory-to-CPU Read Buffer (CRMB) with 1 QW Deep.
  - 1 level Memory-to-PCI Read Buffer (PRMB) with 1 QW Deep.
- **Near Zero Wait State Performance on CPU-to-Memory and CPU-to-PCI Writes.**
- **Operates Synchronously to the 66.7 MHz CPU and 33.3 MHz PCI Clocks.**
- **Provides Parity Generation for Memory Writes.**
- **208-Pin PQFP.**
- **0.6µm CMOS Technology.**

3.2 SiS5102 Functional Block Diagram

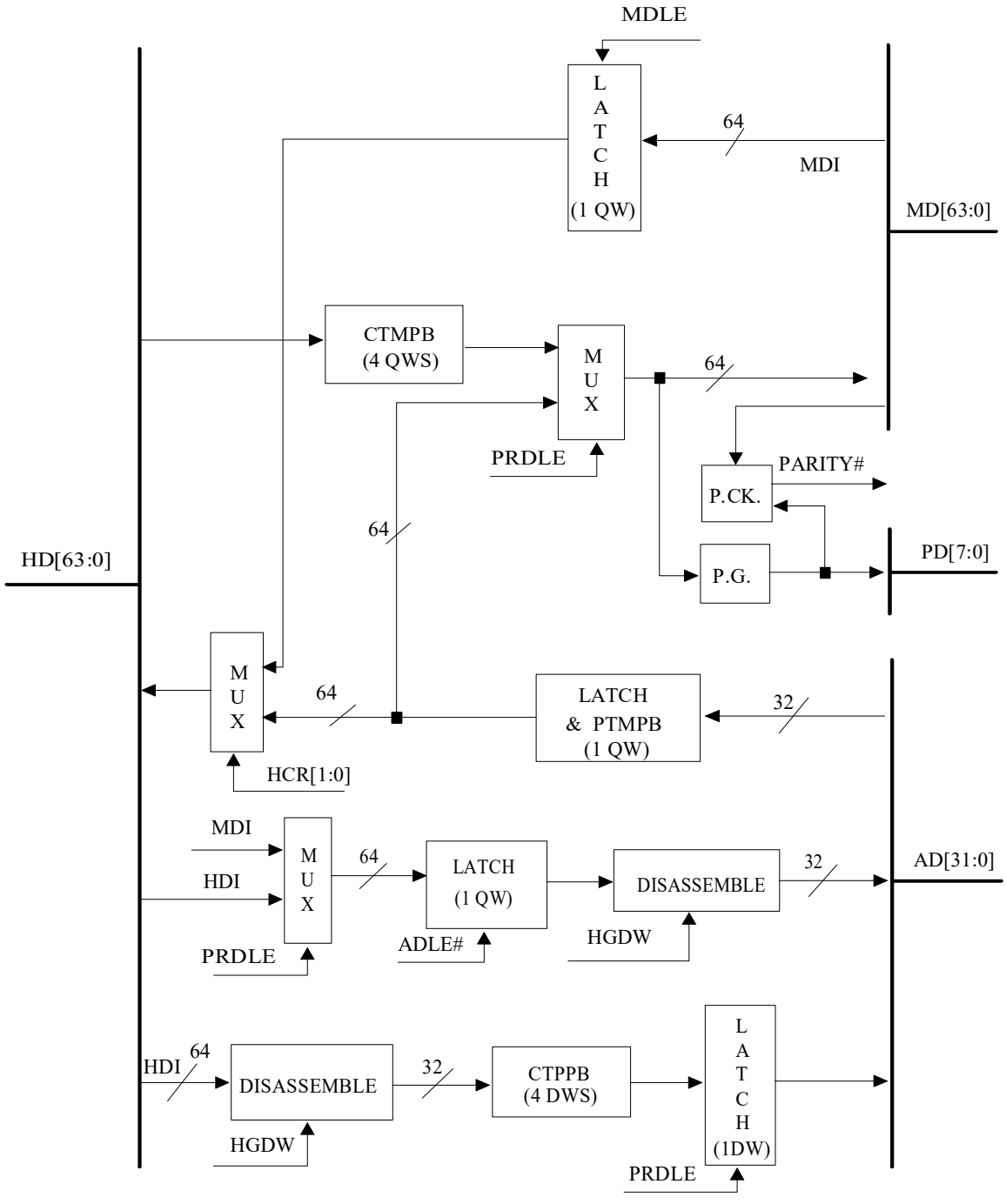


Figure 3.1 SiS5102 Functional Block Diagram

3.3 SiS5102 General Description

The SiS5102 PCI Local Data Buffer (PLDB) provides a bi-directional data buffering among the 64-bit Host Data Bus, the 64-bit Memory Data Bus, and the 32-bit PCI Address/Data Bus. The PLDB incorporates three Posted Write Buffers and two Read Buffers along the bridges of the CPU, PCI and Memory buses. This buffering scheme smoothes the differences in access latencies and bandwidths among three buses, therefore improves the overall system performance.

A four level/4DWs deep write buffer (CTPPB) provides buffering on CPU write to PCI bus. A single level/4QWs deep write buffer (CTMPB) is used for buffering write data from the CPU to Memory. A single level/1QW deep write buffer (PTMPB) is used to buffer PCI write to Memory data.

A single QW Read Buffer (CRMB) is used to latch CPU read Memory data and a single QW Read Buffer (PRMB) is used to latch data in a PCI master read from L2 Cache or DRAM cycle.

During bus operation between the Host, PCI and Memory, the PLDB receives control signals from the PCMC, performs functions such as latching data, forwarding data to destination bus, data assemble and disassemble.

3.3.1 Data Flow Between HD Bus and MD Bus

- **HD Bus to MD Bus**

Data flows from HD bus to MD bus when the CPU writes to local memory or the PCMC writes back a dirty line from the L2 cache to local memory in a CPU read miss/line fill cycle. All the data written to memory are first pushed into the CPMPB. The data are then popped from the buffer and written to Memory.

- **MD Bus to HD Bus**

During a CPU read local memory cycle, the data read are first latched in the 64-bit read buffer (CRMB) in order to provide enough hold time for the CPU and the L2 cache. The PLDB also checks the parity on the read data.

3.3.2 Data Flow Between HD Bus and AD Bus

- **HD Bus to AD Bus**

This path is used in the following two cases. The first case is in a CPU writes PCI slave cycle. The second case is in a PCI master read cycle that hits modified data in local cache which is implemented using write-back policy. All the CPU data sent to PCI memory slave is first pushed into the CTPPB. The data are then popped onto the PCI AD bus at later time when the PCI bus is not busy. Any further write to the PCI bus is suspended if the CTPPB is full. The I/O writes are not posted, but still exploit the CTPPB write buffer.

The path for PCI master read from the L2 cache is implemented through the PRMB, a built-in 64-bit PCI read memory buffer. Since one QW is read each time, the PCMC always sustains 1 wait state for reading the second DW.

- **AD Bus to HD Bus**

This path is exercised in two cases. The first case is during CPU reads PCI slave and the second case is during PCI master write cycles. All the CPU reads PCI cycle is stalled until the CTPPB is empty. When the CPU reads PCI slave, the data are latched and assembled in the PTMPB before they are transmitted to HD bus. During PCI master writes to local memory, the PCI data are first posted in the PTMPB. They are then transferred to local memory and host bus if the PCI master write also hits L2 cache.

3.3.3 Data Flow Between AD Bus and MD Bus

- **AD Bus to MD Bus**

Write data from PCI master is buffered in PTMPB before transferred to local memory. Parity is generated for memory write data.

- **MD Bus to AD Bus**

PCI masters receive data from local memory through this path. The PRMB, a 64-bit PCI read Memory buffer is implemented on this path. The read parity is ignored inside the PLDB.

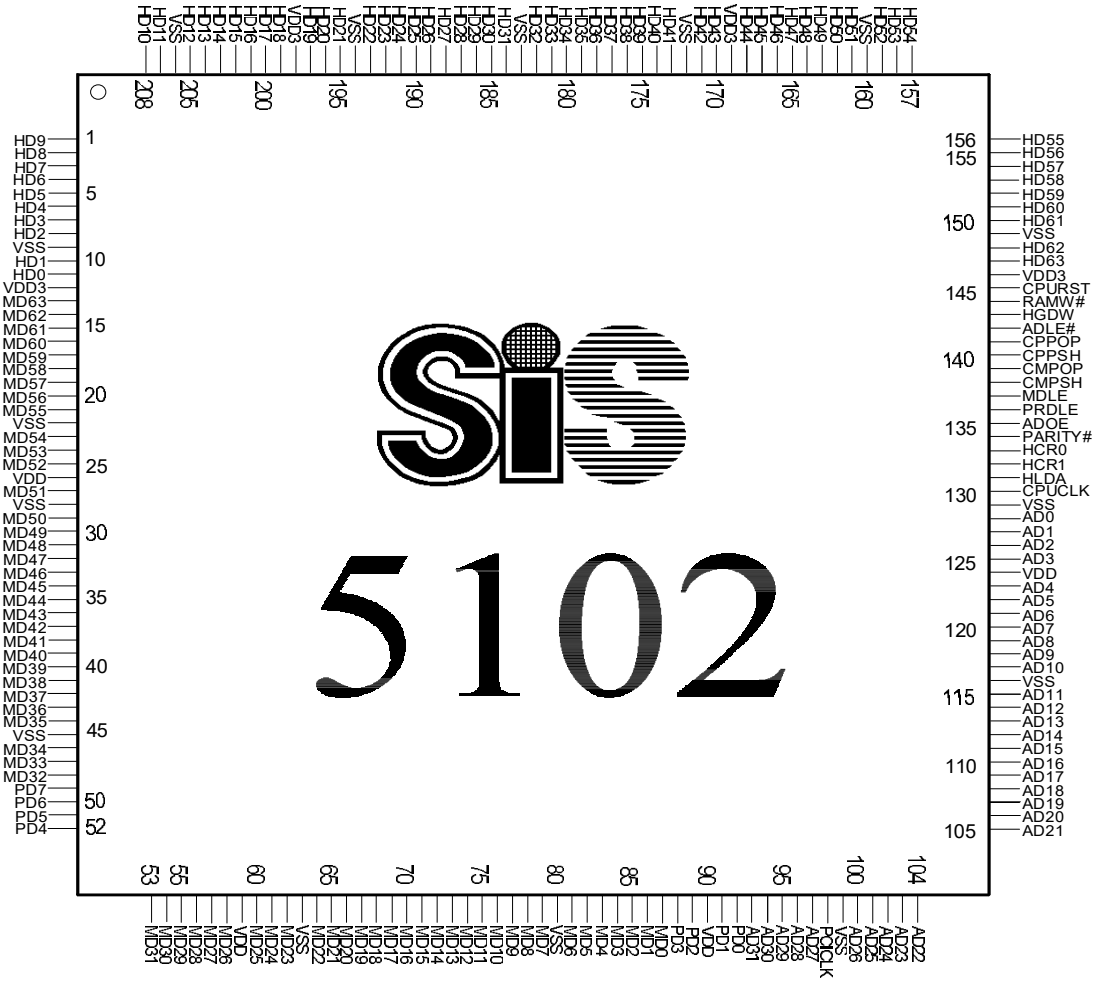
3.3.4 Address Flow and Data Flow of Basic Cycles

Cycles	Address Flow	Data Flow
1. CPU/R/PCI	HAÜ5101ÜAD	ADÜ5102ÜHD
2. CPU/W/PCI	HAÜ5101ÜAD	HDÜ5102ÜAD
3. CPU/R/ISA	HAÜ5101ÜADÜ5103ÜLA,SA	SDÜ5103ÜADÜ5102ÜHD
4. CPU/W/ISA	HAÜ5101ÜADÜ5103ÜLA,SA	HDÜ5102ÜADÜ5103ÜSD
5. CPU/R/DRAM	HAÜ5101ÜMA	MDÜ5102ÜHD
6. CPU/W/DRAM	HAÜ5101ÜMA	HDÜ5102ÜMD
7. CPU/R/L2	Independent	Independent
8. CPU/W/L2	Independent	Independent
9. CPU/R/PCI (master abort)	HAÜ5101ÜAD	5102ÜHD
10. PCI/R/L2	ADÜ5101ÜHA	HDÜ5102ÜAD
11. PCI/W/L2	ADÜ5101ÜHA	ADÜ5102ÜHD
12. PCI/R/DRAM	ADÜ5101ÜHA	MDÜ5102ÜAD
13. PCI/W/DRAM	ADÜ5101ÜHA	ADÜ5102ÜMD
14. ISA/R/L2	LA,SAÜ5103ÜADÜ5101ÜHA	HDÜ5102ÜADÜ5103ÜSD
15. ISA/W/L2	LA,SAÜ5103ÜADÜ5101ÜHA	SDÜ5103ÜADÜ5102ÜHD
16. DMA/R/L2	5103ÜADÜ5101ÜHA, 5103Ü LA,SA	HDÜ5102ÜADÜ5103ÜSD
17. DMA/W/L2	5103ÜADÜ5101ÜHA, 5103Ü LA,SA	SDÜ5103ÜADÜ5102ÜHD

18. ISA/R/DRAM	LA,SAÜ5103ÜADÜ5101ÜMA	MDÜ5102ÜADÜ5103ÜSD
19. ISA/W/DRAM	LA,SAÜ5103ÜADÜ5101ÜMA	SDÜ5103ÜADÜ5102ÜMD
20. DMA/R/DRAM	5103ÜADÜ5101ÜMA, 5103Ü LA,SA	MDÜ5102ÜADÜ5103ÜSD
21. DMA/W/DRAM	5103ÜADÜ5101ÜMA, 5103Ü LA,SA	SDÜ5103ÜADÜ5102ÜMD
22. ISA Refresh	5103ÜSA	

3.4 Pin Assignment and Description

3.4.1 SiS5102 Pin Assignment



3.4.2 SiS5102 Pin Listing

1=HD9	B	53=MD31	A	105=AD21	A	157=HD54	B
2=HD8	B	54=MD30	A	106=AD21	A	158=HD53	B
3=HD7	B	55=MD29	A	107=AD19	A	159=HD52	B
4=HD6	B	56=MD28	A	108=AD18	A	160=VSS	
5=HD5	B	57=MD27	A	109=AD17	A	161=HD51	B
6=HD4	B	58=MD26	A	110=AD16	A	162=HD50	B
7=HD3	B	59=VDD5	A	111=AD15	A	163=HD49	B
8=HD2	B	60=MD25	A	112=AD14	A	164=HD48	B
9=VSS		61=MD24	A	113=AD13	A	165=HD47	B
10=HD1	B	62=MD23	A	114=AD12	A	166=HD46	B
11=HD0	B	63=VSS		115=AD11	A	167=HD45	B
12=VDD1	B	64=MD22	A	116=VSS		168=HD44	B
13=MD63	A	65=MD21	A	117=AD10	A	169=VDD1	B
14=MD62	A	66=MD20	A	118=AD9	A	170=HD43	B
15=MD61	A	67=MD19	A	119=AD8	A	171=HD42	B
16=MD60	A	68=MD18	A	120=AD7	A	172=VSS	
17=MD59	A	69=MD17	A	121=AD6	A	173=HD41	B
18=MD58	A	70=MD16	A	122=AD5	A	174=HD40	B
19=MD57	A	71=MD15	A	123=AD4	A	175=HD39	B
20=MD56	A	72=MD14	A	124=VDD5	A	176=HD38	B
21=MD55	A	73=MD13	A	125=AD3	A	177=HD37	B
22=VSS		74=MD12	A	126=AD2	A	178=HD36	B
23=MD54	A	75=MD11	A	127=AD1	A	179=HD35	B
24=MD53	A	76=MD10	A	128=AD0	A	180=HD34	B
25=MD52	A	77=MD9	A	129=VSS		181=HD33	B
26=VDD5	A	78=MD8	A	130=CPUCLK	A	182=HD32	B
27=MD51	A	79=MD7	A	131=HLDA	A	183=VSS	
28=VSS		80=VSS		132=HCR1	A	184=HD31	B
29=MD50	A	81=MD6	A	133=HCR0	A	185=HD30	B
30=MD49	A	82=MD5	A	134=PARITY#	A	186=HD29	B
31=MD48	A	83=MD4	A	135=ADOE	A	187=HD28	B
32=MD47	A	84=MD3	A	136=PRDLE	A	188=HD27	B
33=MD46	A	85=MD2	A	137=MDLE	A	189=HD26	B
34=MD45	A	86=MD1	A	138=CMPSH	A	190=HD25	B
35=MD44	A	87=MD0	A	139=CMPOP	A	191=HD24	B
36=MD43	A	88=PD3	A	140=CPPSH	A	192=HD23	B
37=MD42	A	89=PD2	A	141=CPPOP	A	193=HD22	B
38=MD41	A	90=VDD5	A	142=ADLE#	A	194=VSS	
39=MD40	A	91=PD1	A	143=HGDW	A	195=HD21	B
40=MD39	A	92=PD0	A	144=RAMW#	A	196=HD20	B
41=MD38	A	93=AD31	A	145=CPURST	A	197=HD19	B
42=MD37	A	94=AD30	A	146=VDD1	B	198=VDD1	B
43=MD36	A	95=AD29	A	147=HD63	B	199=HD18	B
44=MD35	A	96=AD28	A	148=HD62	B	200=HD17	B
45=VSS		97=AD27	A	149=VSS		201=HD16	B
46=MD34	A	98=PCICLK	A	150=HD61	B	202=HD15	B
47=MD33	A	99=VSS		151=HD60	B	203=HD14	B
48=MD32	A	100=AD26	A	152=HD59	B	204=HD13	B
49=PD7	A	101=AD25	A	153=HD58	B	205=HD12	B
50=PD6	A	102=AD24	A	154=HD57	B	206=VSS	
51=PD5	A	103=AD23	A	155=HD56	B	207=HD11	B
52=PD4	A	104=AD22	A	156=HD55	B	208=HD10	B

Remark : "A"=Power Group A "B"=Power Group B

3.4.3 5102 Pin Description

Pin No.	Symbol	Type	Function
147,148 150-159 161-168 170,171 173-182 184-193 195-197 199-205 207,208 1-8,10,11	HD[63:0]	I/O	CPU data bus.
13-21,23-25, 27,29-44,46-48, 53-58 60-62,64-79, 81-87	MD[63:0]	I/O	Memory data bus.
93-97, 100-115, 117-123 125-128	AD[31:0]	I/O	PCI address/data bus.
91,92,49-52, 88,89	PD[7:0]	I/O	Parity bit bus.
134	PARITY#	O	Parity Error signal , no parity system should be pull high
135	ADOE	I	Drive PCI AD bus. This signal is used to enable the 5102 to drive PCI AD bus. It is asserted in CPU writes PCI or PCI master reads local memory cycles.
131	HLDA	I	Hold Acknowledge is asserted in response to the assertion of CPUHLDA.
137	MDLE	I	Memory data Read Latch Enable. This signal latches the data on the MD bus when negated.
142	ADLE#	I	AD Bus Data Latch Enable. This signal has the following functions: 1.Latch HD or MD data into the PCI read buffer (PRMB) 2.Latch AD data into CPU read PCI buffer on the rising edge of PCICLKI. 3.Latch AD data into PCI posted write buffer (PTMPB) on the rising edge of PCICLKI.

140	CPPSH	I	Push Post Write Data into the CTPPB of the 5102. The data on the HD bus is latched into the CTPPB on CPPSH rising edge. The edge also increases the write pointer to the next available loading entry in the buffer.
141	CPPOP	I	On the rising edge of CPPOP, the read pointer is changed to address the next available reading location.
138	CMPSH	I	When this signal is asserted, the data on the HD bus is written into the CPU to memory posted write buffer (CTMPB) on the rising edge of CPUCLK, and the write pointer is also changed to address the next available location.
139	CMPOP	I	When this signal is asserted, the read pointer of the CTMPB is increased on the rising edge of CPUCLK.
136	PRDLE	I	This signal latches the current output entry of the CTPPB, the CPU to PCI post write buffer, into the prelatch in the 5102. The output of the prelatch is driven to the PCI AD bus. In the PCI master cycles, PRDLE is also asserted when PCI master is reading data from the secondary cache, or when PCI master is writing data to local memory.
143	HGDW	I	High Double Word Indicator. The signal is driven high by the 5101 when : (1) a high DW from HD bus is written into CPU to PCI Posted Write Buffer, (2) the CPU reads a high DW from PCI bus, (3) PCI master writes a high DW to local memory, (4) PCI master reads a high DW from local memory.
132,133	HCR[1:0]	I	Host Data Bus Control. These signals are driven by the 5101 and they are used to control the 5102 HD[63:0] bus. They are defined as: 00: 5102 floats HD bus 01: 5102 drives FFFFFFFF to HD bus 10: 5102 drives data from AD bus to HD bus 11: 5102 drives data from MD bus to HD bus
144	RAMW#	I	DRAM Write Enable.
145	CPURST	I	CPU Reset.
130	CPUCLK	I	CPU Clock.
98	PCICLK	I	PCI Bus Clock.
26,59,90, 124	VDD5		For Power Group A

12, 146, 169, 198	VDD1		For Power Group B
9,22,28,45,6,3,80,99,116,129,149,160,172,183,194,206	VSS		Ground

3.5 Electrical Characteristics

3.5.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{O}C
Storage temperature	-40	125	^{O}C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V
Power Dissipation		1	W

Note:
Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

3.5.2 DC Characteristics

TA = 0 - 85 ^{O}C, VSS = 0V , VDD5=5V$\pm$5%, VDD1=3.3V$\pm$5% or 5V$\pm$5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL1}	Input Low Voltage	-0.3	0.8	V	*Note 1*, VDD1
V_{IH1}	Input High Voltage	2.2	VDD3+0.3V	V	*Note 1*
V_{IL2}	Input Low Voltage	-0.3	0.8	V	*Note 2*
V_{IH2}	Input High Voltage	2.2	VDD+0.3	V	*Note 2*
V_{OL1}	Output Low Voltage		0.45	V	*Note 3*
V_{OH1}	Output High Voltage	2.4		V	*Note 3*
V_{OL2}	Output Low Voltage		0.4	V	*Note 4*
V_{OH2}	Output High Voltage	2.0	VDD3	V	*Note 4*
I_{OL1}	Output Low Current	4		mA	*Note 5*
I_{OH1}	Output High Current	4		mA	*Note 5*
I_{IH}	Input Leakage Current		+10	mA	
I_{IL}	Input Leakage Current		-10	mA	
C_{IN}	Input Capacitance		12	pF	Fc=1 Mhz
C_{OUT}	Output Capacitance		12	pF	Fc=1 Mhz
$C_{I/O}$	I/O Capacitance		12	pF	Fc=1 Mhz
ICC3	Power Supply Current of VDD1		27	mA	3.3V, 66MHz

Note:

1. V_{IL1} and V_{IH1} apply to the following signals: HD[63:0].
2. V_{IL2} and V_{IH2} apply to the following signals: MD[63:0], AD[31:0], CPURST, PD[7:0], CPUCLK, ADOE, HLDA, HCR[1:0], PRDLE, MDLE, CMPSH, CMPOP, CPPSH, CPPOP, ADLE#, HGDW, RAMW#.
3. V_{OL1} and V_{OH1} apply to the following signals: MD[63:0], AD[31:0], PD[7:0], PARITY#.
4. V_{OL2} and V_{OH2} apply to the following signals: HD[31:0].
5. I_{OL1} and I_{OH1} apply to the following signals: HD[63:0], MD[63:0], AD[31:0], PD[7:0], PARITY#.

3.5.3 AC Characteristics

Symbol	Parameter	Min	Typ	Max	Fig
T1	MD Data Setup Time to MDLE falling		6		3.2, 3.9
T2	MD Data Hold Time to MDLE falling	2			3.2, 3.9
T3	HD Data Valid Delay from MD data valid	10	15		3.2
T4	ADLE# Setup Time to PCICLK rising	6			3.3,3.8
T5	ADLE# Hold Time to PCICLK rising	2			3.3,3.8
T6	HGDW Setup Time to PCICLK rising	6			3.3,3.8
T7	HGDW Hold Time to PCICLK rising	2			3.3,3.8
T8	AD Data Setup Time to PCICLK rising	6			3.3,3.8
T9	AD Data Hold Time to PCICLK rising	2			3.3,3.8
T10	HD Data Valid Delay from PCICLK rising	10	15		3.3,3.8
T11	CMPSH Setup Time to CPUCLK rising	6			3.4
T12	CMPSH Hold Time to CPUCLK rising	2			3.4
T13	CMPOP Setup Time to CPUCLK rising	6			3.4
T14	CMPOP Hold Time to CPUCLK rising	2			3.4
T15	HD Data Setup Time to CPPSH rising	6			3.4,3.5
T16	HD Data Hold Time to CPPSH rising	2			3.4,3.5
T17	MD Data Valid Delay from CPUCLK rising	12	20		3.4
T18	PD Data Valid Delay from CPUCLK rising	15	25		3.4
T19	RAMW# Setup Time to MDLE rising				3.7
T20	RAMW# Hold Time to MDLE falling				3.7
T21	PARITY# Active Delay from MDLE falling	6	9		3.7
T22	AD Data Valid from PRDLE rising	7	11		3.6
T23	AD Data Valid from MD data valid	12	18		3.10
T24	HGDW Setup Time to CPPSH rising	6			3.5
T25	HGDW Hold Time to CPPSH rising	2			3.5
T26	MD Data Valid Delay from PCICLK rising	12	18		3.8
T27	PD Data Valid Delay from PCICLK rising	15	23		3.8
T28	HD Data Setup Time to ADLE# falling	6			3.9
T29	HD Data Hold Time to ADLE# falling	2			3.9

T30	AD Data Valid Delay from HD data valid	12	18		3.9
T31	MD Output Delay from RAMW# asserted	5	7.5		3.11
T32	MD Output Float Delay from RAMW# inactive	25	43		3.11
T33	AD Output Delay from ADOE asserted	4	6		3.12
T34	AD Output Float Delay from ADOE inactive			26	3.12
T35	HD Output Delay from HCR asserted	6	9		3.13
T36	HD Output Float Delay from HCR inactive				3.13

Unit :ns

3.5.4 AC Timing Diagram

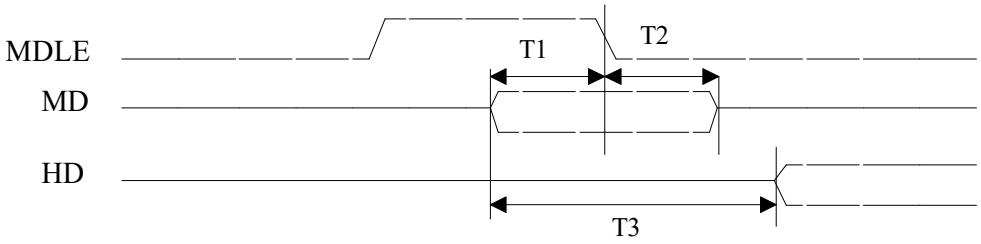


Figure 3.2 CPU Read DRAM Cycle

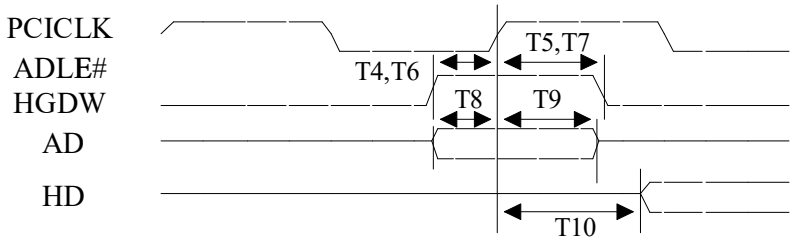


Figure 3.3 CPU Read PCI Slave Cycle

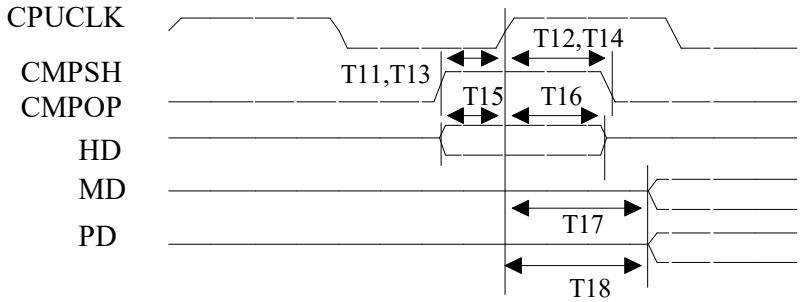


Figure 3.4 CPU Write DRAM Cycle

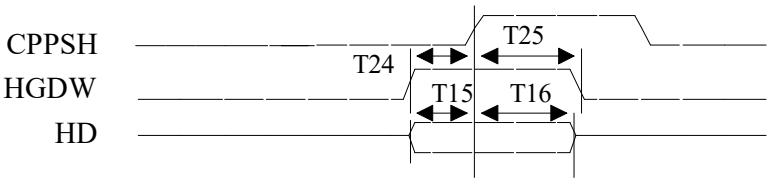


Figure 3.5 CPU Write PCI Post Write Buffer

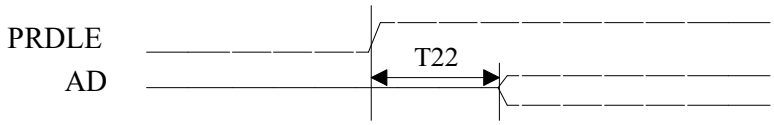


Figure 3.6 Write Posted Data onto PCI Bus

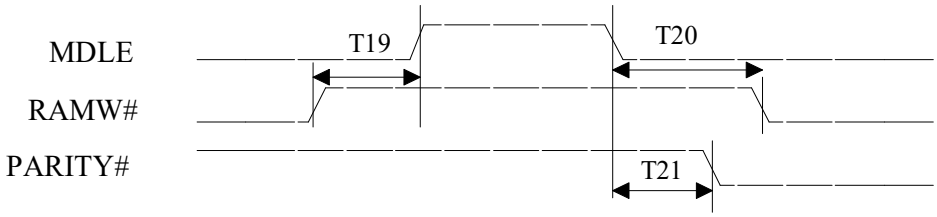


Figure 3.7 PARITY# Generation Reading DRAM Cycle

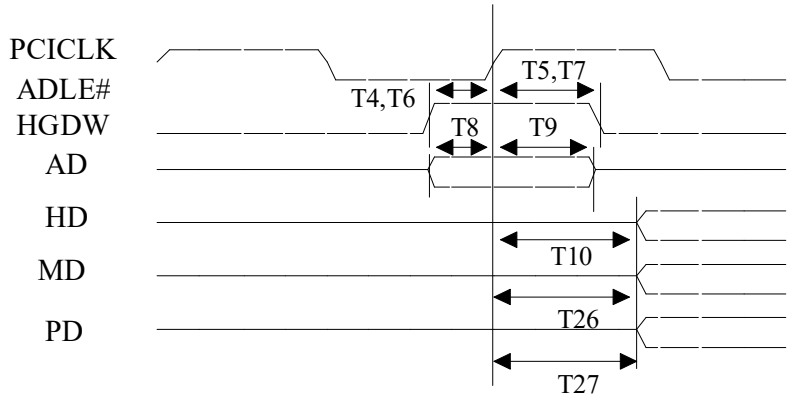


Figure 3.8 CPU Read PCI Slave Cycle

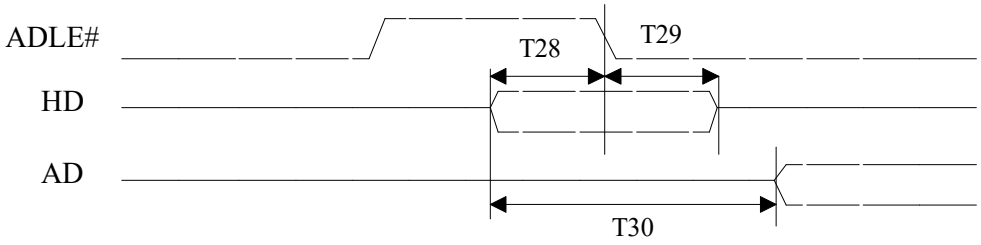


Figure 3.9 PCI Master Read Secondary Cache

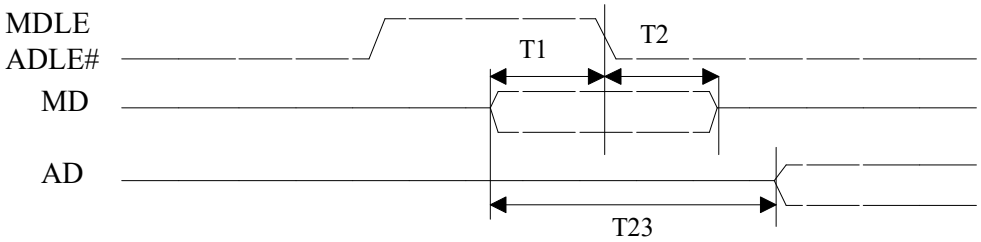


Figure 3.10 PCI Master Read DRAM

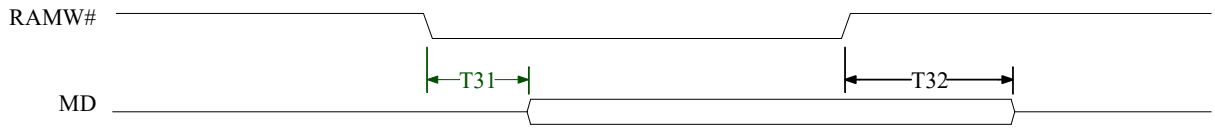


Figure 3.11 CPU Write DRAM Cycle

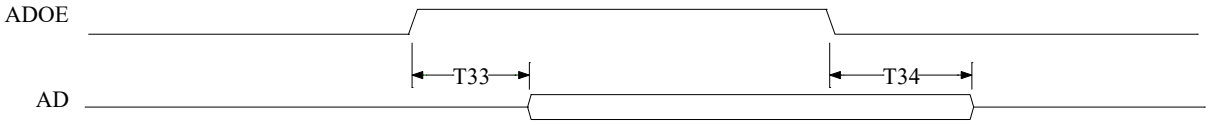


Figure 3.12 Write Posted Data onto PCI Bus

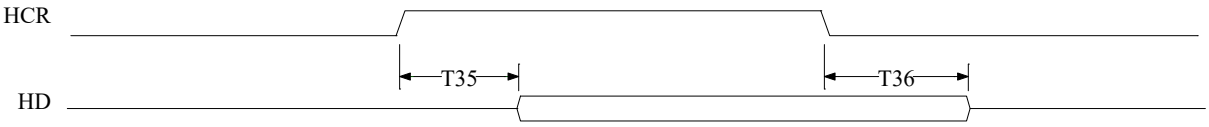


Figure 3.13 CPU Read DRAM or PCI Cycle

4. SiS5103

4.1 Features

- **Integrated Bridge Between PCI Bus and ISA Bus**
  - Translates PCI Bus Cycles into ISA Bus Cycles
  - Translates ISA Master or DMA Cycles into PCI Bus Cycles
  - Provides PCI-to-ISA Memory one Double Word Posted Write Buffer
- **Integrated ISA Bus Compatible Logic**
  - ISA Bus Controller
  - ISA Arbiter for ISA Master, DMA Devices, and Refresh
  - Built-in Two 8237 Compatible DMA Controllers
  - Built-in Two 8259A Compatible Interrupt Controllers
  - Built-in One 8254 Timer
- **Supports Reroutibility of four PCI Interrupts to Any Unused IRQ Interrupt**
- **Supports Flash ROM**
- **Built-in RTC with 242 Bytes Extended CMOS SRAM**
- **Built-in PCI IDE**
  - Fully compatible with PCI local bus specification V2.0.
  - Accommodates 8 bits, 16 bits, and 32 bits data transfer.
  - Supports PCI burst read/write operation.
  - Supports read ahead & posted write buffers for concurrent system operation.
  - Controls two IDE channels and max. connects 4 IDE drives.
  - Supports PIO mode 4 timing proposal on enhanced IDE specifications.
  - Programmable command and recovery timing for reads and writes per channel.
  - Auto IDE channel speed setting with software driver.
  - Hardware and software chip disable capability
  - Supports power down feature
- **Meet PCI Specification Buffer Strength**
- **Supports CPU Thermal Detection**
- **Supports CPU Throttling and Clock Slow Down**
- **Supports Software SMI and Software Stop Clock Port**
- **Supports Microsoft APM spec.**
- **Supports User Register 32-bit**
- **External Hardware SMI Request Support**
  – EXTSUSP , GPIO[3:0] , PIO[6:0] , UIP[2:0]
- **Supports Four Power Management Mode**
  – Local Auto Doze Mode
  – Global Auto Doze Mode
  – Standby Mode
  – Suspend Mode

- **Supports Programmable PMU Timer**
  - Seven sub-Doze Timer: 31mS/ 125mS/ 05.Sec/ 1Sec/ 1.5Sec/ 2Sec/ 3Sec
  - Standby Time: 4 Sec ~5 min
  - Suspend Time: 1 min ~ 60 min
  - Hard Disk Monitor Timer ÷ 1 min ~ 30 min
  - General Purpose Timer during SUSPEND ÷ 1 sec ~ 60 min
- **Battery Management**
  - AC Power Indicator
  - Multi-level low Battery Monitor: LB, LLB
  - Battery low SMI Generation
- **Supports Suspend to Hard Disk**
  - Read only Shadow Register
- **Supports Suspend to Memory**
- **Supports DOZE , STANDBY and SUSPEND Modes Status Output Pin**
- **Supports ISA Leakage Control**
- **Standby/Resume Toggle Switch**
- **Suspend/Resume Button Switch**
- **Modem Ring/GPIO Wake Up**
- **Supports Hot Docking**
- **208-Pin PQFP/TQFP Package**
- **0.6µm CMOS Technology**

4.2 SiS5103 Functional Block Diagram

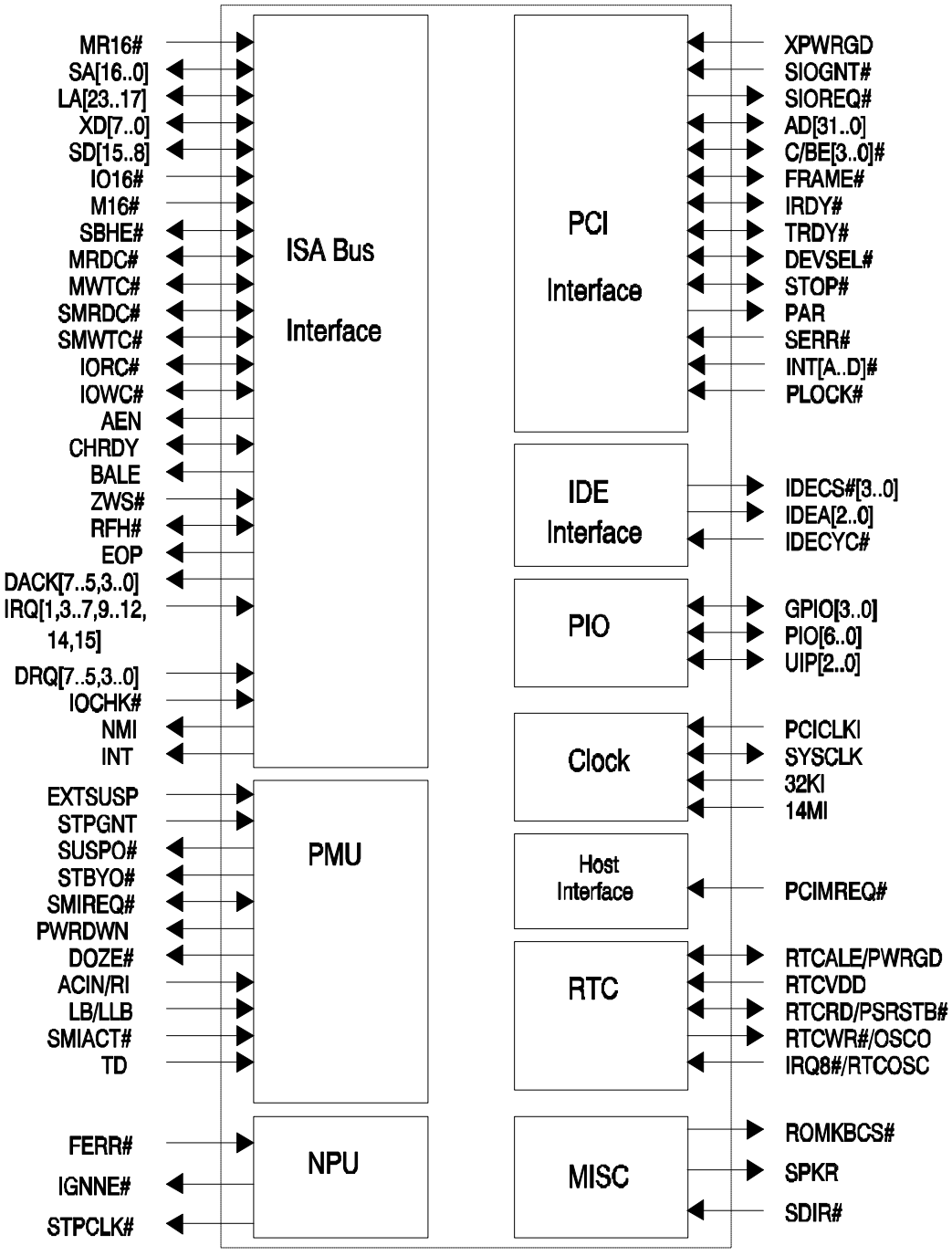


Figure 4.1 SiS 5103 Functional Diagram

4.3 SiS5103 Functional Description

The SiS5103 is a highly integrated PCI/ISA System I/O and Power Management Unit (SIOP) device that integrates all the necessary system control logic used in PCI/ISA specific applications and the Power Management Unit. The System I/O consists of a PCI bridge that translates PCI cycles onto ISA bus, and ISA master/DMA device cycles onto PCI bus; a seven-channel programmable DMA Controller, a sixteen-level programmable interrupt controller, a programmable timer with three counters, a built-in RTC with 242 bytes extended CMOS SRAM, and a built-in PCI IDE.

Since SiS5103 includes a PCI to ISA bridge and a PCI IDE, it becomes a multifunction device. The PCI/ISA bridge is defined as function 0 device while PCI IDE is function 1 device. The following two examples describe how to write register XX in PCI to ISA bridge configuration space and register YY in PCI IDE configuration space.

Example 1:
MOV EAX, 800010XXh
OUT 0CF8h, EAX
MOV AL, data
OUT 0CFDh, AL

Example 2:
MOV EAX, 800011YYh
OUT 0CF8h, EAX
MOV AL, data
OUT 0CFDh, AL

Power management is an indispensable feature of portable computer, SiS5100 offers three PMU modes (DOZE, STANDBY and SUSPEND) and leakage control for reducing power consumption. Seven timers are provided to support DOZE mode. In addition, special I/O control pins such as four GPIOs, seven PIOs, three UIPs are provided to support STANDBY mode and SUSPEND mode. Maximum Power saving can be achieved by well managed of the above three modes. For detailed flow chart of PMU, please refer to figure 4.1.

4.3.1 PCI Bridge

The SiS5103 PCI bus interface provides the interface between SIOP and the PCI bus. It contains both PCI master and slave bridge to the PCI bus. When SIOGNT# is asserted, the master bridge translates the ISA master or DMA cycles onto the PCI bus based on the decoding status from ISA address decoder. When SIOGNT# is negated, the slave bridge accepts these cycles initiated on the PCI bus targeted to the SIOP internal registers or ISA bus, and then forwards the cycles to the ISA Bus Interface that further translates them onto the ISA Bus. The PCI address decoder provides the information on which the slave bridge depends to respond and process the cycle initiated by PCI Masters.

4.3.2 PCI Slave Bridge

As a PCI slave, SIOP responds to both I/O and memory transfers. SIOP always target-terminates after the first data phase for any bursting cycle.
SiS5103 always converts the single interrupt acknowledge cycle (from 5101) into two cycles that the internal 8259 pair can respond to.
The SIOP is assigned as the subtractive decoder in the Bus 0 of the SiS PCI/ISA system by accepting all accesses not positively decoded by some other agent. In reality, the SIOP only subtractively responds to low 64K I/O or low 16M memory accesses. SIOP also positively decodes I/O addresses for internal registers, and BIOS memory space by asserting DEVSEL# on the medium timing.

4.3.3 PCI Master Bridge

As long as SIOGNT# is asserted, the PCI master bridge on behalf of DMA devices or ISA Masters starts to drive the AD bus, C/BE[3:0]# and PAR signal. When MRDC# or MWTC# is asserted, the SIOP will generate FRAME#, and IRDY# to PCI bus if the targeted memory is not on the ISA side.
The valid address and command are driven during the address phase, and PAR is asserted one clock after that phase. SIOP always activated FRAME# for 2 PCLKs because it does not conduct any bursting cycle.
The ISA address decoder is used to determine the destination of ISA master or DMA devices.

This decoder provides the following options as they are defined in configuration registers 48 to 4B.

a. Memory: 0-512K
b. Memory: 512K-640K
c. Memory: 640K-768K(video buffer)
d. Memory: 768K-896K in eight 16K sections(Expansion ROM)
e. Memory: 896K-960K(lower BIOS area)
f. Memory: 1M-XM-16M within which a hole can be opened. Access to the hole is not forwarded to PCI bus.
g. Memory : > 16Mb automatically forwards to PCI.

4.3.4 ISA Bus Controller

The SiS5103 ISA Bus Interface accepts those cycles from PCI bus interface and then translates them onto the ISA bus. It also requests the PCI master bridge to generate PCI cycle on behalf of DMA or ISA master.
The ISA bus interface thus contains a standard ISA Bus Controller and a Data Buffering logic. IBC provides all the ISA control, such as ISA command generation, I/O recovery control, wait-state insertion, and data buffer steering.
The PCI to/from ISA address and data bus bufferings are also all integrated in SiS5103. The SiS5103 can directly support six ISA slots without external data or address buffering.

Standard ISA bus refresh is requested by Counter 1, and then performed via the IBC. IBC generates the pertinent command and refreshes address to the ISA bus.
Since the ISA refresh is transparent to the PCI bus and the DMA cycle, an arbiter is employed to resolve the possible conflicts among PCI cycles, refresh cycles, and DMA cycles.

4.3.5 DMA Controller

The SiS5103 contains a seven-channel DMA controller. The channel 0 to 3 is for 8-bit DMA devices while channel 5 to 7 is for 16-bit devices. The channels can also be programmed for any of the four transfer modes, which include single, demand, block, and cascade.
Except in cascade mode, each of the three active transfer modes can perform three different types of transfers, which include read, write, and verify.
The address generation circuitry in SiS5103 can only support 24-bit address for DMA devices.

4.3.6 Interrupt Controller

The SiS5103 provides an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 14 external and two internal interrupts are supported.
The master interrupt controller provides IRQ<7:0> and the slave one provides IRQ<15:8>. The two internal interrupt are used for internal functions only and are not available externally. IRQ2 is used to cascade the two controllers together and IRQ0 is used as a system timer interrupt and is tied to interval Counter 0. The remaining 14 interrupt lines are available for external system interrupts.

Priority	Label	Controller	Typical Interrupt Source
1	IRQ0	1	Timer/Counter 0 Out
2	IRQ1	1	Keyboard
3-10	IRQ2	1	Interrupt from Controller 2
3	IRQ8#	2	Real Time Clock
4	IRQ9	2	Expansion bus pin B04
5	IRQ10	2	Expansion bus pin D03
6	IRQ11	2	Expansion bus pin D04
7	IRQ12	2	Expansion bus pin D05
8	IRQ13	2	Coprocessor Error FERR#
9	IRQ14	2	Fixed Disk Drive Controller Expansion bus pin D07
10	IRQ15	2	Expansion bus pin D06
11	IRQ3	1	Serial port 2, Expansion Bus B25
12	IRQ4	1	Serial port 1, Expansion Bus B24
13	IRQ5	1	Parallel Port 2, Expansion Bus B23
14	IRQ6	1	Diskette Controller, Expansion Bus B22
15	IRQ7	1	Parallel Port, Expansion Bus B21

In addition to the ISA features, the ability to do interrupt sharing is included. Two registers(ECLR) located at 4D0h and 4D1h are defined to allow edge or level sense selection

to be made on an individual channel by channel basis instead of on a complete bank of channels.
Note that the default of IRQ0, IRQ1, IRQ2, IRQ8# and IRQ13 is edge sensitive, and can not be programmed. Also, each PCI Interrupt(INTx#) can be programmed independently to route to one of the eleven ISA compatible interrupts(IRQ<7:3>, IRQ<15:14>, and IRQ<12:9>) through configuration registers 41h to 44h.

4.3.7 Timer/Counter

The SiS5103 contains 3 channel counter/timer that is equivalent to those found in the 82C54 programmable interval timer. The counters use a division of 14.31818MHz OSC input as the clock source.
The outputs of the timers are directed to key system functions. Counter 0 is connected to the interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or the other system timing function. Counter 1 generates a refresh-request signal and Counter 2 generates the tone for the speaker.

4.3.8 Built-in RTC

The 5103 incorporates a real-time clock and system configuration memory. The RTC combines:
- A complete time-of-day clock with alarm
- 100 year calendar
- Programmable periodic interrupt
- 14 bytes of clock and control registers and 242 bytes of lower power general purpose SRAM

The method of accessing the upper 128 bytes of CMOS SRAM is to write 80h to I/O port 22h and then setting bit 3 of I/O port 23h.

4.3.9 Built-in PCI IDE

The internal PCI IDE contains five blocks. They are PCI Bus interface and decode, system configuration & control, IDE interface ckt, read ahead buffers, and posted write buffers.

PCI Bus Interface and Decode

The internal PCI IDE operates as a slave device. It decodes and interprets PCI cycles and generates signals to start and terminate IDE cycles.
This block responds only to cycles that belong to IDE I/O address space. It supports both 16-bit and 32-bit I/O data transfer at address 1F0/170. All other IDE registers R/W are 8-bit only.

System Configuration & Control & PCI Configuration

This block contains PCI configuration header and registers to meet PCI specifications.
The internal PCI IDE supports PCI type 0 configuration cycles of configuration mechanism #1.

IDE Interface Ckt

Proper cycle timing is generated to fit PCI Bus speed and different mode of IDE drive. All cycle timings can be programmed by software.

Posted Write Buffers & Read Ahead Buffers

The internal PCI IDE has two kinds of buffers, posted write buffers and read ahead buffers. They can be enabled or disabled independently.
The posted write buffers can enhance the transfer rate of the PCI Bus interface to IDE interface write operation by decoupling the wait-states effect from the slower IDE side to the faster PCI Bus side.
The read ahead buffers can eliminate the idle cycle of the PCI Bus side to improve read operation.

4.4 PMU Function

DOZE Mode

Doze is the first level PMU mode. After turning the notebook on, users don't work at all times. The SiS 5100 offer a very short timer to monitor whether system is working. These timers' periods are 31.25 ms, 125 ms, 0.5 sec, 1 sec, 1.5 sec, 2 sec and 3 sec. Figure 4.2 shows the doze timer flow chart. If system is idle and timer is time out, system goes into Doze mode. In Doze mode, SiS 5100 provide two functions for customers to design. One is throttling, the other is to slow down clock frequency. In addition, the 5103 also forces system into Doze mode if Reg AAh bit 7 is set to 1 and thermal is detected.

STANDBY Mode

The STANDBY mode is the second level of power conservation.
The SiS 5100 offer a unit of 4 sec timer to program Standby mode. In Standby mode, system clock is slowed down and some of peripheral devices can be turned off by GPIO or PIO or UIP pins. In addition, the SiS 5100 can go straight into Standby mode through any GPIO pin.

SUSPEND Mode

The SUSPEND mode is the deepest level of power conservation. The SiS 5100 offer a unit of 1 min. timer to program Suspend mode. System can enter into this mode by external switch or time out. In this mode, user can use GPIO, PIO and UIP to control peripheral devices.
The 5103 also offers leakage function in this mode.

Leakage Control

Leakage current has a big effect for power saving in portable computer. The SiS 5100 have leakage function to control leakage current in suspend mode. When leakage function is enable and system is in suspend mode, the SiS 5100 force signal to 0 level among CPU, PCI and ISA interface. In addition, the refresh function of SiS 5101, the PMU function and RTC function of SiS 5103 run at 32k frequency. Figure 4.3 shows the leakage function flow chart.

SMI#

The SMI function allows an external source to generate an SMI by asserting the SMI pin. The best way is to generate SMI routine through chipset. There are eleven paths to generate SMI routine in SiS 5100, including hardware time out, software register, LB, LLB, GPIO[3:0] and UIP[2:0]. The priority for these paths from highest to lowest is hardware time out, LLB, LB, GPIO3, GPIO2, GPIO1, GPIO0, UIP2, UIP1, UIP0 and software register. For application convenient, SiS 5100 offers 11 registers for BIOS to read and clear these registers automatically after SMI routine.

General Purpose I/O

For turning device power off and generating SMI# routine, the SiS 5100 utilize any GPIO pin to implement these function. The GPIO controls peripheral device power automatically in Standby or Suspend mode. When a GPIO pin is programmed to be an output pin, the SiS 5100 can turn peripheral device power off. When a GPIO pin is programmed to be an input pin, a peripheral device can regret the CPU to implement SMI function or enter Standby mode via the SiS 5100. In addition, the GPIO0 can be programmed to be a port enable signal. Figure 4.4 shows the SiS5100 GPIO flow chart.

PIO

The 5103 also offers a flexible way to read system status or to write a value to control peripheral device. Figure 4.5 shows the SiS5100 PIO flow chart.

When a PIO is programmed to be an output pin, the 5103 can control peripheral device through the PIO pin. When a PIO is programmed to be an input pin, it can lean any external signal or device status through the PIO pin.

UIP

For more SMI# toggle sources, the 5103 offers another way to enter SMI# function and write a value to control peripheral devices. Figure 4.5 shows the SiS5100 UIP flow chart.

When a UIP is programmed to be an output pin, the 5103 can control peripheral devices through the UIP pin. When a UIP just generates SMI# request as an input pin., a peripheral device can request SMI# through 5103.

Battery Management

The LB and LLB are two dedicated inputs. They are generated by external voltage compactor. They are used to show that the system is in low battery power if LB is active, or in very low battery power when LLB is active.

The LB and LLB can be used to issue SMI# to CPU, and enter proper power saving mode by SMI service routine. The system will wake up when system is in suspend mode and LLB is active.

This function is useful to inform the SMI handler to save the system's current status and then return power off mode or other proper power saving mode.

a. When Reg AAh bits[5:4] are set to [11], LB and LLB can generate SMI# signal.
b. When Reg ABh bits [1:0] are set to [11], LB and LLB can generate wakeup sources.
c. In the 5103, Reg AFh bits [5:4] are two read-only register bits to indicate the LB and LLB status.
d. When the PC is supplied with an AC power, the LB and LLB status registers are cleared, and the AC read-only register REG AFh bit 3 is set to 1.

Figure 4.5 shows the SiS5100 AC Power and LB/ LLB flow chart.

Throttling state

In throttling state, STPCLK# is asserted and de-asserted periodically. (i.e. STPCLK# keeps 1 ms high and 1 ms low)

Software SMI#

The software SMI function can be used by application software to take advantage of the power management features on the SiS5100. When Reg B6h bit 3 is set to 1, 5103 will generate SMI# source. 5103 will clear this bit automatically if Reg B4h bit 7 is set to 1.

Software STPCLK#

When Reg B6h bit 4 is set to 1, 5103 will generate STPCLK#. 5103 will de-assert STPCLK# if any programmed wakeup source is working.

External Switch

5103 offers an external switch for system to enter SUSPEND mode or leave SUSPEND mode. If Reg. AAh bit 6 is enable and system is not in SUSPEND mode, the external switch is pressed and it will let system enter SUSPEND mode. If system is in SUSPEND mode, the external switch is pressed and it will return system to NORMAL mode.

WakeUp Events

a. CPU is accessing PCI device or ISA device (Reg ABh bit 7)
b. IRQ is acting (Reg ABh bit 6, Reg 88h, Reg 89h)
c. DMA is acting (Reg ABh bit 5)
d. PCI master is acting (Reg ABh bit 4)
e. IO address trap (Reg ABh bit 3, Reg ACh)
f. RI is acting (Reg ABh bit 2)
g. LB is acting (Reg ABh bit 1)
h. LLB is acting (Reg ABh bit 0)
i. RTC alarm is acting (Reg A8h bit 2)

SiS5100 PMU Flow Chart

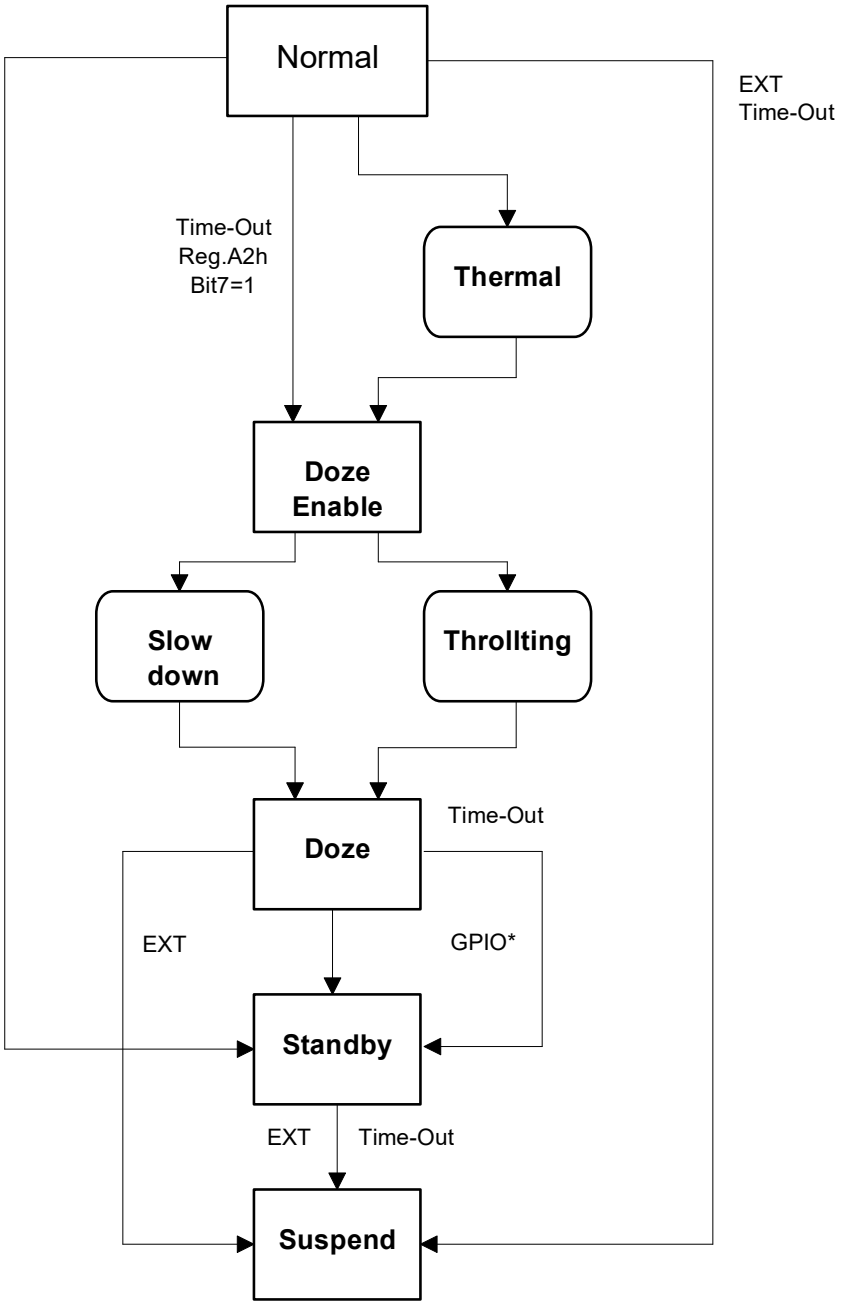


Figure 4.1 SiS5100 PMU Flow Chart

SiS5100 Doze Timer Flow Chart

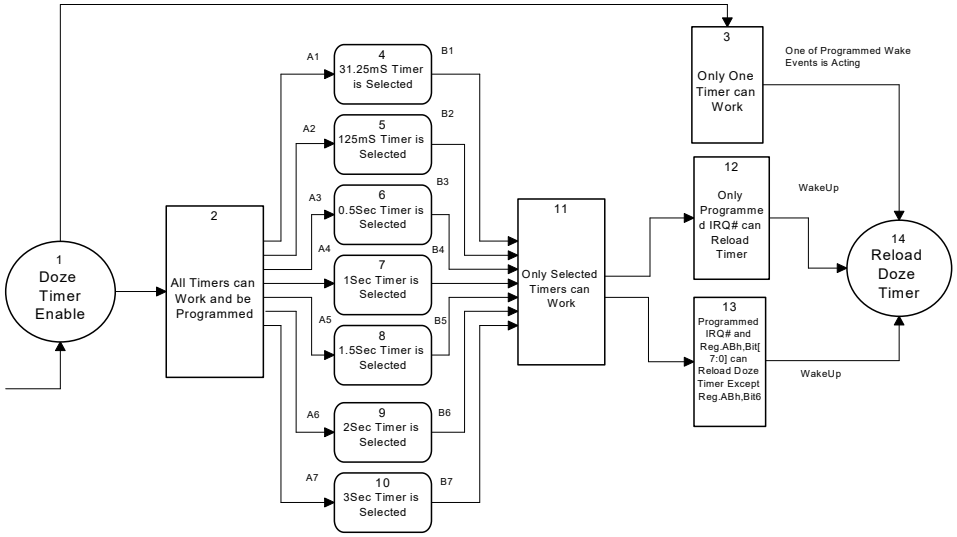


Figure 4.2 SiS5100 Doze Timer Flow Chart

Leakage Function Flow Chart

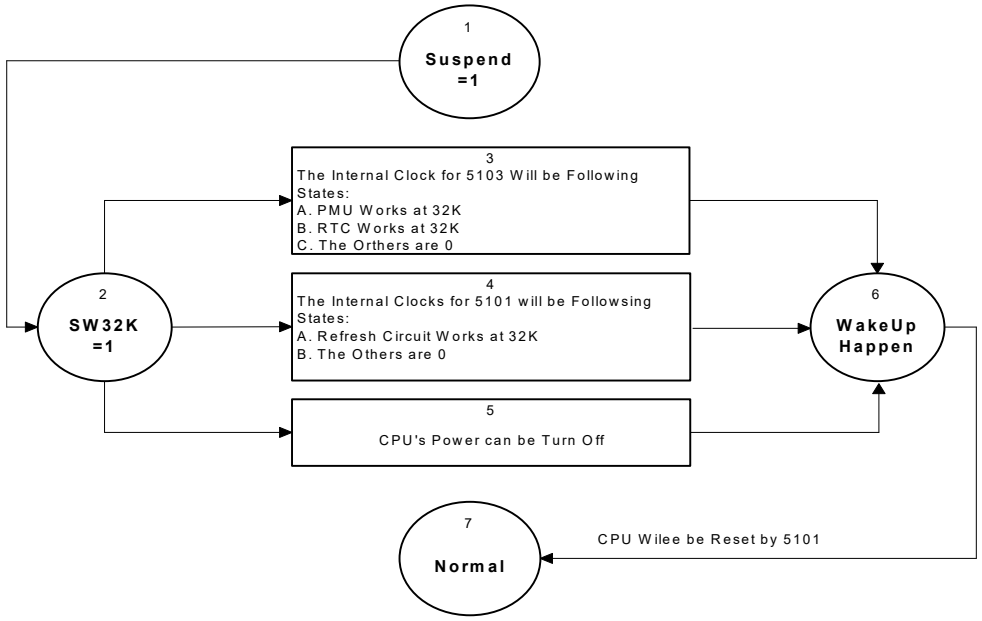


Figure 4.3 Leakage Function Flow Chart

Doze Function Flow Chart

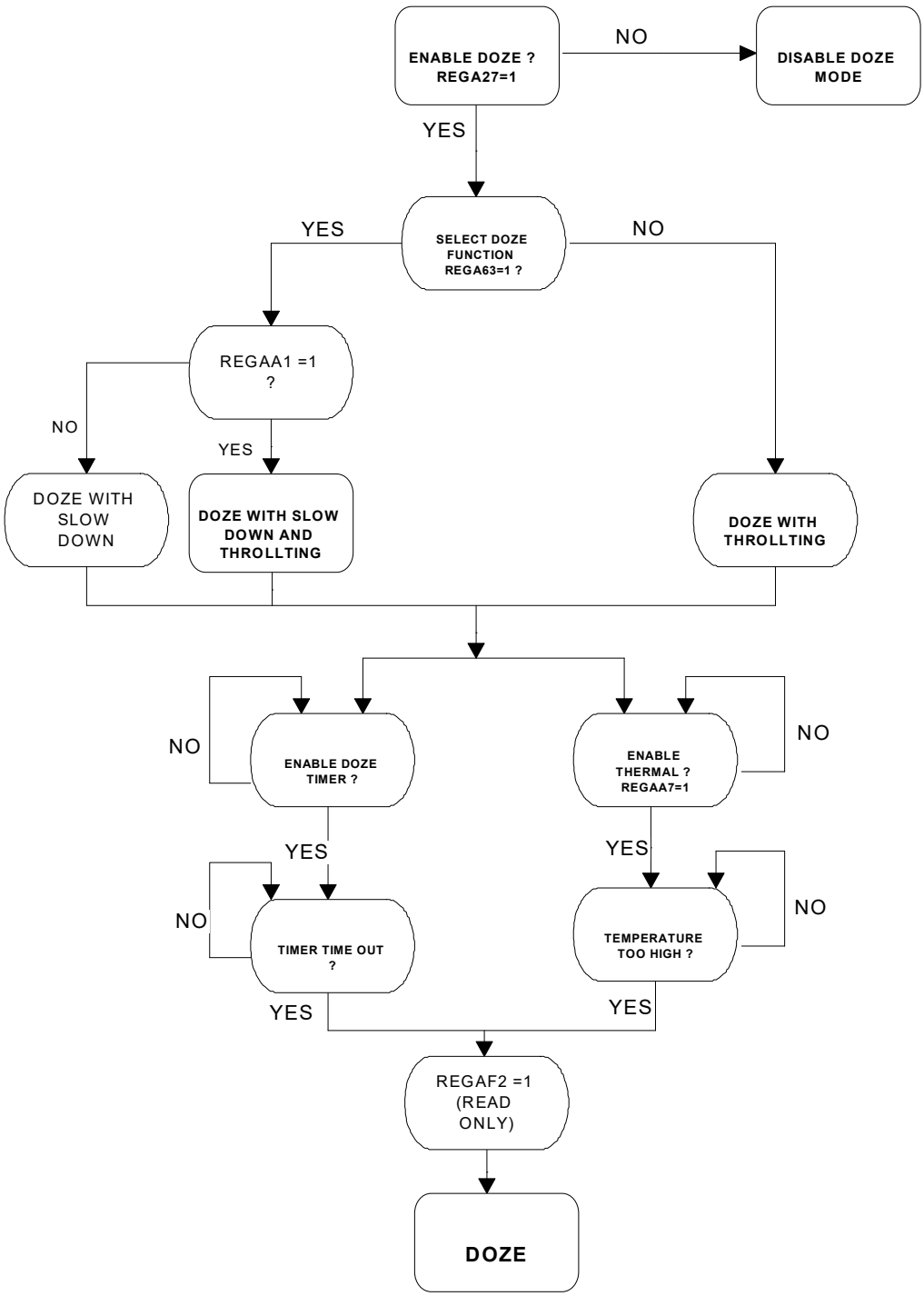


Figure 4.4 Doze Function Flow Chart

Standby Fucntion Flow Chart

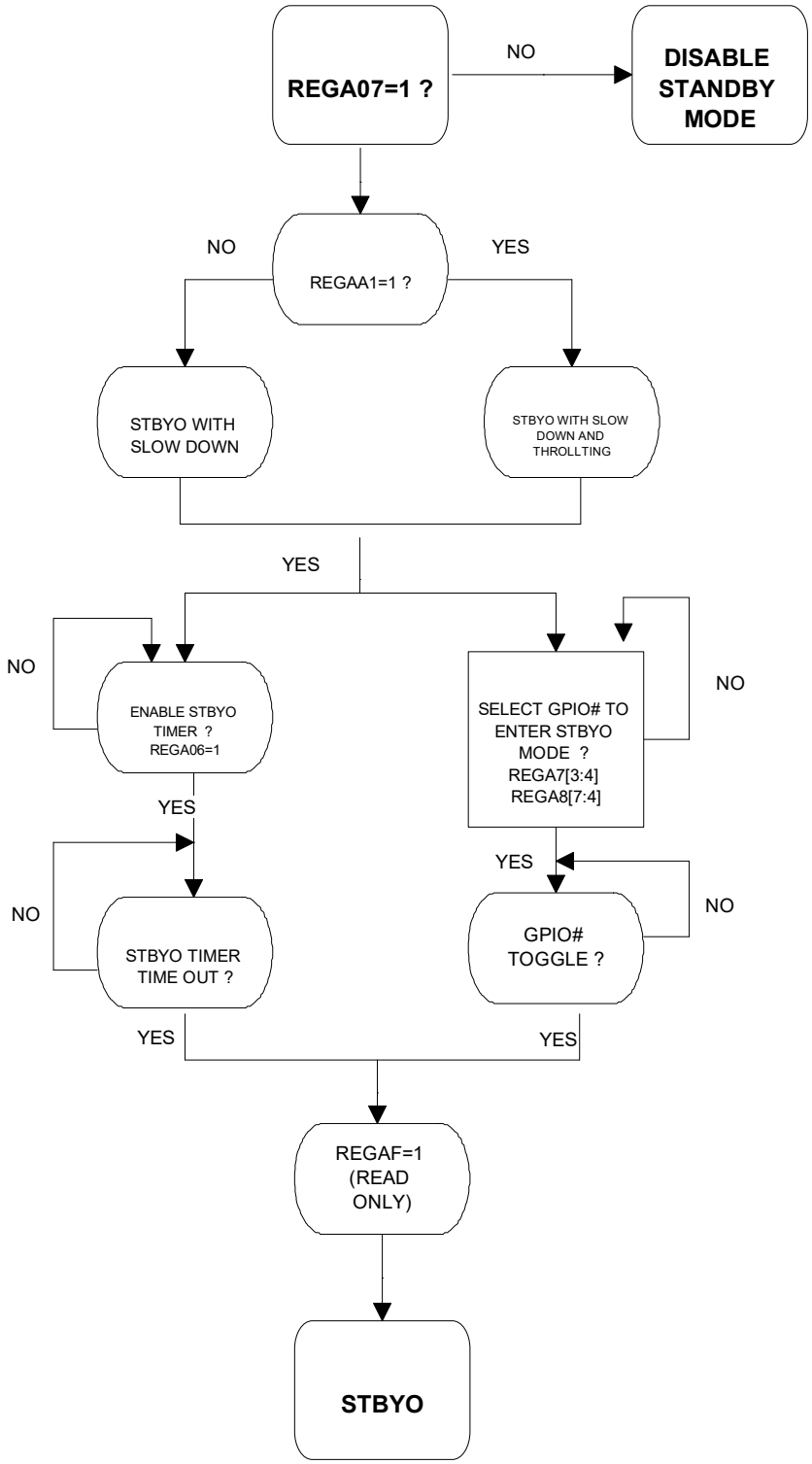


Figure 4.5 Standby Fucntion Flow Chart

Enable SMI Function Flow Chart

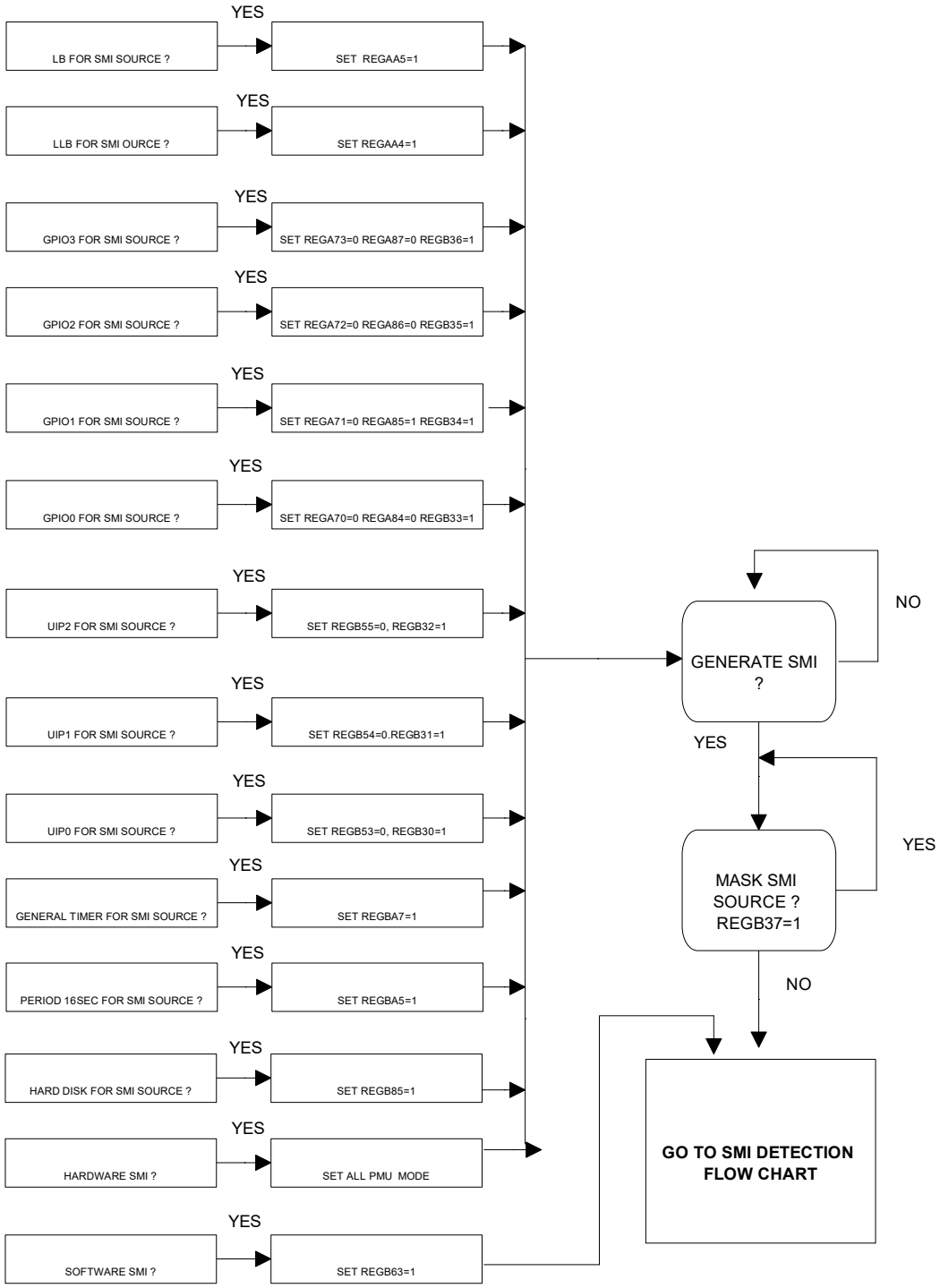
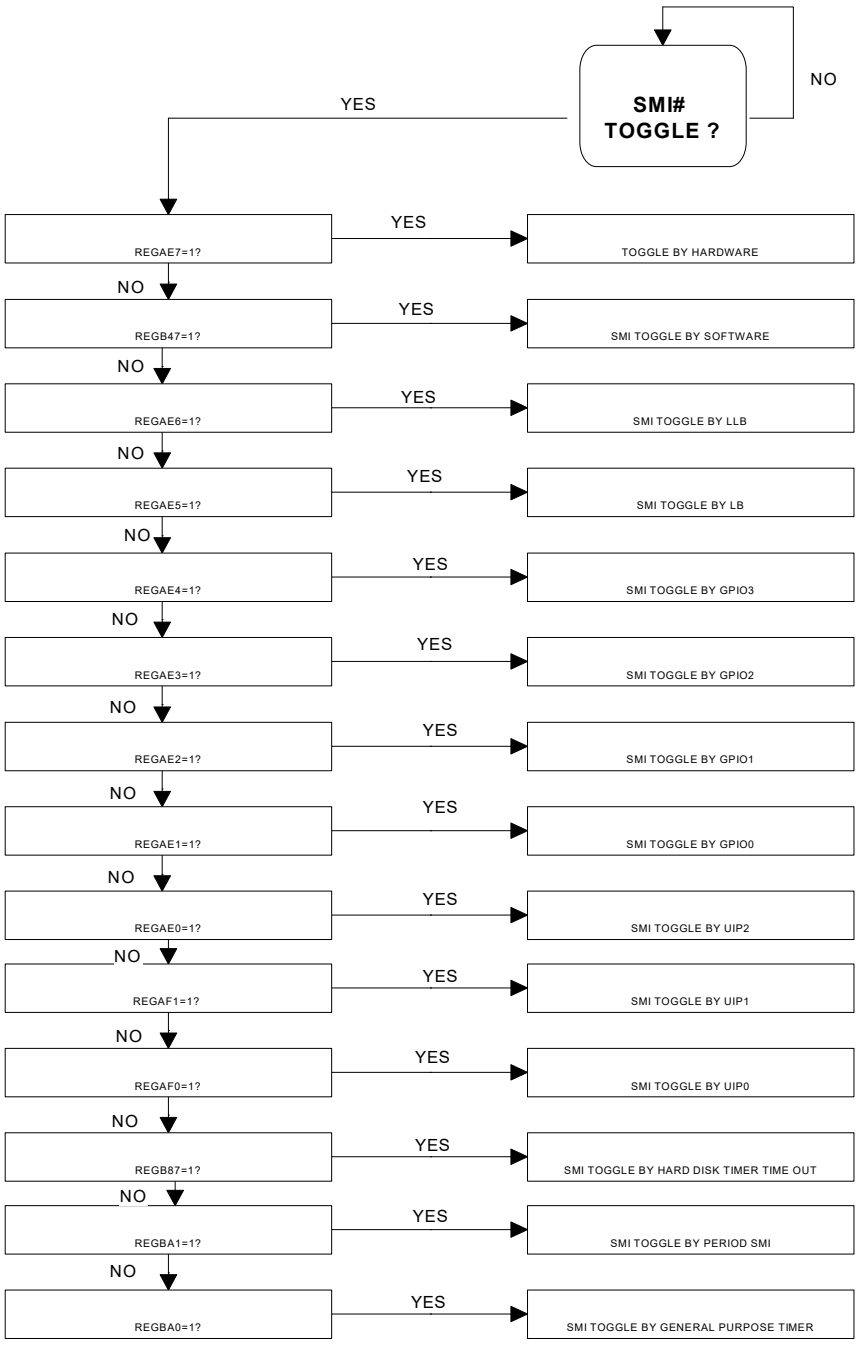


Figure 4.6 Enable SMI Function Flow Chart

SMI# Detection Flow Chart



NOTE : * The checking SMI sequence can be changed by user.

Figure 4.7 SMI# Detection Flow Chart

SiS5100 GPIO Flow Chart

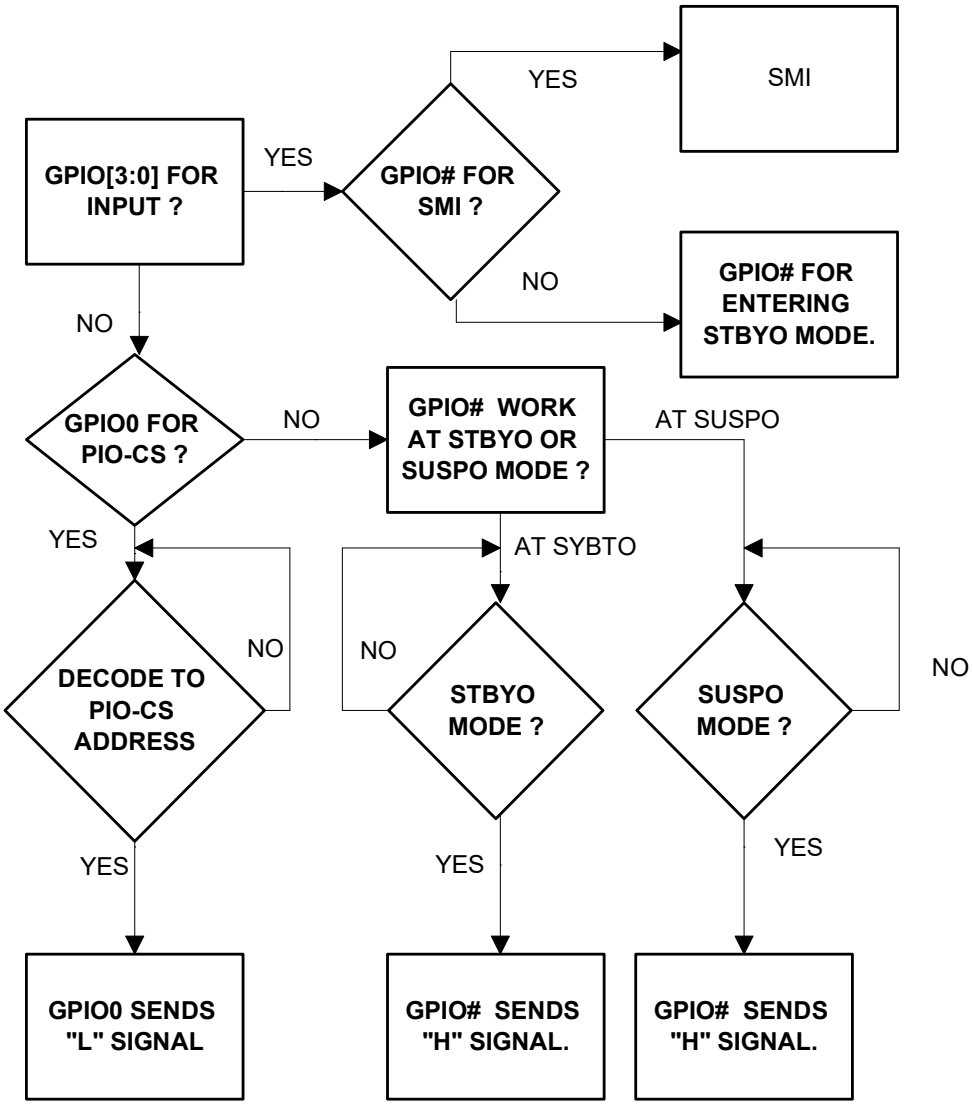


Figure 4.8 SiS5100 GPIO Flow Chart

SiS5100 PIO Flow Chart

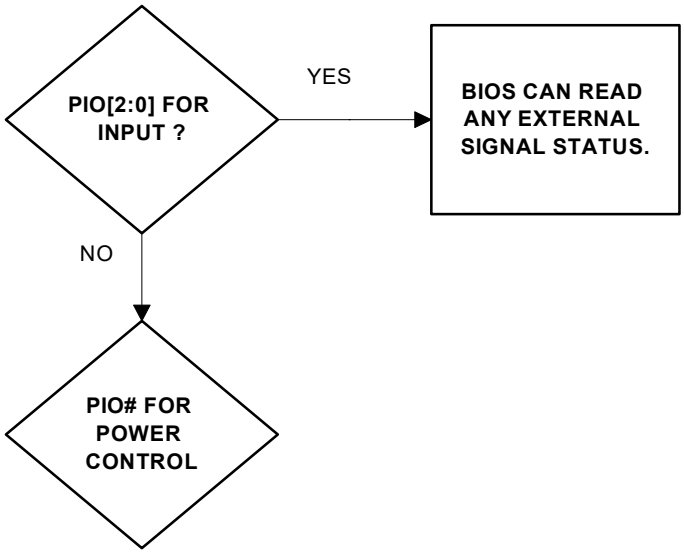


Figure 4.9 SiS5100 PIO Flow Chart

SiS5100 UIP Flow Chart

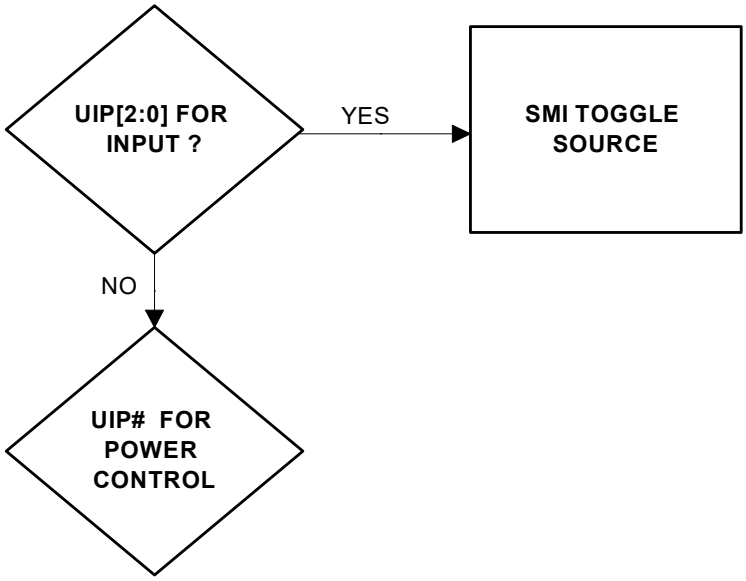


Figure 4.10 SiS5100 UIP Flow Chart

SiS5100 AC Power and LB/ LLB Flow Chart

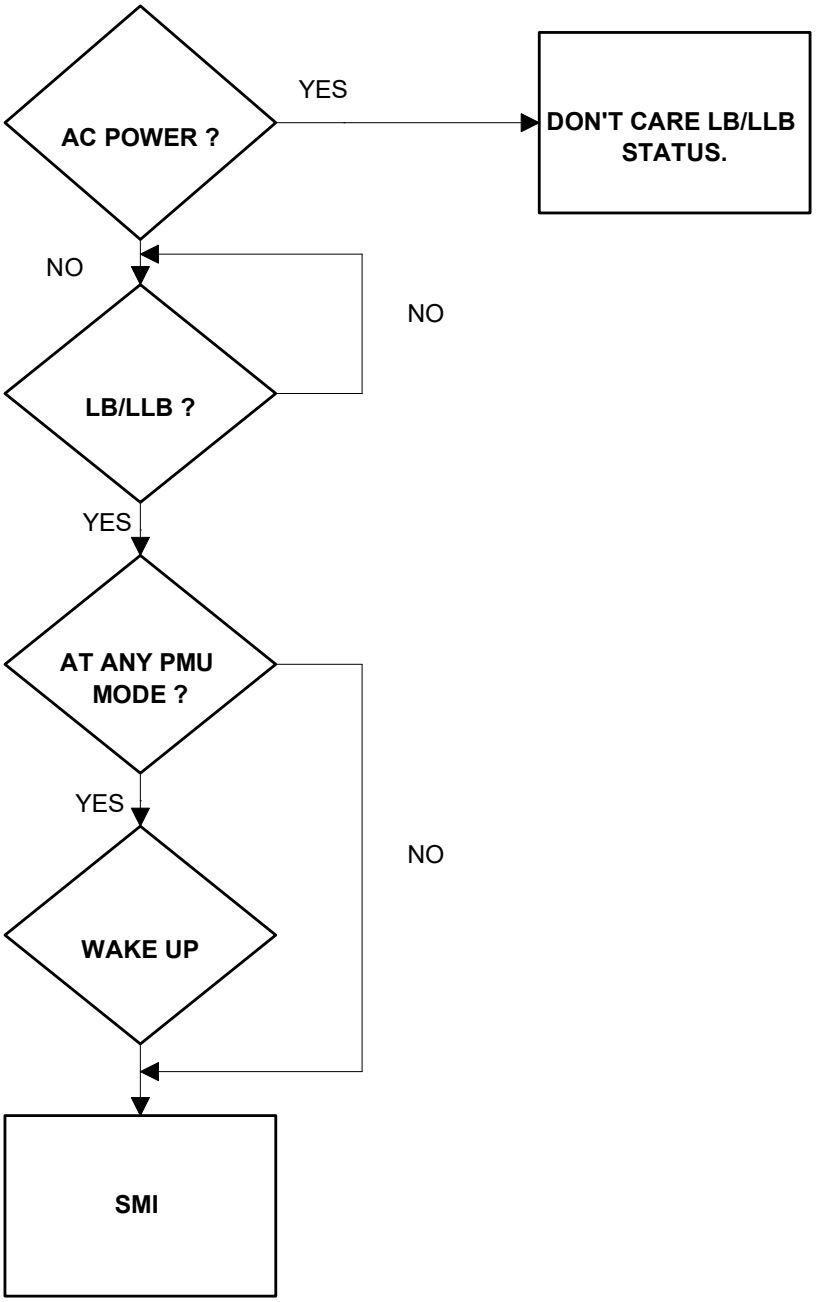


Figure 4.11 SiS5100 AC Power and LB/ LLB Flow Chart

SiS5100 AMP Flow Chart

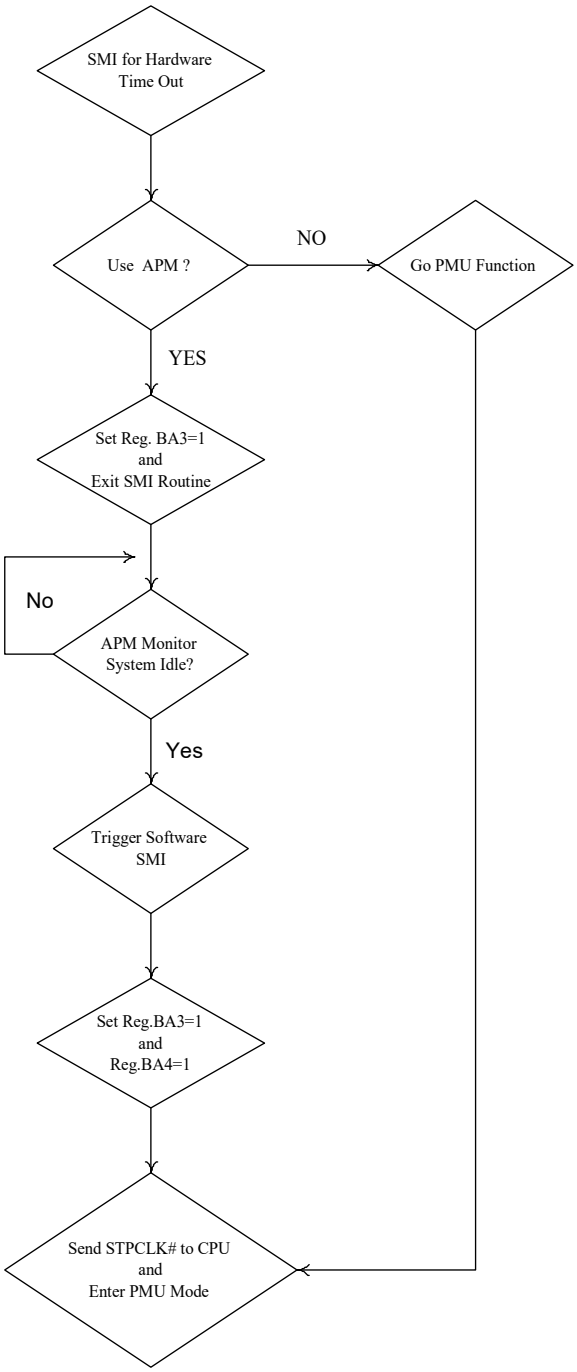


Figure 4.12 SiS5100 APM Flow Chart

4.5 SiS5103 Configuration Registers

Registers 00h, 01h Vendor ID

Bits 15:0 = 1039h (Read Only)

Registers 02h, 03h Device ID

Bits 15:0 = 0008h (Read Only)

Registers 04h, 05h Command = 07h

Bits 15:4 Reserved. Read as 0's
Bit 3 Monitor Special Cycle Enable = 0
Bit 2 Behave as Bus Master Enable = 1
Bit 1 Respond to Memory Space Accesses = 1
Bit 0 Respond to I/O Space Accesses = 1

Registers 06h, 07h Status

Bits 15:14 Reserved. Read as 0's

Bit 13 Received Master-Abort

When the 5103 generates a master-abort, this bit is set to a 1. This bit is cleared to 0 by writing a 1 to this bit.

Bit 12 Received Target-Abort

When the 5103 receives a target-abort, this bit is set to a 1. Software clears this bit to 0 by writing a 1 to this bit location.

Bit 11 Reserved. Read as a 0

Bits 10:9 DEVSEL# Timing

The 5103 always generates DEVSEL# with medium timing, these two bits are always set to 01.

Bits 8:0 Reserved. Read as 0's.

Register 08h Revision ID

Bits 7:0 = 00h (Read Only)

Registers 0B-09h Class Code

Bits 23:0 060100h (Read Only)

Register 40h BIOS Control Register

Bit 7 Reserved. Read as a 0.

Bit 6 Reserved. Read as a 0.

Bit 5 When ISA MASTER retries, Arbiter deasserts SIOGNT#. This bit defaults to 0.

Bit 4 **PCI Posted Write Buffer Enable**

The default value is 0 (disabled).

Bits 3:0 **Determine how the 5103 responds to F segment, E segment, and extended segment (FFF80000-FFFDFFFF) accesses. 5103 will positively respond to extended segment access when bit 0 is set. Bit 1, combining with bits [3:2], enables 5103 to respond to E segment access.**

Bit 3 **Positive Decode of Upper 64K BYTE BIOS Enable.**

Bit 2 **BIOS Subtractive Decode Enable.**

bits [3:2]	F segment		E segment		Comment
	+	-	+	-	
00			√ *		5103 positively responds to E segment access.
01		√			5103 subtractively responds to F segment access.
10	√		√ *		5103 positively responds to E and F segment access.
11	√				5103 positively responds to F segment access.

*: enabled if bit 1 is set.

Bit 1 **Lower BIOS Enable.**

Bit 0 **Extended BIOS Enable. (FFF80000~FFFDFFFF)**

Register 41h INTA# Remapping Control Register

Bit 7 **Remapping Control**

When enabled, INTA#, is remapped to the PC compatible interrupt signal specified in IRQ remapping table. This bit is set to 1 after reset.

0: Enable

1: Disable

Bits 6:4 **Reserved. Read as 0's.**

Bits 3:0 **IRQx Remapping table.**

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	reserved	0101	IRQ5	1010	IRQ10	1111	IRQ15
0001	reserved	0110	IRQ6	1011	IRQ11		
0010	reserved	0111	IRQ7	1100	IRQ12		
0011	IRQ3	1000	reserved	1101	reserved		
0100	IRQ4	1001	IRQ9	1110	IRQ14		

Register 42h INTB# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

Register 43h INTC# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

Register 44h INTD# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

Note: The difference INT[A:D]# can be remapped to the same IRQ signal, but this IRQ signal should be set to level sensitive.

Register 48h ISA Master/DMA Memory Cycle Control Register 1

The ISA master or DMA memory access cycles will be forwarded to PCI bus when the address fall within the programmable region defined by bits[7:4]. The base address of the programmable region is 1Mbyte, and the top addresses is programmed in 1MByte increments from 1MByte to 16MByte. All memory cycles will be forwarded to PCI bus besides the cycle fall within memory hole defined in register 4Ah and 4Bh.

Bits 7:4

Bits 7	6	5	4	Top of Memory
0	0	0	0	1 MByte
0	0	0	1	2 MByte
0	0	1	0	3 MByte
0	0	1	1	4 MByte
0	1	0	0	5 MByte
0	1	0	1	6 MByte
0	1	1	0	7 MByte
0	1	1	1	8 MByte
1	0	0	0	9 MByte
1	0	0	1	10 MByte
1	0	1	0	11 MByte
1	0	1	1	12 MByte

1	1	0	0	13 MByte
1	1	0	1	14 MByte
1	1	1	0	15 MByte
1	1	1	1	16 MByte

ISA master and DMA memory cycles to the following memory regions will be forwarded to PCI bus if they are enabled.

Bit 3 **896-960KByte Memory Region**

0: Disable

1: Enable, the cycle is forwarded to PCI bus.

Bit 2 **640-768KByte memory Region**

0: Disable

1: Enable, the cycle is forwarded to PCI bus.

Bit 1 **512-640KByte Memory Region**

0: Disable

1: Enable

The cycle is forwarded to PCI bus.

Bit 0 **0-512KByte Memory Region**

0: Disable

1: Enable

The cycle is forwarded to PCI bus.

Register 49h ISA Master/DMA Memory Cycle Control Register 2

ISA master and DMA memory cycles to the following memory regions will be forwarded to PCI bus if they are enabled.

Bit 7 **880-896K (DC000h-DFFFFh) Memory region**

0: Disable

1: Enable

Bit 6 **864-880K (D8000h-DBFFFh) Memory Region**

0: Disable

1: Enable

Bit 5 **848-864K (D4000h-D7FFFh) Memory Region**

0: Disable

1: Enable

Bit 4 **832-848K (D0000h-D3FFFh) Memory Region**

0: Disable

1: Enable

Bit 3 **816-832K (CC000h-CFFFFh) Memory Region**

0: Disable

1: Enable

Bit 2 **800-816K (C8000h-CBFFFh) Memory Region**

0: Disable

1: Enable

Bit 1 **784-800K (C4000h-C7FFFh) Memory Region**

0: Disable

1: Enable

Bit 0 **768-784K (C0000h-C3FFFh) Memory Region**

0: Disable

1: Enable

Register 4Ah ISA Master/DMA Memory Cycle Control Register 3

Register 4Ah and register 4Bh are used to define the ISA address hole. The ISA address hole is located between 1Mbyte and 16MByte, and sized in 64KByte increments. ISA master and DMA memory cycles fall within this hole will not be forwarded to PCI bus. Register 4Ah and 4Bh are used to define the bottom and top address of the hole respectively. The hole is located between top and bottom address, and the bottom and top address must be at or above 1MByte. If bottom address is greater than top address, the ISA address hole is disabled.

Bit 7 **A23**

Bit 6 **A22**

Bit 5 **A21**

Bit 4 **A20**

Bit 3 **A19**

Bit 2 **A18**

Bit 1 **A17**

Bit 0 **A16**

Register 4Bh ISA Master/DMA Memory Cycle Control Register 4

This register is used to define the top address of the ISA Address hole.

Bit 7 **A23**

Bit 6 **A22**

Bit 5 **A21**

Bit 4 **A20**

Bit 3 **A19**

Bit 2 **A18**

Bit 1 **A17**

Bit 0 **A16**

4.6 Non-Configuration Registers

Register 4D0h IRQ Edge/Level Control Register 1

Bit 7 **IRQ7**

0: edge sensitive

1: level sensitive

Bit 6 **IRQ6**

0: edge sensitive

1: level sensitive

Bit 5 **IRQ5**

0: edge sensitive

1: level sensitive

Bit 4 **IRQ4**

0: edge sensitive

1: level sensitive

Bit 3 **IRQ3**

0: edge sensitive

1: level sensitive

Bit 2 **IRQ2**

This bit must be set to 0. Read as 0.

Bit 1 **IRQ1**

This bit must be set to 0. Read as 0.

Bit 0 **IRQ0**

This bit must be set to 0. Read as 0.

After reset this register is set to 00h.

Register 4D1h IRQ Edge/Level Control Register 2

Bit 7 **IRQ15**

0: edge sensitive

1: level sensitive

Bit 6 **IRQ14**

0: edge sensitive

1: level sensitive

Bit 5 **IRQ13**

This bit must be set to 0. Read as 0.

Bit 4 **IRQ12**

0: edge sensitive

1: level sensitive

Bit 3 **IRQ11**

0: edge sensitive

1: level sensitive

Bit 2 **IRQ10**

0: edge sensitive

1: level sensitive

Bit 1 **IRQ9**

0: edge sensitive

1: level sensitive

Bit 0 **IRQ8**

This bit must be set to 0. Read as zero.

After reset this register is set to 00h.

Registers 50h-53h

Bits 7:0 **ICW1 to ICW4 of the built-in interrupt controller (slave) can be read from 50h to 53h.**

Registers 54h-55h

Bits 7:0 **OCW2 to OCW3 of the built-in interrupt controller (master) can be read from 54h to 55h.**

Registers 56h-57h

Bits 7:0 **OCW2 to OCW3 of the built-in interrupt controller (slave) can be read from 56h to 57h.**

Register 58h

Bits 7:0 **Low byte of the initial count number of Counter 0 in the built-in CTC can be read from 58h.**

Register 59h

Bits 7:0 **High byte of the initial count number of Counter 0 in the built-in CTC can be read from 59h.**

Register 5Ah

Bits 7:0 **Low byte of the initial count number of Counter 1 in the built-in CTC can be read from 5Ah.**

Register 5Bh

Bits 7:0 **High byte of the initial count number of Counter 1 in the built-in CTC can be read from 5Bh.**

Register 5Ch

Bits 7:0 **Low byte of the initial count number of Counter 2 in the built-in CTC can be read from 5Ch.**

Register 5Dh

Bits 7:0 **High byte of the initial count number of Counter 2 in the built-in CTC can be read from 5Dh.**

Register 5Eh

Bits 7:0 **Control word (43h) of the built-in CTC can be read from 5Eh.**

Register 5Fh

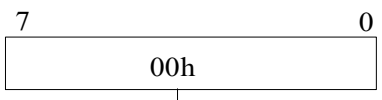
Bits 7:0 **Indicates the status whether the LSB or MSB is read or written when Read/Write word function has been processed for the corresponding counter.**

Address	Function Unit	Register	Register Access	Bus Access
0000h	DMA	DMA1 CH0 Base and Current Address	R/W	PCI Only
0001h	DMA	DMA1 CH0 Base and Current Count	R/W	PCI Only
0002h	DMA	DMA1 CH1 Base and Current Address	R/W	PCI Only
0003h	DMA	DMA1 CH1 Base and Current Count	R/W	PCI Only
0004h	DMA	DMA1 CH2 Base and Current Address	R/W	PCI Only
0005h	DMA	DMA1 CH2 Base and Current Count	R/W	PCI Only
0006h	DMA	DMA1 CH3 Base and Current Address	R/W	PCI Only
0007h	DMA	DMA1 CH3 Base and Current Count	R/W	PCI Only
0008h	DMA	DMA1 Status(r) Command(w) Register	R/W	PCI Only
0009h	DMA	DMA1 Write Request Register	WO	PCI Only
000Ah	DMA	DMA1 Write Single Mask Bit	WO	PCI Only
000Bh	DMA	DMA1 Write Mode Register	WO	PCI Only
000Ch	DMA	DMA1 Clear Byte Pointer	WO	PCI Only
000Dh	DMA	DMA1 Master Clear	WO	PCI Only
000Eh	DMA	DMA1 Clear Mask Register	WO	PCI Only
000Fh	DMA	DMA1 Read/Write All Mask Register Bits	R/W	PCI Only
0020h	Interrupt	INT 1 Control	R/W	PCI/ISA
0021h	Interrupt	INT 1 Mask	R/W	PCI/ISA
0040h	Timer	Timer Counter 1 - Counter 0 Count	R/W	PCI/ISA
0041h	Timer	Timer Counter 1 - Counter 1 Count	R/W	PCI/ISA
0042h	Timer	Timer Counter 1 - Counter 2 Count	R/W	PCI/ISA
0043h	Timer	Timer Counter 1 Command Mode	WO	PCI/ISA
0061h	Control	NMI Status and Control	R/W	PCI/ISA
0070h	Control	CMOS RAM Address and NMI Mask	WO	PCI/ISA
0080h	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
0081h	DMA	DMA Channel 2 Page Register	R/W	PCI/ISA
0082h	DMA	DMA Channel 3 Page Register	R/W	PCI/ISA
0083h	DMA	DMA Channel 1 Page Register	R/W	PCI/ISA
0084h	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
0085h	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
0086h	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
0087h	DMA	DMA Channel 0 Page Register	R/W	PCI/ISA
0088h	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
0089h	DMA	DMA Channel 6 Page Register	R/W	PCI/ISA
008Ah	DMA	DMA Channel 7 Page Register	R/W	PCI/ISA
008Bh	DMA	DMA Channel 5 Page Register	R/W	PCI/ISA
008Ch	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
008Dh	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
008Eh	DMA	DMA Page Register - Reserved	R/W	PCI/ISA
008Fh	DMA	DMA Refresh Page Register	R/W	PCI/ISA
00A0h	Interrupt	INT 2 Control Register	R/W	PCI/ISA

00A1h	Interrupt	INT 2 Mask Register	R/W	PCI/ISA
00C0h	DMA	DMA2 CH0 Base and Current Address	R/W	PCI Only
00C2h	DMA	DMA2 CH0 Base and Current Count	R/W	PCI Only
00C4h	DMA	DMA2 CH1 Base and Current Address	R/W	PCI Only
00C6h	DMA	DMA2 CH1 Base and Current Count	R/W	PCI Only
00C8h	DMA	DMA2 CH2 Base and Current Address	R/W	PCI Only
00CAh	DMA	DMA2 CH2 Base and Current Count	R/W	PCI Only
00CCh	DMA	DMA2 CH3 Base and Current Address	R/W	PCI Only
00CEh	DMA	DMA2 CH3 Base and Current Count	R/W	PCI Only
00D0h	DMA	DMA2 Status(r) Command(w) Register	R/W	PCI Only
00D2h	DMA	DMA2 Write Request Register	WO	PCI Only
00D4h	DMA	DMA2 Write Single Mask Bit Register	WO	PCI Only
00D6h	DMA	DMA2 Write Mode Register	WO	PCI Only
00D8h	DMA	DMA2 Clear Byte Pointer Register	WO	PCI Only
00DAh	DMA	DMA2 Master Clear Register	WO	PCI Only
00DCh	DMA	DMA2 Clear Mask Register	WO	PCI Only
00DEh	DMA	DMA2 Read/Write All Mask Register Bits	R/W	PCI Only
00F0h	Control	Coprocessor Error Register	WO	PCI/ISA

Register 4D0h, 4D1h Edge/Level Control Register - INTCNTRL1, INTCNTRL2

The Edge/Level Control Register is used to set the interrupts to be triggered by either the signal edge or the logic level. INT0, INT1, INT2, INT8, INT13 must be set to edge sensitive. After a reset all the INT signals are set to edge sensitive. The table below shows which bit number represent the various INT signals.



Edge/Level Control(R/W)

Bit	Port 04D0h	Port 04D1h
0	INT0	INT8
1	INT1	INT9
2	INT2	INT10
3	INT3	INT11
4	INT4	INT12
5	INT5	INT13
6	INT6	INT14
7	INT7	INT15

Register Location: 04D0h - INTCNTRL1, 04D1h - INTCNTRL2

- **04D0h INTCNTRL1 Registers**

Bits 7:0 Edge/Level Select.

These bits select if the interrupts are triggered by either the signal edge or the logic level. A 0 bit represents an edge sensitive interrupt, and a 1 is for level sensitive. The Reserved bits MUST be set to 0.

Port 04D0h (INT-CNTRL-1)

0-INT0	0	Reserved. Read as zero.
1-INT1	0	Reserved. Read as zero.
2-INT2	0	Reserved. Read as zero.
3-INT3	x	
4-INT4	x	
5-INT5	x	
6-INT6	x	
7-INT7	x	

x=selectable to either 0 or 1. 0=edge sensitive. 1=level sensitive.

After reset this register is set to 00h.

- **04D1h INT CNTRL-2 Register**

Bits 7:0 Edge/Level Select.

These bits select if the interrupts are triggered by either the signal edge or the logic level. A 0 bit represents an edge sensitive interrupt, and a 1 is for level sensitive. The Reserved bits MUST be set to 0.

Port 04D1h (INT-CNTRL-2)

0-INT8	0	Reserved. Read as zero.
1-INT9	x	
2-INT10	x	
3-INT11	x	
4-INT12	x	
5-INT13	0	Reserved. Read as zero.
6-INT14	x	
7-INT15	x	

x=selectable to either 0 or 1. 0=edge sensitive. 1=level sensitive.

After reset this register is set to 00h.

4.6.1 ISA Internal Register

ISA internal registers are accessed through an address/data registers pair. Address register located at port 22h is written with the index of ISA internal register. Then ISA internal register content can be read or written through the data register at port 23h. The port 22h can be read to get the last written-in value.

Register 80h

Bits 7:6 Bus clock selection

00: 7.159MHz

01: PCICLK/4

10: PCICLK/3

Bit 5 Flash EPROM Control bit 0 (Please refer to Register 80h bit 2 for details.)

Bit 4 Programmable Output Pin

0: Pin 20 is used as WAKEUP0 when internal IDE is disabled

1: Pin 20 is used as "Programmable Output Pin" that can generate one write pulse by writing register 82h when internal IDE is disabled

Bit 3 Access Upper 128 Bytes CMOS SRAM

0: Disable

1: Enable

Bit 2 Flash EPROM Control bit 1

Previous implementation on flash EPROM support limits that EPROM is flashed upon power on till bit 5 of register 80h is set to 1. The new added feature will allow EPROM to be flashed anytime. Bit 2 of the register 80h is added and the setting of both bit 2 and bit 5 will now control the EPROM flash operation.

Register 80h bit 5	Register 80h bit 2	Operation
0	0	EPROM can be flashed
1	0	EPROM can't be flashed again
X	1	EPROM can be flashed whenever bit 5 is 0

Bit 1 Relocatable ISA Configuration Registers Control

ISA configuration registers are now relocatable through bit 1 of ISA configuration register 80h. Upon power on, ISA configuration registers are located between index 80h to 8Fh by default. These index can be relocated to 70h to 7Fh by programming bit 1 of register 80h to 1.

Bit 0 **ISA Slew Rate Control**

The default value of the following ISA signals is 8mA(min), including SA[16-0], LA[23-17], SBHE#, MRDC#, MWTC#, SMRDC#, SMWTC#, IORC#, and IOWC#. Besides, Bit 0 of ISA configuration register 80h is used to program the currents of the above signals to 12mA(min) when it is set to 1.

Register 81h

Bits 7:6 **16-bit I/O cycle command recovery time**

00 : 5 BUSCLK

01 : 4 BUSCLK

10 : 3 BUSCLK

11 : 2 BUSCLK

Bits 5:4 **8-bit I/O cycle command recovery time**

00 : 8 BUSCLK

01 : 5 BUSCLK

10 : 4 BUSCLK

11 : 3 BUSCLK

Bit 3 **Reserved**

Bit 2 **16-bit memory, I/O wait state selection**

0 : 1 wait state

1 : 0 wait state

Bit 1 **Reserved**

Bit 0 **Reserved**

Register 82h **If this register is written by any values, the pin 20 will generate one write pulse when bit 4 of register 80h "Programmable Output Pin" is enabled**

Register 83h

Bits 7:2 **Reserved**

Bit 1 **ISA Bus Refresh Cycle Enable/Disable**

0: Enable

1: Disable

Bit 0 **PCI Output and Bidirectional Buffers Current Selection**

0: 50mA/2.2V (default value)

1: 95mA/2.2V

Register 84h BIOS Register

Bits 7:0 **BIOS can use this register to store data.**

Register 85h

Bits 7:0 **The same value as port 70h.**

Register 88h

Bits 7:1 **Corresponds to the mask bits of the IRQ7-1.**

When disabled, any event from the corresponding IRQ will cause the system reload timer

Bit 0 **Is the mask bit of the NMI.**

When disabled, an event from the NMI will cause the system to reload timer

Register 89h

Bits 7:0 **Corresponds to the mask bits of the IRQ8-15.**

When disabled, any event from the corresponding IRQ will cause the system to reload timer

Register 8Ah Reserved

Register 8Bh Reserved

Register 8Ch IIRQ[A:D] Route Control Register

Bit 7:6 **Controls IIRQ A**

00 : IRQ 9

01 : IRQ 10

10 : IRQ 11

11 : IRQ 15

Bit 5:4 **Controls IIRQ B**

00 : IRQ 10

01 : IRQ 11

10 : IRQ 15

11 : IRQ 9

Bit 3:2 **Controls IIRQ C**

00 : IRQ 11

01 : IRQ 15

10 : IRQ 9

11 : IRQ 10

Bit 1:0 **Controls IIRQ D**

00 : IRQ 15

01 : IRQ 9

10 : IRQ 10

11 : IRQ 11

Register 8Dh IDRQ[A:B] Route Control Register

Bit 7,6 **Reserved**

Bit 5 **Routing of IDRQ B**

When enabled, IDRQ B can be routed to the DRQ x signal specified in bits 5,4 . Following a reset this bit is disabled (set to 0) , and IDRQ B will be routed to DREQ 7

Bit 4:3 **Controls IDRQ B**

00 : Reserved

01 : DRQ 5

10 : DRQ 6

11 : DRQ 7

Bit 2 **Routing of IDRQ A**

When enabled, IDRQ A can be routed to the DRQ x signal specified in bits 1,0. At reset ,this bit is disabled (set to 0) , and IDRQ A will be routed to DREQ 3

Bit 1:0 **Controls IDRQ A**

00 : DRQ 0

01 : DRQ 1

10 : DRQ 2

11 : DRQ 3

4.7 PCI IDE Configuration Register

31 16	15 0			
Device ID = 0601h		Vendor ID = 1039h		00h
Status = 0000-0010-0000-0000		Command = 0000-0000-0000-0000		04h
Base Class = 01h	Sub-Class = 01h	Prog. If = 00h	Revision ID = 01h	08h
BIST = 00h	Header Type = 80h	Latency Timer = 00h	Cache Line Size = 00h	0Ch
XXXX17xx			0 1	10h
XXXX1Fxx			0 1	14h
XXXX37xx			0 1	18h
XXXX3Fxx			0 1	1Ch
Reserved (00000000)			0 1	20h
Reserved (00000000)			0 1	24h
Reserved (00000000)				28h
Reserved (00000000)				2Ch
Expansion ROM Base Address None (00000000)				30h
Reserved (00000000)				34h
Reserved (00000000)				38h
Max_Lat = 00h	Min_Gnt = 00h	Interrupt Pin = 00h	Interrupt Line	3Ch

Register 40h Built-in PCI IDE Control Register 1

Bits 7:4 Address 1FX/3F6 DRIVE 1 READ Active Time

Bits 3:0 Address 1FX/3F6 DRIVE 0 READ Active Time

Register 41h

Bits 7:4 Address 17X/376 DRIVE 1 Read Active Time

Bits 3:0 Address 17X/376 DRIVE 0 Read Active Time

Register 42h

Bits 7:4 Address 1FX/3F6 Drive 1 Write Active Time

Bits 3:0 Address 1FX/3F6 Drive 0 Write Active Time

Register 43h

Bits 7:4 Address 17X/376 Drive 1 Write Active Time

Bits 3:0 Address 17X/376 Drive 0 Write Active Time

Register 44h

Bits 7:4 Address 1FX/3F6 Drive 1 Read Recovery Time

Bits 3:0 Address 1FX/3F6 Drive 0 Read Recovery Time

Register 45h

Bits 7:4 Address 17X/376 Drive 1 Read Recovery Time

Bits 3:0 Address 17X/376 Drive 0 Read Recovery Time

Register 46h

Bits 7:4 Address 1FX/3F6 Drive 1 Write Recovery Time

Bits 3:0 Address 1FX/3F6 Drive 0 Write Recovery Time

Register 47h

Bits 7:4 Address 17X/376 Drive 1 Write Recovery Time

Bits 3:0 Address 17X/376 Drive 0 Write Recovery Time

Wait-State	Read/Write Active Time	Read/Write Recovery Time
0	1	1
1	2	2
2	3	3
3	4	4
4	5	5
5	6	6
6	7	7
7	8	8
8	9	9
9	10	10
10	11	11
11	12	12
12	13	13
13	13	14
14	13	16
15	13	18

Register 48h

Bit 7 **Reserved**

Bit 6 **Post Write Buffer**

1 : Enable

0 : Disable

Bit 5 **Read Prefetch Buffer**

1 : Enable

0 : Disable

Bit 4 **Reserved**

Bits 3:2 **IDE Channel And Address Select**

BIT3	BIT2	
0	0	CH0 1FX, 3F6 Only (IDECS0, IDECS1)
0	1	CH0 17X, 376 Only (IDECS0, IDECS1)
1	0	CH0 1FX, 3F6/CH1 17X, 376 (IDECS0, IDECS1, IDECS2, IDECS3)
1	1	Undefined

Bit 1

1 : Enable

0 : Disable

Bit 0 **Auto Power Down Mode**

1 : Enable

0 : Disable

Register 49h

Bits 7:2 **Reserved**

Bit 1 **Reserved should be written with 0**

Bit 0 **Reserved**

4.8 PMU Configuration Registers

Register A0h

Bit 7 **Standby State**

1 : Enable

0 : Disable

Bit 6 **Standby Counter**

1 : Enable

0 : Disable

Bits 5:0 **Standby Counter Values**

The unit is about 4 sec.

Register A1h

Bit 7 **Suspend State**

1 : Enable

0 : Disable

Bit 6 **Suspend Counter**

1 : Enable

0 : Disable

Bits 5:0 **Suspend Counter Values**

The unit is about 1 min.

Register A2h

Bit 7 **Doze State**

1 : Enable

0 : Disable

Bit 6 **3 Sec Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Bit 5 **2 Sec Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Bit 4 **1.5 Sec Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Bit 3 **1 Sec Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Bit 2 **0.5 Sec Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Bit 1 **125 mS Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Bit 0 **31 mS Doze Timer Monitor One Of IRQ [15:0]**

1 : Enable

0 : Disable

Register A3h

Bits 7:4 **3 Sec Timer Selects One of IRQ [15:0] to Monitor**

0000	Reserved
0001	Select IRQ 1
0010	Reserved
0011	Select IRQ 3
0100	Select IRQ 4
0101	Select IRQ 5
0110	Select IRQ 6
0111	Select IRQ 7
1000	Select IRQ 8
1001	Select IRQ 9
1010	Select IRQ 10
1011	Select IRQ 11
1100	Select IRQ 12
1101	Select IRQ 13
1110	Select IRQ 14
1111	Select IRQ 15

Bits 3:0 **2 Sec Timer Selects One of IRQ [15:0] to Monitor**

Register A4h

Bits 7:4 **1.5 Sec Timer Selects One of IRQ [15:0] to Monitor**

Bits 3:0 **1 Sec Timer Selects One of IRQ [15:0] to Monitor**

Register A5h

Bits 7:4 **0.5 Sec Timer Selects One of IRQ [15:0] to Monitor**

Bits 3:0 **125 mS Timer Selects One of IRQ [15:0] to Monitor**

Register A6h

Bits 7:4 31.25 mS Timer Selects One of IRQ [15:0] to Monitor

Bit 3 Doze Function

1 : Slow Down

0 : Throllting

Bits 2:0 Doze Timers

000	Only 31.25 mS Timer can Act
001	Only 125 mS Timer can Act
010	Only 0.5 Sec Timer can Act
011	Only 1 Sec Timer can Act
100	Only 1.5 Sec Timer can Act
101	Only 2 Sec Timer can Act
110	Only 3 Sec Timer can Act
111	All Doze Timer can Act

Register A7h

Bits 7:4 GPIO [3:0] Output Function for Standby or Suspend

1 : For Suspend

0 : For Standby

Bits 3:0 GPIO [3:0] are Selected for Output or Input

1 : For Output (GPIO Active High When it is Output)

0 : For Input (GPIO Active Low When it is Input)

Register A8h

Bits 7:4 GPIO [3:0] Input Function for SMI# or Standby

1 : For Going into Standby Source

0 : For SMI# Toggle Source

Bit 3 GPIO0 is Selected as PIO-CS Signal When it is Output

1 : Enable

0 : Disable

Bit 2 RTC Timer Alarm is Selected as Wakeup Source

1 : Enable

0 : Disable

Bits 1:0 Programmed Bits for PIO-CS Address[9:8]

Register A9h

Bit 7:0 **Programmed Bits for PIO-CS Address[7:0]**

Register AAh

Bit 7 **Thermal Detection**

1 : Enable

0 : Disable

Bit 6 **External Suspend**

1 : Enable

0 : Disable

Bit 5 **LB Toggles SMI# Signal**

1 : Enable

0 : Disable

Bit 4 **LLB Toggles SMI# Signal**

1 : Enable

0 : Disable

Bit 3 **STOPCLK# Keeps Acting or Non-Acting During Standby Mode**

1 : Enable

0 : Disable

Bit 2 **Leakage Function at Suspend Mode**

1 : Enable

0 : Disable

Bit 1 **Throllting Function Acting During Slow Down Function for Doze or Standby Mode**

1: Enable

0: Disable

Bit 0 Period STPCLK#

1 : 500US

0 : 2mS

Register ABh

Bit 7 **CPU Accesses PCI Device or ISA Device to be Wakeup Source**

1 : Enable

0 : Disable

Bit 6 **IRQ to be Wakeup Source**

1 : Enable

0 : Disable

Bit 5 **DMA to be Wakeup Source**

1 : Enable

0 : Disable

Bit 4 **PCI Master to be Wakeup Source**

1 : Enable

0 : Disable

Bit 3 **IO Address Trap to be Wakeup source**

1 : Enable

0 : Disable

Bit 2 **RI to be Wakeup Source**

1 : Enable

0 : Disable

Bit 1 **LB to be Wakeup Source**

1 : Enable

0 : Disable

Bit 0 **LLB to be Wakeup Source**

1 : Enable

0 : Disable

Register ACh

Bit 7 **IO Address Trap Monitor 000-01F,0C0-0DF**

1 : Enable

0 : Disable

Bit 6 **IO Address Trap Monitor 020-03F,0A0-0BF**

1 : Enable

0 : Disable

Bit 5 **IO Address Trap Monitor 0F0-0FF,060-06F**

1 : Enable

0 : Disable

Bit 4 **IO Address Trap Monitor 1F0-1F8,3F0-3F7**

1 : Enable

0 : Disable

Bit 3 **IO Address Trap Monitor 278-27F,378-37F,3BC-3BF**

1 : Enable

0 : Disable

Bit 2 **IO Address Trap Monitor 2F8-2FF,3F8-3FF,3E8-3EF,2E8,2EF**

1 : Enable

0 : Disable

Bit 1 **IO Address Trap Monitor 200-21F,36F-38F**

1 : Enable

0 : Disable

Bit 0 **IO Address Trap Monitor 3A0-3DF**

1 : Enable

0 : Disable

Register ADh

Bit 7 **When all Doze Timers are Slected, This Bit can Wakeup Doze by all Wakeup Source Except IRQ**

1 : Enable

0 : Disable

Bits 6:0 **PIO [6:0] functions for Output or Input**

1 : Output

0 : Input

Register AEh Read Only

Bit 7

1 : SMI# Toggle by Hardware

0 : Nothing

Bit 6

1 : SMI# Toggle by LLB

0 : Nothing

Bit 5

1 : SMI# Toggle by LB

0 : Nothing

Bit 4

1 : SMI# Toggle by GPIO3

0 : Nothing

Bit 3

1 : SMI# Toggle by GPIO2

0 : Nothing

Bit 2

1 : SMI# Toggle by GPIO1

0 : Nothing

Bit 1

1 : SMI# Toggle by GPIO0

0 : Nothing

Bit 0

1 : SMI# Toggle by UIP2

0 : Nothing

Register AFh Read Only

Bit 7

1 : System Goes into Standby Mode

0 : Nothing

Bit 6

1 : System Goes into Suspend Mode

0 : Nothing

Bit 5

1 : System Goes into LB Mode

0 : Nothing

Bit 4

1 : System Goes into LLB Mode

0 : Nothing

Bit 3

1 : System Uses AC Power

0 : Nothing

Bit 2

1 : System Goes into Doze Mode

0 : Nothing

Bit 1

1 : SMI# Toggle by UIP1

0 : Nothing

Bit 0

1 : SMI# Toggle by UIP0

0 : Nothing

Register B0h

Bits 7:0 User can Read or Write to This register

Register B1h

Bits 7:0 User can Read or Write to This register

Register B2h

Bits 7:0 User can Read or Write to This register

Register B3h

Bit 7 Mask All SMI Sources Except for software SMI.

When this bit is set to 1, hardware can still latch SMI toggle source. However, SMI can't be generated to CPU.

1: Enable

0: Disable

Bit 6 GPIO3 Input Function for Generating SMI Source

1: Enable

0: Disable

Bit 5 **GPIO2 Input Function for Generating SMI Source**

1: Enable

0: Disable

Bit 4 **GPIO1 Input Function for Generating SMI Source**

1: Enable

0: Disable

Bit 3 **GPIO0 Input Function for Generating SMI Source**

1: Enable

0: Disable

Bit 2 **UIP2 Input Function for Generating SMI Source**

1: Enable

0: Disable

Bit 1 **UIP1 Input Function for Generating SMI Source**

1: Enable

0: Disable

Bit 0 **UIP0 Input Function for Generating SMI Source**

1: Enable

0: Disable

Register B4h

Bit 7

1 : SMI# Toggle by Software (Read Only)

0 : Nothing

Bits 6:0 **PIO[6:0] Status**

When PIO* is Input , User can Read System any Signal by PIO*

When PIO* is Output , User can Writes any Values to system

Register B5h

Bits 7:6 **Programmed Bits for PIO-CS address[11:10].**

Bits 5:3 **UIP[2:0] Functions for Input or Output**

1 : Output

0 : Input

Bits 2:0 **When UIP[2:0] are Output , User can Write any Value to System**

Register B6h

Bits 7:5 **Reserved**

Bit 4 **Software STPCLK#**

1 : STPCLK# Toggle

0 : Nothing

Bit 3 **Software SMI# (APM)**

1 : SMI# Toggle

0 : Nothing

Bits 2:0 **When UIP[2:0] are Output , Wakeup Events will Clear UIP[2:0] to 0**

1 : Enable

0 : Disable

Register B7h

Bit 7 **SMI Is Generated One Time or Two Times by Hardware Time Out Path.**

1: One Time

0: Two Times

Bits 6:0 **When PIO[6:0] are Output , Wakeup Events will Clear PIO[6:0] to 0**

1 : Enable

0 : Disable

Register B8h

Bit 7 **SMI# Toggle by hard disk time out (Read only)**

1:SMI# Toggle

0:Nothing

Bit 6 **Hard disk timer status**

1:Time out

0:Nothing

Bit 5 **Hard disk timer and SMI# source**

1:Enable

0:Disable

Bits 4:0 **Counter values for hard disk (The unit is about 1 Min)**

Register B9h

Bit 7 **General Purpose Timer during SUSPEND mode**

1:Enable
0:Disable

Bit 6 **The unit for General Purpose Timer**

1:1 Min
0:1 Sec

Bits 5:0 **Counter values for General Purpose Timer**

Register BAh

Bit 7 **SMI# Toggle when General Purpose Timer is time out**

1:Enable
0:Disable

Bit 6 **Wake up when General Purpose Timer is time out**

1:Enable
0:Disable

Bit 5 **Period SMI# (16 Sec)**

1:Enable
0:Disable
Note:This bit can use at LB/LLB.

Bit 4 **APM notify system to go into SUSPO,STBYO and Doze mode**

1:Go Inside
0:Wait

Bit 3 **APM involved in any PMU mode**

1:Enable
0:Disable

Bit 2 **The unit for STBYO counter**

1:1 Min
0:4 Sec

Bit 1 **SMI# toggle by period SMI# during LB or LLB (Read only)**

1:Toggle
0:Nothing

Bit 0 **SMI# toggle by General Purpose Timer (Read only)**

1:Toggle
0:Nothing

Register BBh

Bit 7 **VGA to be wakeup source**

1:Enable
0:Disable

Bit 6 **Monitor HI-MEMORY address [31:24] of VGA**

1:Enable
0:Disable

Bit 5 **C0000-C7FFF address trap of VGA**

1:Enable
0:Disable

Bit 4 **A0000-BFFFF address trap of VGA**

1:Enable
0:Disable

Bit 3 **Wakeup from Suspend (BIOS should write 1 to clear this bit after reading it)**

1:Active
0:Nothing

Bit 2 **Wakeup from Stbyo (BIOS should write 1 to clear this bit after reading it)**

1:Active
0:Nothing

Bit 1 **Wakeup from Doze (BIOS should write 1 to clear this bit after reading it)**

1:Active
0:Nothing

Bit 0 **Wake up by General Purpose Timer (BIOS should write 1 to clear this bit after reading it)**

1:Wake up
0:Nothing

Register BCh

Bits 7:0 Programmed HI-MEMORY address [31:24] of VGA linear address.

Register BDh

Bit 7 HI-MEMORY address 31

1:Decode
0:Don't Care

Bit 6 HI-MEMORY address 30

1:Decode
0:Don't Care

Bit 5 HI-MEMORY address 29

1:Decode
0:Don't Care

Bit 4 HI-MEMORY address 28

1:Decode
0:Don't Care

Bit 3 HI-MEMORY address 27

1:Decode
0:Don't Care

Bit 2 HI-MEMORY address 26

1:Decode
0:Don't Care

Bit 1 HI-MEMORY address 25

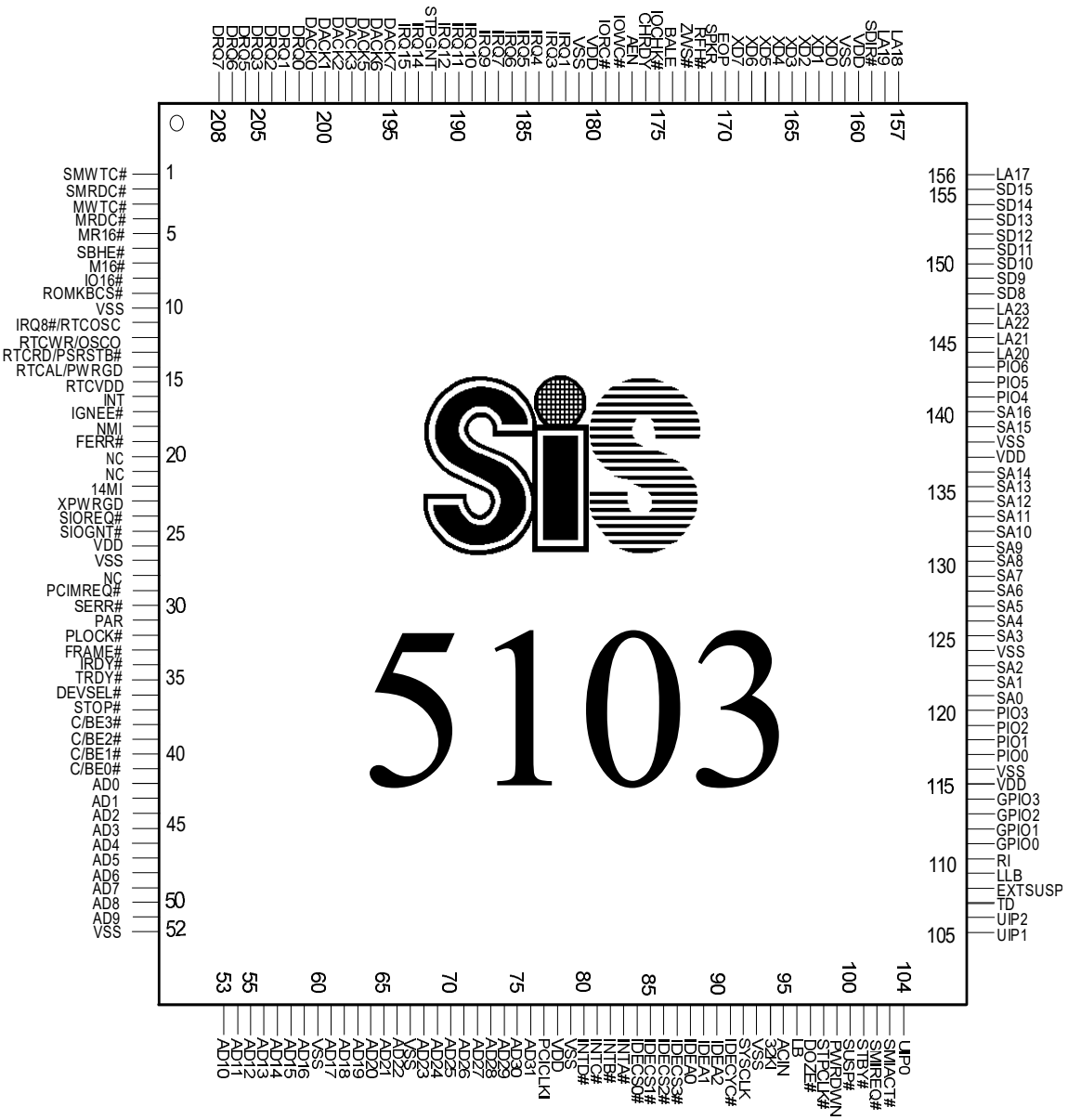
1:Decode
0:Don't Care

Bit 0 HI-MEMORY address 24

1:Decode
0:Don't Care

4.9 Pin Assignment and Description

4.9.1 SiS5103 Pin Assignment



4.9.2 SiS5103 Pin Listing

1=SMWTC#	A	53=AD10	A	105=UIP1	A	157=LA18	A
2=SMRDC#	A	54=AD11	A	106=UIP2	A	158=LA19	A
3=MWTC#	A	55=AD12	A	107=TD	A	159=SDIR#	A
4=MRDC#	A	56=AD13	A	108=EXTSUSP	A	160=VDD	A
5=MR16#	A	57=AD14	A	109=LLB	A	161=VSS	
6=SBHE#	A	58=AD15	A	110=RI	A	162=XD0	A
7=M16#	A	59=AD16	A	111=GPIO0	A	163=XD1	A
8=IO16#	A	60=VSS		112=GPIO1	A	164=XD2	A
9=ROMKBCS#	A	61=AD17	A	113=GPIO2	A	165=XD3	A
10=VSS		62=AD18	A	114=GPIO3	A	166=XD4	A
11=IRQ8#/RTCOSC	A	63=AD19	A	115=VDD	A	167=XD5	A
12=RTCWR/OSCO	A	64=AD20	A	116=VSS		168=XD6	A
13=RTCRD/PSRSTB#	A	65=AD21	A	117=PIO0	A	169=XD7	A
14=RTCAL/PWRGD	A	66=AD22	A	118=PIO1	A	170=EOP	A
15=RTCVDD	A	67=VSS		119=PIO2	A	171=SPKR	A
16=INT	A	68=AD23	A	120=PIO3	A	172=RFH#	A
17=IGNEE#	A	69=AD24	A	121=SA0	A	173=ZWS#	A
18=NMI	A	70=AD25	A	122=SA1	A	174=BALE	A
19=FERR#	A	71=AD26	A	123=SA2	A	175=IOCHK#	A
20=NC	A	72=AD27	A	124=VSS		176=CHRDY	A
21=NC	A	73=AD28	A	125=SA3	A	177=AEN	A
22=14MI	A	74=AD29	A	126=SA4	A	178=IOWC#	A
23=XPWRGD	A	75=AD30	A	127=SA5	A	179=IORC#	A
24=SIOREQ#	A	76=AD31	A	128=SA6	A	180=VDD	A
25=SIOGNT#	A	77=PCICLKI	A	129=SA7	A	181=VSS	
26=VDD	A	78=VDD	A	130=SA8	A	182=IRQ1	A
27=VSS		79=VSS		131=SA9	A	183=IRQ3	A
28=NC	A	80=INTD#	A	132=SA10	A	184=IRQ4	A
29=PCIMREQ#	A	81=INTC#	A	133=SA11	A	185=IRQ5	A
30=SERR#	A	82=INTB#	A	134=SA12	A	186=IRQ6	A
31=PAR	A	83=INTA#	A	135=SA13	A	187=IRQ7	A
32=PLOCK#	A	84=IDECS0#	A	136=SA14	A	188=IRQ9	A
33=FRAME#	A	85=IDECS1#	A	137=VDD	A	189=IRQ10	A
34=IRDY#	A	86=IDECS2#	A	138=VSS		190=IRQ11	A
35=TRDY#	A	87=IDECS3#	A	139=SA15	A	191=IRQ12	A
36=DEVSEL#	A	88=IDEA0	A	140=SA16	A	192=STPGNT	A
37=STOP#	A	89=IDEA1	A	141=PIO4	A	193=IRQ14	A
38=C/BE3#	A	90=IDEA2	A	142=PIO5	A	194=IRQ15	A
39=C/BE2#	A	91=IDECYC#	A	143=PIO6	A	195=DACK7	A
40=C/BE1#	A	92=SYSCLK	A	144=LA20	A	196=DACK6	A
41=C/BE0#	A	93=VSS		145=LA21	A	197=DACK5	A
42=AD0	A	94=32KI	A	146=LA22	A	198=DACK3	A
43=AD1	A	95=ACIN	A	147=LA23	A	199=DACK2	A
44=AD2	A	96=LB	A	148=SD8	A	200=DACK1	A
45=AD3	A	97=DOZE#	A	149=SD9	A	201=DACK0	A
46=AD4	A	98=STPCLK#	A	150=SD10	A	202=DRO0	A
47=AD5	A	99=PWRDWN	A	151=SD11	A	203=DRQ1	A
48=AD6	A	100=SUSP#	A	152=SD12	A	204=DRQ2	A
49=AD7	A	101=STBYO#	A	153=SD13	A	205=DRQ3	A
50=AD8	A	102=SMIREQ#	A	154=SD14	A	206=DRQ5	A
51=AD9	A	103=SMIACT#	A	155=SD15	A	207=DRQ6	A
52=VSS		104=UIP0	A	156=LA17	A	208=DRQ7	A

Remark : "A"=Power Group A

SiS5103 Suspend State

L:Output Force Low , IH:Chipset Internal Gate to High, OT:Output Tri-State , X:Users don't need to take care of anything.

1=SMWTC#	L	53=AD10	OT	105=UIP1	X	157=LA18	L
2=SMRDC#	L	54=AD11	OT	106=UIP2	X	158=LA19	L
3=MWTC#	L	55=AD12	OT	107=TD	X	159=SDIR#	L
4=MRDC#	L	56=AD13	OT	108=EXTSUSP	X	160=VDD	
5=MR16#	IH	57=AD14	OT	109=LLB	X	161=VSS	
6=SBHE#	L	58=AD15	OT	110=RI	X	162=XD0	L
7=M16#	IH	59=AD16	OT	111=GPIO0	X	163=XD1	L
8=IO16#	IH	60=VSS		112=GPIO1	X	164=XD2	L
9=ROMKBCS#	L	61=AD17	OT	113=GPIO2	X	165=XD3	L
10=VSS		62=AD18	OT	114=GPIO3	X	166=XD4	L
11=IRQ8#/RTCOSC	X	63=AD19	OT	115=VDD		167=XD5	L
12=RTCWR/OSCO	X	64=AD20	OT	116=VSS		168=XD6	L
13=RTCRD/PSRSTB#	X	65=AD21	OT	117=PIO0	X	169=XD7	L
14=RTCAL/PWRGD	X	66=AD22	OT	118=PIO1	X	170=EOP	L
15=RTCVDD	X	67=VSS		119=PIO2	X	171=SPKR	L
16=INT	L	68=AD23	OT	120=PIO3	X	172=RFH#	L
17=IGNEE#	L	69=AD24	OT	121=SA0	L	173=ZWS#	IH
18=NMI	L	70=AD25	OT	122=SA1	L	174=BALE	L
19=FERR#	IH	71=AD26	OT	123=SA2	L	175=IOCHK#	IH
20=NC	L	72=AD27	OT	124=VSS		176=CHRDY	OT/IH
21=NC	L	73=AD28	OT	125=SA3	L	177=AEN	L
22=14MI	X	74=AD29	OT	126=SA4	L	178=IOWC#	L
23=XPWRGD	IH	75=AD30	OT	127=SA5	L	179=IORC#	L
24=SIOREQ#	X	76=AD31	OT	128=SA6	L	180=VDD	
25=SIOGNT#	IH	77=PCICLKI	X	129=SA7	L	181=VSS	
26=VDD		78=VDD		130=SA8	L	182=IRQ1	IL
27=VSS		79=VSS		131=SA9	L	183=IRQ3	IL
28=NC	X	80=INTD#	IH	132=SA10	L	184=IRQ4	IL
29=PCIMREQ#	IH	81=INTC#	IH	133=SA11	L	185=IRQ5	IL
30=SERR#	IH	82=INTB#	IH	134=SA12	L	186=IRQ6	IL
31=PAR	OT	83=INTA#	IH	135=SA13	L	187=IRQ7	IL
32=PLOCK#	IH	84=IDECS0#	L	136=SA14	L	188=IRQ9	IL
33=FRAME#	OT/IH	85=IDECS1#	L	137=VDD		189=IRQ10	IL
34=IRDY#	OT/IH	86=IDECS2#	L	138=VSS		190=IRQ11	IL
35=TRDY#	OT/IH	87=IDECS3#	L	139=SA15	L	191=IRQ12	IL
36=DEVSEL#	OT/IH	88=IDEA0	L	140=SA16	L	192=STPGNT	X
37=STOP#	OT/IH	89=IDEA1	L	141=PIO4	X	193=IRQ14	IL
38=C/BE3#	OT	90=IDEA2	L	142=PIO5	X	194=IRQ15	IL
39=C/BE2#	OT	91=IDECYC#	L	143=PIO6	X	195=DACK7	L
40=C/BE1#	OT	92=SYSCLK	L	144=LA20	L	196=DACK6	L
41=C/BE0#	OT	93=VSS		145=LA21	L	197=DACK5	L
42=AD0	OT	94=32KI	X	146=LA22	L	198=DACK3	L
43=AD1	OT	95=ACIN	X	147=LA23	L	199=DACK2	L
44=AD2	OT	96=LB	X	148=SD8	L	200=DACK1	L
45=AD3	OT	97=DOZE#	X	149=SD9	L	201=DACK0	L
46=AD4	OT	98=STPCLK#	L	150=SD10	L	202=DRQ0	IL
47=AD5	OT	99=PWRDWN	X	151=SD11	L	203=DRQ1	IL
48=AD6	OT	100=SUSP#	X	152=SD12	L	204=DRQ2	IL
49=AD7	OT	101=STBYO#	X	153=SD13	L	205=DRQ3	IL
50=AD8	OT	102=SMIREQ#	X	154=SD14	L	206=DRQ5	IL
51=AD9	OT	103=SMIACT#	IH	155=SD15	L	207=DRQ6	IL
52=VSS		104=UIP0	X	156=LA17	L	208=DRQ7	IL

SiS5103 Output & I\O Signal States During Hard Reset

L: Low , H: High, Z: Tri-State , X: Don't Care

1=SMWTC#	Z	53=AD10	Z	105=UIP1	L	157=LA18	H
2=SMRDC#	Z	54=AD11	Z	106=UIP2	L	158=LA19	H
3=MWTC#	Z	55=AD12	Z	107=TD		159=SDIR#	Z
4=MRDC#	Z	56=AD13	Z	108=EXTSUSP		160=VDD	
5=MR16#		57=AD14	Z	109=LLB		161=VSS	
6=SBHE#	X	58=AD15	Z	110=RI		162=XD0	Z
7=M16#		59=AD16	Z	111=GPIO0	L	163=XD1	Z
8=IO16#		60=VSS		112=GPIO1	L	164=XD2	Z
9=ROMKBCS#		61=AD17	Z	113=GPIO2	L	165=XD3	Z
10=VSS		62=AD18	Z	114=GPIO3	L	166=XD4	Z
11=IRQ8#/RTCOSC		63=AD19	Z	115=VDD		167=XD5	Z
12=RTCWR/OSCO	H	64=AD20	Z	116=VSS		168=XD6	Z
13=RTCRD/PSRSTB#	Z	65=AD21	Z	117=PIO0	L	169=XD7	Z
14=RTCAL/PWRGD	Z	66=AD22	Z	118=PIO1	L	170=EOP	L
15=RTCVDD		67=VSS		119=PIO2	L	171=SPKR	L
16=INT	L	68=AD23	Z	120=PIO3	L	172=RFH#	H
17=IGNEE#	Z	69=AD24	Z	121=SA0	H	173=ZWS#	
18=NMI	L	70=AD25	Z	122=SA1	H	174=BALE	L
19=FERR#		71=AD26	Z	123=SA2	H	175=IOCHK#	
20=NC		72=AD27	Z	124=VSS		176=CHRDY	Z
21=NC		73=AD28	Z	125=SA3	H	177=AEN	L
22=14MI		74=AD29	Z	126=SA4	H	178=IOWC#	Z
23=XPWRGD		75=AD30	Z	127=SA5	H	179=IORC#	Z
24=SIOREQ#	H	76=AD31	Z	128=SA6	H	180=VDD	
25=SIOGNT#		77=PCICLKI		129=SA7	H	181=VSS	
26=VDD		78=VDD		130=SA8	H	182=IRQ1	
27=VSS		79=VSS		131=SA9	H	183=IRQ3	
28=NC		80=INTD#		132=SA10	H	184=IRQ4	
29=PCIMREQ#		81=INTC#		133=SA11	H	185=IRQ5	
30=SERR#		82=INTB#		134=SA12	H	186=IRQ6	
31=PAR	Z	83=INTA#		135=SA13	H	187=IRQ7	
32=PLOCK#		84=IDECS0#	H	136=SA14	H	188=IRQ9	
33=FRAME#	Z	85=IDECS1#	H	137=VDD		189=IRQ10	
34=IRDY#	Z	86=IDECS2#	H	138=VSS		190=IRQ11	
35=TRDY#	Z	87=IDECS3#	H	139=SA15	H	191=IRQ12	
36=DEVSEL#	Z	88=IDEA0	X	140=SA16	H	192=STPGNT	
37=STOP#	Z	89=IDEA1	X	141=PIO4	L	193=IRQ14	
38=C/BE3#	Z	90=IDEA2	X	142=PIO5	L	194=IRQ15	
39=C/BE2#	Z	91=IDECYC#	H	143=PIO6	L	195=DACK7	H
40=C/BE1#	Z	92=SYSCLK		144=LA20	H	196=DACK6	H
41=C/BE0#	Z	93=VSS		145=LA21	H	197=DACK5	H
42=AD0	Z	94=32KI		146=LA22	H	198=DACK3	H
43=AD1	Z	95=ACIN		147=LA23	H	199=DACK2	H
44=AD2	Z	96=LB		148=SD8	Z	200=DACK1	H
45=AD3	Z	97=DOZE#	H	149=SD9	Z	201=DACK0	H
46=AD4	Z	98=STPCLK#	Z	150=SD10	Z	202=DRQ0	
47=AD5	Z	99=PWRDWN	L	151=SD11	Z	203=DRQ1	
48=AD6	Z	100=SUSP#	H	152=SD12	Z	204=DRQ2	
49=AD7	Z	101=STBYO#	H	153=SD13	Z	205=DRQ3	
50=AD8	Z	102=SMIREQ#	Z	154=SD14	Z	206=DRQ5	
51=AD9	Z	103=SMIACT#		155=SD15	Z	207=DRQ6	
52=VSS		104=UIP0	L	156=LA17	H	208=DRQ7	

4.9.3 SiS5103 Pin Description

CPU Interface

Pin No.	Symbol	Type	Function
98	STPCLK#	OD	Stop clock indicates a stop clock request to the CPU.
19	FERR#	I	Floating point error from the CPU. It is driven active when a floating point error occurs.
17	IGNEE#	OD	IGNEE# is normally in high impedance state, and is asserted to inform CPU to ignore a numeric error. A resistor connected to either 3.3V (for P54C) or 5V (P5) is required to maintain a correct voltage level to CPU.
18	NMI	OD	Non-maskable, interrupt is rising edge trigger signal to the CPU and is generated to invoke a non-maskable interrupt. Normally, this signal is low. It goes high impedance state when a non-maskable interrupt source comes up. An external pull up resistor is required to be directly connected to CPU.
16	INT	OD	Interrupt goes high impedance whenever a valid interrupt request is asserted. Hence, an external pull up resister is required to be directly connected to the CPU's interrupt pin.

PCI Interface

Pin No.	Symbol	Type	Function
38-41	C/BE[3:0]#	I/O	PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the 5103 is a PCI bus master and inputs when it is a PCI slave.
76-68 66-61 59-53 51-42	AD[31:0]	I/O	Address and data are multiplexed on AD[31:0]. During the address phase of a transaction, AD[31:0] contains a physical address. During the data phase, AD[31:0] contains data. When the 5103 is a PCI master, it drives address on AD[31:2] and drives AD[1:0] low during the address phase. During the data phase, it drives data or latches data on AD[31:0] for write or read cycle respectively. When the 5103 is a target, AD[31:0] are inputs during the address phase. During the data phases, the 5103 drives data on AD[31:0] for read cycle, or latches data for write cycle.

33	FRAME#	I/O	FRAME# is asserted to indicate the beginning of a bus transaction and asserted until the last data phase. When the PCI master is ready to complete the final data phase, it deasserts FRAME#. When the 5103 is the target, FRAME# is an input to the 5103. 5103 drives FRAME# out when it is the PCI master. FRAME# is tri-state during reset.
34	IRDY#	I/O	When 5103 is the PCI master, it drives IRDY# to complete the current data phase of the transaction. During write cycles, the assertion of IRDY# indicates the 5103 has driven valid data on AD[31:0]. During read cycles, it indicates the 5103 is ready to latch the data. IRDY# is an input to the 5103 when the 5103 is the target and an output when the 5103 is a master.
35	TRDY#	I/O	TRDY# is an output when the 5103 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the 5103 is a PCI master, TRDY# is an input signal.
36	DEVSEL#	I/O	The 5103 asserts DEVSEL# when 5103's configuration registers or internal registers are addressed. DEVSEL# is also asserted when the 5103 subtractively decodes a cycle. When 5103 is the PCI master, DEVSEL# is an input to indicate a PCI target has responded to a 5103 initiated transaction. For all PCI transactions, the 5103 also samples DEVSEL# to decide to subtractively decode the cycle.
37	STOP#	I/O	When the 5103 is a target it asserts STOP# to request master to stop the current transaction. When 5103 is a master, the inputted STOP# causes the 5103 to stop the current transaction.

31	PAR	O	PAR is even parity across AD[31:0] and C/BE[3:0]# and regardless of whether or not all lines carry meaningful information. Both address and data phases the PAR is generated. PAR is driven one PCI clock after the corresponding address or data. PAR is driven by 5103 during the address phase of 5103 initiated transactions. During the data phase, 5103 also drives PAR when (1) 5103 is the master of a PCI write transaction. (2) 5103 is the target of a read transaction.
30	SERR#	I	The 5103 generates a NMI to the CPU when SERR# is active.
32	PLOCK#	I	The 5103 is locked when it samples PLOCK# is negated during the address phase. Any master attempt to access 5103 at this time, 5103 will initiate a retry to terminate the transaction. The locked state lasts until 5103 samples both PLOCK# and FRAME# are negated.
77	PCICLKI	I	PCICLK provides the fundamental timing and the internal operating frequency for the 5103. PCICLK is a buffered input of 5101 PCICLKO.
23	XPWRGD	I	Power Good is a power on reset and push button reset input.
83-80	INT[A:D]#	I	PCI Interrupt A to Interrupt D. INT[A:D]# can be remapped to one of eleven ISA compatible interrupts, please refer to registers 41h to 44h for more detailed information.
24	SIOREQ#	O	SIO Request. The 5103 SIOREQ# to request the PCI bus.
25	SIOGNT#	I	SIO Grant. It is driven by the 5101 to indicate that the PCI arbiter has granted the use of the PCI bus to the 5103.

ISA Interface

Pin No.	Symbol	Type	Function
140-139 136-125 123-121	SA[16:0]	I/O	System address. They are inputs when an external bus master is in control and are outputs at all other times.
158-156	LA[19:17]	I/O	Latched system address. They are inputs when an external bus master is in control and are outputs at all other times.

147-144	LA[23:20]	I/O	Normally, these signals are ISA latched system address. Latched system address. They are inputs when an external bus master is in control and are outputs at all other times.
169-162	XD[7:0]	I/O	Peripheral Data Bus lines.
155-148	SD[15:8]	I/O	System Data Bus are directly connected to the ISA slots.
8	IO16#	I	16-bit I/O chip select indicates that the AT bus cycle is a 16-bit I/O transfer when asserted or an 8-bit I/O transfer when it is negated.
7	M16#	I	16-bit memory chip select indicates a 16-bit memory transfer when asserted or an 8-bit memory transfer when it is negated.
6	SBHE#	I/O	Byte high enable signal indicates that the high byte has valid data on the ISA 16-bit data bus. This signal is an output except during ISA master cycles.
5	MR16#	I	Master* is an active low signal from AT bus. When active, it indicates that the ISA bus master has the control of the system. The address and control signals are all driven by the ISA bus master.
4	MRDC#	I/O	AT bus memory read command signal is an output pin during AT/DMA/refresh cycles and is an input pin in ISA master cycles.
3	MWTC#	I/O	AT bus memory write command signal is an output pin during AT/DMA cycles and is an input pin in ISA master cycles.
2	SMRDC#	I/O	AT bus memory read. It instructs the memory devices to drive data onto the data bus. It is active only when the memory being accessed is within the lowest 1MB.
1	SMWTC#	I/O	AT bus memory write. It instructs the memory devices to store the data presented on the data bus. It is active only when the memory being accessed is within the lowest 1MB.
179	IORC#	I/O	AT bus I/O read command signal is an output pin during AT or DMA cycles and is an input pin in ISA master cycles. When low, it strobes an I/O device to place data on the data bus.

178	IOWC#	I/O	AT bus I/O write command signal is an output pin during AT or DMA cycles and is an input pin in ISA master cycles. When low, it strobes data on the data bus into a selected I/O device.
177	AEN	O	Address Enable is driven high on the ISA bus to indicate the address lines are valid in DMA or ISA master cycles. It is low otherwise.
176	CHRDY	I/O	I/O channel ready is normally high. It can be pulled low by the slow devices on the AT bus to add wait states for the ISA memory or I/O cycles. When a DMA or an ISA master accesses a VL-Bus target, IORDY is an output to control the wait states.
175	IOCHK#	I	I/O channel Check is an active low input signal which indicates that an error has taken place on the I/O bus.
174	BALE	O	Bus address latch enable is used on the ISA bus to latch valid address from the CPU. Its falling edge starts the ISA command cycles.
173	ZWS#	I	Zero wait state is an active low signal. The system ignores the IORDY signal and terminates the AT bus cycle without additional wait state when it is asserted.
92	SYSCLK	I/O	ISA bus clock, for ISA bus controller, ISA bus interfaces and the DMA controller. It can be programmed to derive from the SYSCLK or from the 14MHz clock.
22	14MI	I	14MI is the buffered input of the external 14.318MHz oscillator.
172	RFH#	I/O	Refresh signal is used to initiate a refresh cycle. This signal is an input in ISA bus master cycles and is an output in other cycles.
170	EOP	O	Terminal Count of DMA. A pulse is generated by the DMA controller when the terminal count (TC) of any channel reaches 1. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and the TC bit in the Status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.

208-206, 205-202	DRQ7-5,3-0	I	DMA Request inputs are used by external devices to indicate when they need service from the internal DMA controllers.
182-191, 193,194	IRQ1, 3-7, IRQ 9, 10-12,14,15	I	These are the asynchronous interrupt request inputs to the 8259 controller.
195-201	DACK7-5,3-0	O	The DACK output line indicate that a request for DMA service has been granted by the 5103 or that a 16 bit master has been granted the bus.
9	ROMKBCS#	O	Keyboard or System ROM Chip Select.
171	SPKR	O	Speaker is the output for the speaker.
159	SDIR#	I/O	SD Low Byte Data Direction controls the direction of the low byte buffer between SD and XD. A high sets the data path direction from XD to SD and a low sets the data path direction from SD to XD.

Multi-function Pins

Pin No.	Symbol	Type	Function
11	IRQ8#/RTCOSC	I	When using internal RTC: This pin is used as the time base of the built-in RTC. This signal is from the 32.768 KHz crystal oscillator. When using external RTC: This pin is used as IRQ8#, which is the asynchronous interrupt request input to the 8259 controller.
13	RTCRD/PSRSTB#	I/O	When using internal RTC: This signal is used as PSRSTB# (power strobe). PSRSTB# establishes the condition of the control register in RTC when power is first applied to the device. When using external RTC: The signal is used as the data read strobe of RTC. It is used to drive the RTC data onto the XD bus when the CPU accesses the RTC.
12	RTCWR/OSCO	O	When using internal RTC:this pin should be connected the other end of the 32.768khz crystal or left unconnected if an oscillator is used. When using external RTC: This pin is used as data write strobe of RTC. It is used to store the data presented on the XD bus when CPU accesses the RTC. This pin must be connected to the R/W pin of RTC.

14	RTCALE/PWRGD	I/O	When using internal RTC: The signal must be high for bus cycles in which the CPU accesses the RTC. All address, data, data strobe, and R/W pins of the internal RTC are disconnected from the processor when this signal is low. When using external RTC: The signal is used to latch the address from the XD bus when CPU accesses RTC.

IDE Interface

Pin No.	Symbol	Type	Function
87-84	IDECS[3:0]#	O	When IDECYC# is asserted, they become IDE Chip Select signals, selects the command block register and selects the control block register.
91	IDECYC#	I	IDE Cycle.
90-88	IDEA[2:0]	O	Address bits indicating which register is to read from or write into.

PMU Interface

Pin No.	Symbol	Type	Function
94	32KI	I	32KI is the suspend clock source of the 32KHz oscillator.
29	PCIMREQ#	I	the pin is served as PCIMREQ#.
192	STPGNT	I	Stop Grant input signal form 5101,that the following cycle is in stop grant state, the signal will active high.
95	ACIN	I	The pin is served as AC power indicator.
96	LB	I	The pin is served as input for low battery indicator.
97	DOZE#	O	Doze Output. It can be used in controlling peripheral's clock generator's selector. Default status during initialization is : Power on state: High; Power good state: High.
99	PWRDWN	O	This signal outputs to 5101 for power down. Default status during initialization is : Power on state: Low; Power good state: Low.
100	SUSPO#	O	Suspend output status. This pin will be active when system enters suspend mode. Default status during initialization is : Power on state: High; Power good state: High.
101	STBYO#	O	Standby output status. This pin will be active when system enters standby mode. Default status during initialization is : Power on state: High; Power good state: High.

102	SMIREQ#	O	The pin is served as SMI request to 5101. Default status during initialization is : Power on state: High; Power good state: High

103	SMIACT#	I	SMI acknowledge from CPU
110	RI	I	Ring indicator. This input provides a wake-up call from a modem.
109	LLB	I	Very low battery indicates a very low battery condition.
114-111	GPIO[3:0]	I/O	General purpose I/O signals. These four I/O signals are provided for general purpose usage. Initialized to be input after power on.
143-141, 120-117	PIO[6:0]	I/O	Programmable I/O Signals. Initialized to be input after power on.
106-104	UIP[2:0]	I/O	User define programmable I/O signals. The I/O port is readable and writable individual. Initialized to be input after power on.
107	TD	I	Thermal indicator active high.
108	EXTSUSP	I	External suspend.
20,21,28	NC		No connection.
15	RTCVDD		Battery power for RTC.
26, 78, 115, 137, 160, 180	VDD		For Power Group A.
10, 27, 52, 60, 67, 79, 93, 116, 124, 138, 161, 181	VSS		Ground.

4.10 Electrical Characteristics

4.10.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{O}C
Storage temperature	-40	125	^{O}C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V
Power Dissipation		1	W

Note:
Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

4.10.2 DC Characteristics

TA = 0 - 85 ^{O}C, VSS = 0V , VDD=5V$\pm$5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage			V	

V_{OL}	Output Low Voltage		0.45	V	
V_{OH}	Output High Voltage	2.4		V	
I_{OL1}	Output Low Current	4		mA	*Note 1*
I_{OH1}	Output High Current	4		mA	*Note 1*
I_{OL2}	Output Low Current	8		mA	*Note 2*
I_{OH2}	Output High Current	8		mA	*Note 2*
I_{OL3}	Output Low Current	8,12		mA	*Note 3*
I_{OH3}	Output High Current	8,12		mA	*Note 3*
I_{OL4}	Output Low Current	6		mA	*Note 4*
I_{OH4}	Output High Current	6		mA	*Note 4*
I_{IL}	Input Leakage Current		+10	mA	
I_{OL}	Output Leakage Current		-10	mA	
C_{IN}	Input Capacitance		12	pF	
C_{OUT}	Output Capacitance		12	pF	
$C_{I/O}$	I/O Capacitance		12	pF	

Note:

1. I_{OL1} and I_{OH1} apply to the following signals: ROMKBCS#, RTCWR#, RTCRD/PSRSTB#, RTCALE/PWRGD, SIOREQ#, PAR, C/BE3#, C/BE2#, C/BE1#, C/BE0#, AD[31:0], SDIR#, XD[7:0], SPKR, BCLK, INT, NMI, IGNEE#, STPCLK#, SMI#, PIO[6:0], GPIO[3:0], DOZE#, STBYO#, DACK[7:0], SW32K, SUSP#, UIP[2:0], IDECYC#.
2. I_{OL2} and I_{OH2} apply to the following signals: RFH#, CHRDY, AEN, BALE, EOP, SD[15:8], IDECS[3:0]#, IDEA[2:0].
3. I_{OL3} and I_{OH3} apply to the following signals: SMWTC#, SMRDC#, MWTC#, MRDC#, SBHE#, LA[23:20]/IDECS[3:0]#, LA[21:17], SA[16:0], IOWC#, IORC#. Please refer to Register description.
4. I_{OL4} and I_{OH4} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#.

4.10.3 AC Characteristics

The AC characteristic is measured under the following capacitive condition.

Capacitive load	Pin
35pf	BCLK, DAK[0:2], BALE, AEN, NMI, SDIR, EOP, SPKR, INT
50pf	FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, C/BE[3:0]#, XD[7:0]
150pf	SD[15:8], SBHE#, RFH#, CHRDY, MWTC#, MRDC#, IORC#, IOWC#, SA[19:0], LA[23:17]

Para-meter	Description	Min	Typ	Max	Unit

ISA Bus Interface Signals					
	BCLK High		63.2		ns
	BCLK Low		56.8		ns
t1	BALE valid delay from BCLK		4.5	7	ns

t2	IORC#, IOWC#, MRDC#, MWTC# valid delay from BCLK		16.5	24	ns
t3	IORC#, IOWC#, MRDC#, MWTC# invalid delay from BCLK		12	18	ns
t5a	M16# setup time to BCLK rising		15		ns
t5b	M16# hold time from BCLK rising		6		ns
t6a	IO16# setup time to BCLK falling		19		ns
t6b	IO16# hold time from BCLK falling		6		ns
t7	16 bit IORC#, IOWC# pulse width		1.5		BCLK
	8 bit IORC#, IOWC# pulse width		4.5		BCLK
	16 bit MRDC#, MWTC# *1		2		BCLK
	8 bit MRDC#, MWTC#		4.5		BCLK
	ROM MRDC#, MWTC# *1		2		BCLK
Data Buffer Interface					
t8	SD, XD data set up time to IORC#, MRDC# inactive	10			ns
t9	SD, XD data hold time to IORC#, MRDC# inactive	3			ns
t10	SD, XD valid data delay from IOWC#,	15	22		ns
	MWTC# active (for data swapping)				
t11a	SD, XD data hold time from IOWC#, MWTC# inactive in write disassembly cycle	15	22		ns
t11a	SD, XD data hold time from IOWC#, MWTC# inactive in write cycle		172		ns
t12	SD, XD valid to IOWC#, MWTC# active		142		ns
t13	SDIR deassertion to IORC#, MRDC# active (16 bit)		1	2	BCLK
	SDIR deassertion to IORC#, MRDC# active (8 bit)	1.5		2.5	BCLK
t14	SDIR assertion delay from IORC#, MRDC# inactive		2		BCLK
Address Buffer Interface					
t15	SA, LA propagation delay from PCICLK in Frame# address phase		34	51	ns
t16	SA0, SA1, SBHE# hold time from the negation of IORC#, IOWC#, MWTC#, MRDC#	10			ns

t17a	CHRDY setup time to BCLK rising		15.2		ns
t17b	CHRDY hold time to BCLK rising	14.8			ns
t44	ZWS# setup time to BCLK falling		10		ns
t45	ZWS# hold time to BCLK falling	20			ns

DMA Compatible Timings					
t18	DAK active to IORC# active		0.5		DMACLK
t19	DAK active to IOWC# active		1.5		DMACLK
t20	DAK active hold from IORC# inactive		0.5		DMACLK
t21	DAK active hold from IOWC# inactive		0.5		DMACLK
t22a	AEN active to IORC# active		6		DMACLK
t22b	AEN active to IOWC# active		7		DMACLK
t23a	AEN inactive from IORC# inactive		3		DMACLK
t23b	AEN inactive from IOWC# inactive		4		DMACLK
t24a	BALE active to IORC# active		1.5		DMACLK
t24b	BALE active to IOWC# active		2.5		DMACLK
t25a	BALE inactive from IORC# inactive		1		DMACLK
t25b	BALE inactive from IOWC# inactive		1		DMACLK
t26a	LA, SA, SBHE# valid set up time to IORC#		1		DMACLK
t26b	LA, SA, SBHE# valid set up time to IOWC#		2		DMACLK
t27a	LA, SA, SBHE# valid hold from IORC#		0.5		DMACLK
t27b	LA, SA, SBHE# valid hold from IOWC#		0.5		DMACLK
t28	IORC# pulse width		4		DMACLK
t29	IOWC# pulse width		2		DMACLK
t30	MRDC# pulse width		3		DMACLK
t31	MWTC# pulse width		3		DMACLK
t32	MWTC# active from IORC# active		1		DMACLK
t33	IOWC# active from MRDC# active		1		DMACLK
t34	MWTC# inactive from IORC# inactive		0		ns
t35	IOWC# inactive from MRDC# inactive		1.5		ns
t36	Read data valid from IORC# active		267.5		ns
t37	Read data valid hold from IORC# inactive		32.2		ns
t38	Write data valid setup to IOWC# inactive		162.5		ns
t39	Write data valid hold from IOWC# inactive		13.2		ns
t40	EOP active delay from IOWC# active		-7.6		ns
t41	EOP active delay from IORC# active		112.3		ns
t42	EOP active delay from IOWC# inactive		0.7		ns
t43	EOP active delay from IORC# inactive		0.8		ns
Note: DMACLK = BCLK or BCLK/2 depends on bit 0 of ISA configuration register 01H.**Refresh Timing**					

t44	RFH# active setup to MRDC# active		2		BCLK
t45	RFH# active hold from MRDC# inactive		0.5		BCLK
t46	AEN active to RFH# active delay		3		ns
Miscellaneous Timing					
t47	SERR#, IOCHK# active to NMI output floating active			200	ns
t48	INT output floating delay from IRQ active			100	ns
t49	IRQ active pulse width	100			ns
t50	IGNEE# active from IOWC# active for port F0h access			220	ns
t51	IGNEE# inactive from FERR# inactive			150	ns
t52	SPKR valid delay from OSC timing			200	ns
t53	RTCALE pulse width		532.3		ns
t54	RTCALE active from IORW# active		4		ns
t54a	RTCWR active from IOWR# active		5		ns
t54b	RTCRD active from IORD# active		5		ns
t54c	RTCWR inactive from IOWR# inactive	3.5	5	10	ns
t54d	RTCRD inactive from IORD# inactive	3.5	5	10	ns

*1: No command delay

PCI Bus AC Specifications					
PCI shared signals A.C. Characteristics (VDD=5V±5%, Tcase=0 to 85°C)					
		Min	**Max**	**Units**	**Notes**
t57	PCICLK to signal valid delay		11	ns	CL=50pf
t58	PCICLK to signal invalid delay	2		ns	
t59	Hi-Z to Active delay from PCICLK	2		ns	
t60	Active to Hi-Z delay from PCICLK		28	ns	
t61	Input signal valid setup time before PCICLK	7		ns	
t62	Input signal hold time from PCICLK	0		ns	

Note: PCI shared signals are AD[31:0], C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, IDSEL#, DEVSEL#, PAR, SERR#

PCI IDE Timing					
Para-meter	**Description**	**Min**	**Typ**	**Max**	**Unit**
t63	Read Active Time	1		13	PCICLK
t64	Read Recovery Time	1		18	PCICLK
t65	Write Active Time	1		13	PCICLK
t66	Write Recovery Time	1		18	PCICLK
t67	Read Cycle Time (Prefetch Buffer Enable)	3	4		PCICLK

t68	Write Cycle Time (Post Write Buffer Enable)	5	6		PCICLK

4.10.4 AC Timing Diagram

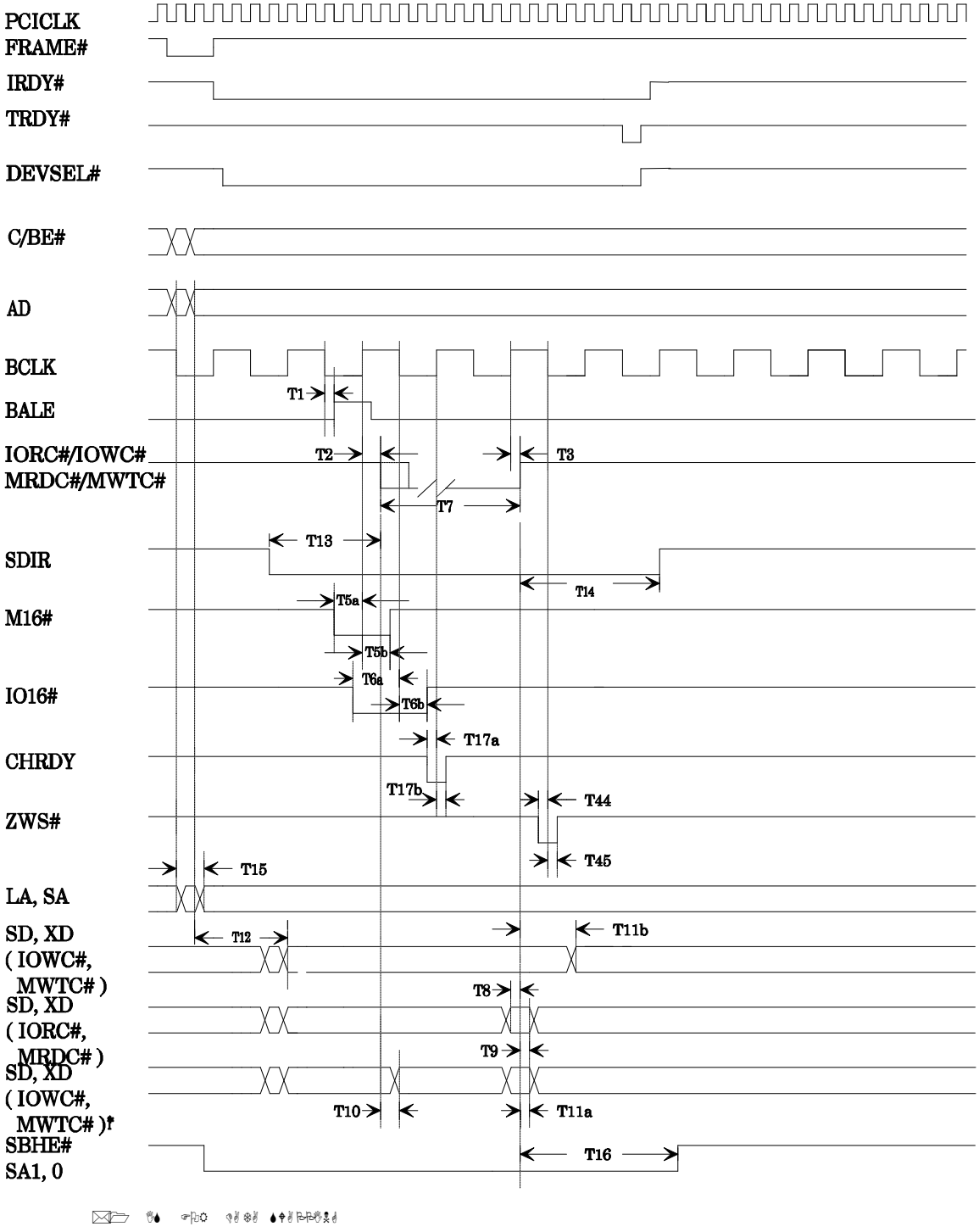
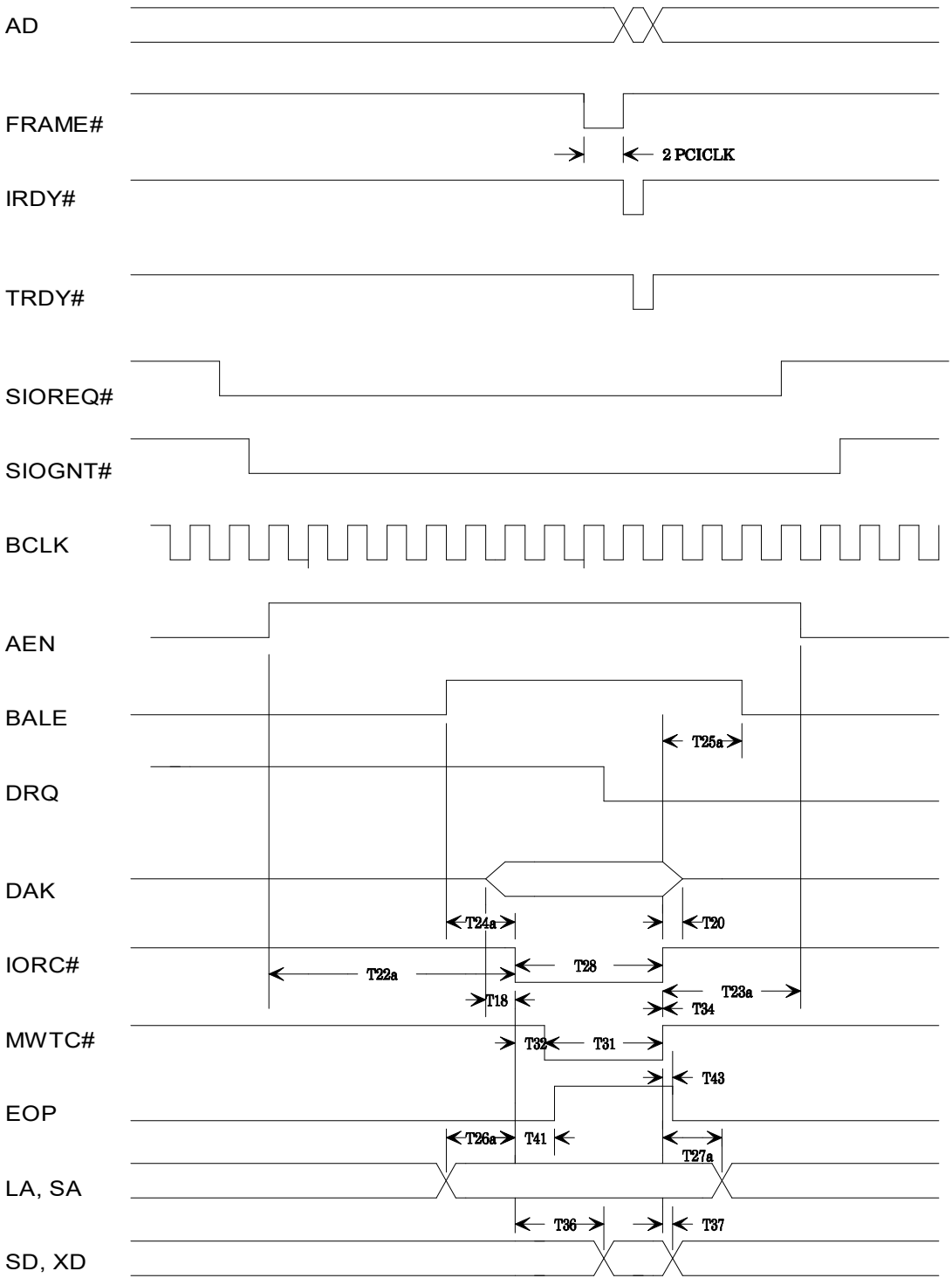
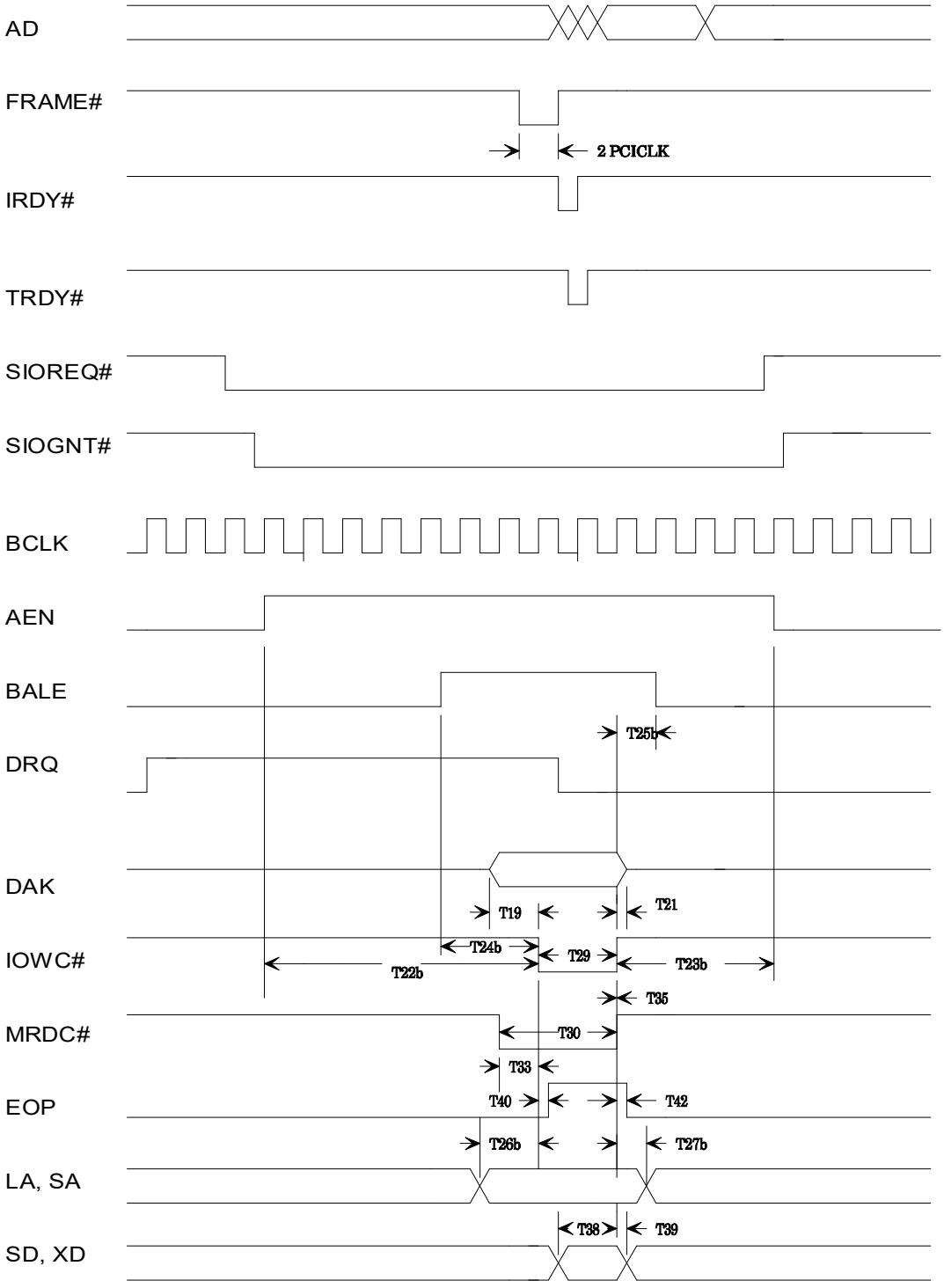


Figure 4.8 PCI to AT Bus Cycle



DMA cycle (IOWC#, MRDC#), DMACLK = BCLK

Figure 4.9 DMA Cycle (IOWC#, MRDC#)



DMA cycle (IORC#, MWTC#), DMACLK = BCLK

Figure 4.10 DMA Cycle (IORC#, MWTC#)

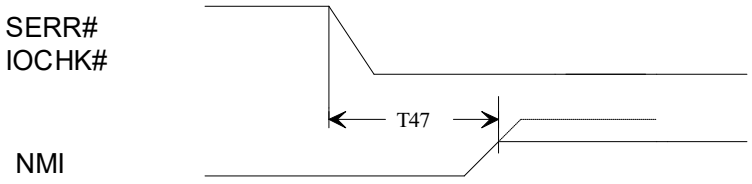


Figure 4.11 NMI Timing

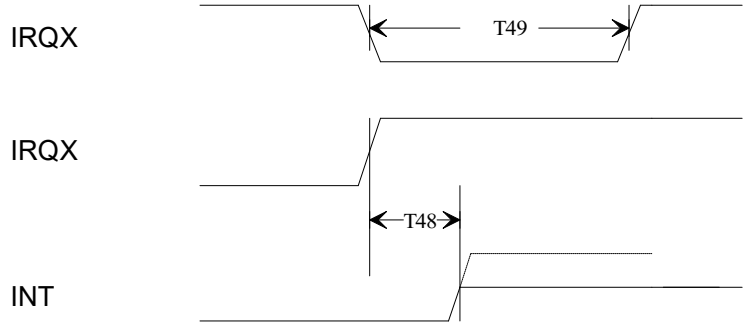


Figure 4.12 Interrupt Timing

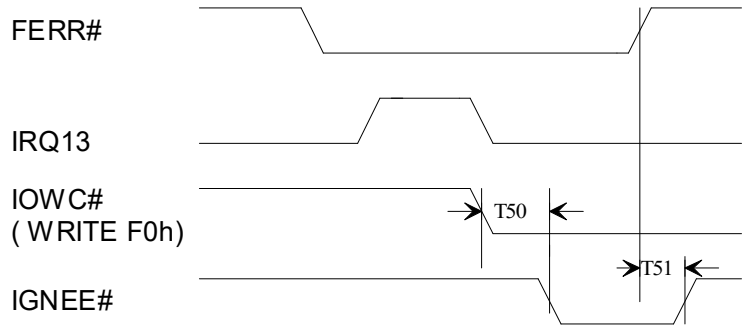


Figure 4.13 Coprocessor Error Support Timing

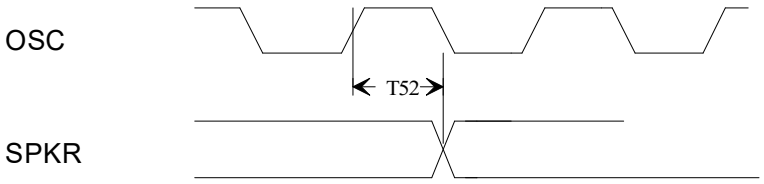


Figure 4.14 Speaking Timing

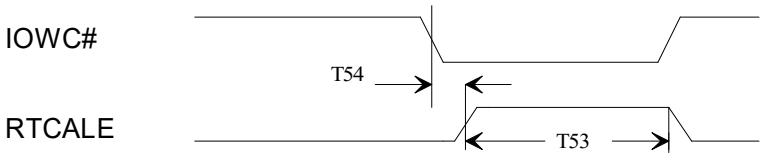


Figure 4.15 RTC Timing

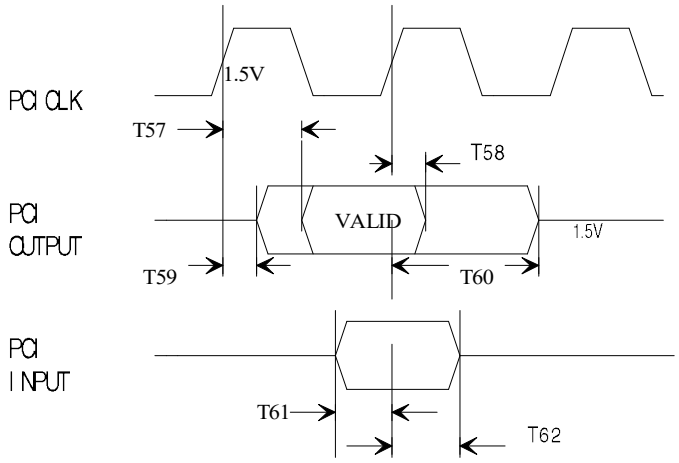


Figure 4.16 PCICLK Timing

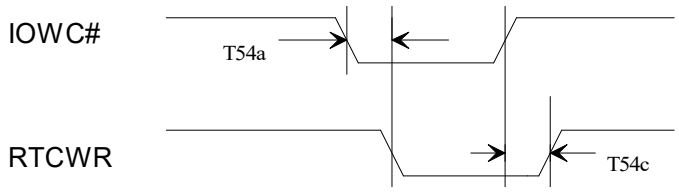


Figure 4.17 RTC Timing

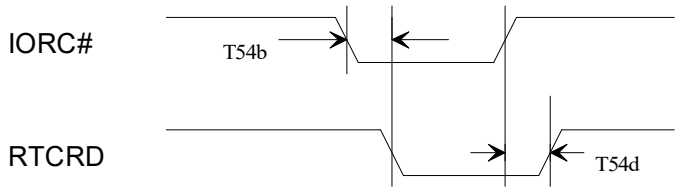


Figure 4.18 RTC Timing

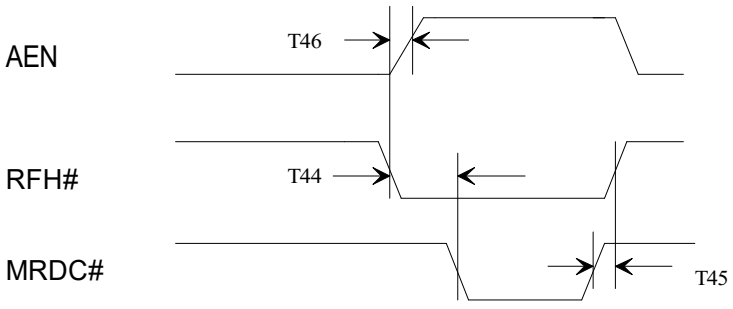


Figure 4.19 Refresh Timing

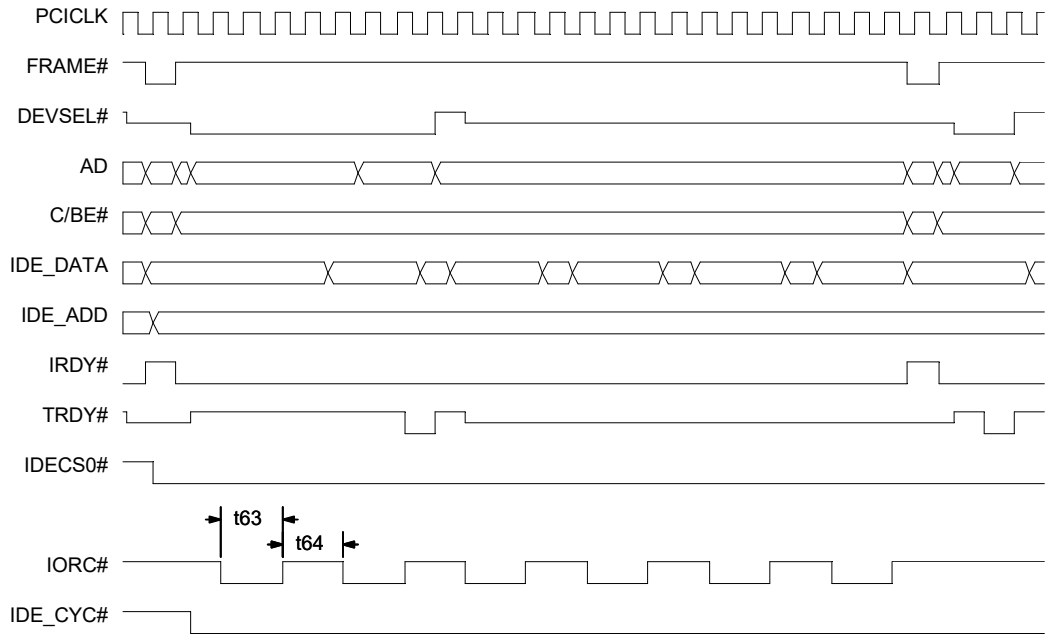


Figure 4.20 IDE Read Cycle

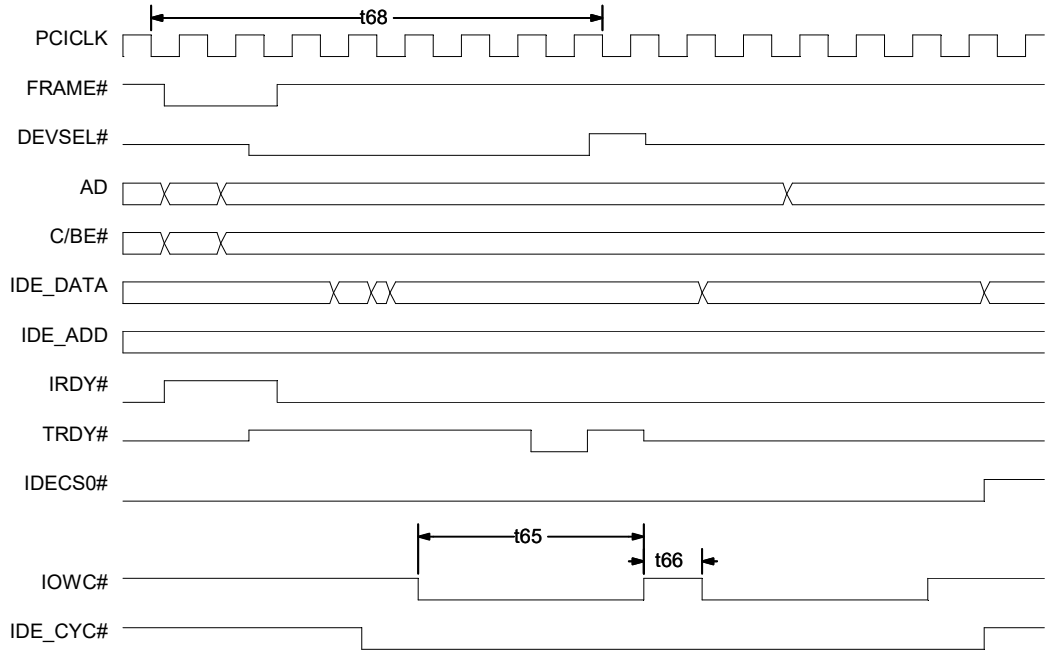


Figure 4.21 IDE Write Cycle

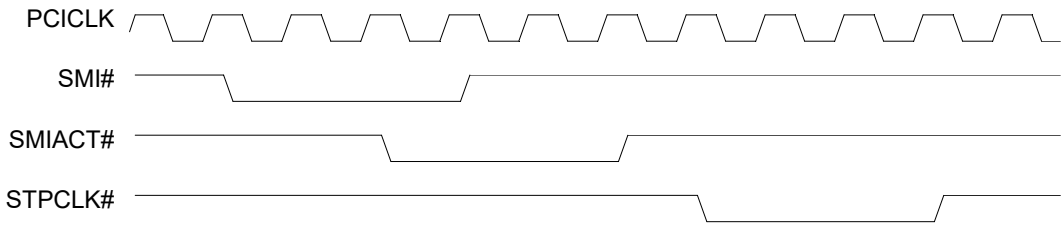


Figure 4.22 PMU Timing 1

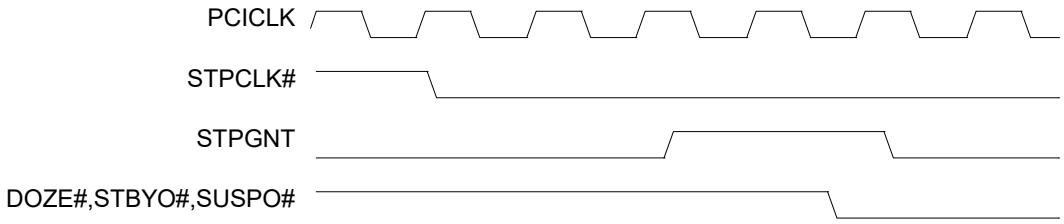


Figure 4.23 PMU Timing 2

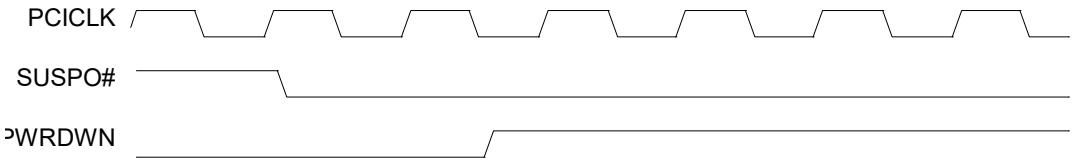
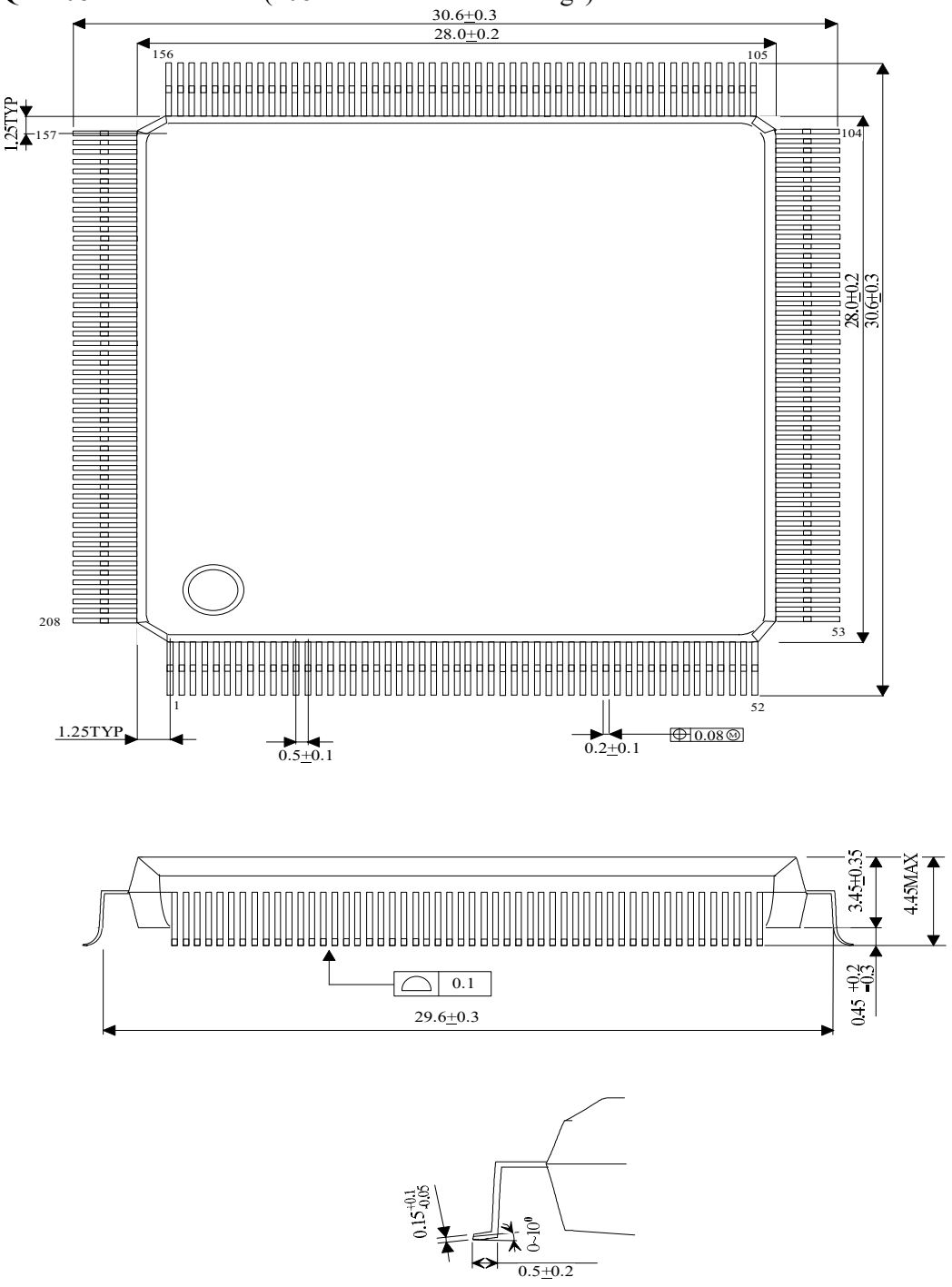


Figure 4.24 Leakage Timing

6. MECHANICAL DIMENSION

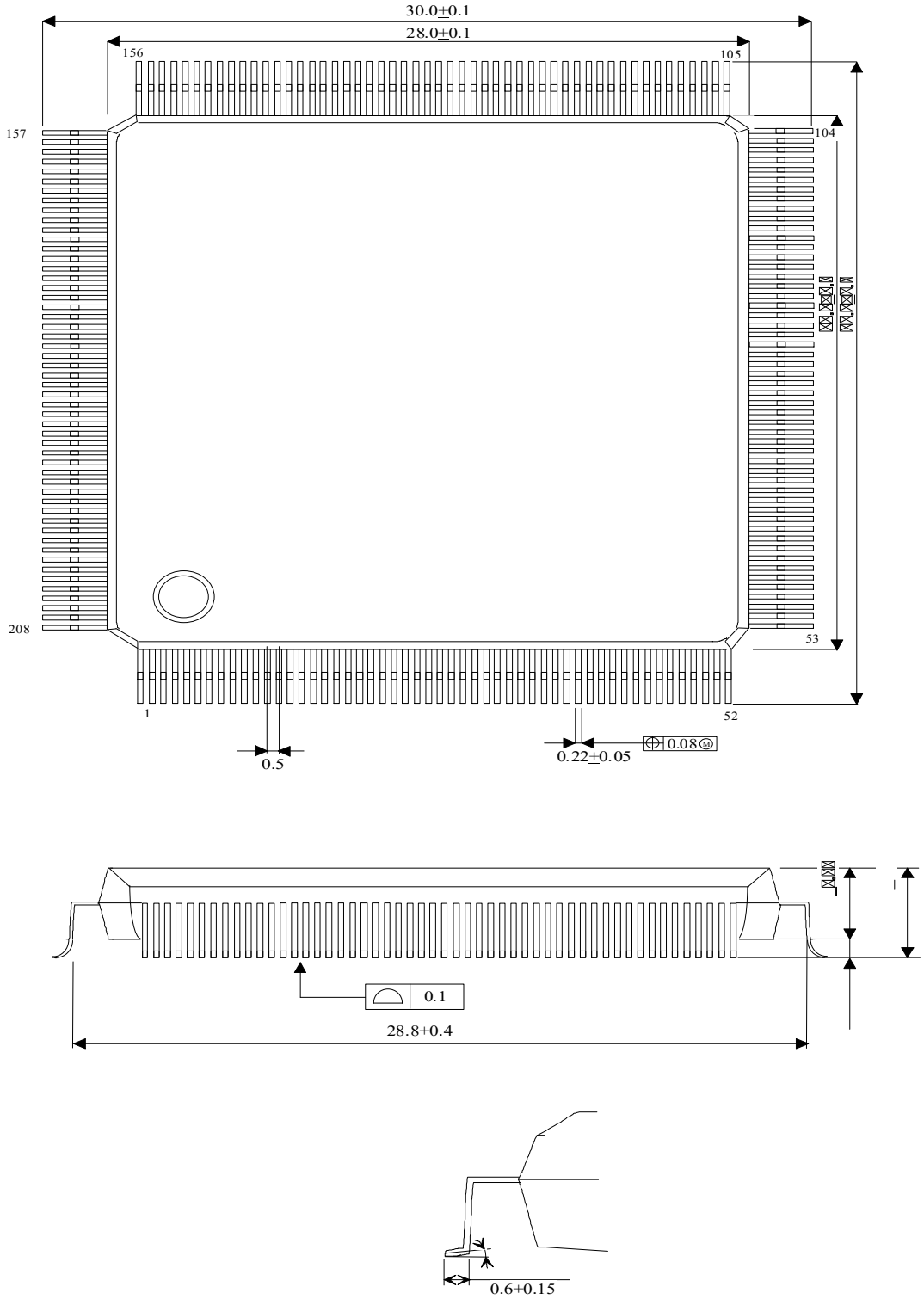
6.1 SiS5101, SiS5102, SiS5103 (208 pins)

QFP208-P (208-Pin Plastic Flat Package) Unit:mm



6.3 SiS5101, SiS5103 (208 pins)

TQFP208-P (208-Pin Plastic Flat Package) Unit:mm



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