Intel 430TX PCIset
Desktop Design Guide

June 1997

297739-001

CG-041493

TABLE OF CONTENTS

1

Overview

CHAPTER 1
OVERVIEW

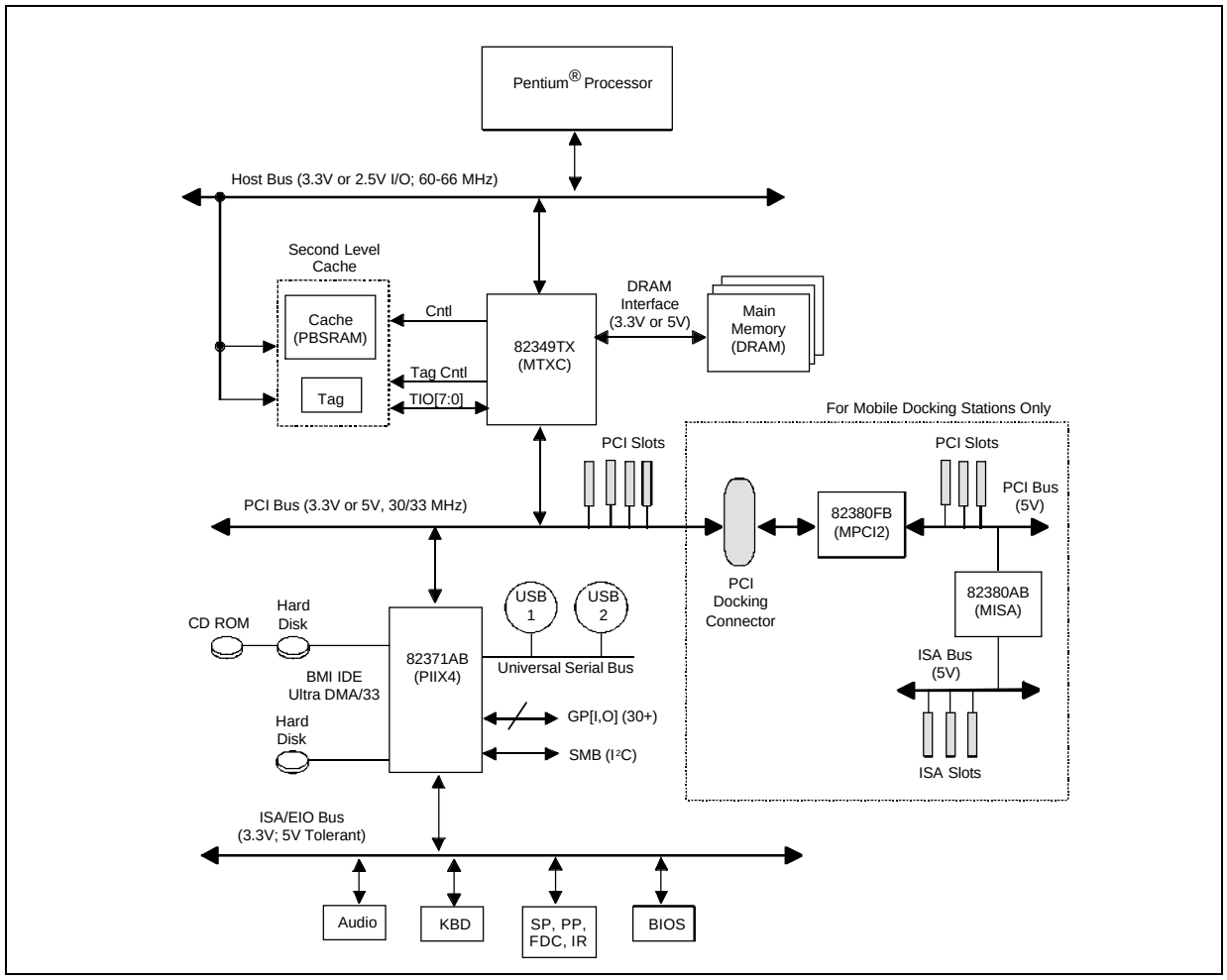


Figure 1-1. Intel 430TX PCIset System Block Diagram

1. Overview

1.1 Intel 430TX PCIset

The MTXC host bridge provides a completely integrated solution for the system controller and datapath components in a Pentium® processor system. The MTXC supports all Pentium family processors since P54C, it has 64-bit Host and DRAM Bus Interface, 32-bit PCI Bus Interface, Second level Cache Interface, and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus (see Figure 1-1).

The MTXC bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. The MTXC implements 2.5V and 3.3V drivers and 5V tolerant receivers. The MTXC connects directly to the

Pentium processor 3.3V or 2.5V host bus, directly to 5V or 3.3V DRAMs, and directly to the 5V or 3.3V PCI bus. The 430TX also interfaces directly to the 3.3V or 5.0V TAGRAM and 3.3V Cache.

The MTXC works with the PCI IDE/ISA Accelerator 4 (PIIX4). The PIIX4 provides the PCI-to-ISA/EIO bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Plug-n-Play port, APIC interface, PCI 2.1 Compliance, SMBUS interface, and Universal Serial Bus Host Controller functions.

DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard (or Fast) Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 6-1-1-1 for SDRAM, 5-2-2-2 for EDO, and 6-3-3-3 for FPM.

The DRAM interface supports 4 Mbytes to 256 Mbytes with six RAS lines. The MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit DRAM and SDRAM technology, both symmetrical and asymmetrical. Parity is not supported, and for loading reasons, x32 and x64 SIMMs/DIMMs/SO-DIMMs should be used.

Second Level Cache

The second level cache is direct mapped and supports both 256-Kbyte and 512-Kbyte SRAM configuration using Pipeline Burst SRAM or DRAM Cache SRAM. The Cache performance is 3-1-1-1 for line read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cacheless configuration is also supported.

PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX4 bus master requests.

Datapath and Buffers

The MTXC contains three sets of data buffers for optimizing data flow. A five QWord deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write backs, and PCI-to-DRAM transfers. This buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides DWord merging and burst merging for CPU-to-DRAM write cycles. In addition, an extra line of buffering is provided that is combined with the DRAM Write Buffer to supply an 18 DWord deep buffer for PCI to main memory writes. A five DWord buffer is provided for CPU-to-PCI writes to help maximize the bandwidth for graphic writes to the PCI bus. Also, five QWords of prefetch buffering has been added to the PCI-to-DRAM read path that allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interfaces directly to the Host and DRAM data bus.

Enhanced Power Management Features

The MTXC implements extensive power management features. The CLKRUN# feature enables controlling of the PCI clock (on/off). The MTXC supports POS, STR, STD, and Soft-off suspend states. SUSCLK and SUSSTAT1# signals are used for implementing Suspend Logic. The MTXC supports two SMRAM modes; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). The C_SMRAM is the traditional SMRAM feature implemented in Intel PCIsets. The E_SMRAM is a new feature that supports writeback cacheable SMRAM space up to 1 Mbytes. In order to minimize the idle power, the internal clock in MTXC is turned off (gated off) when there is no activity on the Host and PCI Bus.

PIIX4's power management functions include enhanced clock control, local and global monitoring support for 14 individual devices, and various low-power (suspend) states, such as Power-On Suspend, Suspend-to-DRAM, and Suspend-to-Disk. A hardware-based thermal management circuit permits software-independent entrance to low-power states. PIIX4 has dedicated pins to monitor various external events (e.g., interfaces to a notebook lid, suspend/resume button, battery low

indicators, etc.). PIIX4 contains full support for the Advanced Configuration and Power Interface (ACPI) Specification.

PCI to ISA/EIO Bridge

PIIX4 is compatible with the PCI Rev 2.1 specification, as well as the IEEE 996 specification for the ISA (AT) bus. On PCI, PIIX4 operates as a master for various internal modules, such as the USB controller, DMA controller, IDE bus master controller, distributed DMA masters, and on behalf of ISA masters. PIIX4 operates as a slave for its internal registers or for cycles that are passed to the ISA or EIO buses. All internal registers are positively decoded.

PIIX4 can be configured for a full ISA bus or a subset of the ISA bus called the Extended IO (EIO) bus. The use of the EIO bus allows unused signals to be configured as general purpose inputs and outputs. PIIX4 can directly drive up to five ISA slots without external data or address buffering. It also provides byte-swap logic, I/O recovery support, wait-state generation, and SYSCLK generation. X-Bus chip selects are provided for Keyboard Controller, BIOS, Real Time Clock, a second microcontroller, as well as two programmable chip selects.

PIIX4 can be configured as either a subtractive decode PCI to ISA bridge or as a positive decode bridge. This gives a system designer the option of placing another subtractive decode bridge in the system (e.g., a 380FB PCI Docking StationPCIset).

IDE Interface (Bus Master capability and synchronous DMA Mode)

The fast IDE interface supports up to four IDE devices providing an interface for IDE hard disks and CD ROMs. Each IDE device can have independent timings. The IDE interface supports PIO IDE transfers up to 14 Mbytes/sec. and Bus Master IDE transfers up to 33 Mbytes/sec. It does not consume any ISA DMA resources.The IDE interface integrates 16x32-bit buffers for optimal transfers.

PIIX4's IDE system contains two independent IDE signal channels. They can be electrically isolated independently, allowing for the implementation of a "glueless" Swap Bay. They can be configured to the standard primary and secondary channels (4 devices) or primary drive 0 and primary drive 1 channels (2 devices). This allows flexibility in system design and device power management.

Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 82C37 DMA controllers, with seven independently programmable channels. Channels [0:3] are hardwired to 8-bit, count-by-byte transfers, and channels [5:7] are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers. The DMA controller also generates the ISA refresh cycles.

The DMA controller supports two separate methods for handling legacy DMA via the PCI bus. The PC/PCI protocol allows PCI-based peripherals to initiate DMA cycles by encoding requests and grants via three PC/PCI REQ#/GNT# pairs. The second method, Distributed DMA, allows reads and writes to 82C37 registers to be distributed to other PCI devices. The two methods can be enabled concurrently. The serial interrupt scheme typically associated with Distributed DMA is also supported.

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function, refresh request, and speaker tone. The 14.31818-MHz oscillator input provides the clock source for these three counters.

PIIX4 provides an ISA-Compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, PIIX4 supports a serial interrupt scheme. PIIX4 provides full support for the use of an external IO APIC.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the circuit.

Enhanced Universal Serial Bus (USB) Controller

The PIIX4 USB controller provides enhanced support for the Universal Host Controller Interface (UHCI).This includes support that allows legacy software to use a USB-based keyboard and mouse.

RTC

PIIX4 contains a Motorola* MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768-kHz crystal and a separate 3V lithium battery that provides up to 7 years of protection.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC also supports a date alarm, that allows for scheduling a wake up event up to 30 days in advance, rather than just 24 hours in advance.

GPIO and Chip Selects

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on PIIX4 configuration. Two programmable chip selects are provided which allows the designer to place devices on the X-Bus without the need for external decode logic.

Pentium and Pentium® Pro processor Interface

The PIIX4 CPU interface allows connection to all Pentium and Pentium Pro processors. The Sleep mode for the Pentium Pro processors is also supported.

System Management Bus (SMBus)

PIIX4 contains an SMBus Host interface that allows the CPU to communicate with SMBus slaves and an SMBus Slave interface that allows external masters to activate power management events.

Configurability

PIIX4 provides a wide range of system configuration options. This includes full 16-bit I/O decode on internal modules, dynamic disable on all the internal modules, various peripheral decode options, and many options on system configuration.

1.1.1 82439TX MTXC Features

- **Supports Mobile and Desktop**
- **Supports the Pentium Processor Family Host Bus at 66 MHz and 60 MHz at 3.3V and 2.5V**
- **PCI 2.1 Compliant**
- **Integrated Data Path**
- **Integrated DRAM Controller**
  - **— 4-Mbytes to 256-Mbytes main memory**
  - **— 64-Mbit DRAM/SDRAM Technology Support**
  - **— FPM (Fast Page Mode), EDO and SDRAM DRAM Support**
  - **— 6 RAS Lines Available**
  - **— Integrated Programmable Strength for DRAM Interface**
  - **— CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO**
  - **— CAS-Before-RAS and Self Refresh for SDRAM**
- **Integrated L2 Cache Controller**
  - **— 64-MB DRAM Cacheability**
  - **— Direct Mapped Organization—Write Back Only**
  - **— Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM**
  - **— Cache Hit Read/Write Cycle Timings at 3-1-1-1**
  - **— Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1**
  - **— 64K x 32 SRAM also supported**
- **Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface**
  - **— Five PCI Bus Masters (including PIIX4)**
  - **— 10 DWord PCI-to-DRAM Read Prefetch Buffer**
  - **— 18 DWord PCI-DRAM Post Buffer**
  - **— Multi-Transaction Timer to Support Multiple Short PCI Transactions**
- **Power Management Features**
  - **— PCI CLKRUN# Support**
  - **— Dynamic Stop Clock Support**
  - **— Suspend to RAM (STR)**
  - **— Suspend to Disk (STD)**
  - **— Power On Suspend (POS)**
  - **— Internal Clock Control**
  - **— SDRAM and EDO Self Refresh During Suspend**
  - **— ACPI Support**
  - **— Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM)**
  - **— SMM Writeback Cacheable in E_SMRAM Mode up to 1 MB**
  - **— 3.3/5V DRAM, 3.3/5V PCI, 3.3/5V Tag and 3.3/2.5 SRAM Support**
- **Test Features**
  - **— NAND Tree Support for all Pins**
- **Supports the Universal Serial Bus (USB)**
- **324-Pin MBGA 430TX PCIset Xcelerated Controller (MTXC) with integrated Data Paths**

The Intel 430TX PCIset (430TX) consists of the 82439TX System Controller (MTXC) and the 82371AB PCI ISA IDE Xcelerator (PIIX4). The 430TX supports both mobile and desktop architectures. The 430TX forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The MTXC integrates the cache and main memory DRAM control functions and provides bus control to transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a writeback cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with pipelined burst SRAMs or DRAM cache SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the MTXC DRAM controller, six rows are supported for up to 256 Mbytes of main memory. The MTXC is highly integrated by including the Data Path into the same BGA chip. Using the snoop ahead feature, the MTXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the MTXC integrates posted write and read prefetch buffers. The 430TX integrates many Power Management features that enable the system to save power when the system resources become idle.

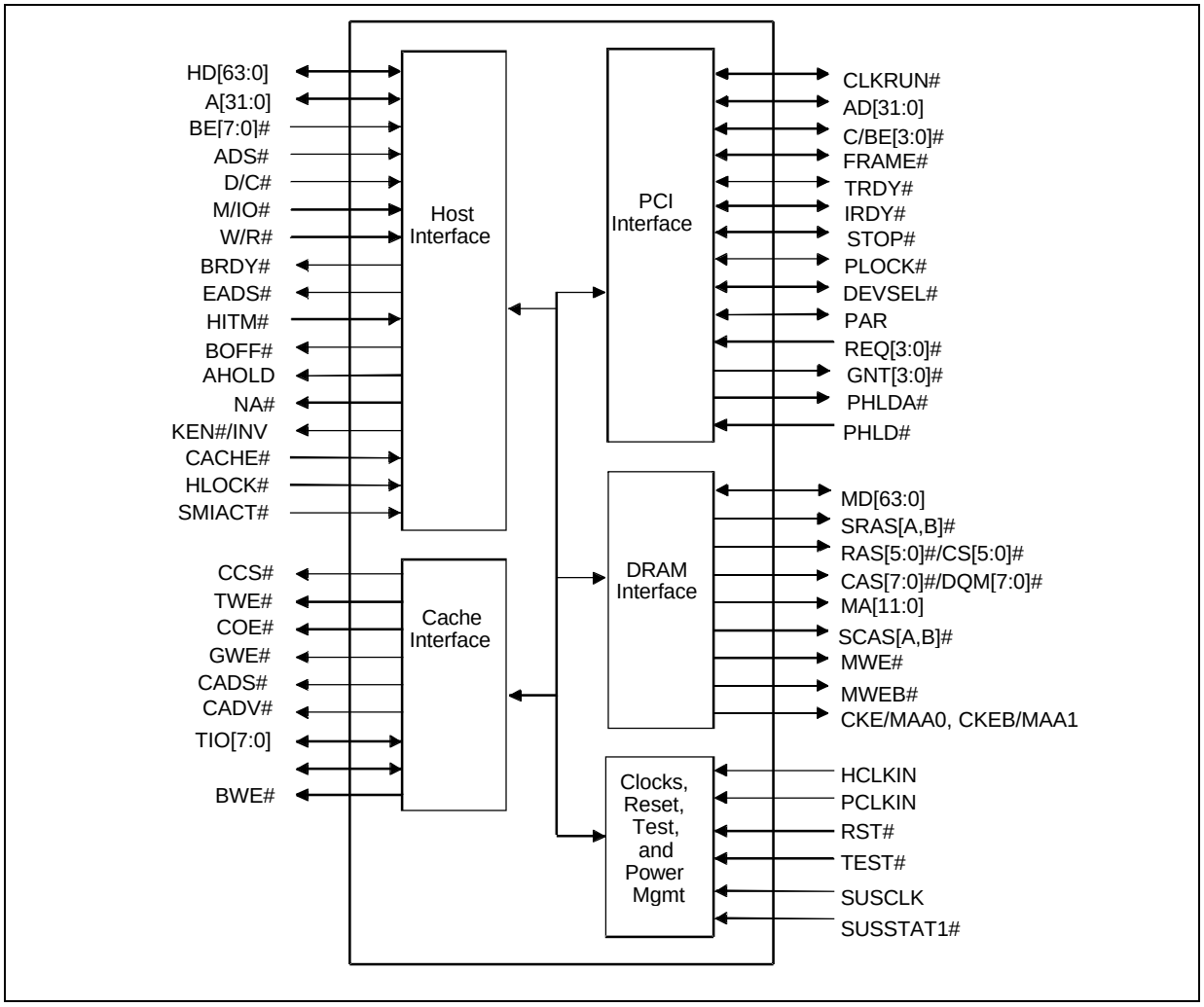


Figure 1-2. MTXC Simplified Block Diagram

1.1.2 82371AB PIIX4 Features

- **Supported Kits for both Pentium and Pentium Pro Microprocessors**
  - **82430TX ISA Kit**
  - **82440LX ISA/DP Kit**
- **Multifunction PCI to ISA Bridge**
  - **Supports PCI at 30 MHz and 33 MHz**
  - **Supports PCI Rev 2.1 specification**
  - **Supports Full ISA or Extended I/O (EIO) Bus**
  - **Supports full Positive Decode or Subtractive Decode of PCI**
  - **Supports ISA and EIO at 1/4 of PCI frequency**
- **Supports both Mobile and Desktop Deep Green Environments**
  - **3.3V Operation with 5V tolerant buffers**
  - **Ultra-low power for mobile environments supports**
  - **Power-On Suspend, Suspend to RAM, Suspend to Disk, and Soft-OFF System States**
  - **All registers readable and restorable for proper resume from 0V suspend**
- **Power Management Logic**
  - **Global and Local Device Management**
  - **Suspend and Resume Logic**
  - **Supports Thermal Alarm**
  - **Support for external microcontroller**
  - **Full support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power Management**
- **Integrated IDE Controller**
  - **Independent Timing of up to 4 drives**
  - **PIO Mode 4 and Bus Master IDE transfers up to 14 Mbytes/sec**
  - **Supports "Ultra DMA33" Synchronous DMA mode transfers up to 33 Mbytes/sec**
  - **Integrated 16 x 32-bit buffer for IDE PCI Burst transfers**
  - **Supports glue-less 'Swap-Bay" option with full electrical isolation**
- **Enhanced DMA Controller**
  - **Two 82C37 DMA controllers**
  - **Supports PCI DMA with three PC/PCI channels and Distributed DMA protocols (simultaneously)**
  - **Fast Type-F DMA for reduced PCI bus usage**
- **Interrupt Controller based on two 82C59**
  - **15 interrupt support**
  - **Independently programmable for Edge/Level sensitivity**
  - **Supports Optional I/O APIC**
  - **Serial Interrupt input**
- **Timers based on 82C54**
  - **System Timer, Refresh Request, Speaker Tone Output**
- **USB**
  - **Two USB 1.0 ports for serial transfers at 12 or 1.5 Mbit/sec**
  - **Supports legacy keyboard and mouse software with USB-based keyboard and mouse**
  - **Supports UHCI Design Guide**
- **SMBus**
  - **Host interface allows CPU to communicate via SMBus**
  - **Slave interface allows external SMBus master to control resume events**
- **Real-Time Clock**
  - **256-byte Battery-Back CMOS SRAM**
  - **Includes Date Alarm**
  - **Two 8-byte Lockout Ranges**
- **Microsoft Win95* Compliant**
- **324 MBGA Package**

The PCI ISA IDE Xcelerator (PIIX4) is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. As a PCI-to-ISA bridge, PIIX4 integrates many common I/O functions found in ISA-based PC systems—two 82C37 DMA Controllers, two 82C59 Interrupt Controllers, an 82C54 Timer/Counter, and a Real Time Clock. In addition to Compatible transfers, each DMA channel supports Type F transfers. PIIX4 also contains full support for both PC/PCI and Distributed DMA protocols implementing PCI based DMA. The Interrupt Controller has Edge or Level sensitive programmable inputs and fully supports the use of an external I/O Advanced Programmable Interrupt Controller (APIC) and Serial Interrupts. Chip select decoding is provided for BIOS, Real Time Clock, Keyboard Controller, second external microcontroller, as well as two Programmable Chip Selects. PIIX4 provides full Plug and Play compatibility. PIIX4 can be configured as a Subtractive Decode bridge or as a Positive Decode bridge. This allows the use of a subtractive decode PCI-to-PCI bridge such as the 380FBPCIset which implements a PCI/ISA docking station environment.

PIIX4 supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. Up to four IDE devices can be supported in Bus Master mode. PIIX4 contains support for “Ultra DMA/33” synchronous DMA compatible devices.

PIIX4 contains a Universal Serial Bus (USB) Host Controller that is Universal Host Controller Interface (UHCI) compatible. The Host Controller’s root hub has two programmable USB ports.

PIIX4 supports Enhanced Power Management, including full Clock Control, Device Management for up to 14 devices, and Suspend and Resume logic with Power On Suspend, Suspend to RAM or Suspend to Disk. It fully supports Operating System Directed Power Management via the Advanced Configuration and Power Interface (ACPI) specification. PIIX4 integrates both a System Management Bus (SMBus) Host and Slave interface for serial communication with other devices.

`

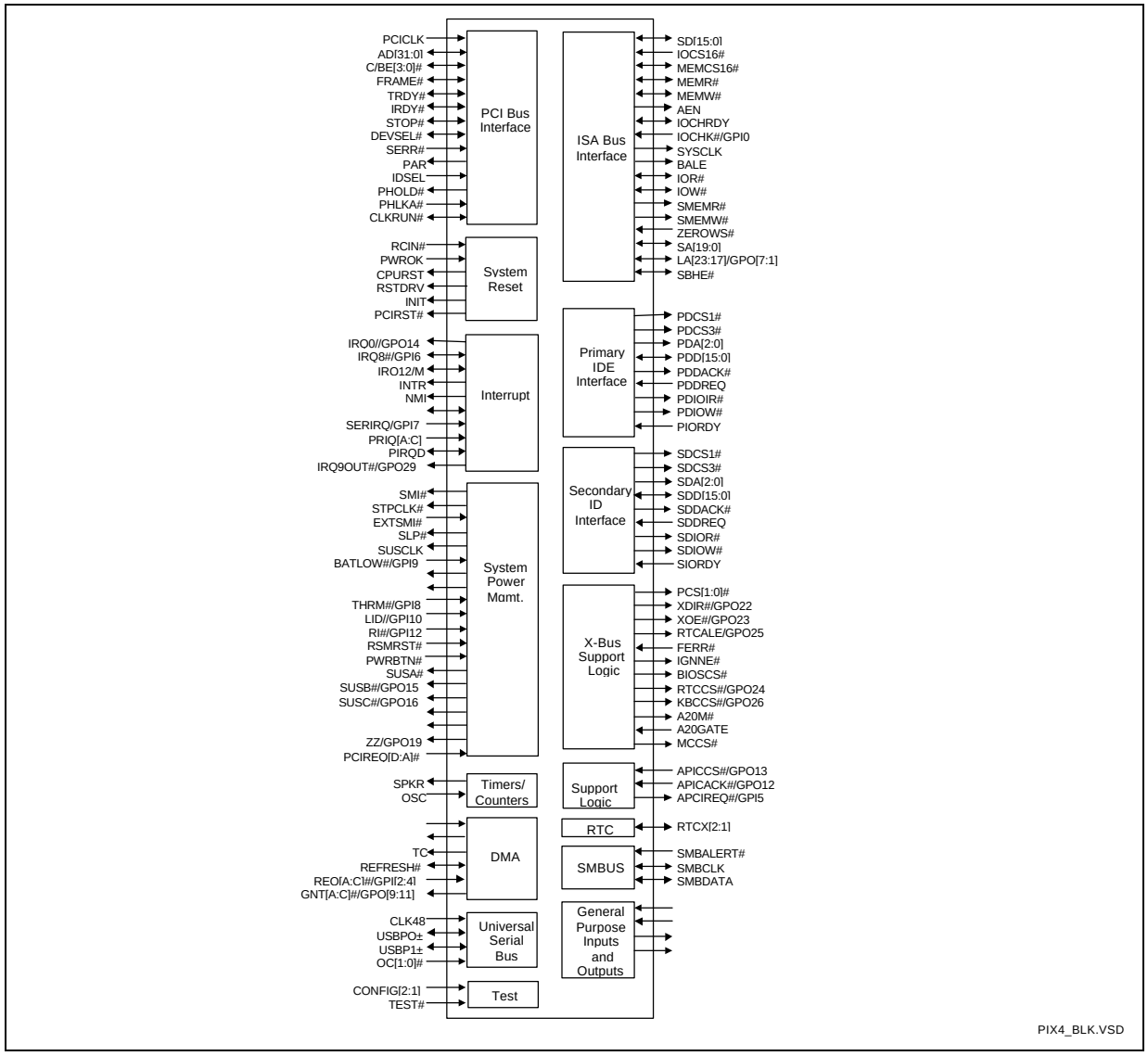


Figure 1-3. PIIX4 Simplified Block Diagram

2

Flexible Motherboard Design Layout Review Checklist

CHAPTER 2
FLEXIBLE MOTHERBOARD DESIGN LAYOUT REVIEW CHECKLIST

2. Flexible Motherboard Design Layout Review Checklist

The following checklist is a guide when designing or reviewing a board design that uses the Intel 430TX PCIset (430TX).

2.1 MTXC Design Checklist

2.1.1 Clocks

- Refer to Section 3 for clock layout and routing recommendations.
- The CPU and MTXC clock should be on the same net. Only two PBSRAMs per clock net. Four separate clocks are connected to a double sided SDRAM DIMM.
- Two separate clocks are connected to a COAST module when supporting 512K dual bank configuration.
- CPU clocks—The CLK input on the P54 family is 5V tolerant. The CLK input on the P55C family is **not** 5V tolerant.
- The clock synthesizer used should be compliant to the "CKDM66-M Clock Synthesizer Specification."
- The latest CKDM66-M clock synthesizer specification redefines the functionality of pin 47. Pin 47 used to be a clock output (14.318 MHz), but the new spec requires that pin 47 be used for strapping of the voltage level. For desktop designs, pin 47 should be left as a No Connect, as a weak pull up is integrated in the clock synthesizer. The extra clock output will be provided by adding another load to the clock output from either pin 1 or pin 2. A series termination of 33 ohm is recommended when adding a clock trunk to pin 1 or pin 2. Please contact your clock synthesizer vendor for more details.

2.1.2 MTXC Power

- To avoid any leakage issues, the designer must take care that pull-up resistors on any signal are tied to the power plane in which that signal resides. Likewise, any external logic or buffer to which a signal is connected should be powered up only while that signal's power plane is powered up. Generally, no signal should see a voltage potential higher than that of the plane in which it resides. The only exceptions are the 5V tolerant signals, which may see 5V potentials during active states if the V_{REF} pin has been tied to a 5V supply.
- V_{CC}(CORE) must be tied to 3.3V.
- V_{CC}(CPU)—For all desktop designs, V_{CC}(CPU) must be tied to 3.3V.
- V_{CC}(SUS) must be tied to a 3.3V supply that is active during Suspend to RAM. If Suspend to RAM state is not used then V_{CC}(SUS) must be tied directly to 3.3V.
- All three V_{CC}s (i.e. V_{CC}(CORE), V_{CC}(CPU), and V_{CC}(SUS)) can be tied to the same 3.3V plane.

- If implementing the MTXC V_{CC}(CPU) and CPU CPUVIO voltages through independent power planes, it should be verified that the CPU will not drive any signals to the MTXC above V_{IH}=V_{CC}(CPU) + 0.3.
- In a system that implements V_{CC}(CORE) and V_{CC}(CPU) as independent power planes, the V_{CC}(CPU) pins must power up after or simultaneous to V_{CC}(CORE), and must power down before or simultaneous to V_{CC}(CORE). At any time, V_{CC}(CORE) should not be more than 1.2V below the V_{CC}(CPU) plane. V_{CC}(SUS) can power up and power down independent of all other power planes.
- $V_{CC}5_{REF}$ MTXC Power Up Requirements—Refer to the 82439TX System Controller datasheet. $V_{CC}5_{REF}$ must be tied to 5V in a 5V tolerant system. This signal must be powered up before or simultaneous to V_{CC}(CORE), and it must be powered down after or simultaneous to V_{CC}(CORE). $V_{CC}5_{REF}$ can be tied directly to V_{CC}(CORE) in a non-5V tolerant system. The $V_{CC}5_{REF}$ circuitry can be shared between MTXC and PIIX4. If the circuitry is placed close to the MTXC, then please ensure that an extra 1µf capacitor is placed on the V_{REF} pin of the PIIX4.
- Tie V_{SS} to ground.

Table 2-1. MTXC Power Pin Summary

POWER PINS	BALL#
V_{CC}(CORE)	F05, L16, E12, F14, F15, P15, R15, T13
V_{CC}(CPU)	F06, G06, R06, R07
$V_{CC}5_{REF}$	E14
V_{CC}(SUS)	P16, R16, N16
V_{SS}	E15, J09, J10, J11, J12, K09, K10, K11, K12, L09, L10, L11, L12, M09, M10, M11, M12, T06, T16

2.1.3 Host Interface

- A27 strapping option—This MTXC signal has a weak pull-down and should be pulled up (with an external pull-up) for a host bus frequency of 60 MHz, and left as a no connect for a host bus frequency of 66 MHz. The inverted state of A27 at reset rising determines the DRAM refresh rate and host bus frequency for the TX. The state is sampled and stored in bit 7 of DRTH—DRAM ROW TYPE REGISTER HIGH. BIOS can use this bit to determine if the system host bus frequency is 60 MHz or 66 MHz.
- A26 strapping option—This strap should be tied to V_{SS} (weak pull-down) for a 2.5V CPU interface, and should be tied to 3.3V V_{CC}(CORE) for a 3.3V CPU I/O interface. For all desktop designs, A26 should be tied to 3.3V through a weak pull up (2Rohm).
- Pull-ups to 3.3V (CPU I/O voltage)—A20M#, SMI#, STPCLK#, INTR, NMI, and IGNNE# (4.7 kohm). These are open collector outputs from the PIIX4 component.
- No external logic is required between INIT and Keyboard Reset. This logic has been integrated in PIIX4. Keyboard Reset is tied into RCIN# input of PIIX4. Refer to reference schematics for implementation details.
- Internal CPU connections for BF0 and BF1 on the P54 are different from the way BF0 and BF1 are connected internally on the P55C. Please see the table below.

Table 2-2. Bus Frequency Pull-ups

	BF0	BF1
P54C	Internal pull-up (default is 1)	Internal pull-up (default is 1)
P55C	Internal pull-down (default is 0)	Internal pull-up (default is 1)

- Refer to the “P55C/FMB Design Review Checklist,” “Socket 7 Design Review Checklist,” and “Socket 7 Specification” for additional information on CPU related requirements including CPU decoupling requirements.
- V_{CC}2DET (P55C)—This signal can be used as a safeguard to prevent plugging a P54C into a socket set up for P55C support (2.8 Vcore). The P55C will always drive V_{CC}2DET low. This pin can be used in a flexible motherboard implementation to correctly set the voltage regulator to drive the correct V_{CC} to the CPU.
- ADSC# should be used to drive the cache subsystem and ADS# should be used to drive the chip set. These signals are functionally identical to each other and two copies are provided by the processor for loading reasons.
- INV and KEN# should be tied together at the CPU. The 430TX muxes these signals. KEN# is used during CPU read cycles and INV is used during L1 snoop cycles.
- Pull-ups (3V)—FLUSH#, FRCMC#, WB/WT#, AP, & PEN# (8k2ohm).
- The HOLD and EWBE# pins on the processor are tied to ground.
- No Connects—R/S#, TCK, TDI, TMS, TRST#, APCHK#, BP[3:0], HIT#, HLDA, IERR#, PCHK#, PRDY, PWT, PCD, SCYC, TDO, PICCLK, PICDO, PICD1, PHITM#, PHIT#, PBGNT#, CPUTYP, PBREQ#, U/O# (or D/P#), UPVRM (or KEY), BUSCHK#, BRDYC#, BREQ#. Please note that BUSCHK# and BRDYC# have pull up resistors shown on the schematics. These two signals can be left as no connects also.
- Host Bus Parity—The 430TX does not support host bus parity so these signals are not used. Data parity pins DP[7:0] on the CPU are pulled up through weak pull up resistors on the motherboard.
- Unlike the Pentium processor, these inputs on the P55C are not 5V tolerant: CLK, PICCLK, AHOLD, BRDYC#, EADS#, KEN, WB/WT#, INV, NA#, EWBE#, BOFF#.
- Split Core V_{CC}2 for P55C—The P55C requires two supply voltages; 2.8V±5% on its Vcore pins. Its external I/O pins operate at STDE (3.125-3.6V) levels. If a dual regulator is used to support the P54CS and P55C, then the core current requirement is 5.7A and the I/O requirements is 1A. These regulators supply voltages exclusively for the CPU plane. The I/O regulator is set up for 2.8/3.5V and the I/O regulator is set up for 3.3/3.5V. The VRE CPU’s operate at the voltage level of 3.5V for both core and I/O. It is not an absolute requirement to set these regulators to 3.5V. The main goal is to keep the voltage levels within the specified voltage range of the CPU.
- The PCIRST# signal from PIIX4 is used to reset the MTXC RST# signal.
- Internal pull-downs—HD[63:0] on the MTXC have internal pull-downs. External pull-ups/ pull-downs are not required.
- CPURST and INIT are timing critical, open collector outputs from the PIIX4 and need strong pull-ups (1 kohm).

2.1.4 L2 Cache

- A31:A30 Strapping Option—Secondary Cache Size. 1 = pull-up (4.7 kohm), 0 = pull-down (4.7 kohm)

  1 1 Cache NOT POPULATED
  1 0 256 Kbytes
  0 1 512 Kbytes
  0 0 Reserved

  Note: These values are inverted from the value stored in the configuration register.

- A29:A28 Strapping Option—L2 SRAM Type. 1 = pull-up (4k7ohm), 0 = pull-down (4.7kohm)

  1 1 PBSRAM
  1 0 Reserved
  0 1 Reserved
  0 0 2 Banks of PBSRAM

  Note: These values are inverted from the value stored in the configuration register. If the 512K cache is implemented using four 32Kx32 PBSRAMs, then select the “2 Banks of PBSRAM” option from the above table. If the 512K cache is implemented using two 64Kx32 PBSRAMs, then select the “PBSRAM” option from the above table.
- GWE# and BWE#—The MTXC only supports PBSRAM devices that use GWE# (Global Write Enable) and BWE#. GWE# and BWE# must be connected from the MTXC to each of the PBSRAMs.
- Proper Speed Parts—Intel recommends the use of PBSRAMs with tco of 8.5 ns and cycle times of 15 ns, and 15 ns Tag for operation at 66 MHz host bus frequencies.
- TIO[7:0] on the MTXC have internal pull-downs (20kohm). Externals are not required.
- 512K PBSRAM Support—A18 determines which bank is accessed in a dual bank 512K configuration. This address is connected to CE2 on the PBSRAMs of the lower bank and CE3# of the upper bank PBSRAMs. A18 is required when the 512K cache is implemented using four 32Kx32 PBSRAMs. If the 512K is implemented using two 64Kx32 PBSRAMs then A18 should not be used for depth expansion. In other words, tie the CE2 and CE3# on both the PBSRAMs to an active state. Please note that A18 is still required for the Tag RAM addressing as shown in the schematics. It is also required for addressing the PBSRAMs.
- COAST Modules—If a COAST module is used, all recommendations and specifications contained in the COAST specification (Rev 3.1 and 3.1a) must be followed.
- DRAM cache logic—The 430TX provides an option for DRAM cache implementation. Additional logic is required to support this option. Refer to the cache pages in the reference schematics for information. (1) PCIRST# should be used for the reset to the DRAM CACHE. (2) KRQAK pin needs a weak pull up resistor for strapping DRAM cache (~10 kohm). If DRAM cache is not used, then no external pull-up or pull-downs are needed. (3) Only one of the DRAM cache devices should be strapped as Master.

2.1.5 DRAM

- For desktop designs we do not recommend the use of CKE and CKEB pins from the MTXC. These pins should be pulled high to 3.3V at the DIMM connector on the motherboard (pins 63 and 128 of DIMM).
- CKEB is not in the Suspend Well. This signal cannot be used on systems that implement Suspend to RAM (STR). For desktop designs we do not recommend the use of STR state.
- The MTXC A-1 provides a second copy of MA lines by muxing the CKE(MAA0) and CKEB(MAA1) signals. This means that CKE and CKEB function cannot be used if the second copy of MA lines are implemented. CKE functionality is not required in a desktop system.
- The first pair of MA0 and MA1 lines should be tied to the first DIMM. The second pair of MAA0 and MAA1 lines should be tied to the second DIMM. The CKE0 and CKE1 pins on both the DIMMS should be tied to 3.3V

  Note: It is recommended that this feature only be implemented on those boards that are intended to be used with the A-1 MTXC (or beyond) stepping (i.e. boards that are populated with the A-0 MTXC, should not implement this feature).
- MA[11:0] and WE# buffering—External buffering on the MA lines and WE# lines is not required, and must not be implemented in a system with four rows of memory. These lines must be connected directly to the DRAM. The MTXC provides integrated programmable buffers on the MA lines and two copies of MWE# (MWE# and MWEB#). The MTXC also provides two copies of

SRAS# (SRASA# and SRASB#) and SCAS# (SCASA# and SCASB#). Two copies of these signals were provided for loading reasons and should be evenly distributed throughout the DRAM subsystem. Please refer to the last paragraph of this section for series termination on memory control and address signals.

- The desktop reference design shows implementation using 4 rows of memory (2 DIMMs). If a design is implemented using more than 4 rows of memory, then please follow the guidelines listed in the 430TX Data Sheet. External buffering of signals is required for certain cases.
- Internal pull-downs—MD[63:0] on the MTXC have internal pull-downs. External pull-ups/ pull-downs are not required.
- SDRAM—Refer to the latest Unbuffered Standard SDRAM DIMM specification for the latest DIMM and connectorpinout.
- The MTXC supports unbuffered DIMM modules only. SDRAM DIMMs require four separate HCLKs.
- Most SDRAM will be 3V only (i.e. SDRAM I/O pins will not be 5V tolerant). When mixing and matching SDRAM with EDO/FPM, the EDO/FPM should also be 3V (i.e. receive and drive 3V levels).
- 64-Mbit SDRAM Support—This feature is supported on A-1 MTXC. A-0 MTXC does not support 64-Mbit SDRAM.

  When 64MTEN = 0, (TIEN is Address offset 54, bit 1)

  RAS5#/CS5#/MA13 drives RAS5#/CS5#

  RAS4#/CS4#/BA1 drives RAS4#/CS4#

  MA11/BA0 drives MA11

  When 64MTEN = 1,

  RAS5#/CS5#/MA13 drives MA13

  RAS4#/CS4#/BA1 drives BA1

  MA11/BA0 drives MA11

  DIMM wiring guideline

  - Connect MA11/BA0 to pin 122 of DIMM (BA0 for SDRAM, A11 for EDO/FPM)
  - Connect RAS4#/CS4#/BA1 to pins 39 and 126 of DIMM (BA1, A12 for SDRAM, A12 for EDO/FPM)
  - Connect RAS5#/CS5#/MA13 to pin 123 of DIMM (A11 for SDRAM, A13 for EDO/FPM)
- The A-1 MTXC will support five rows of 64-Mbit SDRAM.

  In a five row SDRAM system that supports 64-Mbit SDRAM devices, KRQAK is muxed to provide the 5th CS# (or CS4#) function. This means that a system that supports DRAM cache cannot support five rows of 64-Mbit SDRAM. However, four rows of 64-Mbit SDRAM with DRAM cache is supported. ***Note: It is recommended that the 5th row feature only be implemented on those boards that are intended to be used with the A-1 MTXC (or beyond) stepping (i.e. boards that are populated with the A-0 MTXC, should not implement this feature).***

  When 64MTEN = 1 and DRAM Cache is not in the system (Bit 5 in Reg. offset 53h = 0)—64-Mbit SDRAM support is enabled for Five rows. If DRAM cache is in the system, then a pull-up resistor is present on the KRQAK pin. If DRAM cache is not in the system, then no resistor is present on the KRQAK line. Bit 5 in register offset 53h reflects the level of the KRQAK signal at power-up.

  RAS5#/CS5#/MA13 drives MA13

  RAS4#/CS4#/BA1 drives BA1

  KRQAK/FRCL# drives FRCL# (or CS4#)
- Address input A13 to the DIMMs should not be left floating. The reference schematics use a 100 ohm pull down to ground on A13.

- Generally, only SDRAM and EDO come on DIMMs, however the DIMM spec also specifies FPM. To support EDO/FPM on the same DIMM, OE0# (pin 31) and OE2# (pin 44) on the DIMM connector must be connected to ground on the motherboard, and WE2# (pin 48) must be connected to one of the MTXC's memory write enable signals (MWE# or MWEB#).
- Parity—The 430TX does not support parity and requires that non-parity SIMMs and DIMMs be used.
- Since the DIMMs have only 3 address bits for the SMBus (SA2, SA1 and SA0), the BIOS should handle all address aliasing issues. The twoDIMMs should be strapped to unique addresses.
- SMBCLK and SMBDATA should be pulled up to the 3.3V core plane through 8.2 kohm resistors. It follows that the SMBus cannot be used as a resume event during STD/Soft-off since it is not tied to a standby voltage. These should not be pulled up to 3 VSB when used with devices being powered from the core voltage (e.g. SDRAM) due to excessive leakage when the core voltage is off. If they are pulled up to 3VSB then all the devices on the SMBus should be tied to 3 VSB. (This checklist item is not reflected in reference board schematics Rev. 2.1 ogerber files.)
- To insure that DRAM interface signal integrity is maintained for lightly loaded desktop systems, series termination and/or diodes (ground and V_{CC} diodes) are recommended on the following signals: CAS#/DQMx, MWEx, SCASx, SRASx, CKEx, and all MA lines (Note: RAS4# and RAS5# are also used as MA lines, depending on the configuration, and should be terminated when used as MA lines). This will insure that the overshoot, undershoot, and most importantly, ring-back does not cause any problems.
- If series termination is used, use 10 ohm. This value provides the best signal integrity and flight time results. Place as close to the driver as possible. If diodes are used, the diodes should have a forward current of at least 200 mA at 1V. A MMBD1203 diode or equivalent meets this requirement. The diodes should be placed at the end of the trace. Diodes improve signal integrity without increasing the flight time. A 10 ohm series resistor will increase the flight time by approximately 300 ps. Both provide similar signal integrity results. The reference schematics show this implementation using 10 ohm series resistors.

2.2 PIIX4 Design Checklist

2.2.1 Power and Ground Pins

- To avoid any leakage issues, the designer must take care that pull-up resistors on any signal are tied to the power plane in which that signal resides. Likewise, any external logic or buffer to which a signal is connected should be powered up only while that signal's power plane is powered up. Generally, no signal should see a voltage potential higher than that of the plane in which it resides. The only exceptions are the 5V tolerant signals, which may see 5V potentials during active states if the V_{REF} pin has been tied to a 5V supply.
- V_{CC}, V_{CC}(RTC), and V_{CC}(USB) must be tied to 3.3V.
- Standby voltage from the power supply is used to power the resume well V_{CC}(SUS), V_{CC}(RTC) and the RSMRST# signal. If the standby voltage from power supply is at 5V, it must be divided down to 3.3V. In the 430TX reference board design, a Zener diode voltage regulator circuitry is used to provide the 3V standby voltage. This circuitry consists of a series resistor and a Zener diode with two capacitors provided to filter out noise. The Zener diode/series resistor should be validated to make sure the standby voltage is clamped to 3.3V. The series resistor value can be changed to correct the standby voltage and current requirements. The reference design uses a Zener diode that requires approximately 20 mA to sustain 3.3V, however a different Zener diode, requiring less current, can be used. Also note that the standby voltage connection to V_{CC}(RTC) helps in preserving the on-board battery. Please refer to the schematics for implementation details.
- V_{REF} must be tied to 5V in a 5V tolerant system. This signal must be powered up before or simultaneous to V_{CC}, and it must be powered down after or simultaneous to V_{CC}. The V_{REF}

circuitry can be shared between the MTXC and PIIX4. If the circuitry is placed close to the PIIX4, then please ensure that an extra 1 µf capacitor is placed on the $V_{CC}5_{REF}$ pin of the MTXC.

- V_{REF} can be tied to 3.3V V_{CC} in a non-5V tolerant system.
- Tie V_{SS} and V_{SS}(USB) to ground.

Table 2-3. PIIX4 Power Pin Summary

POWER PINS	BALL#
V_{CC}	E9, E11, E12, E16, F5, F6, F14, F15, G6, P15, R6, R7, R15, T6
V_{CC}(RTC)	L16
V_{CC}(SUS)	N16, R16
V_{CC}(USB)	K5
V_{SS}(USB)	J5
V_{SS}	D10, E7, E13, J9–J12, K9–K12, L9–L12, M9–M12
No Connects	J4, M5, M16, N3, N18, R5

- The reference schematics show an implementation with a power supply capable of providing a standby voltage. It is not a requirement to design a system that relies on power supplies capable of providing standby voltages. In such cases, the pull-ups which are to 3.3 VSB can be replaced with pull-ups to 3.3V.

2.2.2 PCI Bus Signals

- 5V PCI environment—2.7 kohm pull-up resistors to 5V on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# and PAR on PCI connectors. Resistors (10kohm) on REQ[3:0]#.
- 3.3V PCI environment—10 kohm pull-up resistors to 3.3V on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, and REQ64# and ACK64# and PAR on PCI connectors. Resistors (10kohm) on REQ[3:0]#.
- Pull-ups to 3V—10kohm pull-ups on GNT[3:0]#
- PCI slots—The 430TX supports up to four PCI masters with REQ[3:0]# and GNT[3:0]#. Also, it is recommended, per the PCI Spec. 2.1, to place series resistors (~100 ohm) on each of the PCI connector IDSEL lines.
- PHLD# and PHLDA#—10kohm pull-ups to 3V.
- The PCI Boundary Scan signals on the PCI connector are TRST#, TMS, TDI, TDO, and TCK. Pull-up and pull-down resistor values for these signals should follow the recommendations listed in the PCI Specification, Rev 2.1. If boundary scan is not supported on the motherboard, then TMS (connector pin A3) and TDI (connector pin A4) should be independently bused and pulled up, each with ~5 kohm resistors. TRST# (connector pin A1) and TCK (connector pin B2) should be independently bused and pulled down, each with ~5 kohm resistors. TDO (connector pin B4) should be left open. This checklist item is not reflected in reference board schematics Rev. 2.1.

2.2.3 ISA Signals

- 10 kohm pull-up on SD[15:0].
- 1 kohm pull-up on IOCHRDY and REFRESH#.
- 8.2 kohm pull-up on IRQx, MEMR#, MEMW#, IOR#, IOW#, LA [23:17], SA [19:0], SMEMR#, SMEMW#, SBHE#, BALE. The PIIX4 is not 5V tolerant on IRQ8 as V_{CC}(SUS) is tied to the 3V levels. Please refer to the data sheet for a list of signals that are not 5V tolerant. If an external RTC is used, then please ensure that IRQ8 is not driven to the 5V levels.

- If Power-On-Suspend (POS) is to be implemented, the pull-ups on ISA SA[19:0] signals should be removed due to possible reverse current leakage on the ISA bus during this state. The ISA specification does not require pull-ups on the SA[19..0] lines. This checklist item is not reflected in the reference board schematics Rev. 2.1.
- 5.6 kohm pull-down on DRQx.
- MASTER#—The PIIX4 doesn't require connection with the MASTER# signal from the ISA bus (same as the PIIX3). Place a pull-up resistor (300 ohm) on MASTER# signal from ISA connectors.
- 1 kohm pull-up on MEMCS16#, IOCS16#, ZEROWS#. This checklist item is not reflected in reference board schematics Rev. 2.1.
- 4.7 kohm pull-up on IOCHK#.
- Some of the ISA signals shown in the schematics will have slightly different pull-up resistor values than recommended in this checklist. This was done to optimize for resistor packs selected for the design.

2.2.4 X-Bus Signals

- XOE# and XDIR# are connected to the ULTRA I/O device.
- If the internal RTC is used, RTCALE and RTCCS# are no connect or become general purpose outputs by programming the General Configuration Register(GENCFG) in Function 0, Offset B0h-B3h.

2.2.5 Power Management Signals

- CLKRUN#—If CLKRUN# is not connected between PIIX4 and MTXC, it should be tied low through a 100 ohm resistor at the MTXC. If CLKRUN# is connected between PIIX4 and MTXC, it should have a weak pull-up resistor on the CLKRUN# signal.
- SUS_STAT1# and SUSCLK are connected between the MTXC and PIIX4. These are required for all designs even if power management features are not utilized.
- SUSC# is connected to the power supply through an inverter to control the remote-off function.
- ZZ is connected to the ZZ pin on the cache when the ZZ feature is used.
- PCIREQ[3:0]# is connected between the PIIX4 and the PCI bus. Bus master requests are considered as power management events.
- PWRBTN#—This signal is connected to front panel on/off power button. The logic on power button circuitry should be powered using the 3V standby voltage.
- RSMRST#—Standby voltage should be provided to RSMRST# input at a 3V level. The RSMST# connection requires a minimum time delay of 1 millisecond from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 millisecond delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure the Schmitt trigger has sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed V_{CC}(RTC). Refer to the reference schematics for implementation details. If standby voltage is not provided by the power supply, tie the PWROK signal on the PIIX4 to the RSMRST# signal.

  Based on the resistor values and input capacitance of the PIIX4 RSMRST# pin, the rise time in the reference board schematics is approximately 170 ns (within the max. 250 ns requirement for the PIIX4). It is important that if any other components are connected to RSMRST#, the resistor divider values may need to be adjusted to meet a faster rise time required by the other parts and increased loading. 3V driving devices, such as an 74LVC14 could also be used as a replacement for the voltage divider.
- THRM# is connected to thermal protection logic if used.

- RI# is connected to the modem if this feature is used. To implement ring indicate as a wake event from STD, the source driving the RI# signal must be powered when the PIIX4 suspend well is powered.

2.2.6 Power Button Implementation

The items below should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1 - POS (CPU context not lost)
S2 - POSCCL (CPU context lost)
S3 - STR
S4 - STD
S5 - Soft-off

- Wake: Pressing the power button wakes the computer from S1-S5.
- Sleep: Pressing the power button signals software/firmware in the following manner:
  - If SCI is enabled, the power button will generate an SCI to the OS.
    - The OS will implement the power button policy to allow orderly shutdowns.
    - Do not override this with additional hardware.
  - If SCI is not enabled:
    - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
    - Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
    - Always install an SMI handler for the power button that operates until ACPI is enabled.
- Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
  - This is only to be used in EMERGENCIES when software is locked-up.
  - This will cause user data to be lost in most cases.
- Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off—**this violates ACPI**
- To be compliant with the latest PC97 Specification, machines must appear off to the user when in the S1–S4 sleeping states. This includes:
  - All lights except a power state light must be off.
  - The system must be inaudible: Silent or stopped fan; drives are off.
- Please contact Microsoft for the latest information concerning PC97 and Microsoft Logo programs.

2.2.7 USB Interface

- Refer to Section 3.6 for the layout recommendations for USB signals.

2.2.8 IDE Interface

- 5.6 kohm pull-down resistors on PDDREQ and SDDREQ.
- 1 kohm pull-up resistors on PIORDY# and SIORDY#.
- 470 ohm pull-down resistor on pin 28 of the IDE connectors(CSEL). The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
- Primary IDE connector uses IRQ14 and the secondary IDE connector uses IRQ15.

- All signals running to the two IDE connectors (except for PIORDY# and SIORDY# which are 47 ohm) have series termination resistors of 33 ohm. These series termination resistors should be placed as close as possible to the ATA connectors.
- Layout—Proper operation of the IDE circuit depends on the total length of the IDE bus. The total signal length from the IDE drivers to the end of the IDE cables should not exceed 18". Therefore, the PIIX4 should be located at close as possible to the ATA connectors to allow the IDE cable to be as long as possible.
- Use ISA reset signal RSTDRV from PIIX4 through a Schmitt trigger for RESET# signals.
- Ground pin 19, 2, 22, 24, 26, 30, 40 on both ATA connectors
- No connect on pin 20, 32, 34 on both ATA connectors.
- Please note that the Primary IDE connector and the Secondary IDE connector have separate sets of DATA lines on the PIIX4. This has changed from PIIX3, where a single set of data line was only provided by the PIIX3.
- There is no internal pull-up or down on PDD7 or SDD7 of the PIIX4. The ATA3 specification requires a 10 Kohm pull-down on DD7 in section 4.3.1. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 Kohm pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in the next revision of this standard.
- Please refer to Section 3.5 for IDE routing recommendations.

2.2.9 System and Test Signals

- 1 kohm pull-up resistor on TEST#.
- In a Pentium processor system, CONFIG[1] should be connected to ground. In a Pentium Pro Processor system, CONFIG[1] should be connected to V_{CC}. CONFIG[2] should be tied to ground in all 430TX based designs.

2.2.10 Clocks

- Refer to Section 3 for clock and general board layout recommendations.

2.3 Flash

- 1-Mbit flash—1 Mbit of flash is generally all that is required to support the 430TX in all configurations. However, it is highly recommended that support for an optional 2M Boot Block Flash be designed in, even if a 1-Mbit device is planned (each size comes in a different package type). By simply laying out 2 pad sets, one for the 1-Mbit device, and another for a 2-Mbit device, the board will allow the use of a 2-Mbit flash if the BIOS becomes larger than 1Mbit.
- For a 2-Mbit flash implementation, there is no need to externally OR BIOSCS# with XOE# to drive the CE# input of the flash device. This logic is integrated in PIIX4.
- Connect V_{PP} to GND for write protection.
- Use 0.01 µf–0.1 µf capacitors for power supply(V_{CC} and V_{PP}) decoupling.
- Connect BYTE# to GND if a x16 device is used.

2.3.1 Miscellaneous

- It is highly recommended that the PWRGOOD signal from the power supply **not** be connected directly to logic on the board without first going through a Schmitt trigger type circuit to square-off and maintain the signal integrity of PWROK.
- If the PWRGOOD signal from the power supply is at 5V level, then it must be divided down to 3V before connecting to the PIIX4. Please ensure that the voltage level on PWROK does not exceed

the V_{CC}(RTC) level. The reference schematics meet this requirement by using a divide by two voltage divider on the 5V signal.

- Based on the resistor values and input capacitance of the PIIX4 PWROK pin, the rise time in the reference board schematics is approximately 170 ns (within the max. 250 ns requirement for the PIIX4). It is important that if any other components are connected to PWROK, the resistor divider values may need to be adjusted to meet a faster rise time required by the other parts and increased loading. 3V driving devices, such as an 74LVC14 could also be used as a replacement for the voltage divider.
- The 32-kHz oscillator is always required by the PIIX4, even if the internal RTC is not used. Also, if the internal RTC is not used then the on board battery is not required. In this case, connect V_{CC}(RTC) of the PIIX4 directly to 3 VSB.
- A20GATE and KBRESET output signals from the SMC ULTRA I/O device need a pull-up to 5V through a 10 kohm resistor.
- All unused GPIx inputs on the PIIX4 should be tied high through pull-up resistors (8.2 kohm–10 kohm) to a power plane. Tying them directly to the power plane is also acceptable. In the 430TX reference board, GPI13–GPI21 are tied to the 3.3V core power plane through 8.2k resistors. GPI1 is tied to 3 VSB through an 8.2 kohm resistor. If GPI1 is left floating, this will violate ACPI compliance by preventing the GPI_STS bit (register base + 0Ch, bit 9) from functioning properly. Please note that GPI1 is tied to the resume well.
- To maintain RTC accuracy, the external capacitor values for the RTC crystal circuit should be chosen to provide the manufacturer's specified load capacitance for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package, which can vary from 0 pF to 8 pF. When choosing the capacitors, the following equation can be used:

  Specified Crystal Load = (Cap1 * Cap2)/(Cap1 + Cap2) + parasitic capacitance

  The reference board uses 22 pF capacitors and a crystal with a specified load of 12.5 pF. This provides an accuracy of approximately 20 ppm (10.5 minutes per year), however, using the above guidelines, the capacitors should be between 16 pF and 18 pF. This increases the accuracy from 20 ppm using the 22 pF capacitors, to between 0–7ppm (3.5 minutes per year, worst case) using 16 pF to 18 pF capacitors. Note that while 20 ppm is still within spec, using these guidelines can improve the RTC accuracy.

3

Board Layout and Routing Guidelines

CHAPTER 3
BOARD LAYOUT AND ROUTING GUIDELINES

3. 430TX Board Layout and Routing Guidelines

This section describes the 430TX layout and routing recommendations to insure a robust design. These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

3.1 Placement

The pins on the MTXC have been assigned in order to simplify routing. The major signal sections of the MTXC (i.e. Host, DRAM and PCI) are shown in Figure 3-1. The component placement on the motherboard should be done with this general flow in mind. This will simplify routing and minimize the number of signals which must cross. The individual signals within the respective groups have also been laid out in order to minimize any signal crossing.

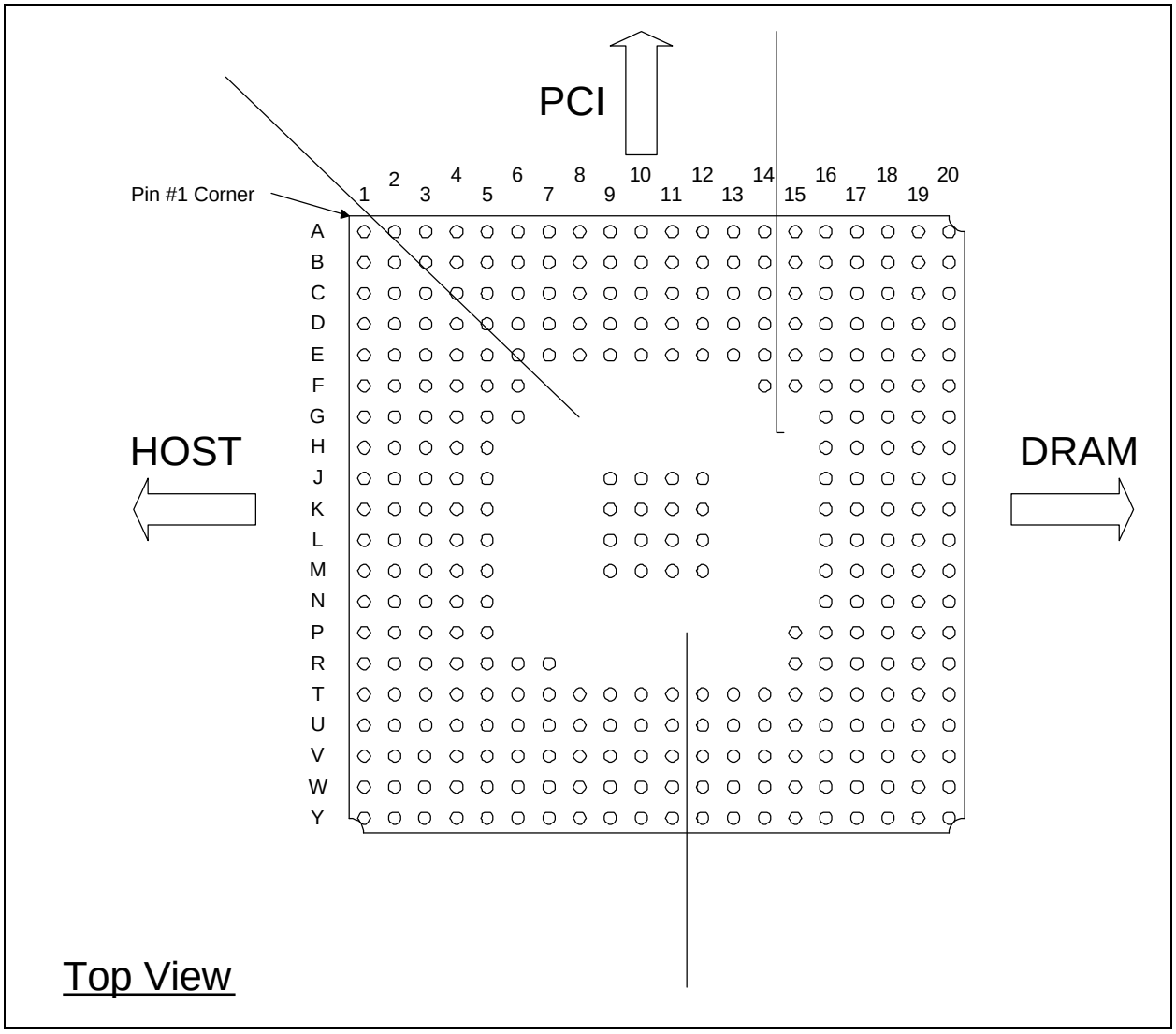


Figure 3-1. 430TX Pinout

Examples of the recommended component placement for Pentium processor 430TX designs are shown below for a 2/3 baby AT form factor and an ATX form factor. An ATX layout will allow more open full length ISA and PCI slots for better CPU cooling, more I/O connectors on the motherboard for I/O peripherals (serial, parallel ports, video....), and a better USB connector implementation that will allow the USB connectors to be soldered directly to the motherboard. The following two examples show a 2/3 baby AT with two DIMMs that support EDO, FPM, or SDRAM memory and an ATX with the same memory configuration.

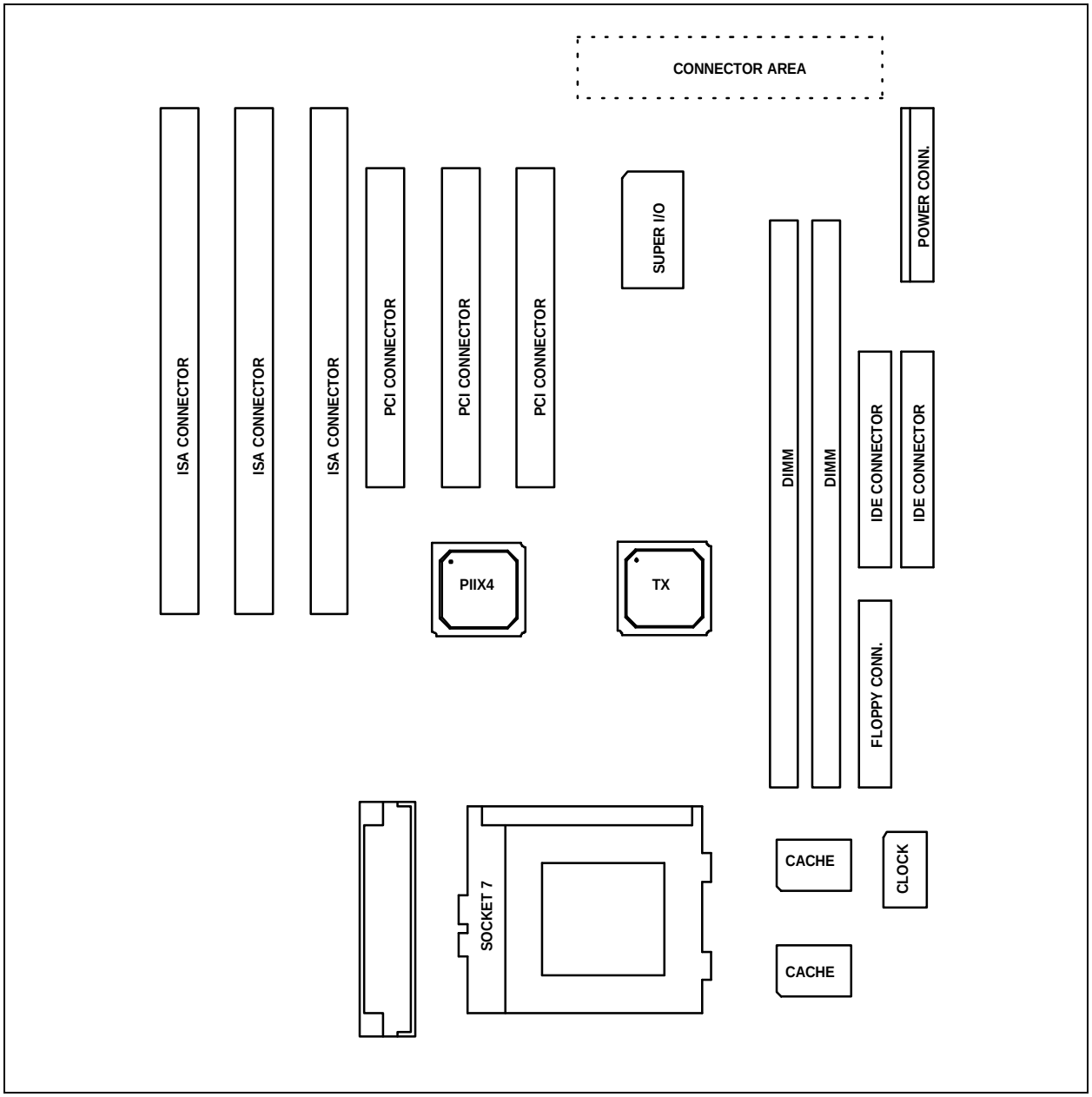


Figure 3-2. Example Placement for 2/3 baby AT and EDO/FPM/SDRAM DRAM 430TX Design

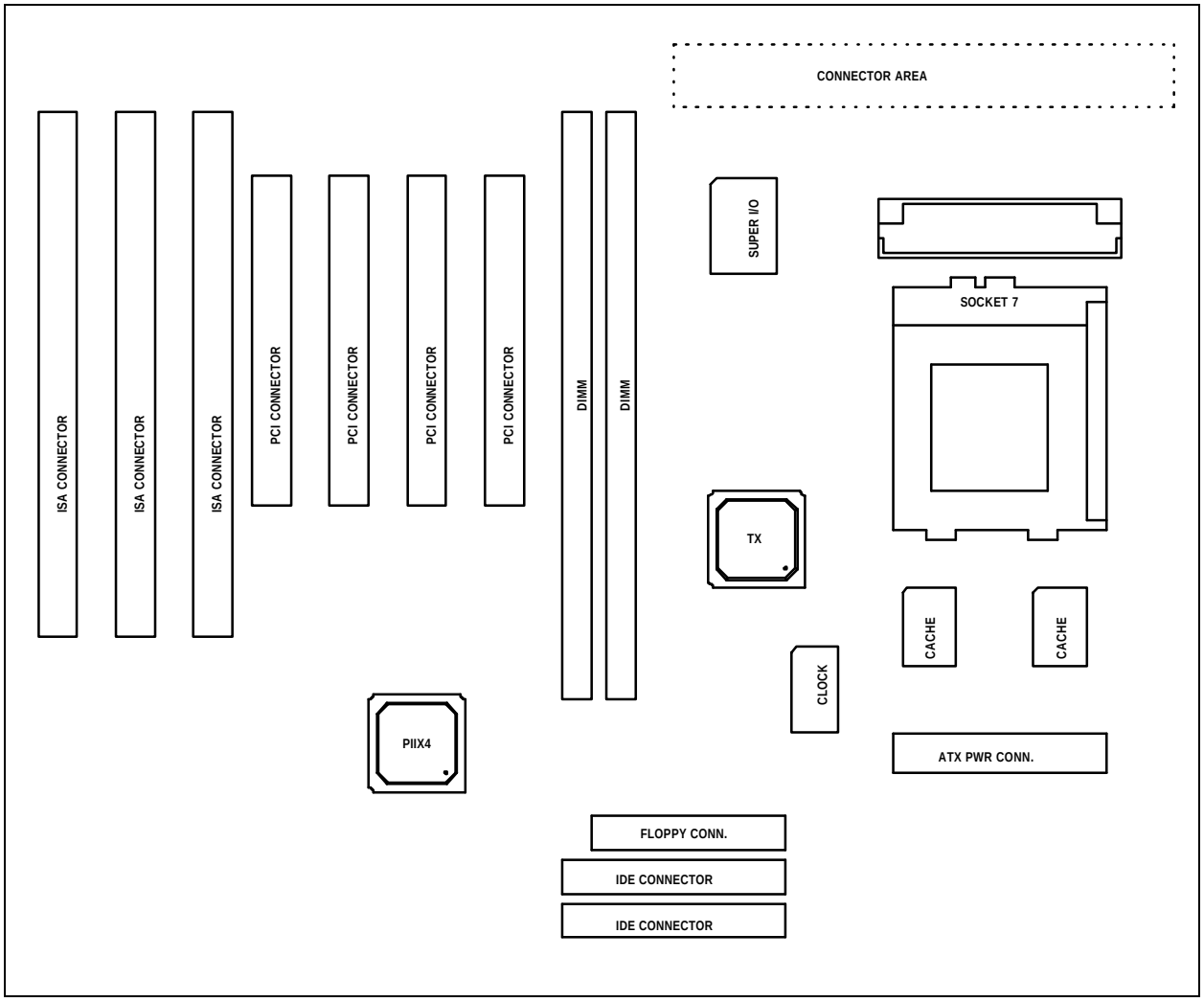


Figure 3-3. Example Placement for an ATX form factor EDO/FPM DRAM, SDRAM 430TX Design

3.2 Board Description

A 430TX motherboard can be designed using a four layer stack-up arrangement. The stack up of the board is shown in Figure 3-4. The impedance of all the signal layers are to be 60 and 90 ohms. The overall board thickness is to be .062 inch.

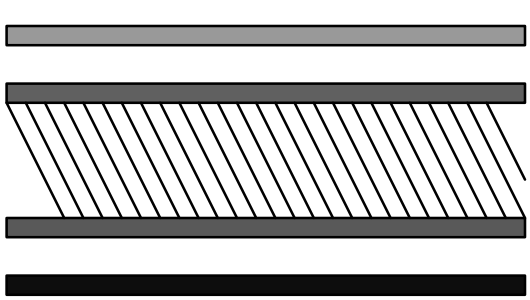


Figure 3-4. Four Layer Board Stack-up

Note that the top and bottom routing layers specify 1/2 oz. cu. However, by the time the board is plated, the traces will end up being about 1 to 1.5 oz. cu. Please check with your fab vendor on the exact value and insure that any signal simulation accounts for this.

As mentioned above, the layout of this board will first be attempted using a four layer stack-up. If for some reason it becomes apparent that more signal layers will be needed to complete the routing of the board, the following six layers stack-up should be used.

If a six layer stack-up is used, routes on the two inner layers should be orthogonal to reduce crosstalk between the layers.

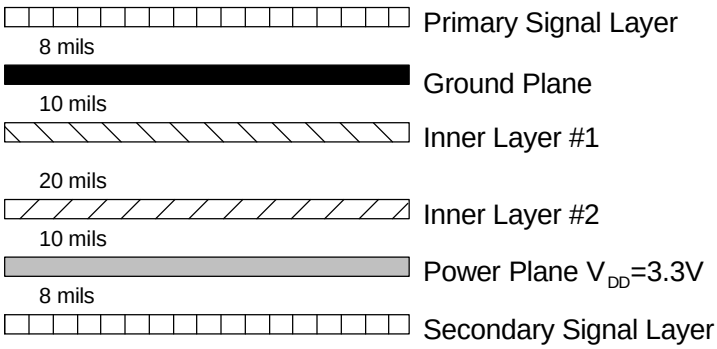


Figure 3-5. Six Layer Board Stack-up

Additional guidelines on board buildup, placement and layout include:

- The board impedance (Z) must be between 60 and 90 ohms (75 ohms ± 20%)
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power plane, then it should be routed on the V_{CC} plane, not the ground plane.
- Group 5V and 3V components near each other. This will allow for fewer isolated V_{CC} islands on the power plane.
- Place vias for decoupling capacitors inside the footprint for the capacitor if possible.
- Use the first (nearest) available via site for decoupling caps if inside footprint is not possible.

3.3 Layout and Routing Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order of which signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed here are followed.

3.3.1 BGA Component Layout Guidelines

3.3.1.1 BGA Pad Size

Since the BGA component contains 5 rows of balls, it is necessary to route two traces between pads in order to route in a four layer board. The figure below shows a routing example for 24 mil and 20 mil ball pads. In order to route two tracks between pads, 5 mil traces and 5 mil spaces are required for a 24 mil pad size. For a 20 mil pad size, 6 mil traces and 6 mil spacing can be used. Either pad size is acceptable, so the choice is primarily determined by the manufacturer's preferred line width and spacing technology. If larger trace widths are desired, another alternative is to route 5/5 or 6/6 within the BGA pads, and then "neck up" to the larger trace widths once you have cleared the BGA component area.

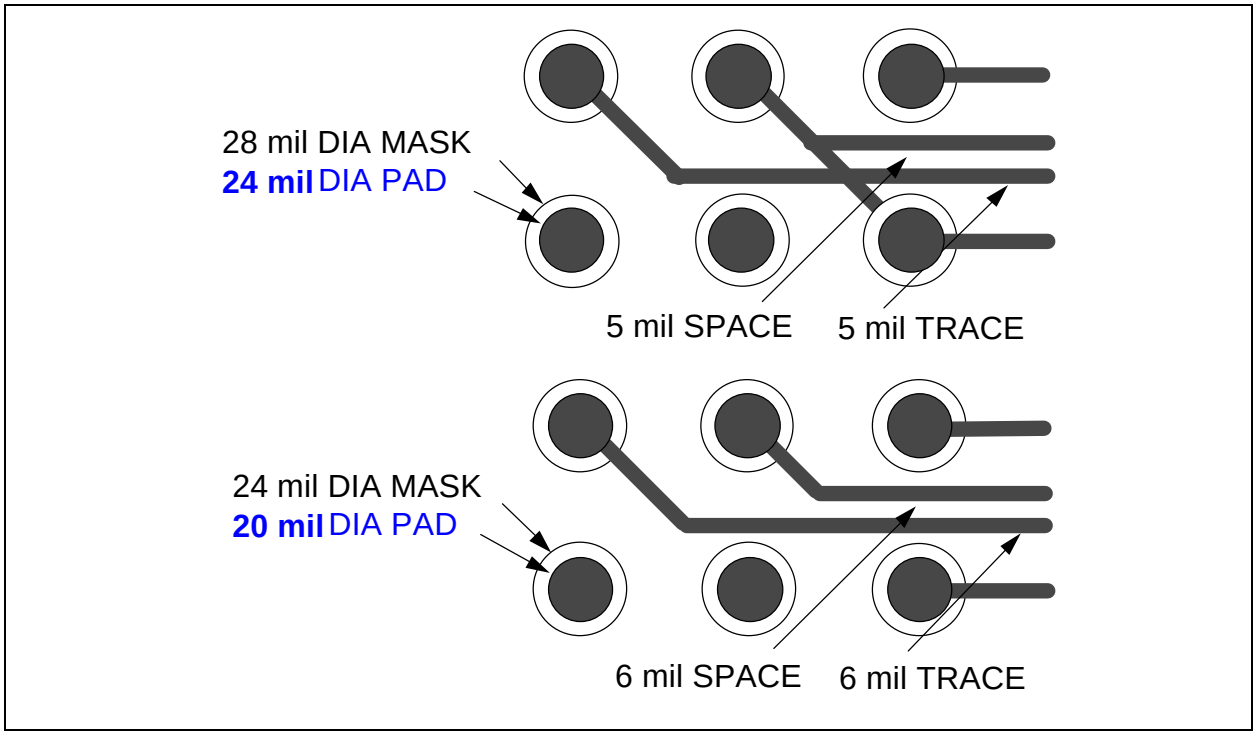


Figure 3-6. BGA Routing

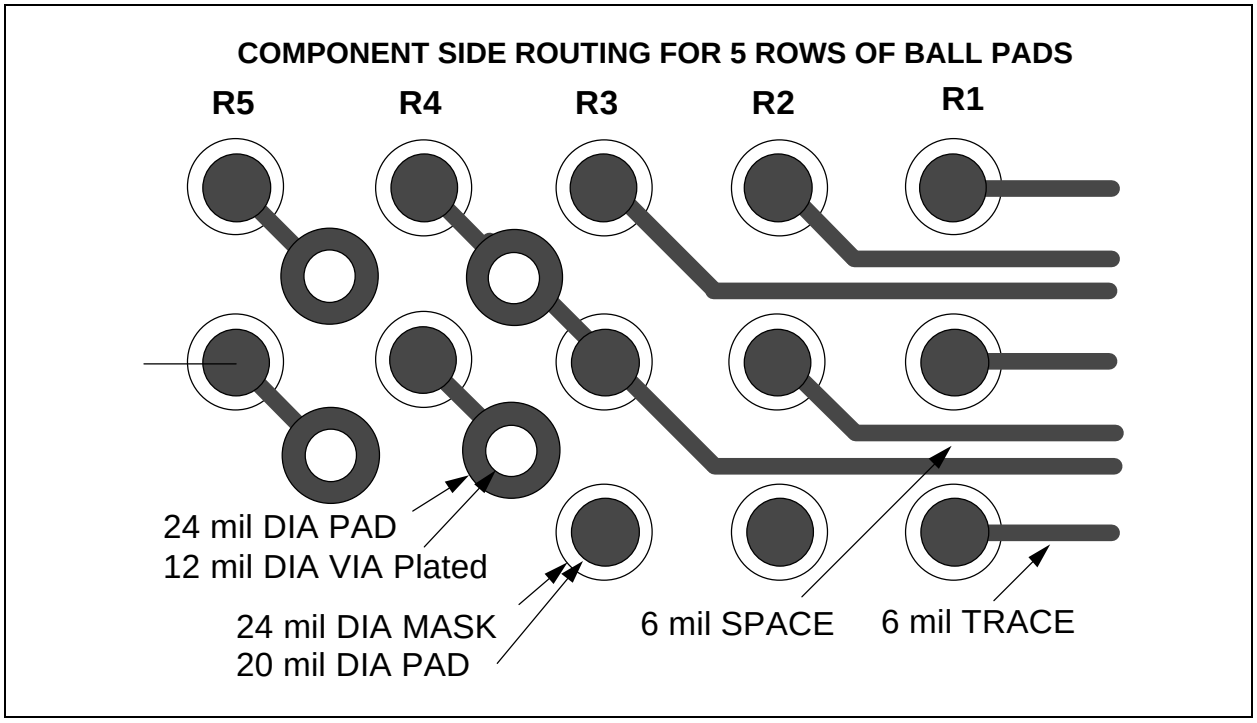


Figure 3-7. BGA Routing Example

Using the routing scheme shown above, the first three rows of balls can be routed on the top signal layer. The inner two rows must be routed on the bottom side of the board. As a result, vias are required in between the BGA pads. The vias will be discussed in the next section.

3.3.1.2 BGA Vias

The figure below shows the connection between the BGA ball pad and a via. **All vias located between the BGA ball pads must be covered with solder mask.** This will prevent solder from wicking over to the via pad. A via pad size of 24 mils is recommended.

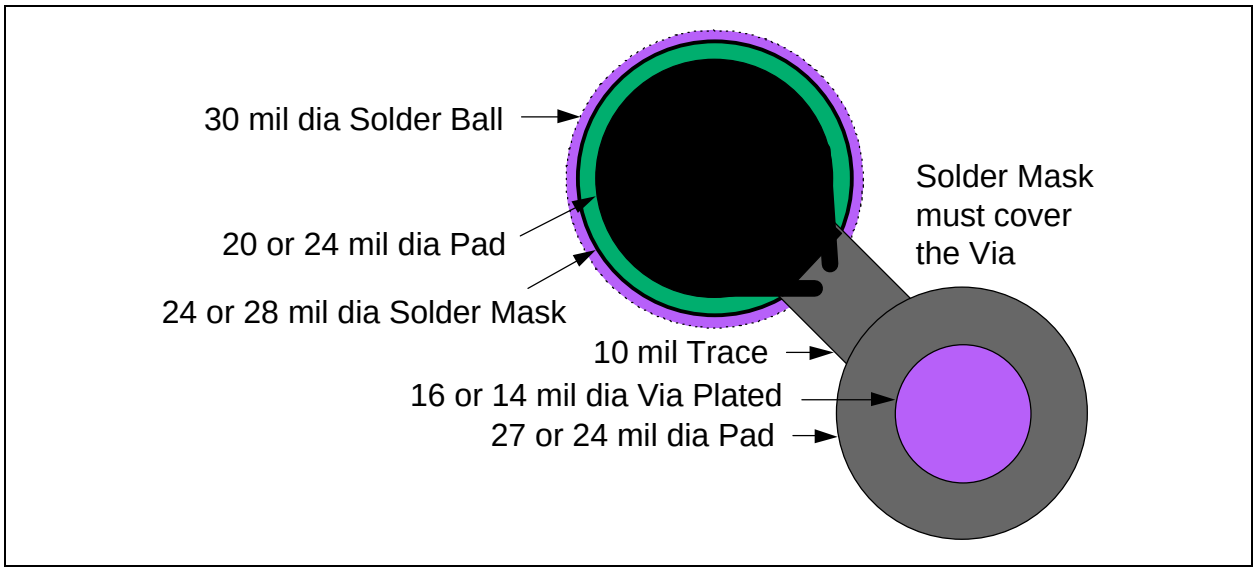


Figure 3-8. BGA Pads and Vias

3.4 BGA Routing

The figures below show a routing example for both the component and solder sides of a four layer board. The first three rows are routed on the component side, while the inner two rows are routed on the solder side of the board. This example shows 6 mil trace widths.

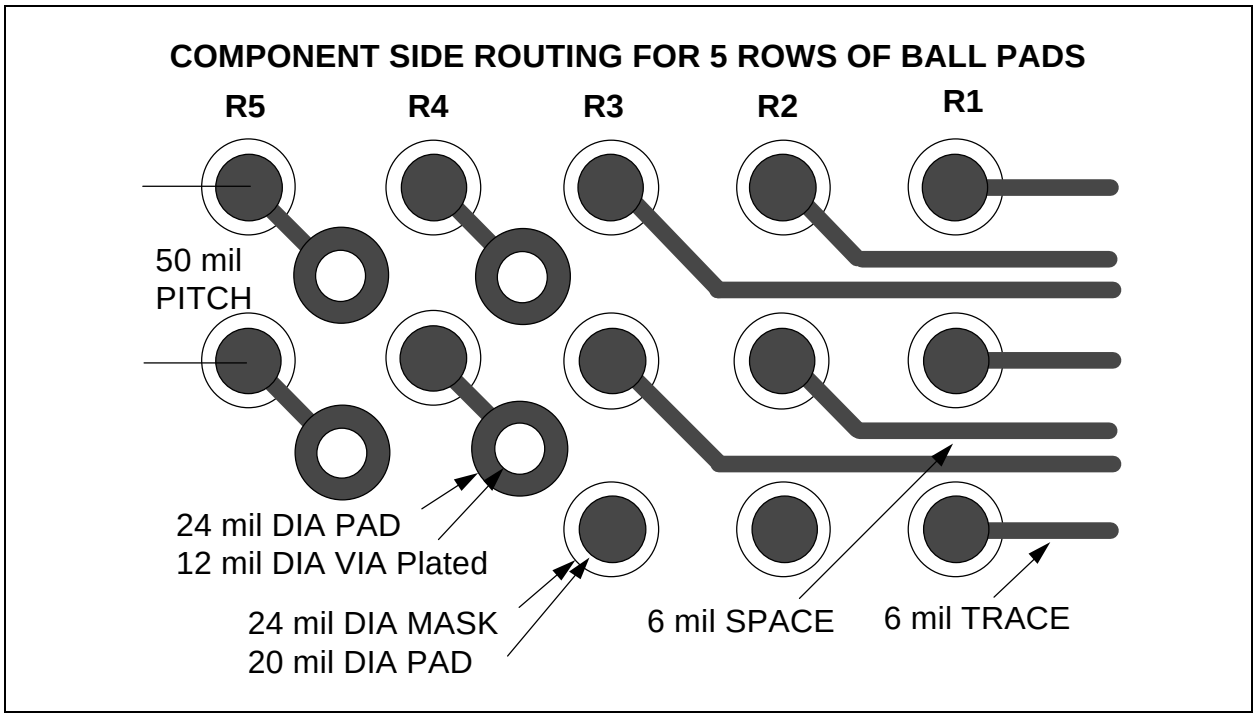


Figure 3-9. BGA Component Side Routing Example

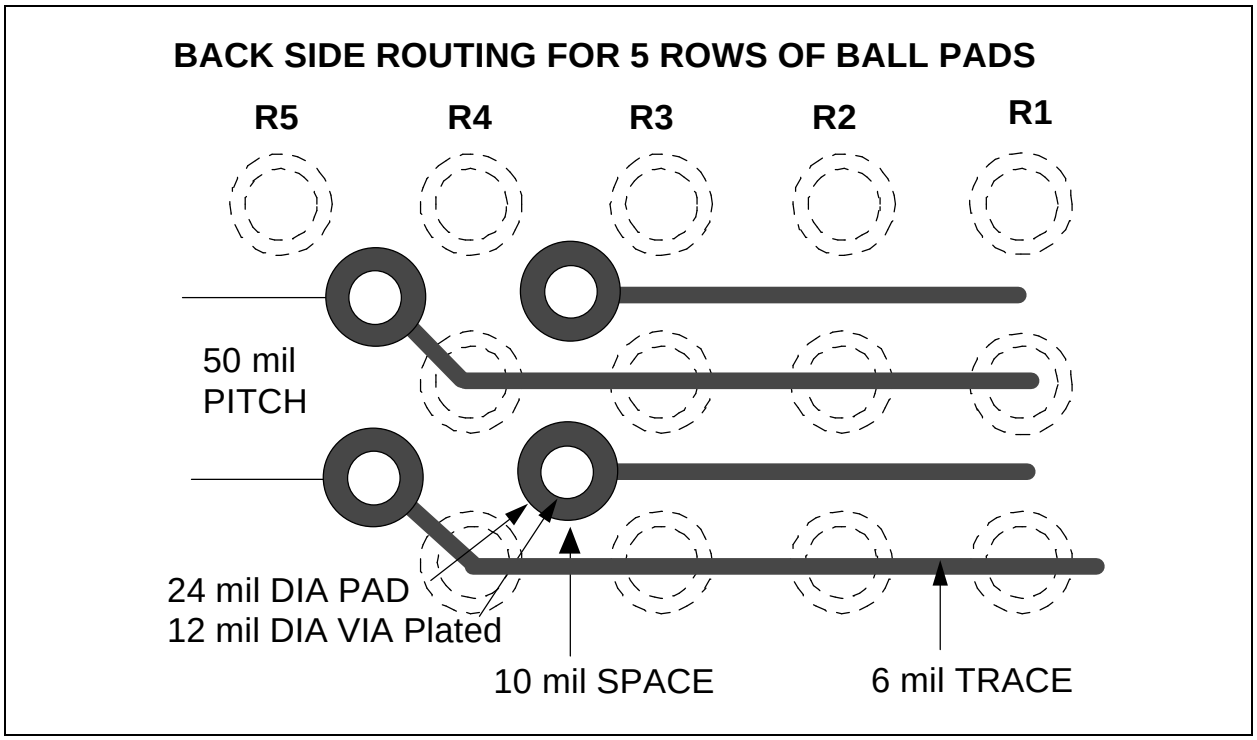


Figure 3-10. BGA Solder Side Routing Example

3.4.1 General Guidelines

It is recommended that the address, data and control signals are routed using a “daisy chain” topology. The use of this topology implies that no stubs are to be used to connect any devices on the net. Figure 3-11 shows two possible techniques to achieve a stubless trace.

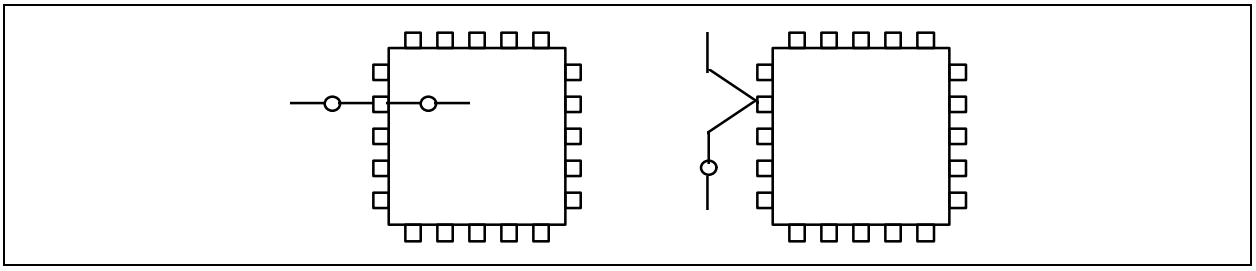


Figure 3-11. Stubless Routing Examples

In instances where it’s not possible to apply one of these two techniques due to congestion, a very short stub is allowed. The length of this stub should be kept short. Figure 3-12 shows a trace with a short stub connecting the pin.

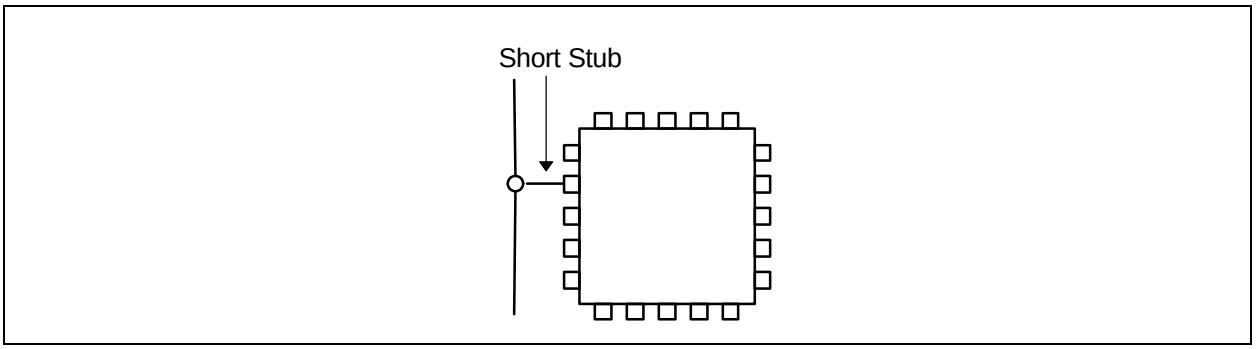


Figure 3-12. Short Stub Routing Example

3.4.2 Memory/Cache Layout Guidelines

The 430TX PCIset supports a wide range of design options. The following are key options that must be determined before layout and routing.

- How many rows of memory will the design support.
- Which type of DRAM module will be used (DRAM, SDRAM, or both).
- How much cache memory will be supported (256K vs. 512K).

The possible DRAM and system options supported by the 430TX PCIset are shown in the following table.

Table 3-1. Memory/Cache Types Supported by 430TX

DRAM Type	FPM, EDO, SDRAM
DRAM/SDRAM Module Type	72-pin SIMM: 32 bit, 168-pin DIMM: 64 bit
DRAM/SDRAM Voltage	3.3V, 5.0V
Number of rows of memory	1 to 6
DRAM Speed	50, 60, 70 ns
DRAM Component Width	x4, x8, x16
SDRAM Speed	66/60 MHz, RAS-to-CAS latency=2 or 3 clocks
SDRAM Component Width	x8, x16
CPU Bus Frequency	60, 66 MHz

The text below will use the term ‘row’ or ‘row of memory’ to describe 64 bits of memory connected to the same RAS# signal. There are a few different ways to create a row of memory that include the following:

- 2 single density 72-pin SIMMs = 1 row (1 RAS# line) of memory
- 2 double density 72-pin SIMMs = 2 rows (2 RAS# lines) of memory
- 1 single density 168-pin DIMM = 1 row (1 RAS# line) of memory
- 1 double density 168-pin DIMM = 2 rows (2 RAS# lines) of memory
- A fifth row is available that supports x8 or x16, 4-Mbit or 16-Mbit DRAM or 16-Mbit SDRAM devices. In a design with only 5 RAS lines, the 5th RAS line is intended for soldered down memory. Note that for designs that use more than 4 RAS lines, all RAS lines must use the same type of memory as the 5th RAS line (i.e. EDO/FPM vs. SDRAM). An additional 6th RAS line is also provided. In EDO only designs, buffers must be used to support more than 5 rows of memory. Buffering SDRAM rows must not be done. See the 82439TX System Controller data sheet for further details on supported DRAM configurations.

With the above options available, the following layout guidelines are provided.

- 2 to 4 rows of memory using SIMM or DIMM modules.
- 1 to 5 rows of memory using DRAM SIMM or DIMM modules. The 5th row is soldered down.
- 2 rows of DRAM SIMMs with 2 rows of SDRAM DIMMs.
- 1 to 5 rows of memory using SDRAM DIMMs.
- 1 to 6 rows of memory using DRAM SIMMs (buffered for a 6 row system).
- 256K/512K Pipelined Burst SRAM.

Table 3-2. Analyzed Possibilities 1–4 Rows of Memory

Performance	DRAM Type	DRAM Speed (ns)	CPU Bus Freq. (MHz)
x-1-1-1	SDRAM	CL=2 or CL=3	60, 66
x-2-2-2	EDO	60	60, 66
x-3-3-3	FPM	60	60, 66

Table 3-3. Analyzed Possibilities 5–6 Rows of Memory

Performance	DRAM Type	DRAM Speed (ns)	CPU Bus Freq. (MHz)
x-1-1-1[1]	SDRAM	CL=2 or CL=3	60, 66
x-3-3-3[2]	EDO	60	60, 66
x-4-4-4[2]	FPM	60	60, 66

- SDRAM must not be buffered and is limited to x8 and x16, 4-Mbit or 16-Mbit devices
- MA lines and MWE# lines must be buffered for 6 row designs. Requires additional clock to be added to leadoff and burst portion of the cycle when buffered and due to additional loading on CAS# and WE# signals.

The tables below show the recommended maximum trace lengths for each of the 430TX high speed interfaces. The maximum trace lengths are divided into the following tables.

- Table 3-4 Host/Cache interface for PBSRAM (256K/512K)
- Table 3-5 EDO/FPM/ SDRAM interface (4 RAS lines)
- Table 3-6 SDRAM only design (5 RAS lines)
- Table 3-7 EDO/FPM only design (5 RAS lines)
- Table 3-8 EDO/FPM only design (6 RAS lines)

These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

Table 3-4. Host/Cache Interface Guidelines for a Pipelined Burst SRAM Cache Design

Signals	Driver	Receiver(s)	Max Length (point-to-point)	Comments
HA(18:3)	CPU	SRAM	5.5”	Note 1
HA(18:3)	CPU	Tag	4.0”	Note 1
HA(18:3)	MTXC	SRAM	6.5”	Note 1
HA(31:3)	CPU	MTXC	6.0”	Note 1
HA(31:3)	MTXC	Tag	4.0”	Note 1
BE(7:0)#	CPU	MTXC	6.0”	Note 1
BE(7:0)#	CPU	SRAM	7.0”	Note 1
HD(63:0)	CPU	MTXC	4.0”	Note 2
HD(63:0)	MTXC	SRAM	4.0”	Note 2
HD(63:0)	CPU	SRAM	4.0”	Note 2
BRDY#, BOFF#, NA#, KEN#/INV, AHOLD, EADS#	MTXC	CPU	5.0”	
ADS#, MIO#, D/C#, HLOCK#, W/R#, HITM#, SMIACT#, CACHE#	CPU	MTXC	5.0”	
W/R#	CPU	SRAM	6.0”	Note 3
ADSC#	CPU	SRAM	6.0”	
CADV#, CADS#	MTXC	SRAM	6.0”	
CCS#	MTXC	SRAM	6.0”	
COE#	MTXC	SRAM	6.0”	
GWE#	MTXC	SRAM	6.0”	
BWE#	MTXC	SRAM	6.0”	
TIO(7:0)	MTXC	Tag	6.0”	
TWE#	MTXC	Tag	6.0”	
KRQAK	MTXC	SRAM	6.0”	

Notes:

1. Keep the total cumulative Host Address length less than 12”.
2. Keep the total cumulative Host Data Bus less than 8.0”.
3. Keep the total cumulative W/R# less than 7.0”.

Table 3-5. Memory Interface Guidelines for an EDO/FPM/SDRAM Design with 1 to 4 Rows

Signals	Driver(s)	Receiver(s)	Max Length (point-to-point)	Comments
CS(3:0)#	MTXC	SDRAM	7”	Note 2
DQM(7:0)	MTXC	SDRAM	6”	Note 1
SRAS(B:A)#	MTXC	SDRAM	7”	Notes 2,3
SCAS(B:A)#	MTXC	SDRAM	7”	Notes 2,3
MA(14:0)	MTXC	SDRAM	6”	Note 2
WE(B:A)#	MTXC	SDRAM	6”	Notes 2,3
CKE(B:A)	MTXC	SDRAM	6”	Notes 2,3
RAS(3:0)#	MTXC	DRAM	8”	Note 2
CAS(7:0)#	MTXC	DRAM	8”	Note 1
MA(14:0)	MTXC	DRAM	7”	Note 2
WE(B:A)#	MTXC	DRAM	7”	Note 3
MD(63:0)	MTXC	DRAM/ SDRAM	7”	

Notes:

1. Series termination of 10 ohms is required. The series termination should be placed at the driver.
2. To reduce undershoot, series termination or ground clamp diodes are recommended on these lines to support the minimum load cases. If series termination is used, use 10 ohms placed as close to the driver as possible. This value provides the best signal integrity and flight time results. The terminating diodes should be placed at the end of the trace (receiver) and have a forward on current of at least 200 mA at 1 volt. An MMBD1203 diode or equivalent meets this requirement. Diodes improve signal integrity without increasing the flight time.
   A 10 ohm series resistor will increase the flight time by approximately 300 ps.
3. Should be evenly distributed throughout DRAM array.

Table 3-6. Memory Interface Guidelines for an SDRAM only design with 1 to 5 Rows

Signals	Driver(s)	Receiver(s)	Max Length (point-to-point)	Comments
CS(4:0)#	MTXC	SDRAM	7”	Note 2
DQM(7:0)	MTXC	SDRAM	6”	Note 1
SRAS(B:A)#	MTXC	SDRAM	7”	Notes 2,3
SCAS(B:A)#	MTXC	SDRAM	7”	Notes 2,3
MA(13:0)	MTXC	SDRAM	7”	Note 2
WE(B:A)#	MTXC	SDRAM	6”	Notes 2,3
CKE(B:A)	MTXC	SDRAM	6”	Notes 2,3
MD(63:0)	MTXC	SDRAM	6”	

Notes:

1. Series termination of 10 ohms is required. The series termination should be placed at the driver.
2. To reduce undershoot, series termination or ground clamp diodes are recommended on these lines to support the minimum load cases. If series termination is used, use 10 ohms placed as close to the driver as possible. This value provides the best signal integrity and flight time results. The terminating diodes should be placed at the end of the trace (receiver) and have a forward on current of at least 200 mA at 1 volt. An MMBD1203 diode or equivalent meets this requirement. Diodes improve signal integrity without increasing the flight time.
   A 10 ohm series resistor will increase the flight time by approximately 300 ps.
3. Should be evenly distributed throughout DRAM array.

Table 3-7. Memory Interface Guidelines for an EDO/FPM only Design with 1 to 5 Rows

Signals	Driver(s)	Receiver(s)	Max Length (point-to-point)	Comments
RAS(3:0)#	MTXC	DRAM	9”	Note 2
CAS(7:0)#	MTXC	DRAM	9”	Note 1
MA(11:0)	MTXC	DRAM	7”	Note 2
WE(B:A)#	MTXC	DRAM	7”	Notes 2,3
MD(63:0)	MTXC	DRAM	7”	

Notes:

1. Series termination of 10 ohms is required. The series termination should be placed at the driver.
2. To reduce undershoot, series termination or ground clamp diodes are recommended on these lines to support the minimum load cases. If series termination is used, use 10 ohms placed as close to the driver as possible. This value provides the best signal integrity and flight time results. The terminating diodes should be placed at the end of the trace (receiver) and have a forward on current of at least 200 mA at 1 volt. An MMBD1203 diode or equivalent meets this requirement. Diodes improve signal integrity without increasing the flight time.
   A 10 ohm series resistor will increase the flight time by approximately 300 ps.
3. Should be evenly distributed throughout DRAM array.

Table 3-8. Memory Interface Guidelines for an EDO/FPM only Design with 1 to 6 Rows

Signals	Driver(s)	Receiver(s)	Max Length (point-to-point)	Comments
RAS(3:0)#	MTXC	DRAM	9”	Note 2
CAS(7:0)#	MTXC	DRAM	9”	Note 1
MA(11:0)	MTXC	Buffer	3”	Notes 2,4,5
MA(11:0)	Buffer	DRAM	4”	Notes 2,4,5
WE(B:A)#	MTXC	Buffer	4”	Notes 2,3,4,5
WE(B:A)#	Buffer	DRAM	3”	Notes 2,3,4,5
MD(63:0)	MTXC	DRAM	7”	

Notes:

1. Series termination of 10 ohms is required. The series termination should be placed at the driver.
2. To reduce undershoot, series termination or ground clamp diodes are recommended on these lines to support the minimum load cases. If series termination is used, use 10 ohms placed as close to the driver as possible. This value provides the best signal integrity and flight time results. The terminating diodes should be placed at the end of the trace (receiver) and have a forward on current of at least 200 mA at 1 volt. An MMBD1203 diode or equivalent meets this requirement. Diodes improve signal integrity without increasing the flight time. A 10 ohm series resistor will increase the flight time by approximately 300 ps.
3. Should be evenly distributed throughout DRAM array.
4. Keep the cumulative trace length less than 8”.
5. These signals are buffered using 74FCT3255A devices. Each buffered MA output should be connected to two rows of memory.

3.4.3 Memory/Cache Routing Guidelines

Below are four figures showing the recommended component placement and routing. Figure 3-13 shows the routing for the host address and memory address lines and Figure 3-14 shows the data line routing for an ATX form factor. Figure 3-15 and Figure 3-16 show the same layout, but with a 2/3 baby AT form factor. The memory data line routing applies both to SIMM and DIMM implementations.

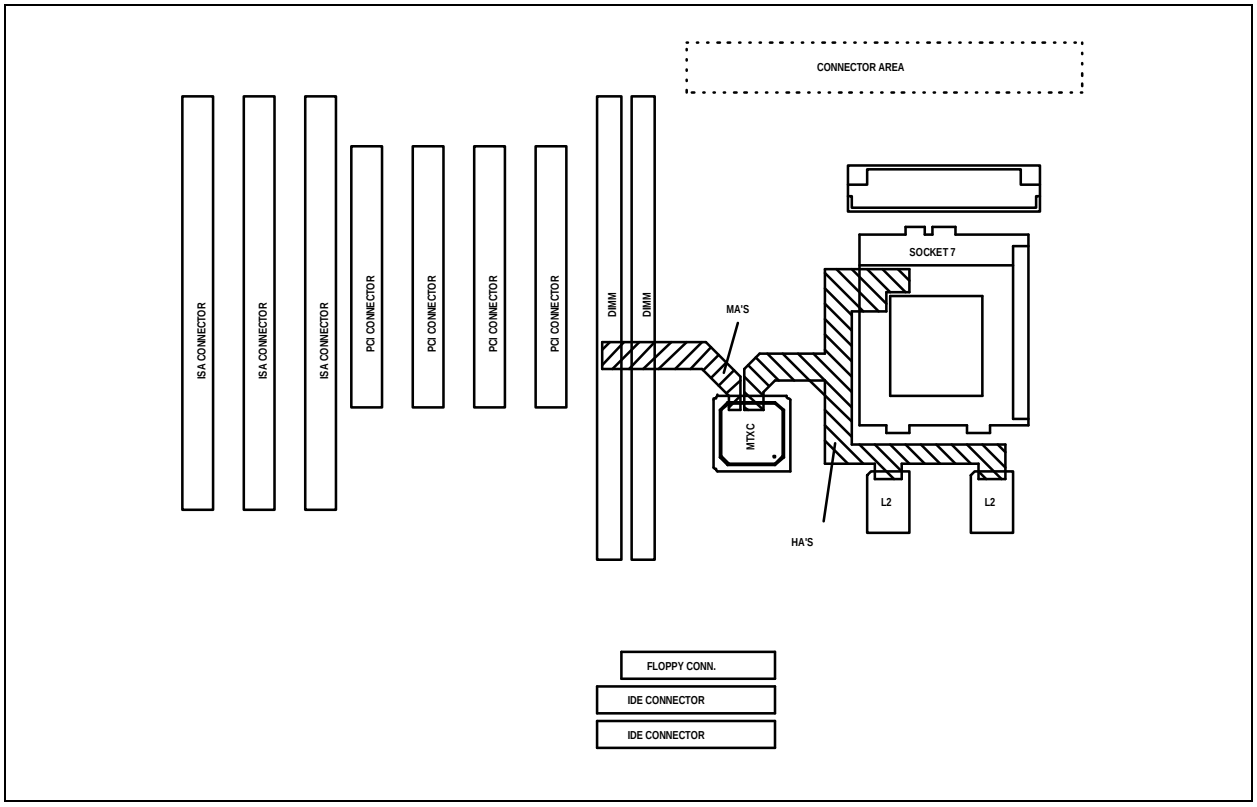


Figure 3-13. 430TX Routing Example of HA, MA lines, in an ATX form factor

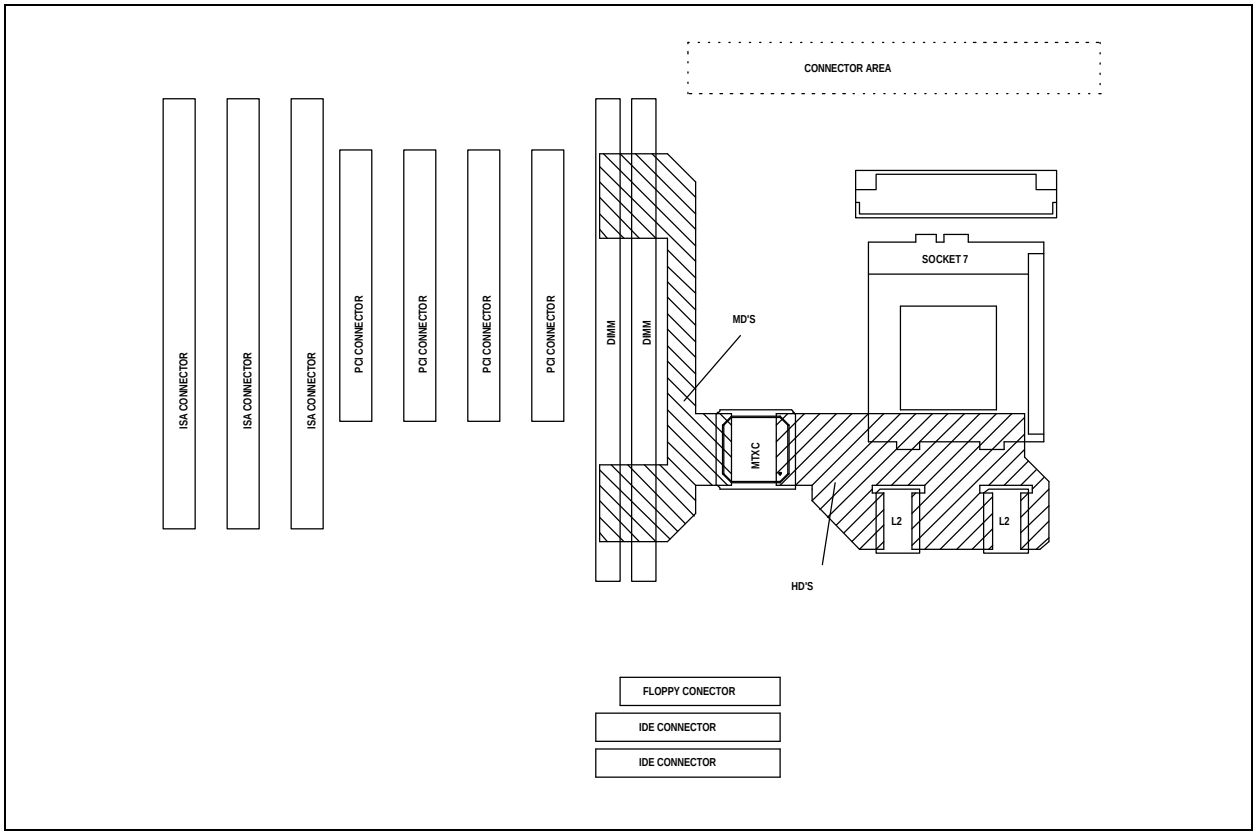


Figure 3-14. 430TX Routing Example of the MD and HD lines in an ATX form factor

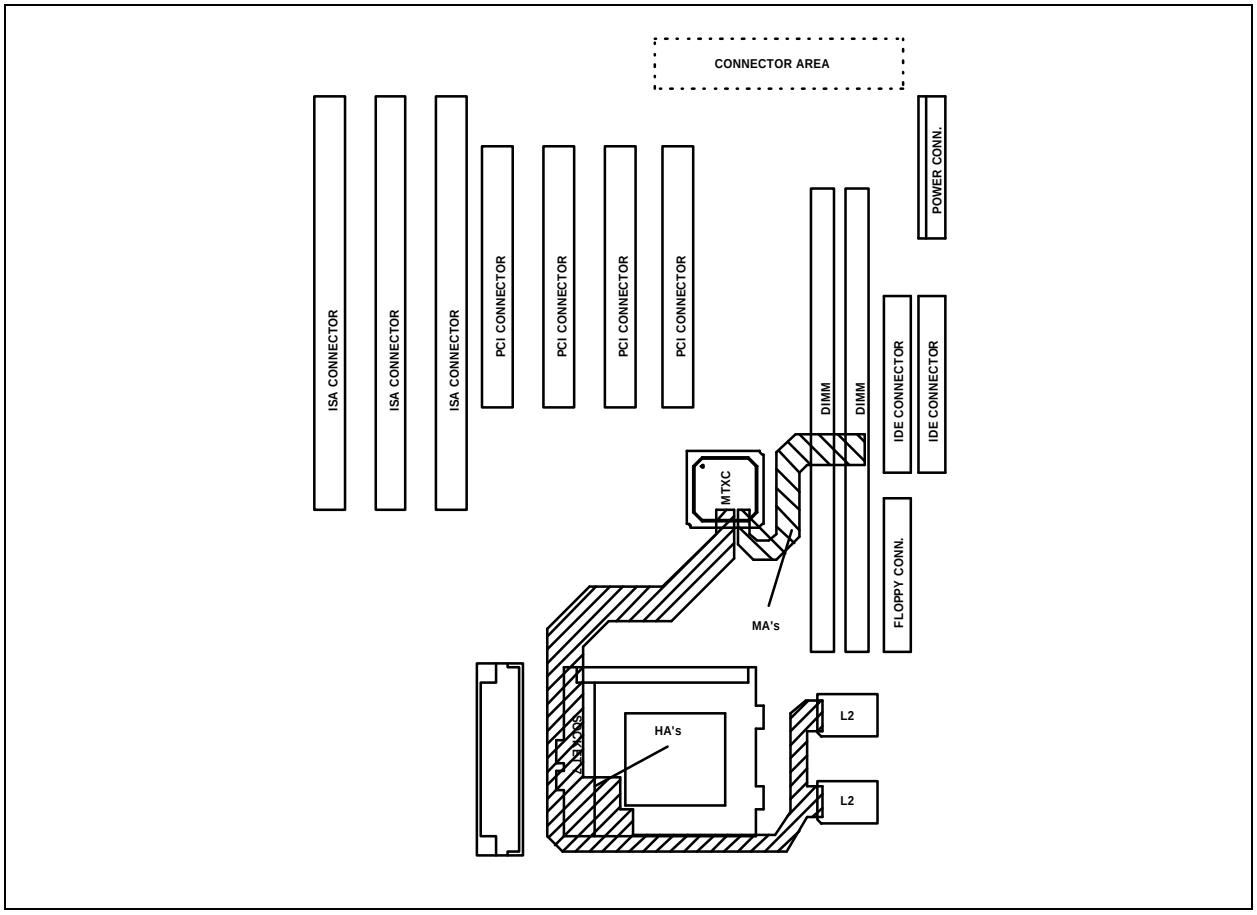


Figure 3-15. 430TX Routing Example of HA, MA lines in a 2/3 baby AT form factor

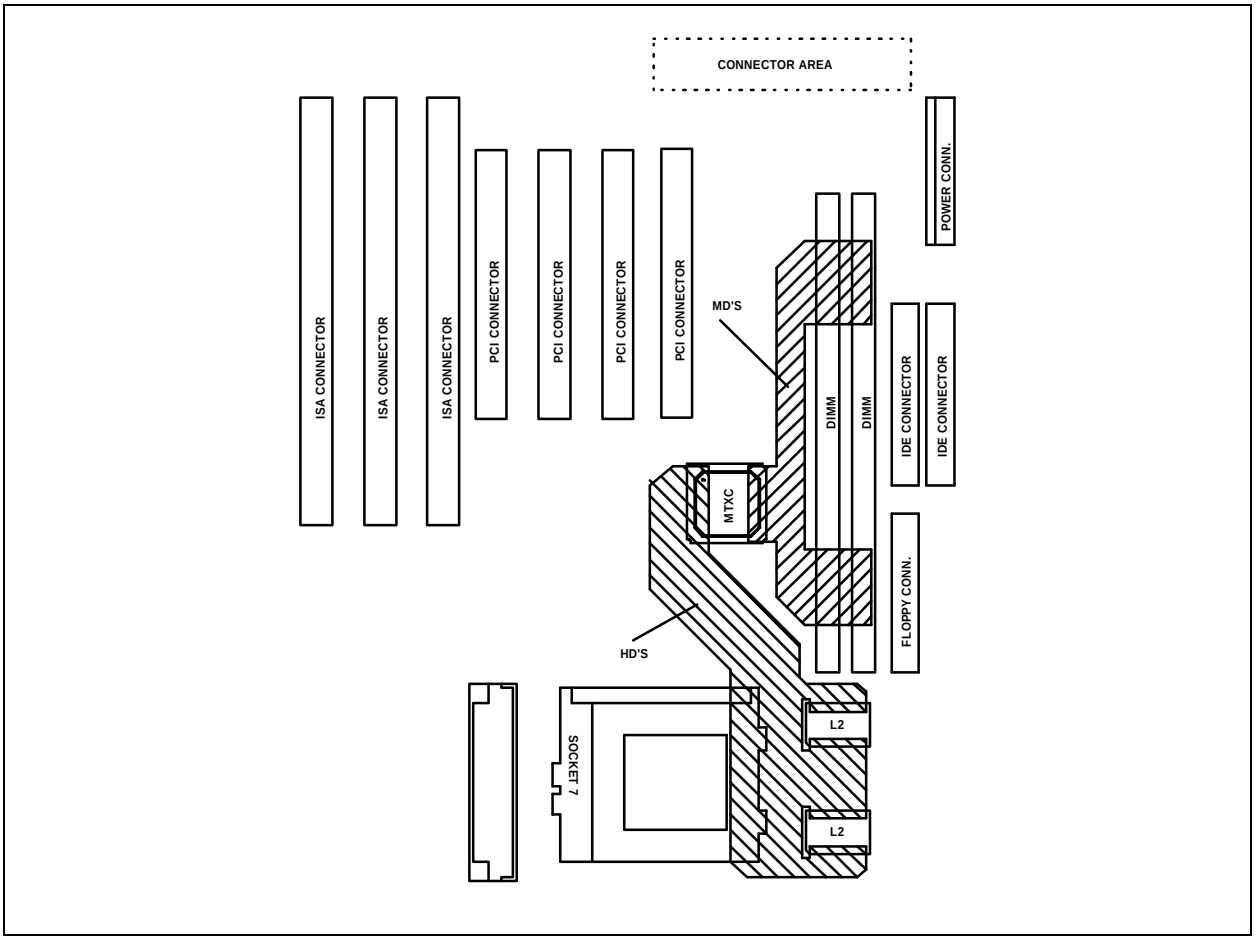


Figure 3-16. 430TX Routing Example of the MD and HD lines in a 2/3 baby AT form factor

3.4.4 Clock Routing Guidelines

Table 3-9 summarizes the clocking requirements in a 430TX system design.

Table 3-9. Clocks in a 430TX System

Host Clocks	PCI Clocks	Miscellaneous
Pentium®	MTXC	USB (48 MHz)
MTXC	PIIX4	Keyboard (12 MHz)
SDRAM (4 clocks per DIMM socket)	4 PCI Slots	Floppy clock (24 MHz)
SRAM (1 clock per 2 loads)		ISA bus OSC (14 MHz)
		Bus Clock (8 MHz from PIIX4)

The host and PCI clock routing require the most attention to detail. Below are some additional host and PCI clock routing guidelines.

3.4.4.1 Clock Skew Requirements

The following are the rising edge maximum skew requirements for the host clock and PCI clock signals being driven from the clock chip.

Table 3-10. Clock Skew Requirements

Clock Relationship	Skew Requirements	Comments
Host clock	±1.0 ns	Measured at 1.5V rising edge at the inputs
PCI clock	±2.0 ns	Measured at 1.5V rising edge at the inputs
CPU clock to MTXC clock	±0.3 ns	Measured at 1.5V rising edge at the inputs
MTXC Host clock to MTXC PCI clock	+1.0 ns to +6.0 ns	Measured at 1.5V rising edge at the MTXC inputs
SDRAM host clocks to other host clocks	±1.0 ns	Measured at 1.5V rising edge at SDRAM inputs
Clock Synthesizer output pin-to-pin skew	250 ps	Measured at 1.5V rising edge at the output buffer

3.4.4.2 Host Clock Skew Requirements

The total skew between any two host clock loads must be less than ±1.0 ns, with the exception of the Pentium to the MTXC which must be ±0.3 ns. The CPU to MTXC requirement of ±0.3 ns is based on 430TX timing analysis with worst case flight times and does not guarantee the setup and hold time margins will be met. The clock synthesizer must guarantee a maximum skew of 250 ps between any two host clock outputs. The system design must guarantee a maximum flight time skew of 750 ps between any two host clock receivers. One clock output pin should be used to drive the host clocks for the CPU and MTXC.

Extreme care should be taken when routing the SDRAM host clocks in order that a ±1.0 ns maximum skew is maintained with respect to the other host clocks. The DIMMs can place 1 load/per host clock (x16 single density), or up to 4 loads/per host clock (x8 double density), x4 devices are not recommended due to the excessive loading. The SDRAM clock layout needs to take the above factors into consideration to maintain proper signal integrity and clock skew requirements.

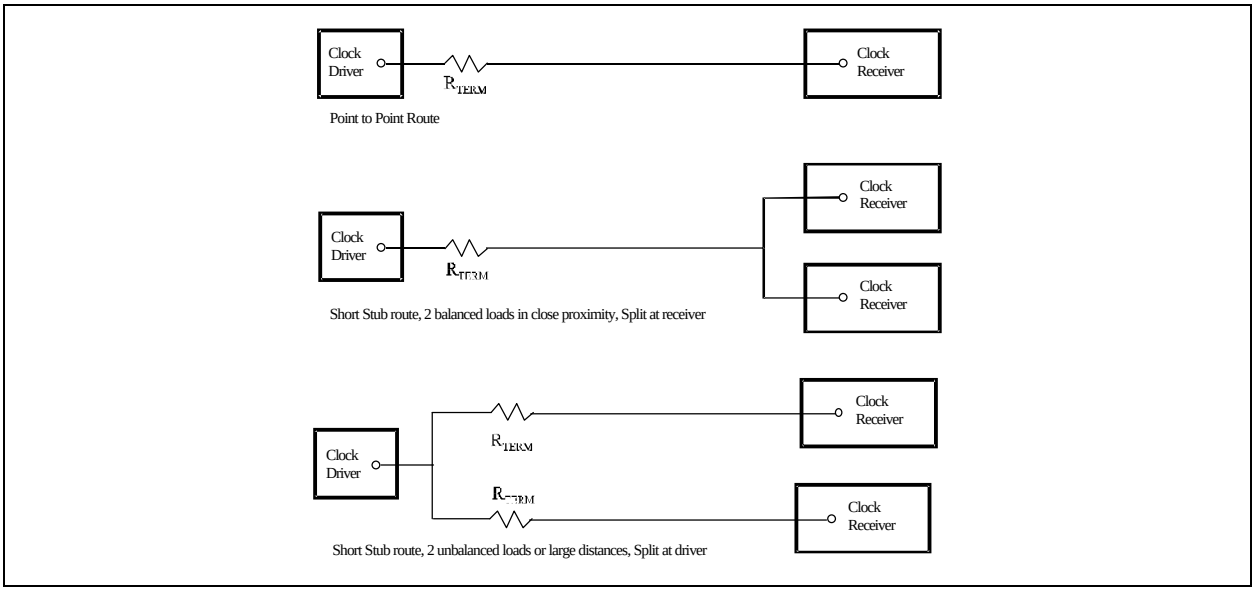


Figure 3-17. Clock Routing Topologies

Notes:

1. Series termination resistors may be required. Selection of layout topologies and buffer drive strength will determine termination requirements (resistor values).
2. Series termination resistors should be placed as close to the driver as possible.

3.4.4.3 Host Clock to PCI Clock

The clock synthesizer must guarantee a delay from the host clock output to the PCI clock outputs. The minimum delay must be 1 ns and the maximum delay should not exceed 4 ns. The system must insure that the host clock to PCI clock skew seen at the MTXC is a minimum of +1 ns and a maximum of +6 ns. This means all of the PCI clock flight times should be guaranteed to be the same or longer than the host clock flight times.

3.4.4.4 PCI Clock Skew

The total skew between any two PCI clock loads must be less than 2.0 ns. The clock synthesizer must guarantee a maximum skew of 500 ps between any two PCI clock outputs. The system design must guarantee a maximum flight time skew of 1.5 ns between any two PCI clock receivers. PCI clock traces to on-board components should be 2.5 inches longer than PCI clock traces going to PCI slots to help minimize skew.

The maximum length on any of the PCI clocks to motherboard devices should be less than 15 inches and should be less than 12.5 inches to any PCI add-in slot. Any clock signals crossing from 3.3V area to 5V should cross the boundary next to the ground plane.

3.4.4.5 Host and PCI Clock Layout for an EDO/FPM/SDRAM Design

The following is the host clock layout for a two DIMM SDRAM/EDO/FPM design. Note that the clock synthesizer component has eleven host clock outputs. If an SDRAM design implementing more than four rows is required, then a clock synthesizer component with 15 host clock outputs will be required.

Host clock layout requirement:

Where: D < 1.0”

C + D = 3.0”

Note that trace length ‘A’ is primarily dictated by the host clock-to-CPU trace.

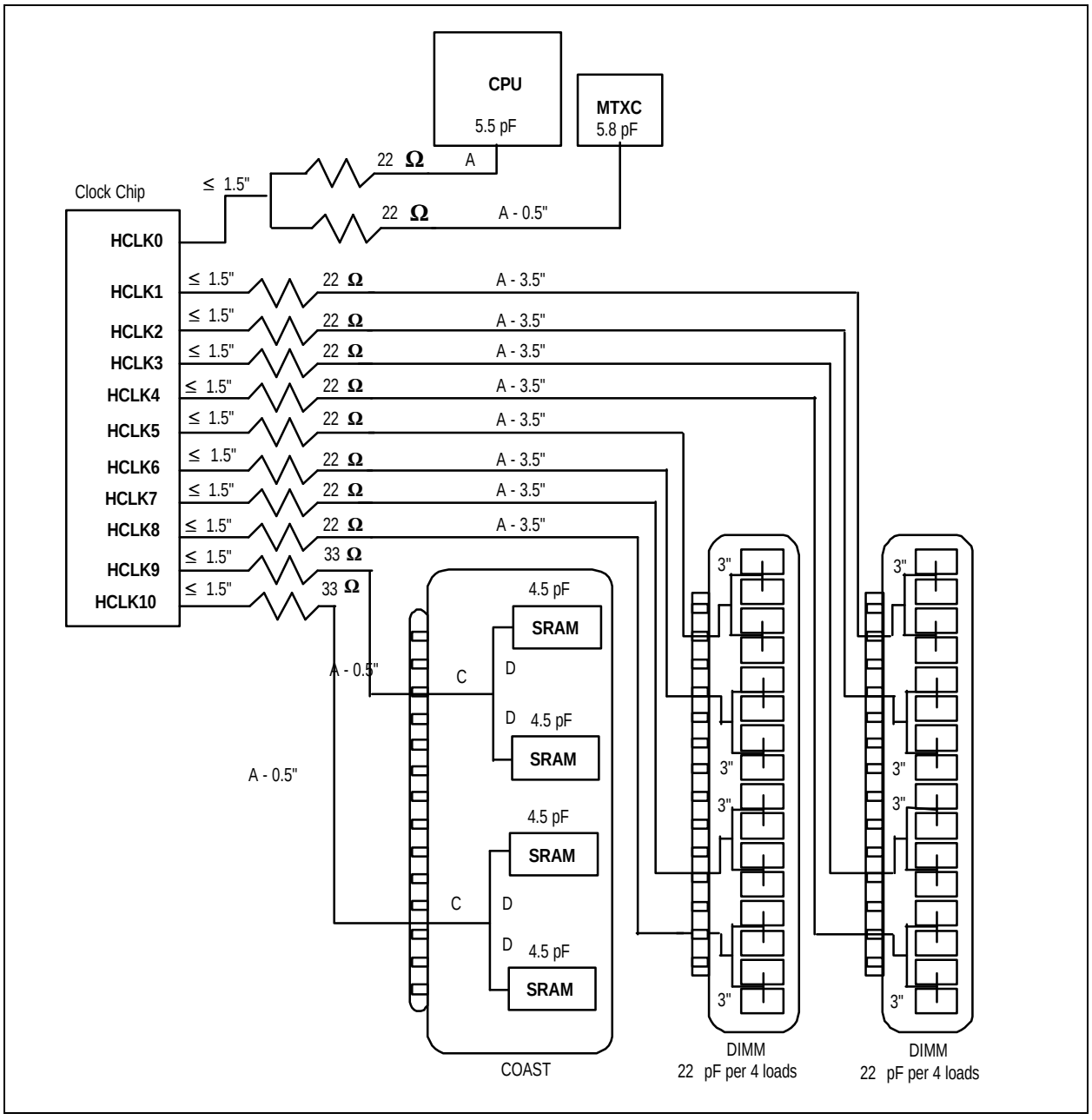


Figure 3-18. Host Clock Layout Recommendation for a two DIMM design (SDRAM/EDO/FPM)

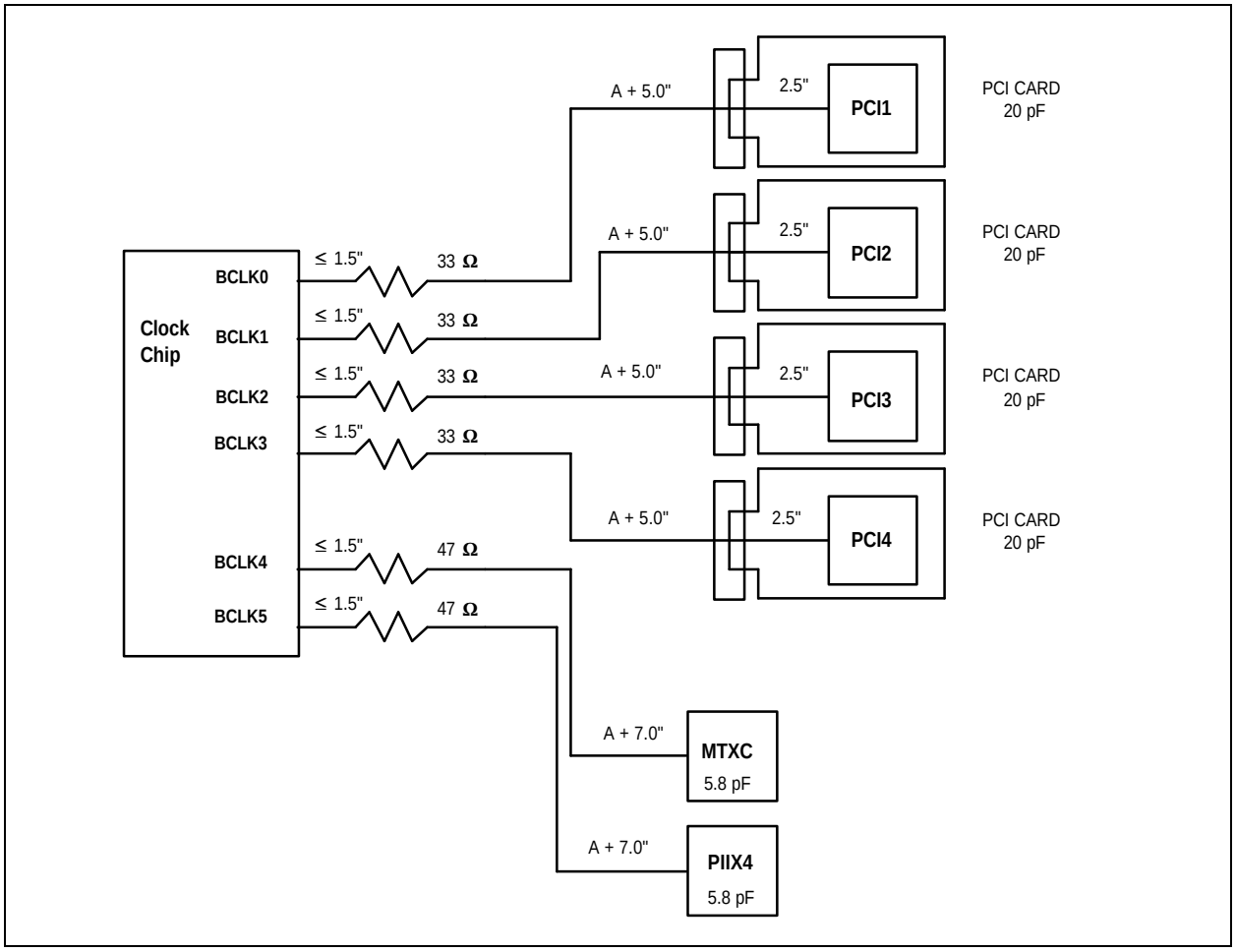


Figure 3-19. PCI Clock Layout Recommendations

3.5 IDE Routing Guidelines

This section contains guidelines for connecting and routing the PIIX4 IDE interface. The PIIX4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The current recommendations use 33 ohm resistors on all the signals running to the two ATA connectors, while the remaining signals use resistors between 22 ohm and 47 ohm resistors.

3.5.1 Cabling

- Length of cable—Each IDE cable must be equal to or less than 18 inches.
- Capacitance—Less than 30 pF.
- Placement—A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- Grounding—Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

3.5.2 Motherboard

- PIIX4 Placement—The PIIX4 should be placed as close as possible to the ATA connector(s).
- Resistor Location—When the distance between the PIIX4 and the ATA connectors exceeds 4 inches the series termination resistors should be placed within 1 inch of the PIIX4. Designs that place the PIIX4 within 4 inches of the ATA connectors can place the series resistors anywhere along the trace. Figure 3-20 shows a placement example.
- PC97 requirement—Support Cable Select for master-slave configuration is a system design requirement for Microsoft PC97. CSEL signal needs to be grounded at the host side by using a 470 ohm pull-down resistor for each ATA connector.
- Capacitance—The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
- Series Termination—The following resistor values are the current recommendations.

Table 3-11. IDE Series Termination Resistor Recommendations

Signal	Resistor	Signal	Resistor
PDD[15:0]	33Ω	SDD[15:0]	33Ω
PDA[2:0]	33Ω	SDA[2:0]	33Ω
PDIOR#	33Ω	SDIOR#	33Ω
PDIOW#	33Ω	SDIOW#	33Ω
PDDREQ	33Ω	SDDREQ	33Ω
PDCS1#	33Ω	SDCS1#	33Ω
PDCS3#	33Ω	SDCS3#	33Ω
PDDACK#	33Ω	SDDACK#	33Ω
IRQ14	22–47Ω	IRQ15	22–47Ω
RESET#	22–47Ω		

- One resistor per IDE connector is recommended for all signals. For signals labeled as 22 ohm–47 ohm, the correct value should be determined for each unique motherboard design, based on signal quality.

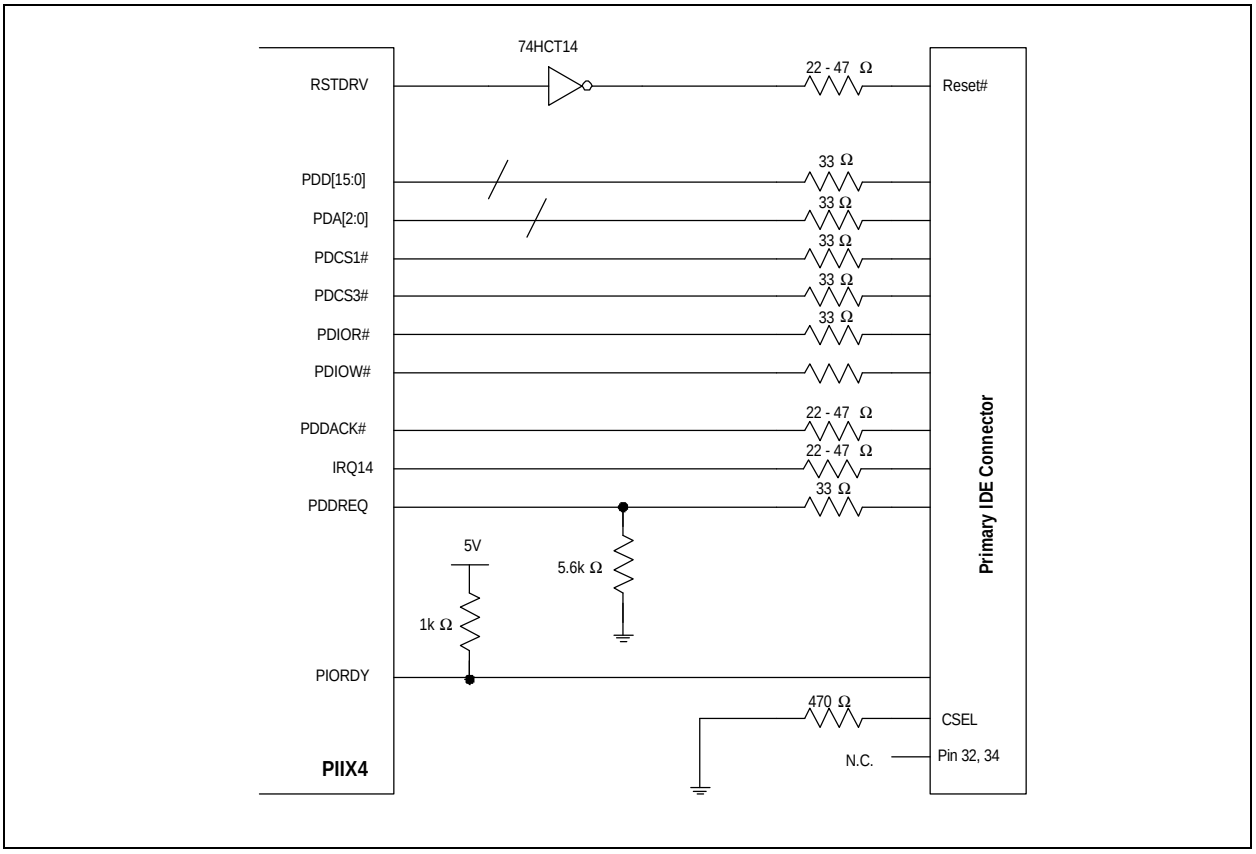


Figure 3-20. Series Resistor Placement for Primary IDE Connectors

The design consideration shown in Figure 3-20 illustrates the series resistor placement for trace lengths not exceeding 4 inches. Note that if the trace length between the PIIX4 and the IDE header exceeds 4 inches, the series resistors should be placed within 1 inch of the PIIX4. The series termination resistors are required in either design.

3.6 Motherboard Layout Guidelines for PIIX4 USB Implementations

The PIIX4 contains a Universal Serial Bus (USB) Host Controller which moves data between the main system memory and devices on the USB. The host controller also includes the root hub with two USB ports. This permits the connection of two USB peripherals or hub devices directly to the PIIX4. The PIIX4 Host Controller completely supports the standard Universal Host Controller Interface (UHCI) and takes advantage of the UHCI software drivers.

The PIIX4 fully supports the USB Specification, Revision 1.0 electrical specifications. The PIIX4 supports both full speed and low speed signaling, 12 Mbps and 1.5 Mbps, and can differentiate between full speed and low speed devices connected to its USB ports.

The key electrical requirements of USB for a motherboard design are:

- The rise and fall times of 12 Mbps data signals are 4 ns to 20 ns.
- The rise and fall times of 1.5 Mbps data signal are 75 ns to 300 ns.
- 90 ohm signal impedance for the full speed differential signal.
- Single-ended zero state on USB ports when no function is attached.
- 500 mA minimum DC supply current for each USB port.
- The voltage supplied by host is 4.65V to 5.25V.

The goal of the following routing guidelines are to minimize the effects of ringing, crosstalk, and EMI radiation in the USB data signal lines. It is very important to ensure that high frequency system signals do not couple to the USB signals and radiate out on the USB cable. This is done by carefully matching the motherboard circuitry impedance to that of the twisted pair USB cable, by controlling signal rise and fall times, and by careful routing of the USB signals on the motherboard.

3.6.1 USB Data Signals Layout Guidelines

Following are general guidelines for the USB interface:

- The unused USB port should be terminated with 15K pull-down resistors on both P+/P- data lines.
- 27 ohm series resistors should be placed as close as possible to the PIIX4 (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the PIIX4 as possible and on the PIIX4 side of the series resistors on the USB data lines (P0±, P1±). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kohm ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0± and P1±), and are REQUIRED for signal termination by USB specification. The length of stub should be as short as possible.
- The trace impedance for the P0±, P1± signals should be 45 ohm (to the ground) for each USB signal P+ or P-. The impedance is 90 ohm between the differential signal pairs P+ and P- to match the 90 ohm USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 ohm is the series impedance of both wires, resulting in an individual wire presenting a 45 ohm impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as ‘critical signals’ (i.e., hand routing preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. (Common mode current is caused by differential signals whose currents are not perfectly matched.)

The following figure illustrates the recommended USB signals schematic.

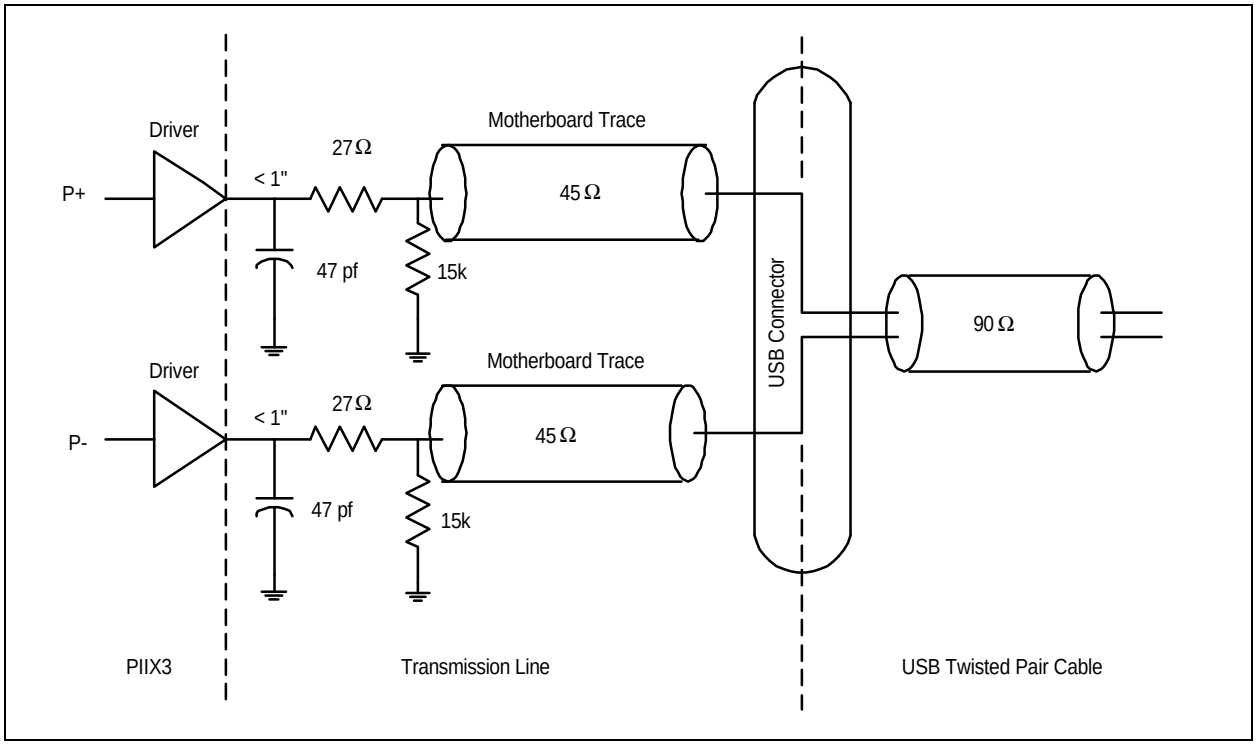


Figure 3-21. USB Data Signals

The following example illustrates a possible configuration for having a 45 ohm transmission trace. The system designer is responsible for ensuring that a particular configuration meets their requirements.

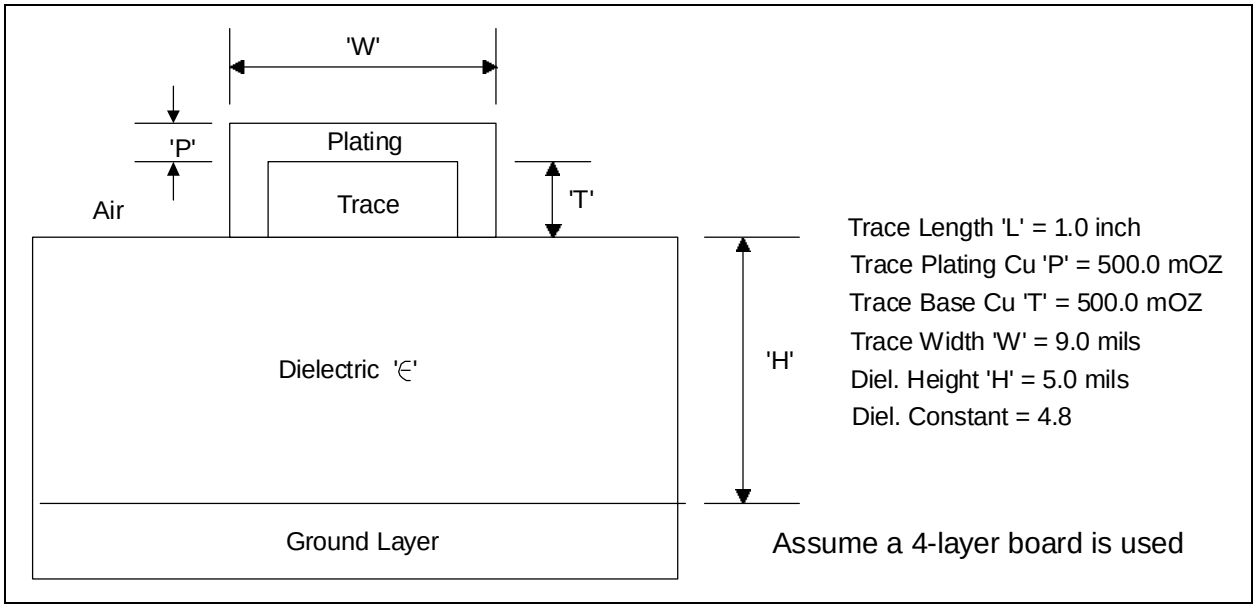


Figure 3-22. 45Ω Transmission Trace Example

The results of above example are:

- Impedance ‘Z0’ = 45.4 ohm
- Line Delay = 160.2 ps
- Capacitance = 3.5 pF

- Inductance = 7.3 nH
- Res @ 20° C = 53.9 mohm
- Trace Height = 1.4 mil

3.6.2 USB Power Distribution Layout Guidelines—Vbus

Following are general guidelines for USB power and ground lines:

- The V_{CC} power lines should be bypassed with a 68 µf or 150 µf tantalum capacitor depending on the layout topologies. It should be placed between fuse and ferrite bead on V_{CC}. The tantalum capacitors should have a low dissipation factor to allow decoupling at higher frequencies. Please refer to Section 3.6.3 in this document for the recommended topologies.
- Ferrite beads (and optional bypass capacitors) are recommended on each V_{CC} and V_{SS}, the USB power and ground lines, to minimize EMI radiation. They should be placed as close as possible to the USB connector. The recommended value of ferrite beads is 100 ohm at 100 MHz. It is important to connect bypass capacitors to chassis ground if they are used. The capacitor values should be between 0.01 µf and 0.10 µf.
- Voltage divider circuits should be used to drive the status of USB power line to OC[1:0]# inputs. OC[1:0]# signals are 3.3V inputs and have a leakage current of maximum ±1 µA. The recommended value (maximum) of resistors are 470 kohm and 560 kohm. Use a 0.001 µf to 0.01 µf capacitor for noise filtering. These resistors should be placed on the motherboard if the riser card option is used for USB connectors.
- PolySwitch fuses, standard fuses, or some type of solid state switch should be used on each power line for overcurrent protection. USB spec requires that current be limited to 5 units load (1 unit = 100 mA) for each USB port. However, the circuit protector must be chosen so that it will not trip for power on or dynamic attach transient current. The reasonable value for the trip current is 1.5A to 2.0A, and it shall not exceed 5A maximum.

Table 3-12. DC Electrical Characteristics on V_{CC}

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Powered Host)	V_{CC}	4.65	5.25	V	1
Supply Current (Powered Host)		500		mA	2,3

Notes:

1. The minimum supply voltage is 4.65V on USB port after voltage drop on power line and connector. The voltage drop on power line consists of trace resistance, the resistance of the fuse, and DC resistance of ferrite beads yielding a total voltage drop of about 100 mv. The lowest transient voltage (AC) that may appear at the host is 4.20V.
2. The supply current cannot exceed 5.0A. The recommended trip current (minimum) is 1.5A–2.0A.
3 The recommended time not to trip is 100 µs minimum for solid state switch circuit for power on and dynamic attach transient current.

The following figure illustrates the recommended USB power line and ground circuit.

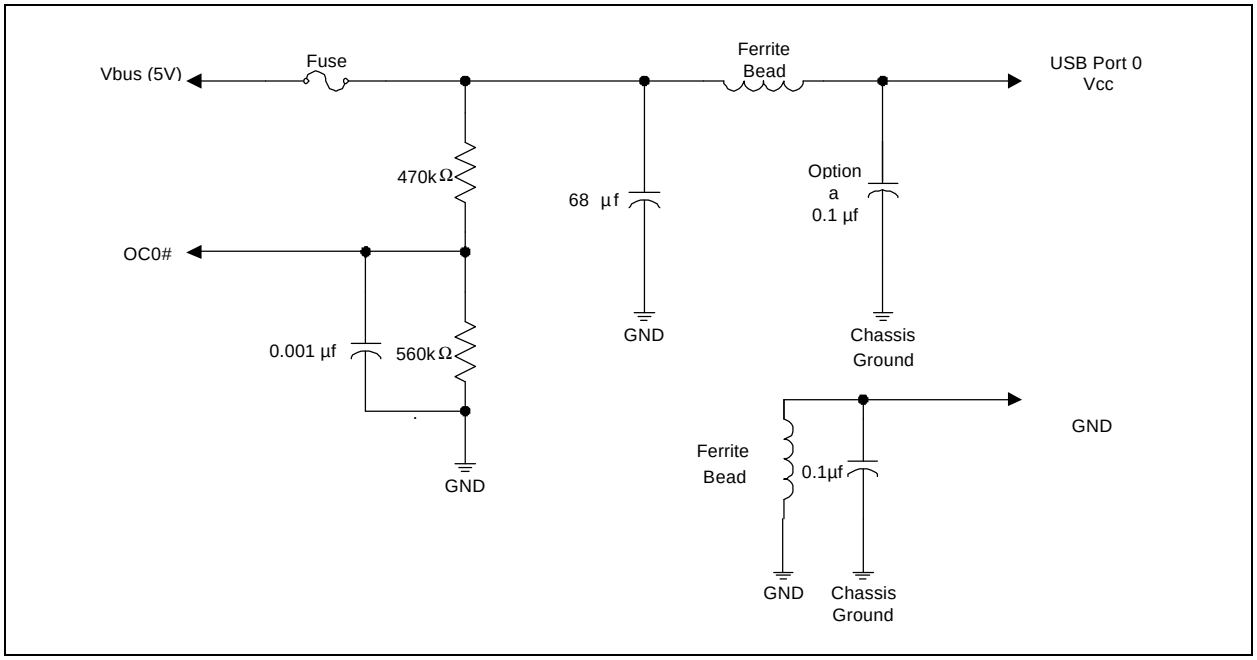


Figure 3-23. USB Power Line Vbus and Ground Line

3.6.3 USB Power Line Layout Topologies

The following power line layout topologies are typical of those found in the platforms. The system designers need to carefully evaluate each recommended topology and choose the appropriate one to meet USB voltage drop and droop requirements.

3.6.3.1 Option #1 An Optimal Design—Recommended

Figure 3-24 represents an optimal design for a downstream USB power connection. IR drop is minimized through use of separate fuses and ferrite beads. Each port has dedicated bulk capacitance. When a hot plug occurs on one port its effect on the second port is minimized because C1, C2 and C_{MB} form a three-way capacitive divider. The per port ferrite beads also have a small resistance, and that resistance acts as an inrush current limiter. Note that the recommended value of C1 and C2 tantalum capacitors is 68 µf, and C_{MB} represents the motherboard capacitance. It is also important that C1 and C2 are located within 1 inch of USB connectors.

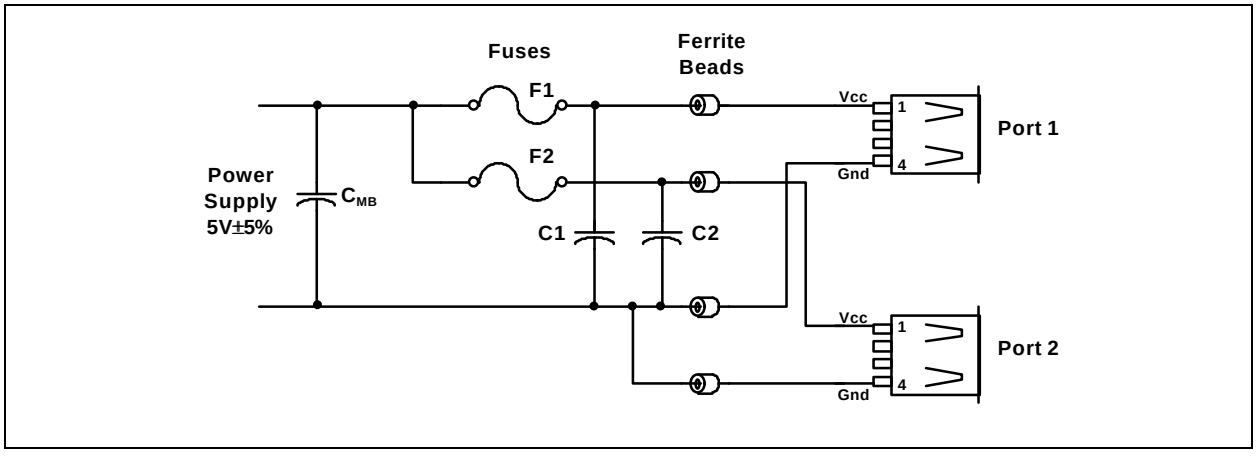


Figure 3-24. Best Downstream Power Connection

3.6.3.2 Option #2 An Effective Design—Recommended

Figure 3-25 is a less expensive but still effective implementation of a USB power output stage. The principal difference is that the per port capacitors and fuses are now shared. If F1 is increased to compensate for the need to carry twice the current then the DC voltage drop through this output circuit remains the same. Droop voltage response will not be quite as good as Figure 3-24 because C1 must now both supply current to both the peripheral already plugged in as well as the peripheral just hot plugged. The resistance of the ferrite beads becomes more critical in this instance because their resistance limits the inrush current seen by C1. The recommended value of C1 tantalum capacitors is 150 µf, and C_{MB} represents the motherboard capacitance. It is important that C1 is located within 1 inch of USB connectors.

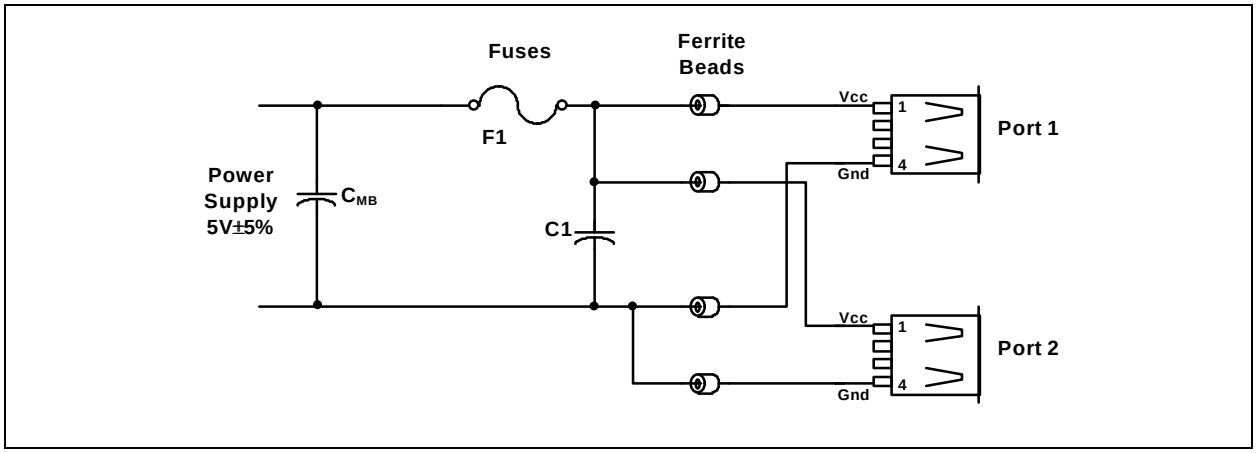


Figure 3-25. Good Downstream Power Connection

3.6.3.3 Option #3 A Less Effective Design

This output circuit is less effective in meeting the V_{DROOP} specification because the bulk capacitor is on the upstream side of the fuse, resulting in a high series resistance between the capacitor and the port. When a peripheral is hot plugged the fuse does tend to limit inrush current, but it also limits the ability of C1 to source current to the port. The recommended value of C1 tantalum capacitors is 150 µf, and C_{MB} represents the motherboard capacitance.

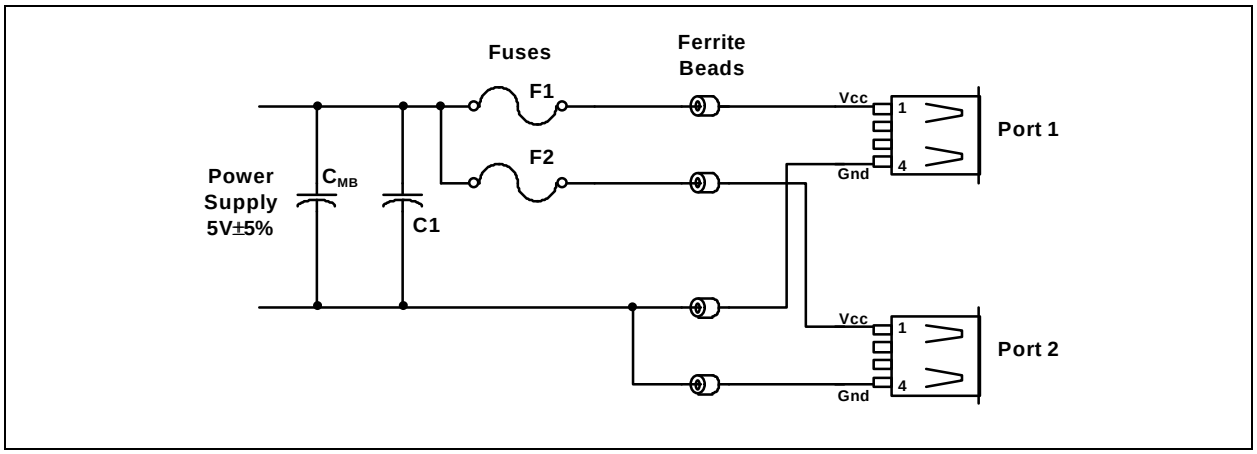


Figure 3-26. Acceptable Downstream Power Connection

3.6.3.4 Power Line Layout Topologies Are Not Recommended

Figure 3-27, Figure 3-28, and Figure 3-29 illustrate unacceptable layout configurations. Topologies of this sort have been tested and were found to fail V_{DROOP} tests. In all cases, the major problem was that the ratio of the impedance that controls inrush current and the impedance that limits how fast C1 can supply charge is too large. In particular, the circuit in Figure 3-27 suffers from having a high impedance in series with the bulk capacitance.

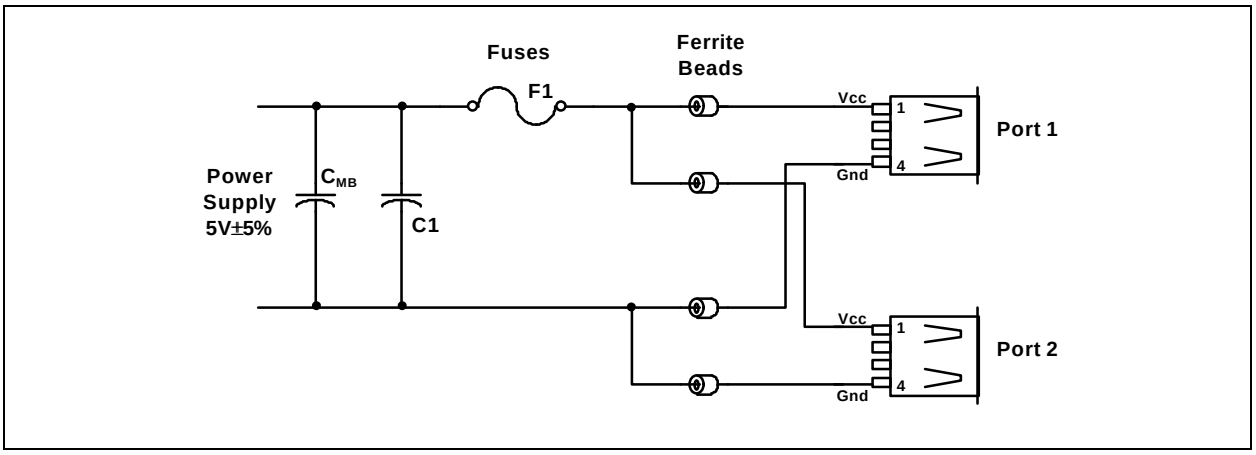


Figure 3-27. Unacceptable Downstream Power Connection

The circuits in Figure 3-28 and Figure 3-29 suffer the problem that there is no inrush current isolation offered by per port ferrite beads. Whatever voltage drop occurs on port 1 also gets reflected onto port 2. The bulk capacitors are also isolated from the ports by the relatively high resistance of the fuse.

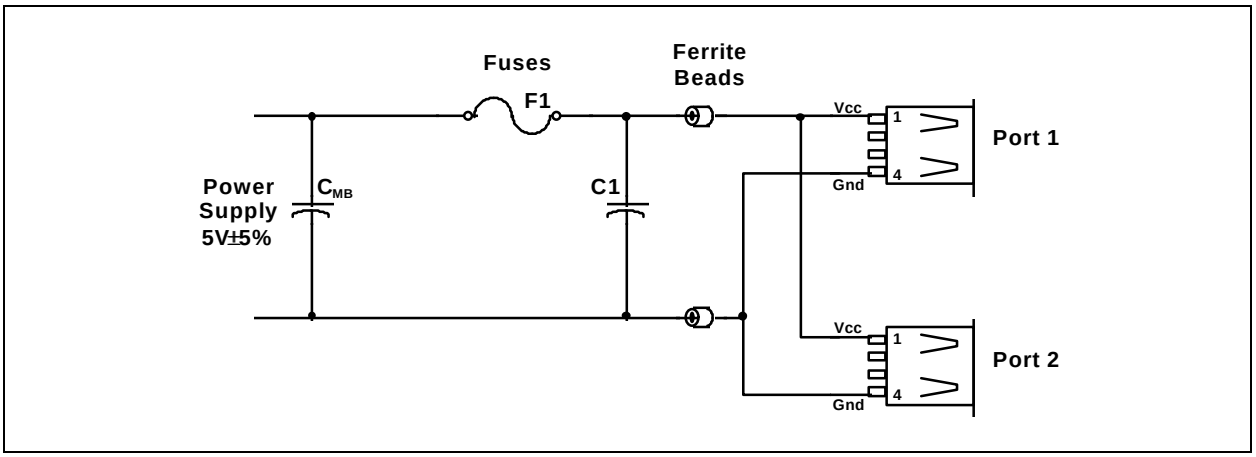


Figure 3-28. Unacceptable Downstream Power Connection

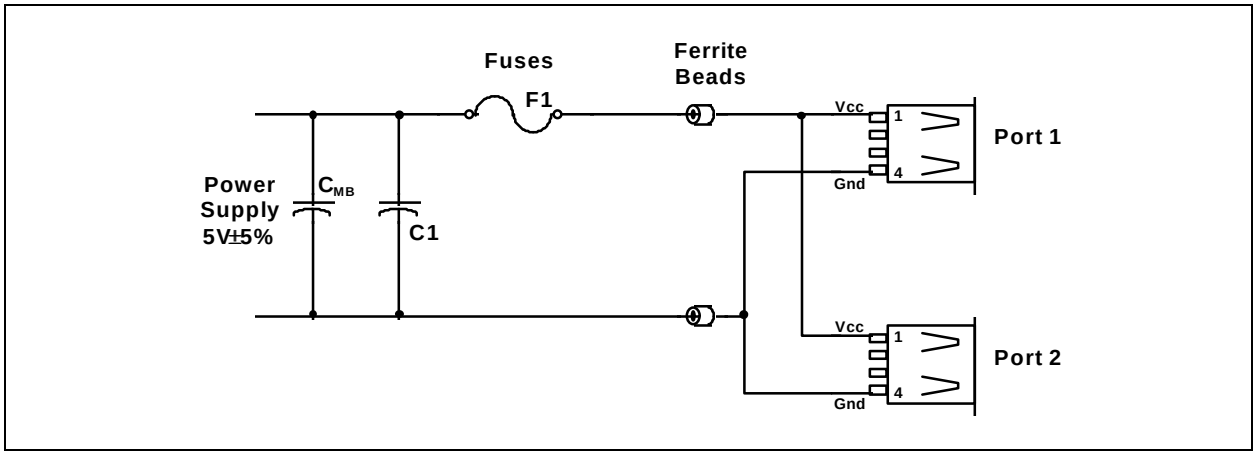


Figure 3-29. Unacceptable Downstream Power Connection

3.6.4 Options for USB Connector Implementation

3.6.4.1 Recommended Options

There are three options recommended for attaching the USB signal and power lines to the external connector.

3.6.4.1.1 Option #1 USB Connector On Motherboard

The first is the simplest, as the connector attaches directly to the motherboard and no further design considerations are necessary.

3.6.4.1.2 Option #2 USB Connector On Riser Card

The second involves use of a printed circuit riser card to connect the USB lines from a motherboard header to a USB connector installed into a standard PC slot tab. The printed circuit riser card must be designed following the guidelines mentioned in the previous section and below:

- The trace impedance for the P0±, P1± signals should be 45 ohm (to the ground) for each USB signal P+ or P-. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- There should be no series resistor on the riser card.
- The ferrite beads (and bypass capacitors if used) for EMI suppression should be placed on the riser card because they need to be as close as possible to USB connectors.
- The 68 µf or 150 µf tantalum capacitor should be placed between fuse and ferrite bead for each USB port on the riser card. Please refer to Section 3.6.1 for the recommended layout topologies.

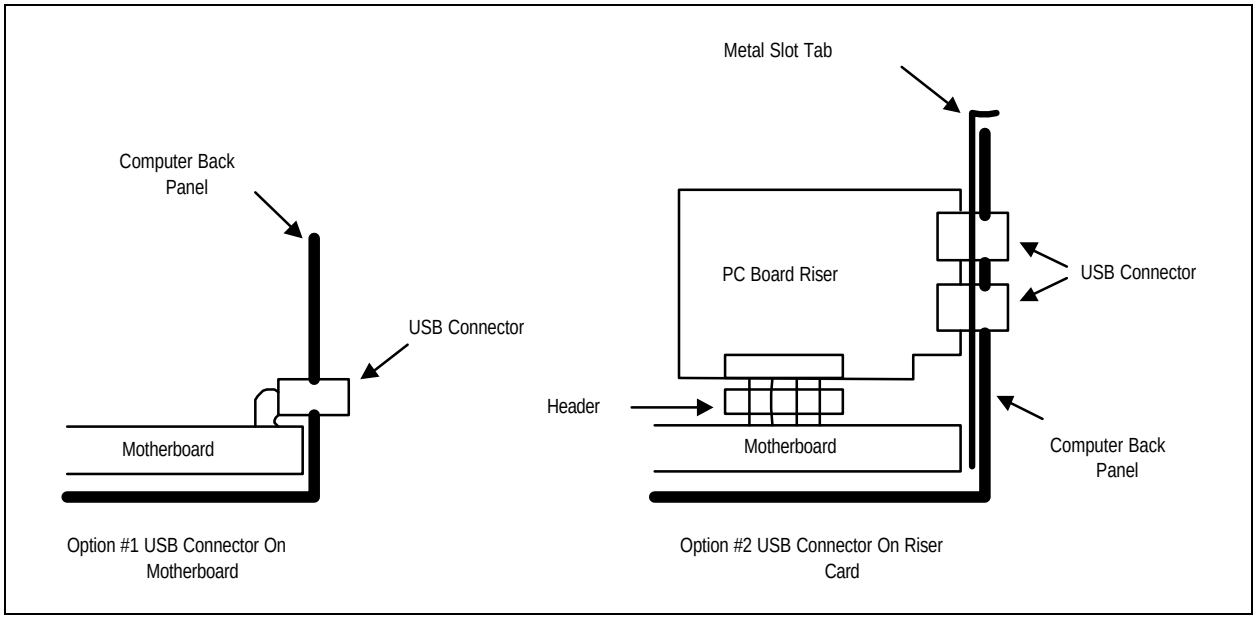


Figure 3-30. Options For USB Connector

For the printed circuit implementation, it is important that the previously described guidelines for USB signal pairs on the motherboard and the riser card are 90 ohm. The following figure shows the impedance model of USB transmission lines with use of a riser card.

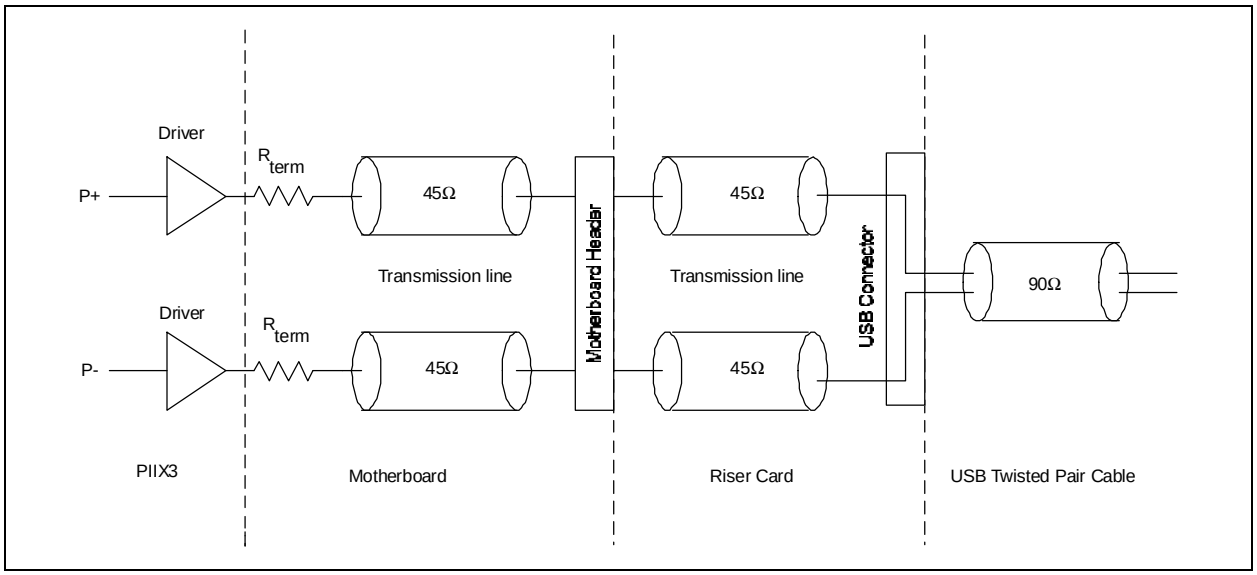


Figure 3-31 USB Data Signals With Riser Card

3.6.4.1.3 Option #3 Use A Full Speed USB Cable

The third option involves use of a full speed USB cable to connect the USB lines from a motherboard header to a standard SHIELDED USB connector on the computer's back panel. A full speed USB cable is a shielded, twisted pair cable with a characteristic impedance (Z_0) of 90 ohm ±15%. The length of the cable needs to be as short as possible. It is recommended that the total length of the motherboard trace and the cable should not exceed one foot. Please refer to the USB Specification for detailed requirements on a full rated cable.

3.6.4.2 Options Are NOT Recommended

3.6.4.2.1 Flat Ribbon Cable or Unshielded Twisted Pair Cable

A flat ribbon cable or an unshielded twisted pair cable is not recommended to be used in place of the printed circuit riser card due to adverse effects on circuit characteristics and EMI radiation. A system using these methods has high probabilities of failing EMI testing and having signal integrity problems.

3.6.4.2.2 Cable/Riser Card Combination

This method is NOT recommended. This method involves use of a cable to connect the USB lines from a motherboard header to a header on a riser card with USB connector on the riser card. A flat ribbon cable or an unshielded twisted pair cable is not recommended due to adverse effects on circuit characteristics and EMI radiation. It is also not recommended to use a full speed USB cable/riser card combination because it requires the match of the signal impedance between all three segments of the USB signals which ideally should be one segment on the motherboard. A system using these methods has high probabilities of failing EMI testing and having signal integrity problems.

3.7 Hardware Checklist

3.7.1 Motherboard Layout

- Terminate the unused USB port with 15K pull-down resistors on both P+/P- data lines.
- 27 ohm series resistors should be placed as close as possible to the PIIX4 (<1 inch).
- 47 pF caps must be placed as close to the PIIX4 as possible.
- 15 kohm ±5% pull-down resistors on the USB data lines (P0±, P1±).
- The trace impedance for the P0±, P1± signals should be 45 ohm (to ground) each trace.
- The P+/P- signal pair must be routed together and not parallel with other signal traces. Double the space from the P+/P- signal pair to adjacent signal traces. The P+/P- signal traces must also be the same length.
- Ferrite beads and bypass caps are on V_{CC} and V_{SS}, the USB power and ground lines.
- A 120 µf tantalum capacitor between ferrite bead and EMI bypass cap on each power line.
- Use a PolySwitch or a standard fuse on V_{CC} for each USB port.

3.7.2 USB Connectors Checklist

- Recommended—USB connectors are attached to the motherboard directly.
  - — Or use USB connectors on the riser card.
  - — Or use a full speed USB cable in the place of the riser card.
- The length of full speed cable should be as short as possible.
- NOT Recommended
  - — Flat ribbon cables or unshielded twisted pair cables.
  - — PC riser card and cable combination, whereboth a riser card and cable (any cable) are used.

3.7.3 USBCLK Checklist

- Use a 48-MHz clock source.
- 40/60 duty cycle for 48 MHz.
- Frequency Tolerance <= 2,500 ppm.
- Cycle-to-Cycle Clock Jitter <= 500 ps.
- Series termination resistors are used on USBCLK routing (see motherboard layout guidelines section).

4

System Clock Requirements

CHAPTER 4
SYSTEM CLOCK REQUIREMENTS

4. 430TX System Clock Requirements

This section outlines the recommended clock synthesizer specifications for a 430TX system design. Table 4-1 lists the AC timing requirements of the clock generation logic.

Table 4-1. AC Timing Requirements

		66 MHz		60 MHz			
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
2.5 volt CPU							
tHKP (2.5V)	Host CLK period	15		16.7		ns	9
tHKH (2.5V)	Host CLK high time	5.2		6.0		ns	4
tHKL (2.5V)	Host CLK low time	5.0		5.8		ns	5
tHRISE (2.5V)	Host CLK rise time	0.4	1.6	0.4	1.6	ns	8
tHFALL (2.5V)	Host CLK fall time	0.4	1.6	0.4	1.6	ns	8
tJITTER (2.5V)	Host CLK Jitter		250		250	ps	
Duty Cycle (2.5V)	Measured at 1.25V	45	55	45	55	%	
tHSKW (2.5V)	Host Bus CLK Skew		250		250	ps	1
tHSTB (2.5V)	Host CLK Stabilization from power-up		3		3	ms	6
3.3 volt CPU							
tHKP (3.3V)	Host CLK period	15		16.7		ns	9
tHKH (3.3V)	Host CLK high time	5.2		6.0		ns	10
tHKL (3.3V)	Host CLK low time	5.0		5.8		ns	5
tHRISE (3.3V)	Host CLK rise time	0.4	1.6	0.4	1.6	ns	11
tHFALL (3.3V)	Host CLK fall time	0.4	1.6	0.4	1.6	ns	11
tJITTER (3.3V)	Host CLK Jitter		250		250	ps	
Duty Cycle (3.3V)	Measured at 1.5V	45	55	45	55	%	
tHSKW (3.3V)	Host Bus CLK Skew		250		250	ps	1
tHSTB (3.3V)	Host CLK Stabilization from power-up		3		3	ms	6
tHSKSD	Host to SDRAM skew		500		500	ps	1
tPKP	PCI CLK period	30.0	∞	33.3	∞	ns	2
tPKPS	PCI CLK period stability		500		500	ps	7

Table 4-1. AC Timing Requirements (Continued)

		66 MHz		60 MHz			
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
tPKH	PCI CLK high time	12		13.3		ns	
tPKL	PCI CLK low time	12		13.3		ns	
tPSKW	PCI Bus CLK Skew		500		500	ps	1
tHPOFFSET	Host to PCI Clock Offset	1.0	4.0	1.0	4.0	ns	1, 3
tPSTB	PCI CLK Stabilization from power-up		3		3	ms	6

Notes:

1. Clock period, jitter, offset and skew are measured on the rising edge CLKs at 1.25V for the 2.5V clocks and at 1.5V for the 3.3V clocks.
2. PCI Clock is the host clock divided by two.
3. The Host CLK must always lead the PCI CLK as shown in Figure 4-3. This must be guaranteed by design under the test load conditions.
4. tHKH is measured at 2.0V for 2.5V CPUs as shown in Figure 4-4.
5. tHKL is measured at 0.4V as shown in Figure 4-4.
6. The time specified is measured from when V_{DDQ} achieves its nominal operating level (typical condition V_{DDQ}=3.3V) till the frequency output is stable and operating within specification.
7. Defined as once the clock is at its nominal operating frequency the adjacent period changes can not exceed the time specified.
8. tHRISE and tHFALL for 2.5V CPUs are measured as a transition through the threshold region Vol=0.4V and V_{OH}=2.0V (1 mA JEDEC Specification).
9. The average period over any 1 µs period of time must be greater or equal to the minimum specified period.
10. tHKH is measured at 2.4V for 3.3V CPUs as shown in Figure 4-4.
11. tHRISE and tHFALL for 3.3V CPUs are measured as a transition through the threshold region Vol=0.4V and V_{OH}=2.4V.

4.1 PIIX4 USBCLK Guidelines

4.1.1 Frequency Tolerance

The USB specification requires a data rate of 12 MHz ± 0.25% (2,500 ppm) and an initial frame interval of 1.0 ms ± 0.05% (500 ppm). The data rate specification can be met with the PIIX4 by providing a USBCLK of 48 MHz with a 2,500 ppm tolerance, including all sources of inaccuracy. The frame interval specification requires that the USBCLK frequency's unknown (variable) sources of inaccuracy are less than 500 ppm. Any known (fixed) offsets from 48 MHz can be compensated by programming the proper value into the PIIX4 SOF Modify Register.

The most straightforward method of providing USBCLK is from a canned 48.000-MHz crystal oscillator. It can provide a stable, exact frequency that is affected little by environment or loading. The default value of the SOF Modify register is sufficient to meet the frame interval timing.

Clock synthesizers provide a less expensive source of USBCLK. Most PC designs use a clock synthesizer for generating the CPU and I/O clocks. However, clock synthesizers are not as accurate and are susceptible to more environmental effects. They use a 14.31818-MHz crystal as the reference clock and a PLL to frequency multiply to the desired frequencies. The output frequency is an N-over-M integer ratio of the reference clock. It is generally not practical to use integers large enough that the

output frequency is exactly 48 MHz. Frequency offsets from +2,273 ppm to -1,858 ppm have been seen from various manufacturers. Also, since clock synthesizers use a crystal as the frequency source, the crystal's tolerance and variations due to voltage, temperature, loading and aging have to be included when analyzing the suitability of using this source for USBCLK. (Some of this variation can be avoided if a 14.31818-MHz canned oscillator is used.)

System designers need to find out frequency offset values for 48 MHz and the crystal's variation due to capacitive loading, supply voltage, temperature, and aging from vendors. These values must meet the following:

-2,500 ppm < Offset + crystal variables < +2,500 ppm.

If multiple clock synthesizer vendors are chosen for a particular solution, system designers can do the following after finding out the offset values and crystal variation:

- Choose clock synthesizers to have a same offset or have their offsets + crystal variables within ±500 ppm of each other so that a single value SOF programming works for all synthesizers.
- If one clock synthesizer offset is bigger than other, the OEM will have to change the BIOS value for the SOF Modify register programming depending on the offset value in order to meet the USB frame interval spec. Please see UHCI Design Guide for actual values to be programmed into the SOF Modify register to get the desired divisor.

For example, if the offsets of clock synthesizers are within ±167 ppm of each other and if the variation for the 14.31818-MHz crystal is < ±330 ppm, then the default value of SOF Modify register is OK. If the crystal variability is > ±330 but < ±500, then the SOF Modify register has to be programmed to divide by 12,002 to meet the 1.000 ms frame time.

4.1.2 PIIX4 USBCLK Requirements

This section outlines the recommended USB clock input specifications for a PIIX4 system design. The table below lists the AC timing requirements of the clock generation logic.

Table 4-1. AC Timing Requirements

Sym	Parameter	48 MHz		Units	Notes
		Min	Max		
Frequency Tolerance	USB CLK Frequency Tolerance		±2,500	ppm	
tUKH	USB CLK high time	7		ns	1
tUKL	USB CLK low time	7		ns	2
tURISE	USB CLK rise time		1.2	ns	3
tUFALL	USB CLK fall time		1.2	ns	3
tJITTER	USB CLK Jitter, Cycle-to-Cycle		500	ps	4
tJITTER, Absolute	USB CLK Jitter, Absolute		±700	ps	
Duty Cycle	Measured at 1.5V	40	60	%	

Notes:

1. tUKH is measured at 2.0V as shown in Figure 4-1.
2. tUKL is measured at 0.8V as shown in Figure 4-1.
3. tURISE and tUFALL are measured as a transition time through the threshold region Vol = 0.8V and Voh = 2.0V.
4. Frequency Tolerance needs to be taken into the consideration in a particular implementation. See Section 4.1.3.

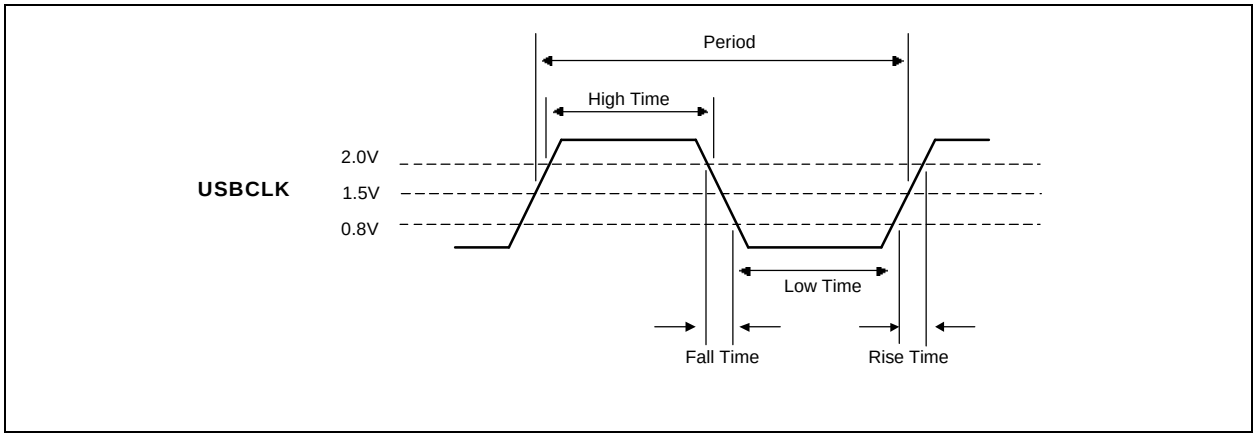


Figure 4-1. USBCLK Waveform

For 3.3V clocks the threshold is 1.5V, and for 2.5 volt clocks the threshold is 1.25 volts. Figure 4-2 and Figure 4-3 below only show 2.5 volt host clocks.

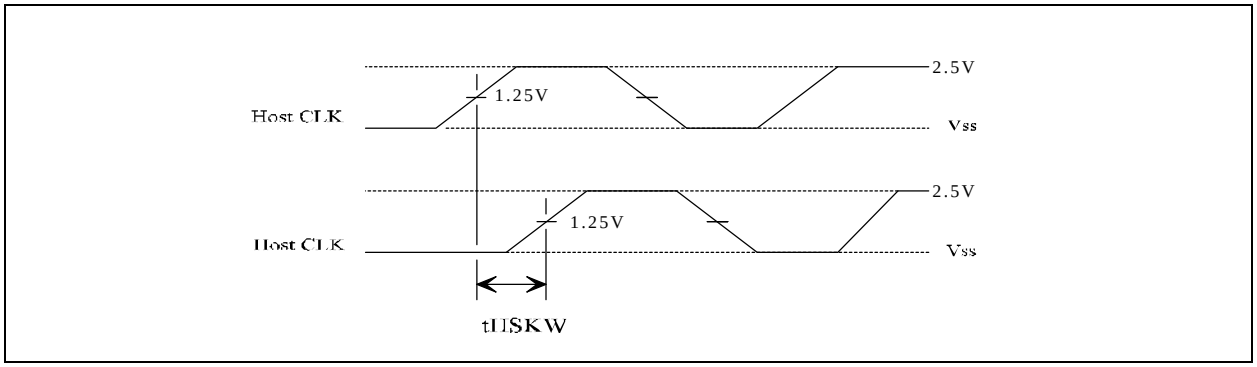


Figure 4-2. Host CLK to Host CLK Skew

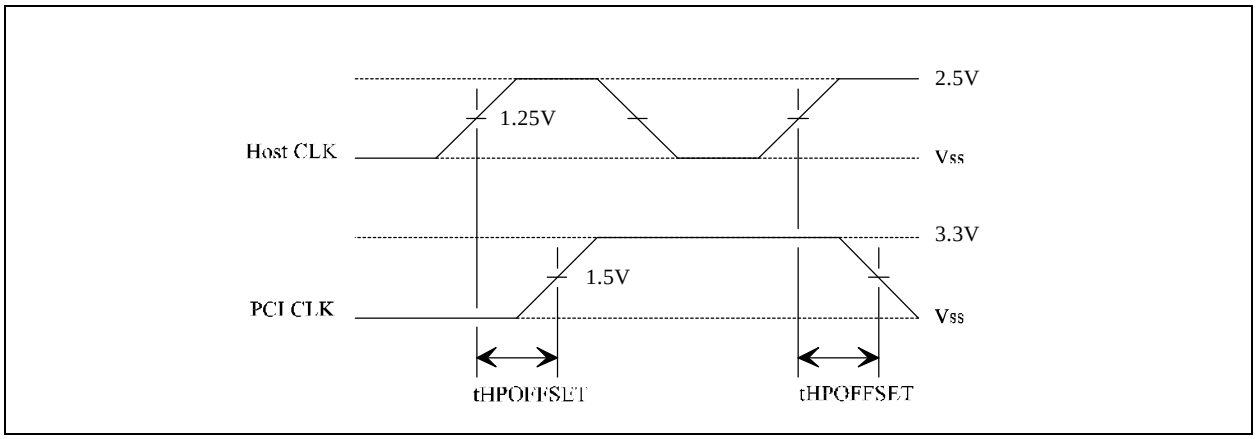


Figure 4-3. Host CLK to PCI CLK Offset

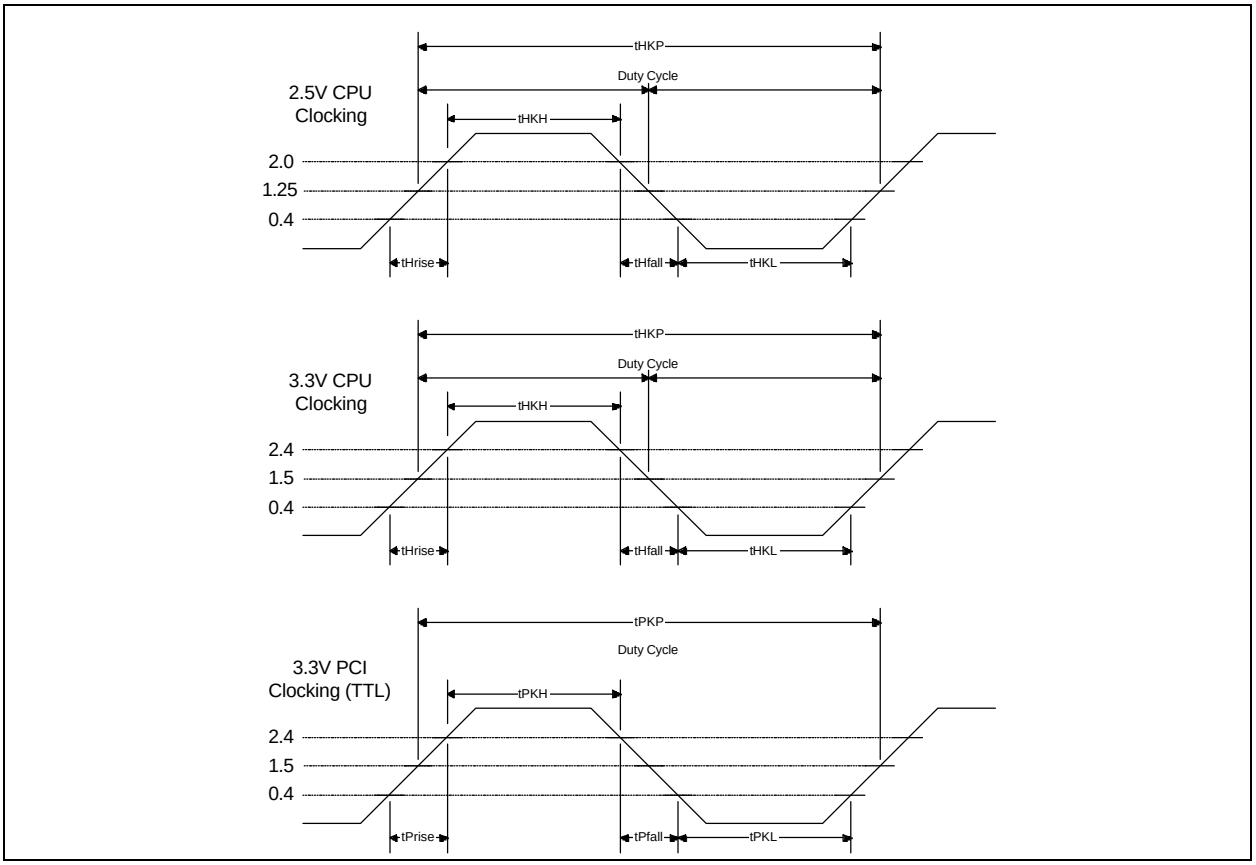


Figure 4-4. Clock Waveform

Table 4-2. Minimum and Maximum Expected Capacitive Loads

Clock	Min Load	Max Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads
PCI Clocks (PCLK)	30	30	pF	Must meet PCI 2.1 requirements
24 MHz	10	20	pF	1 device load
48 MHz	10	20	pF	1 device load
SDRAM	20	30	pF	SDRAM DIMM Spec.
Ref0	20	45	pF	3–4 device loads
Ref1	10	20	pF	1 device load
Ref2	10	20	pF	1 device load
IOAPIC	10	20	pF	2 device load

Notes:

1. Maximum rise/fall times are to be guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are to be guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. Testing may be done with an additional 500 ohm resistor in parallel if properly correlated with the capacitive load.
4. Minimum PCI load of 30 pF is legacy spec from previous clock driver platforms. Does not accurately reflect minimum PCI load.

4.1.3 USBCLK Jitter

In data acquisition or data recovery applications, clock jitter becomes an important system design consideration. The USB specification requires the source jitter for full speed data line to be less than 3.5 ns. This includes the jitter and skew caused by the frequency offset, from the source clock (USBCLK), and from other system variations such as buffer skew, noise effect, crosstalk effect, and loading conditions.

For a robust USB system, the system designer needs to carefully consider the system variations if cycle-to-cycle USBCLK clock jitter is greater than 500 ps or frequency offset+crystal variation is larger than 500 ppm. Choosing a USBCLK with a smaller clock jitter and frequency offset will provide a larger system jitter margin. The source clock jitter can be traded off against the frequency offset in a particular implementation as long as the 3.5ns jitter budget is met.

The amount of the system jitter margin vs. source clock jitter and frequency tolerance is given in Figure 4-5. The system jitter margin is obtained with the following equation.

System Jitter Margin(ns) = Source Data Jitter Budget(ns) - 7x(Frequency Tolerance(ppm)/12,000) - USBCLKJitter(ns)

For example, if clock synthesizers have USBCLK frequency tolerances within 500 ppm and cycle-to-cycle clock jitters within 500ps, the system will have 2.708ns system jitter margin.

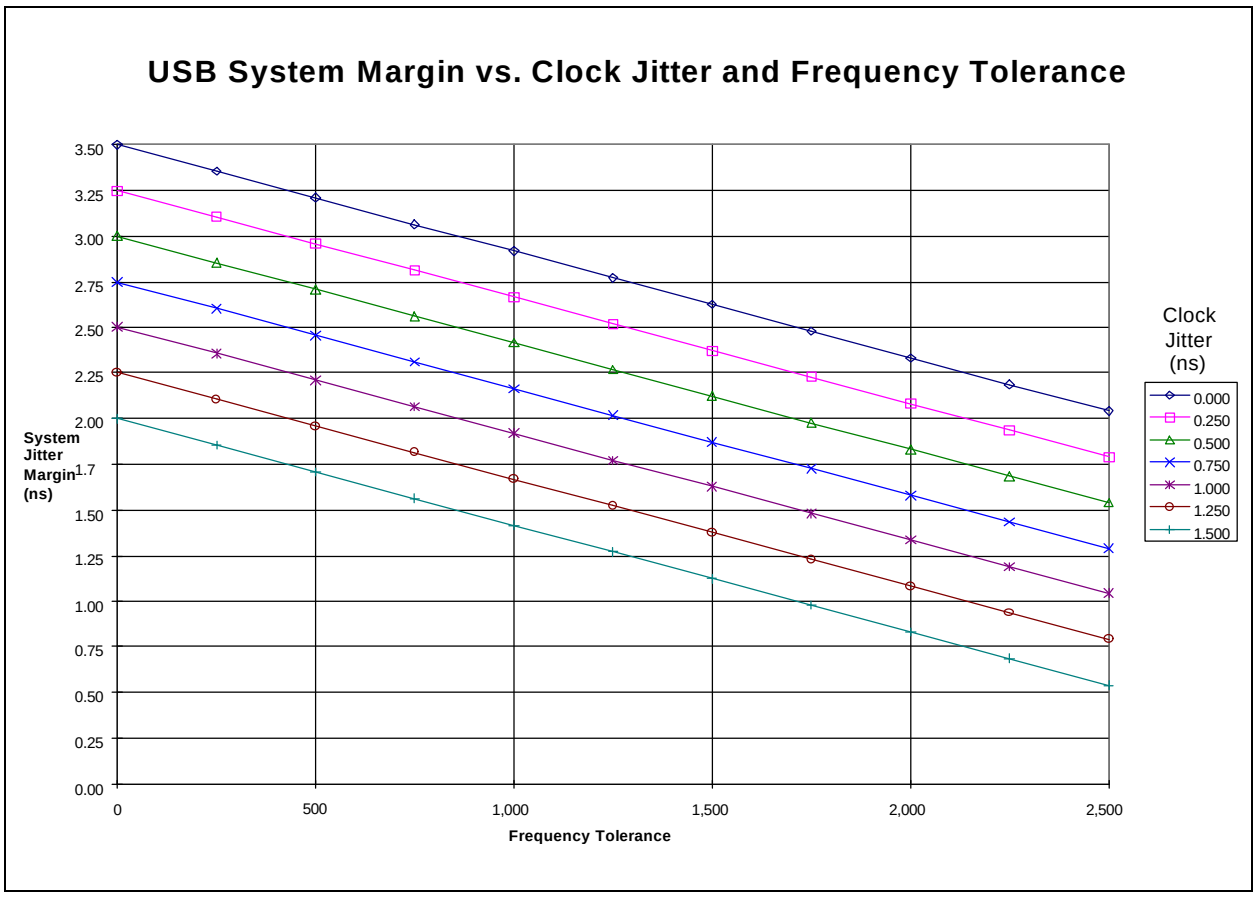


Figure 4-5. System Margin vs. USBCLK Jitter and Frequency Tolerance

4.2 System Considerations

The figures shown below are typical clock driver routing topologies.

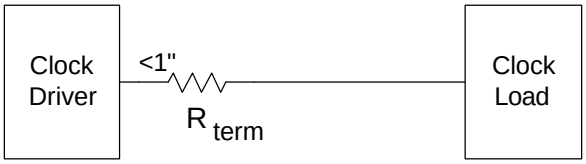


Figure 5.3 Point to Point Route

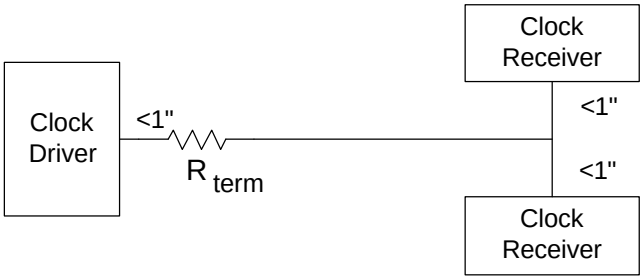


Figure 5.4 Short Stub Route, 2 balanced loads in close proximity, Split at receiver

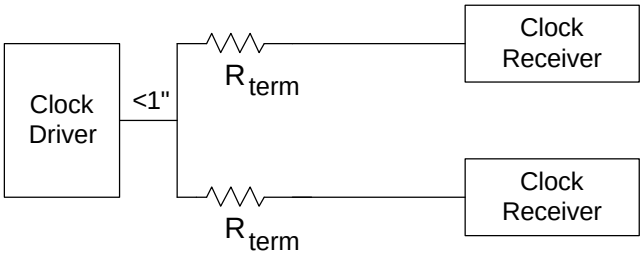


Figure 5.5 Short Stub route, 2 unbalanced loads or large distances, Split at driver

Figure 4-6. Clock Driver Routing Topologies

Notes:

1. Series termination resistors may be required. Selection of layout topologies and buffer drive strength will determine termination requirements (resistor values).
2. Series termination resistors should be placed as close to the driver as possible (within 1 inch).

Table 4-3. Characteristics at Clock Destination

Symbol	Parameter	Min	Max	Units	Notes
V_{ih3}	3.3V Input High Voltage	2.0	V_{DDQ} + .3	V	1
V_{il3}	3.3V Input Low Voltage	-0.3	0.8	V	1
C_{in}	Input Pin Capacitance		6–9	pF	
$C_{insdram}$	SDRAM Input Pin Capacitance	3	5	pF	

Notes:

1. Signal edge is required to be monotonic when transitioning through this region.

4.3 Suggested Pinout Requirements

The following section defines a generic pinout and base requirements for 430TX Reference Platform Designs. This section can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived. Please contact the specific clock synthesizer vendors for their respective decoupling and layout guidelines.

Features (48-Pin Package):

- Four Copies of CPU Clock
- Seven Copies of PCI Clock (Synchronous w/CPU Clock/2)
- One IOAPIC clock @ 14.31818 MHz (power from pin 46)
- Two 48/24-MHz outputs
- Six/eight SDRAM outputs
- Two copies of Ref. Clock @ 14.31818 MHz
- Ref. 14.31818-MHz oscillator input
- Separate 66/60# MHz select pin
- Separate power management mode enable pin
- I2C serial configuration interface
- 3.3/2.5 volt CPU logic input pin
- Power management control input pins
- Package type SSOP: 48 pin

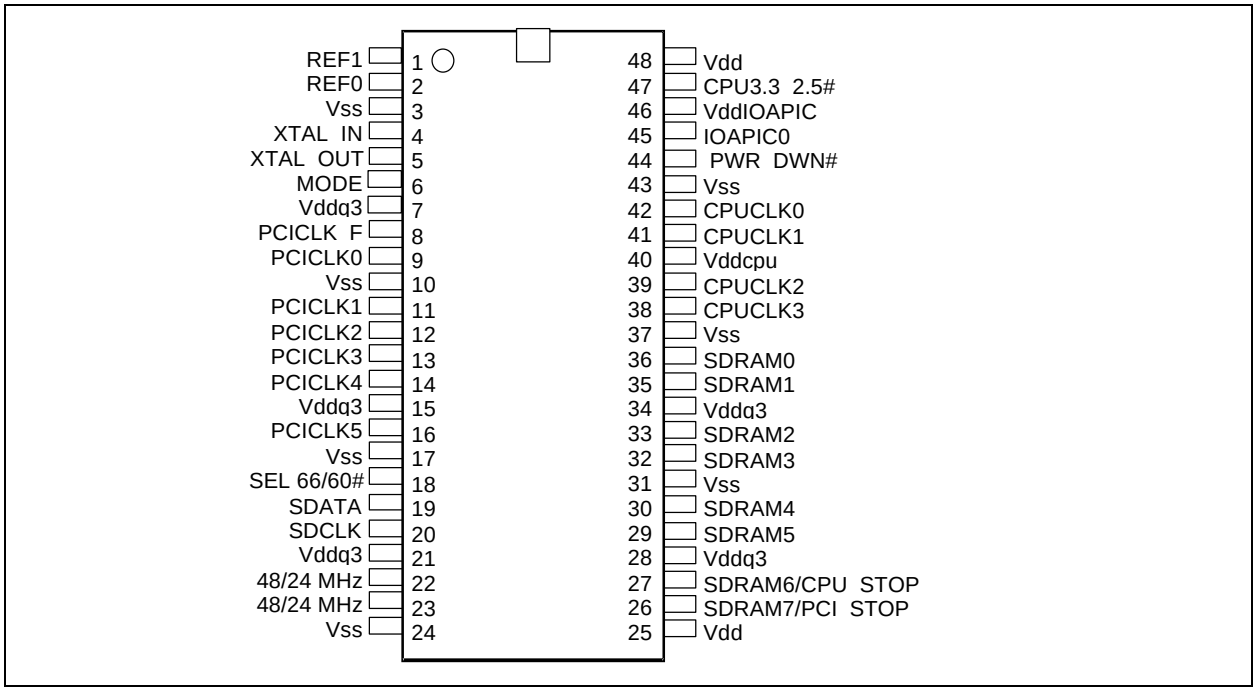


Figure 4-7. Clock Synthesizer

5

Flash Design

5. Flash Design

5.1 Dual-Footprint Flash Design

New features are coming to the PC continue to increase the size of BIOS code, pushing the limits of the 1-Mbit boundary. OEMs have already converted many PC designs to 2-Mbit BIOS and higher, and more will follow.

Since it is difficult to predict when BIOS code will exceed 1 Mbit, OEMs should design motherboards to be flexible. Design in a dual-footprint on the motherboard that accepts both Intel's 1-Mbit flash chips and 2-Mbit boot block chips. This will make the 1M-to-2M transition easier by removing the need for PCB changes to accommodate higher density components.

Intel provides various layout tools to help OEMs design in the dual-footprint. These tools are available from Intel's web site, http://www.intel.com/design/flcomp/devtools/flas4.html, and literature distribution center. Look for Application Note AP-623 "Multi-Site Layout Planning with Intel's Boot Block Flash Memory" (Order #: 292178-002). This document provides detailed information on flexible layouts.

Shown below are three of the reference layouts that Intel furnishes to customers. These layouts are described in AP-623 and are available electronically (Gerber and Postscript formats). Note the small amount of extra board space needed to implement the dual-footprint layouts.

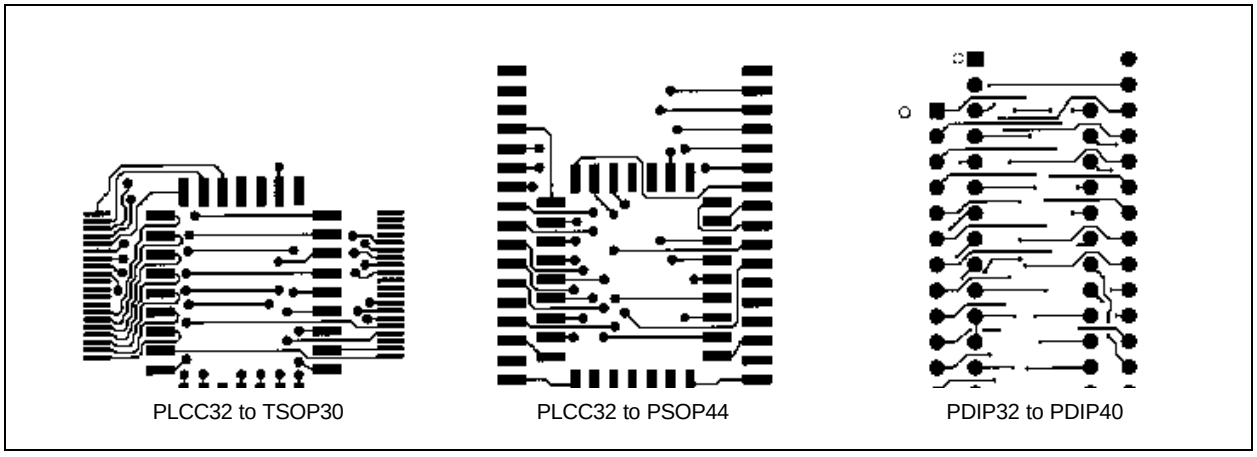


Figure 5-1. Dual Footprint Flash Layouts

5.2 Flash Design Considerations

The Intel's 2-Mbit Flash devices (BX/BL/BV) use an Address Transition Detection (ATD) mechanism to improve their performance. When interfacing Flash devices that employ the ATD mechanism, the designer needs to make sure that the address transition time is not more than 10 ns while CE# is active (low). If the address transition time is more than 10 ns invalid data can result on the data bus. When 2-Mbit Flash devices are interfaced to the ISA bus they can be exposed to address transitions in excess of 10 ns.

5.2.1 Desktop and Mobile

The following are general layout guidelines for using the Intel's boot block flash memories (28F001BX/28F002BC) in the system:

- If adding a switch on V_{PP} for write protection, switch to GND instead of V_{CC}.
- Connect the DU pin of the 2-Mbit devices to ground if anticipating the use of the Intel SmartVoltage boot block flash memory family in the future.
- Use A16 inversion for 1-Mbit devices and A17 inversion for 2-Mbit devices to differentiate between recovery and normal modes.
- Use a 0.01 µf–0.1 µf ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, inherently low inductance capacitors should be placed as close as possible to the package leads.

The following figure illustrates the recommended layout for using Intel's flash devices in desktop design.

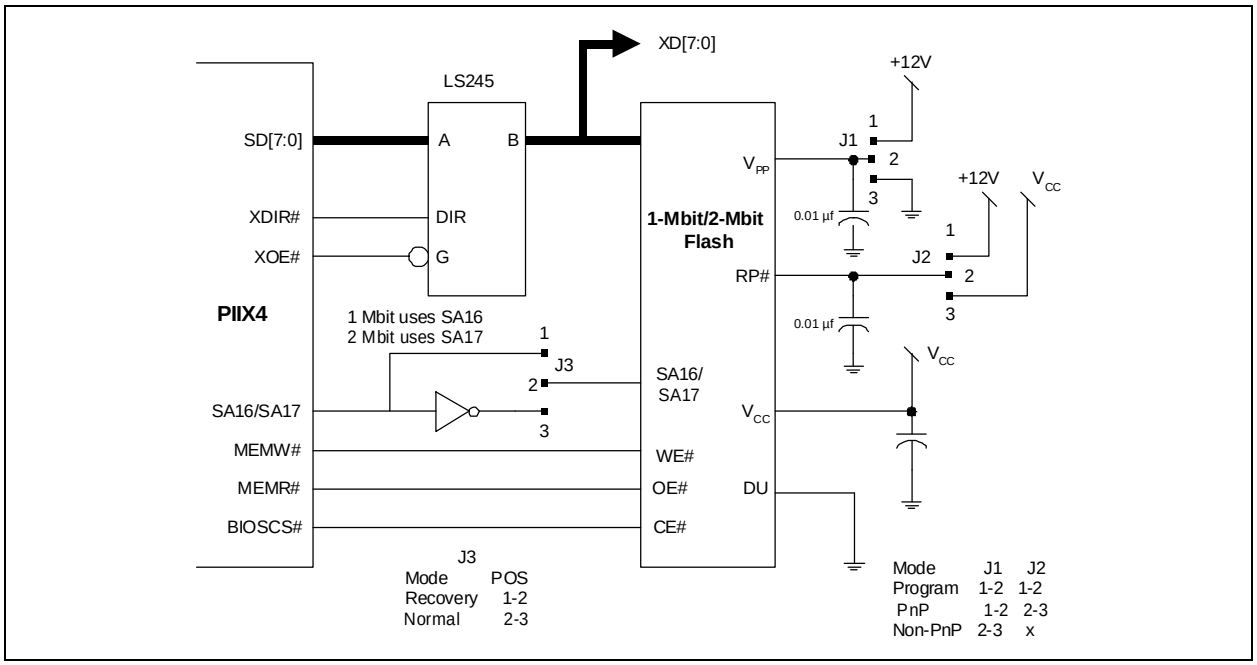


Figure 5-2. Interfacing Flash With PIIX4 (Desktop)

5.2.2 3V/5V Design Considerations (Optional)

The following are general layout guidelines for the Intel's SmartVoltage boot block flash memory (BV) in the 3V/5V design.

- Use 3V/5V program/erase and connect V_{PP} to 3V/5V.
- If adding a switch on V_{PP} for write protection, switch to GND instead of V_{CC}.
- Connect WP# to V_{CC}, GND, or a general purpose output GPO[x] control signal. This pin should not be left floating. WP# pin replaces a DU pin and is used in conjunction with the V_{PP} and RP# pins, as detailed in the table below, to control write protection of the boot block. (WP# pin not available on 8-Mbit 44-lead PSOP. In this package, treat as if the WP# pin is internally tied low, effectively eliminating the last row of the table below.)

Table 5-1. Flash Write Protection Summary

V_{PP}	RP#	WP#	Write Protection
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Block Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

V_{PPLK} is specified at 1.5V(maximum).

V_{IL} is specified at logic low of RP# signal.

V_{IH} is specified at logic high of RP# signal.

V_{HH} is specified at 12V±5%.

- Use SUSA# to drive the SmartVoltage flash into the deep power-down mode when system is in the suspend states.
- Connect BYTE# to GND for byte-wide mode operation if x16 device is used.
- Use a 0.01 µf–0.1 µf ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, inherently low inductance capacitors should be placed as close as possible to the package leads.

The following figure illustrates the recommended layout for Intel's flash devices in mobile or desktop design.

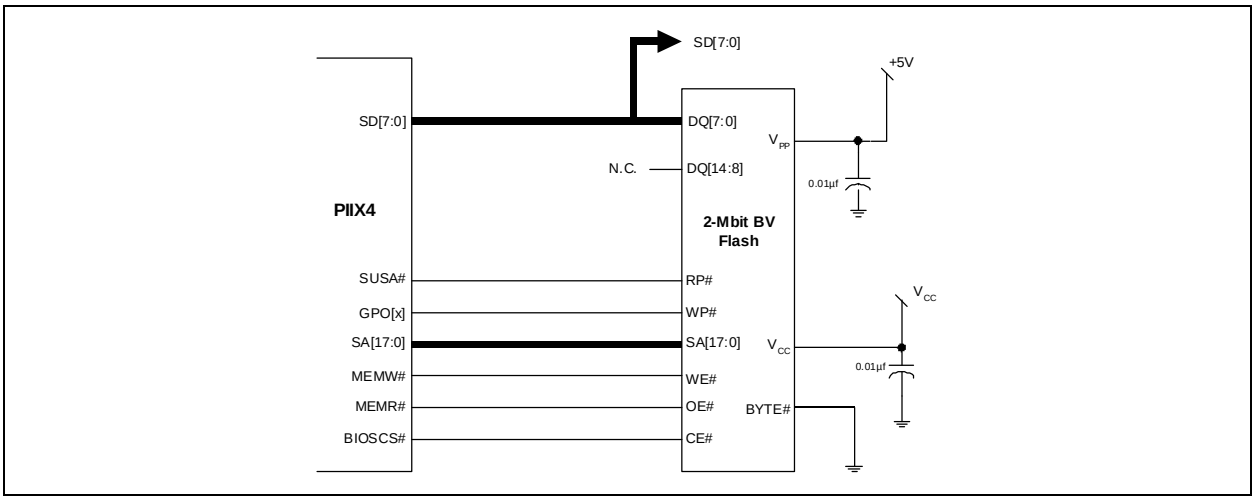


Figure 5-3. Interfacing Flash With PIIX4 (Mobile/Desktop)

6

Customer Reference Board Schematic Overview

CHAPTER 6
CUSTOMER REFERENCE BOARD SCHEMATIC OVERVIEW

6. 430TX PCIset Customer Reference Board Schematic Overview

The 430TX Customer Reference Board is a single Pentium processor, ATX form factor board. The intention of this design is to provide a reference vehicle to showcase the 430TX PCIset features and performance in a desktop environment. The board incorporates a minimum baseline feature set required to meet the current ACPI requirements and Green PC (Energy Star <30W) requirements for the desktop.

This section provides the schematics, jumper settings, and bill of materials for the 430TX customer reference board.

6.1 System Description

The following table summarizes the feature set of the reference design.

Table 6-1. Reference Design Features

Feature Description	ISA UP
ATX form factor	Yes
Number of Board Fab layers	4
Single Pentium processor CPU Socket	Yes
P54C, P54CT and P55C Support	Yes
60, 66 MHz CPU bus frequency support	Yes
P55C VRM connector	No
3V/5V Supplied through Power Connector w/standby voltage and remote off support	Yes
CPU core and I/O voltages supplied through on-board regulator	Yes
Support MTXC	Yes
Support for PIIX4	Yes
Support for external IOAPIC	No
# PCI Slots (Min. 1 Full size slots)	3
# ISA Slots (Min. 2 Full size slots)	2
# Shared PCI/ISA Slots	1
# DIMM Sockets—FPM, EDO, SDRAM	2
# SIMM Sockets—FPM, EDO	0
Support for soldered down 512K	Yes
Support for COAST	No
Support for 3.3V DRAM only	Yes
ACPI Compliant/Ready	Yes

Table 6-1. Reference Design Features (Continued)

Feature Description	ISA UP
I/O Features	
SMC Ultra I/O (with IR support)	Yes
Floppy Disk controller	Yes
1 Parallel Port, 2 Serial Ports	Yes
Real Time Clock with 128-bytes non-volatile CMOS (integrated in PIIX4)	Yes
IDE on motherboard using PIIX4 (2 IDE Headers)—UltraDMA/33 support	Yes
USB Connectors soldered on board	2
Audio on motherboard	No
2-Mbit (256-KB) Flash BIOS with Non-volatile PCI Config storage (Pads for 1M/2M)	Yes
Instant On Button Header	Yes
Keylock, Reset, Speaker, Power State LED	Yes

This section describes some of the features that are unique to the 430TX board that were not present in the 430VX and 430HX boards.

- There is a single clock synthesizer solution that provides all the system clocks including the clocks for the SDRAMs. There are four clocks required per DIMM. This solution supports up to two DIMMs. For specific decoupling and layout recommendations regarding the clock generator, contact the specific clock generator vendors. Care must be given to this area or clock signal integrity issues are likely to arise.
- The L2 cache can be implemented using either two 32Kx32 or two 64Kx32 Pipelined Burst SRAMs. This will result in 256K or 512K cache sizes respectively. The support for DRAM cache is also shown as a build option.
- There are two DIMM connectors shown per the latest JEDEC standard. The DIMMs support Fast Page Mode, EDO and SDRAMs. The memory types can be mixed and matched on a row by row basis. The SMBus logic is also connected to the DIMMs for serial detection of memory parameters.
- The design shows the support for both 1-Mbit and 2-Mbit Flash devices.
- The Real Time Clock (RTC) integrated in the PIIX4 is used in this design. This includes a 256-byte battery backed CMOS SRAM and a Date Alarm.
- The PIIX4 supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. Up to four devices can be supported in Bus Master mode. The PIIX4 contains support for UltraDMA/33 synchronous DMA devices.
- There are two USB ports shown in the design. The PIIX4 contains a USB Host controller that is Universal Host Controller Interface(UHCI) compatible.

Power Button: There is a power button provided for the front panel which interfaces directly to the PIIX4. Pressing the button once will place the system in Sleep State S1 *(implemented to meet Green PC or Energy Star requirements*). Pressing the button for more than 4 seconds will place the system in a Soft-off state S5 *(implemented to meet ACPI requirements*). The PIIX4, on detecting the power button being pressed for more than 4 seconds, will remotely turn the power supply off using the SUSC# signal. In the Soft-off state, there is standby voltage provided by the power supply. This is used to power the Resume well of the PIIX4, RTC and the RSMRST# signal. The RSMRST# connection requires a time delay of 1 millisecond. The standby voltage is assumed to be 5 volts with a minimum trickle current of 10 ma. *Note: APCI compliancy does not require that the power supply be turned off or a power supply with trickle current be used. Soft-off can be implemented by simply turning the CPU clock off via STPCLK#. The reference board implementation is an example of a possible implementation.*

— The following events place the system in Soft-off state: API call, Power Button or RTC Alarm(IRQ8).
— The following events bring the system out of the Soft-off state: Power Button or RTC Alarm(IRQ8).

Green PC Features Sleep state S1 is implemented to meet the Green PC (<30W) requirements for the desktop. This state can be entered by an API call when an idle system is detected, the power button is pressed, or after a programmed delay. In state S1, the PIIX4 can assert STPCLK# to the CPU or the BIOS can do it via a "Stop Grant" instruction. In state S1, the BIOS also turns the monitor and hard disk off. There are means provided in the schematics for the BIOS to turn the CPU fan off also. This is implemented using a general purpose output from the PIIX4. Please note that in state S1 the clocks from the clock synthesizer are not stopped.

— The following events can place the system in sleep state S1: an API call when an idle system is detected, power button, or programmed time.
— The following events bring the system out of the S1 state: Mouse movement, key press, programmed time, power button, phone call.

Power LED: There is a Power LED provided to indicate different system states. A working state is indicated when the LED is on, blinking will indicate Sleep state S1, and off will indicate a Soft-off state.

There are two voltage regulators implemented on the board for the CPU requirements only. All the remaining 3.3V and 5.0V components are powered through the power supply. The core regulator provides either 2.8V or 3.5V depending on the auto-detection of the CPU type. The I/O regulator provides either 3.5V or 3.3V depending upon the auto-detection of the CPU type. The P55C requires 2.8V for core and 3.3V for I/O.

6.2 Power Plane Connections

The following table indicates which power planes the major components are connected to.

Table 6-1. Power Plane Connections

Component	Power Plane	Power Supply Connection	State S1 and On	State S5 (STD/Soff)	Mech Off
CPU:	Core:	2.8V - P55C, 3.3V - P54C CPUVCORE Voltage Regulator	On	Off	Off
	IO:	3.3V CPUVIO Voltage Regulator	On	Off	Off
MTXC:	Main:	3.3V Main Power Supply	On	Off	Off
	CPU:	3.3V Main Power Supply	On	Off	Off
	V_{REF}:	$5V_{REF}$ (5V Main Power Supply)	On	Off	Off
	Suspend:	3.3V Main Power Supply	On	Off	Off
PIIX4:	Main:	3.3V Main Power Supply	On	Off	Off
	Suspend:	3.3V Standby (Power Supply Trickle Current)	On	On	Off
	RTC:	3.3V RTC Battery and Power Supply Trickle Current	On	On	On (RTC Battery)
	USB:	3.3V Main Power Supply	On	Off	Off
DRAM:	Main	3.3V Main Power Supply	On	Off	Off

Table 6-2. Power Plane Connections (Continued)

Component	Power Plane	Power Supply Connection	State S1 and On	State S5 (STD/Soff)	Mech Off
L2	Main	3.3V Main Power Supply	On	Off	Off
Ultra I/O	Main	5V Main Power Supply	On	Off	Off
PCI Bus	Main	5V Main Power Supply	On	Off	Off
ISA Bus	Main	5V Main Power Supply	On	Off	Off

The rest of this section gives a brief description of the logic and components on each page of the 430TX reference schematics.

Sheet 1: Index

This page lists the major active components in the design and the page number where the device is located.

Sheet 2: Processor

A Pentium Processor Socket 7 is shown on this page. Socket 7 is a superset of Socket 5 and supports all 3.3V Pentium processors. This socket also supports the P55C with split power planes and 2.8V required for the P55C core. Bus/Core frequency ratio jumper options are shown on this sheet.

Sheet 3: Clock Synthesizer

This page shows the clock synthesizer. Stuffing options are provided for both IMI652 and IMI671 which includes SMBus support. Please note the MTXC and CPU host clock connection to the same net. This has been done to minimize the host clock skew between the two devices.

Sheet 4, 5: MTXC

The 430TX System Controller is shown on this page. The MTXC is a single-chip host-to-PCI bridge and provides the second level cache control and DRAM control functions. This single chip also provides a 64-bit data path to main memory. The MTXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the MTXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the MTXC also contains read prefetch and posted write buffers.

Sheet 6: Cache and Tag RAM

This page shows the PBSRAMs and tag RAMs. Also located on this page is a table showing the strapping options for the second level cache. The cache memory type must be a pipelined burst SRAM with the global write enable feature. The 430TX PCIset also supports a DRAM cache solution. The implementation for a DRAM cache is shown as a stuffing option.

Sheet 7: Blank

This sheet is intentionally left blank.

Sheet 8, 9: DIMM 0 and DIMM 1

This page shows the DRAM DIMM connectors (0&1). SDRAM, EDO, and FPM DRAM is supported in this design as well as 64-Mbit technology.

Sheet 10: FLASH BIOS

This page shows the Flash BIOS. An optional 2-Mbit stuffing option is shown.

Sheet 11, 12: PIIX4

This page shows the PIIX4. The PIIX4 is a multi-function PCI device implementing a PCI-to-ISA bridge. The PIIX4 also integrates the Universal Serial Bus Controller and IDE Controller.

Sheet 13: PCI IDE Connectors

This page shows the PCI IDE connectors. This IDE implementation supports IDE ATA mode 4 as well as UltraDMA/33.

Sheet 14: Ultra IO

This page shows the Ultra IO which controls the Floppy Disk Connector, two serial ports and one parallel port.

Sheet 15: Parallel Port

Sheet 16: Serial Port, Floppy Connector

Sheet 17: USB Ports

The PIIX4 supports 2 USB ports with overcurrent detection.

Sheet 18: Fan and Front Panel Connectors

Sheet 19: Power Supply

This schematic page shows the control logic for the ATX power supply. It also shows the 3V standby voltage generation circuitry.

Sheet 20, 21: PCI Connectors

Sheet 22, 23, 24: ISA Connectors

Sheet 25: Misc. Pull-ups

Sheet 26: Decoupling Capacitors

Sheet 27: Voltage Regulation

This sheet shows the voltage regulation circuitry for CPUVIO and CPUVCORE. This circuit automatically detects a P55C or P54C processor and outputs the correct CPUVCORE voltage without jumper selection.

Sheet 28: Appendix 1 P28F002BC-T Flash BIOS

This page shows an alternate FLASH BIOS implementation.

Sheet 29: COAST Module

This page shows the implementation of a COAST module.

6.3 Jumpers, Connectors, and Valid Memory Configurations

6.3.1 Jumper Description

Note: Default settings in Bold***Italics*** type

Table 6-3. CPU Clock (Jumper J17, J18)

CPU Clock	Jumper J17 Position	Jumper J18 Position
60 MHz	2-3	2-3
66 MHz	***1-2***	***1-2***

Table 6-4. CPU Clock/Bus Multiplier (Jumper JB1)

CPU Speed	Jumper JB1 Position
2X	***3-5,2-4***
3/2X	1-3,2-4
5/2X	3-5,4-6
3X	1-3,4-6

Table 6-5. System BIOS Mode (Jumper J1, J6, J7)

BIOS Mode	Jumper J1 Position	Jumper J6 Position	Jumper J7 Position
Program Mode	***1-2***	***1-2***	***1-2***
Plug-N-Play	1-2	1-2	2-3
Non Plug-N-Play	1-2	2-3	OUT
Recovery	2-3	x	x

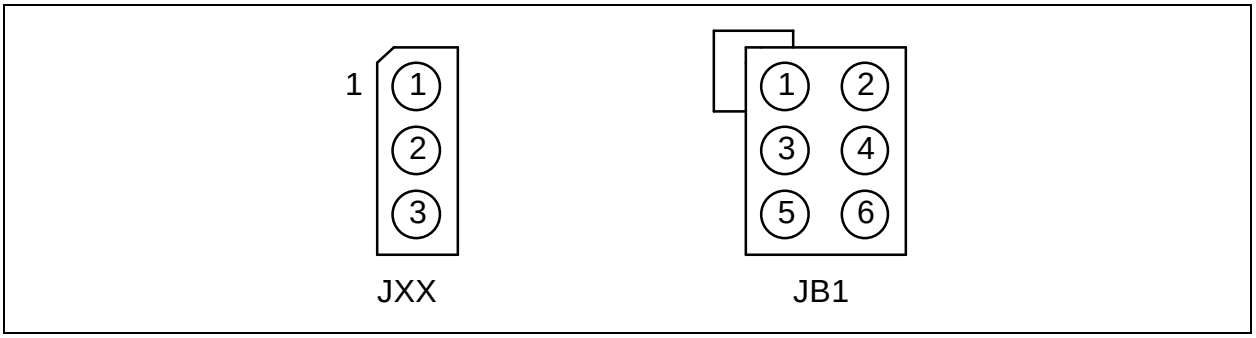
Table 6-6. Battery Source (Jumper J22)

Source	Jumper J22 Position
On-Board	***1-2***
External	OUT

Table 6-7. Speaker Source (Jumper J23)

Voltage	Jumper J23 Position
On-Board	***25-26***
External	OUT

6.3.2 Jumper Header Pin Orientations



6.3.3 Connector Guide

Connector	Function
J2	USB Connectors
J3	Parallel Port Connector
J4	Keyboard and Mouse Connectors
J5	Serial Port Connectors
J8,J9,J10	ISA Slots
J11,J12,J13,J14	PCI Slots
J15	+12V Fan Connector
J16	Power Connector
J19	Floppy Drive Cable Connector
J20	Secondary IDE Cable Connector
J21	Primary IDE Cable Connector
J22	External Battery Connector
J23	Front Panel Connector

6.3.4 Valid Memory Configurations

Bank 0 U5	Bank 1 U6	Total
512Kx64		4M
512Kx64	512Kx64	8M
1Mx64		8M
1Mx64	1Mx64	16M
2Mx64		16M
2Mx64	2Mx64	32M
4Mx64		32M
4Mx64	4Mx64	64M
8Mx64		64M
8Mx64	8Mx64	128M

6.3.5 Stuffing Options

6.3.5.1 Clock Generator Options

Table 6-8. IMISC652 Clock Generator

Remove	Add
U18: IMISC671A clock generator	U18: IMISC652 clock generator
R98: 33Ω resistor	R163: 33Ω resistor
R128: 0Ω resistor	

6.3.5.2 Cache Options

Table 6-9. 256K PBSRAM Cache

Remove	Add
U16: 64Kx32 PBSRAM	U17: 64Kx32 PBSRAM
R54, R59: 4.7 kΩ resistors	R52, R56, R57, R60: 4.7 kΩ resistors
R43: 0Ω resistor	
R112: 0Ω resistor	
R79, R85, R86, R88, R93, R95: 0Ω resistors	
R64: 10 kΩ resistor	
C201, C205: 0.01 µf capacitor	
C208: 3.3 µf capacitor	
C202: 1 µf capacitor	
R98: 1 kΩ resistor	
R78: 10 kΩ resistor	
R80, R87, R92, R94: 0Ω resistor	
C204, C207: 0.01 µf capacitor	
C200: 3.3 µf capacitor	
C209: 1 µf capacitor	

Table 6-10. 512K PBSRAM Cache

Remove	Add
R52, R56, R57, R60: 4.7 kΩ resistors	U16, U17: 64Kx32 PBSRAM
R79, R85, R86, R88, R93, R95: 0Ω resistors	R54, R59: 4.7 kΩ resistors
R64: 10 kΩ resistor	R43: 0Ω resistor
C201, C205: 0.01 µf capacitor	R112: 0Ω resistor
C208: 3.3 µf capacitor	
C202: 1 µf capacitor	
R98: 1 kΩ resistor	
R78: 10 kΩ resistor	
R80, R87, R92, R94: 0Ω resistor	
C204, C207: 0.01 µf capacitor	
C200: 3.3 µf capacitor	
C209: 1 µf capacitor	

Table 6-11. 256K DRAM Cache

Remove	Add
U16, U17: 64Kx32 PBSRAM Cache	U17: 64Kx32 DRAM Cache
R98: 1 kΩ resistor	R79, R85, R86, R88, R93, R95: 0Ω resistors
R78: 10 kΩ resistor	R64: 10 kΩ resistor
R80, R87, R92, R94: 0Ω resistor	C201, C205: 0.01 µf capacitor
C204, C207: 0.01 µf capacitor	C208: 3.3 µf capacitor
C200: 3.3 µf capacitor	C202: 1 µf capacitor
C209: 1 µf capacitor	

Table 6-12. 512K DRAM Cache

Remove	Add
U16, U17: 64Kx32 PBSRAM Cache	U16, U17: 64Kx32 DRAM Cache
	R79, R85, R86, R88, R93, R95: 0Ω resistors
	R64: 10 kΩ resistor
	C201, C205: 0.01 µf capacitor
	C208: 3.3 µf capacitor
	C202: 1 µf capacitor
	R98: 1 kΩ resistor
	R78: 10 kΩ resistor
	R80, R87, R92, R94: 0Ω resistor
	C204, C207: 0.01 µf capacitor
	C200: 3.3 µf capacitor
	C209: 1 µf capacitor

6.3.5.3 Flash Size Options

Table 6-13. 1-Mbit Flash EPROM

Remove	Add
U3: 28F002BC-T	U1: 28F001BX-T
R1: 0Ω resistor	R2: 0Ω resistor
R4: 0Ω resistor	R3: 8.3 kΩ resistor

Table 6-14. 2-Mbit Flash EPROM

Remove	Add
U1: 28F001BX-T	U3: 28F002BC-T
R2: 0Ω resistor	R1: 0Ω resistor
R3: 8.3 kΩ resistor	R4: 0Ω resistor

6.4 Bill of Materials

This section contains a Bill Of Materials (BOM) for 430TX Customer Reference Board.

Table 6-15. Bill Of Materials

Part Number	Package Type	Description	Qty	Reference Design
1N4148SOT23	SOT23	Diode, 1N4148	2	D1, D2
28F002BXTSOP-T120	TSOP40	Flash Mem., 2 Mbit, w/HIGH boot block, 120 nS	1	U3
2N3904SOT23	SOT23	3904 Transistor	2	Q4, Q5
2N7002	SOT23	DMOS FET, 2N7002	1	Q2
32KX8SRAMSN-3V-15	SOJ28	32Kx8 SRAM, 3.3V, (15 ns)	1	U12
6021PB	TH	Heat Sink, stake-on for TO-220	1	HS2
6396B	TH	Heat sink, stake-on, solderable tab for TO-220, 5.6 C/W	1	HS1
64KX32PBSRMPT-8	QFP100	64Kx32 Pipelined Burst SRAM, 8 ns	2	U16, U17
7407S	SOIC14	IC, Hex buffer, open collector	2	U19, U21
74HCT14S	SOIC14	IC, Hex Schmitt trigger inverters	2	U2, U20
82371AB	BGA324	Intel PIIX4 Multifunction PCI to ISA bridge	1	U15
82439TX	BGA324	MTXC System Controller	1	U13
BAT54C	SOT23	Diode, Schottky	2	D3, D4
BT2335C3H	TH	Battery, 300 mAH, 3V Lith, 22.8 mm dia. coin, 3tab	1	BT1
C100CS00ED	SM0603	Cap., cer., 10 pF, 25V, 10%	2	C214, C215
C102CS00EE	SM0603	Cap., cer., 0.001 µf, 25V, 20%	13	C29, C30, C36, C41, C52, C68, C95, C96, C132, C168, C174, C219, C222
C103CS00EM	SM0603	Cap., cer., 0.01 µf, 25V, +80%/-20%	27	C18, C26, C28, C35, C40, C42, C49, C69, C80, C82, C84, C88, C97, C100, C134, C137, C170, C171, C173, C179, C187, C206, C213, C229, C234, C237, C238
C104CS00EM	SM0603	Cap., cer., 0.1 µf, 25V, +80/-20%	42	C1, C2, C3, C7, C8, C9, C17, C19, C21, C22, C25, C27, C31, C32, C33, C34, C37, C39, C43, C44, C45, C46, _C50, C51, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C71, C75, C76, C79, C81, C83, C87

Table 6-16. Bill Of Materials (Continued)

Part Number	Package Type	Description	Qty	Reference Design
C104CS00EM	SM0603	Cap., cer., 0.1 µf, 25V, +80/-20%	35	C92, C93, C94, C98, C99, C101, C102, C105, C106, C107, C108, C109, C110, C111, C116, C117, C119, C120, _C129, C130, C131, C133, C135, C136, C138, C139, C140, C147, C148, C149, C150, C156, C158, C161, C164
C104CS00EM	SM0603	Cap., cer., 0.1 µf, 25V, +80/-20%	34	C165, C166, C169, C172, C176, C177, C180, C181, C182, C183, C184, C186, C188, C189, C190, C191, C193, _C194, C195, C198, C199, C203, C210, C211, C212, C217, C218, C221, C223, C226, C227, C231, C232, C242
C104CS00EM	SM0603	Cap., cer., 0.1 µf, 25V, +80/-20%	19	C243, C248, C249, C250, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, _C272, C273
C105CS02EM	SM1206	Cap., cer., 1.0 µf, 25V, +80/-20%	28	C72, C103, C104, C112, C113, C114, C115, C118, C121, C122, C123, C124, C127, C128, C141, C142, C143, _C144, C145, C146, C151, C152, C153, C154, C155, C157, C167, C192
C106TS03DE	SM6032	Cap., tant., 10 µf, 16V, 20%	17	C4, C5, C6, C11, C12, C23, C38, C47, C48, C86, C89, C90, C125, C175, C178, C185, C230
C107TS05CE-LE	SM7343H	Cap., tant., 100 µf, 10V, 20%, .125 ESR	1	C91
C157TS05CE	SM7343	Cap., tant., 150 µf, 10V, 20%	2	C10, C20
C220CS00ED	SM0603	Cap., cer., 22 pF, 25V, 10%	2	C78, C85
C224CS01EM	SM0805	Cap., cer., 0.22 µf, 25V, +80/-20%	2	C220, C225
C226TS03CE	SM6032	Cap., tant., 22 µf, 10V, 20%	1	C74

Table 6-17. Bill Of Materials (Continued)

Part Number	Package Type	Description	Qty	Reference Design
C227TS05CE-LE	SM7343H	Cap., tant., 220 µf, 10V, 20%, .125 ESR	8	C53, C54, C55, C73, C77, C126, C270, C271
C334CS01EM	SM0805	Cap., cer., 0.33 µf, 25V, +80/-20%	2	C67, C70
C471CS00EE	SM0603	Cap., cer., 470 pF, 25V, 20%	5	C13, C14, C15, C16, C24
C476ES09BE	SM4mm	Cap., elec., 47 µf, 6V, 20%	1	C216
C476TS03BE	SM6032	Cap., tant., 47 µf, 6V, 20%	1	C216
C500CS00ED	SM0603	Cap., cer., 50 pF, 25V, 10%	4	C159, C160, C162, C163
CI101CS09ED	SM3216	Cap. array, cer., 100 pFx4, 25V, 10%	4	CP6, CP7, CP8, CP9
CI181CS09ED	SM3216	Cap. array, cer., 180 pFx4, 25V, 10%	5	CP1, CP2, CP3, CP4, CP5
CN120ED05B	TH	Conn., 120 pin, PCI	4	J11, J12, J13, J14
CN12MDKFP10B	TH	Conn., Dual 6-pin mini DIN, Stacked	1	J4
CN18DBKMP10BA	TH	Conn., dual 9-pin male d-shell, stacked, AMP	1	J5
CN20MF17C	TH	Conn., 20 pin, mini fit	1	J16
CN25DBFP10B	TH	Conn., 25 pin, female d-shell, w/hex screws installed	1	J3
CN8US09B	TH	Conn., 8 pin, USB right angle, stacked	1	J2
CN98ED10B	TH	Conn., 98-pin card edge	3	J8, J9, J10
CNK18BGSR10B2	TH	Conn., 26x1, RA, key pin 5, 7, 11, 13, 16, 18, 20, 24	1	J23
CNK33SH10B	TH	Conn., 17x2 pin header; key pin 5, shrouded	1	J19
CNK39SH10B	TH	Conn., 20x2 pin header; key pin 20, shrouded	2	J20, J21
CNK3BGS10BA	TH	Conn., 4x1 pin header; key pin 3	1	J22
FBS01K	SM0805	Ferrite bead (ACT material K)	5	L7, L8, L9, L10, L11
FBS01L	SM0805	Ferrite bead (ACT material L)	2	L3, L13
FBS04B	SM1812	Ferrite bead (ACT material B), 300 mA	6	L1, L2, L4, L5, L6, L12
FDC37C932FR	QFP160	SMC, Fast IR Ultra I/O w/AMI K.B. BIOS	1	U10
FUSEP1253S09D	SM9466	Poly Fuse 1.25A hold, 15V	3	F1, F2, F3
GD75232SOP	SOP20	RS 232 Transceiver 5 receivers, 3 drivers	2	U4, U8
HY-05	TH	mini. PC mount speaker (HYCOM)	1	BZ1

Table 6-18. Bill Of Materials (Continued)

Part Number	Package Type	Description	Qty	Reference Design
IMISC652	SSOP48	System clock generator with SDRAM outputs	1	U18
INSILPAD-TO220	TO-220	Silicone insulator w/thermally conductive filters	2	HS1, HS2
JB3	TH	3x2 pin header connector	1	JB1
JP2	TH	2x1 pin header connector	1	J15
JP3	TH	3x1 pin header connector	5	J1, J6, J7, J17, J18
LOCKNUT-4-40	HDWR	4-40 Locknut	2	HS1, HS2
LT1006S	SOP8	Precision, Single supply OP AMP	1	U7
LT1580CTO220V	TO220V-5	Very low dropout regulator	1	U11
LT1587CTO220V	TO-220V	Low drop-out, 3 amp, variable voltage regulator	1	U9
MMBZ5226BLSOT23	SOT23	Zener diode, 5226	1	D5
PCB		Printed Circuit Board	1	PCB1
R0000CS00SC	SM0603	Res., 0Ω, 5%, 1/16W	8	R1, R15, R18, R25, R42, R43, R112, R123
R0020CS00SA	SM0603	Res., 2Ω, 1%, 1/16W	1	R37
R0100CS00SC	SM0603	Res., 10Ω, 5%, 1/16W	12	R47, R48, R62, R63, R66, R67, R107, R113, R156, R157, R158, R159
R0220CS00SC	SM0603	Res., 22Ω, 5%, 1/16W	9	R114, R121, R122, R125, R129, R130, R131, R132, R133
R0330CS00SC	SM0603	Res., 33Ω, 5%, 1/16W	17	R68, R69, R70, R71, R76, R100, R102, R104, R105, R108, R109, R110, R111, R120, R154, R155, R163
R0470CS00SC	SM0603	Res., 47Ω, 5%, 1/16W	6	R96, R101, R124, R147, R150, R152
R0680CS01EC	SM1206	Res., 68Ω, 5%, 1/8W	2	R137, R139
R1000CS00SC	SM0603	Res., 100Ω, 5%, 1/16W	3	R50, R51, R116
R1001CS00SC	SM0603	Res., 1 kΩ, 5%, 1/16W	13	R14, R19, R21, R22, R23, R73, R75, R77, R99, R151, R153, R161, R165
R1002CS00SC	SM0603	Res., 10 kΩ, 5%, 1/16W	12	R24, R30, R31, R45, R65, R82, R91, R140, R141, R160, R164, R166
R1004CS00SC	SM0603	Res., 1 mΩ, 5%, 1/16W	1	R40
R1070CS00SA	SM0603	Res., 107Ω, 1%, 1/16W	1	R36

Table 6-19. Bill Of Materials (Continued)

Part Number	Package Type	Description	Qty	Reference Design
R1100CS00SC	SM0603	Res., 110Ω, 5%, 1/16W	1	R28
R1502CS00SC	SM0603	Res., 15 kΩ, 5%, 1/16W	4	R5, R6, R7, R8
R1780CS00SA	SM0603	Res., 178Ω, 1%, 1/16W	1	R27
R1910CS00SA	SM0603	Res., 191Ω, 1%, 1/16W	1	R26
R2200CS00SC	SM0603	Res., 220Ω, 5%, 1/16W	8	R32, R33, R34, R38, R72, R97, R142, R143
R2201CS00SC	SM0603	Res., 2.2 kΩ, 5%, 1/16W	1	R127
R2202CS00SC	SM0603	Res., 22 kΩ, 5%, 1/16W	1	R49
R3300CS00SC	SM0603	Res., 330Ω, 5%, 1/16W	5	R39, R53, R55, R58, R61
R3304CS00SC	SM0603	Res., 3.3 mΩ, 5%, 1/16W	1	R162
R3900CS00SC	SM0603	Res., 390Ω, 5%, 1/16W	1	R145
R4320CS00SA	SM0603	Res., 432Ω, 1%, 1/16W	1	R35
R4700CS00SC	SM0603	Res., 470Ω, 5%, 1/16W	3	R29, R148, R149
R4701CS00SC	SM0603	Res., 4.7 kΩ, 5%, 1/16W	8	R20, R46, R54, R56, R57, R59, R74, R119
R4703CS00SC	SM0603	Res., 470 kΩ, 5%, 1/16W	2	R10, R11
R5103CS00SC	SM0603	Res., 510 kΩ, 5%, 1/16W	1	R144
R5601CS00SC	SM0603	Res., 5.6 kΩ, 5%, 1/16W	2	R84, R90
R5603CS00SC	SM0603	Res., 560 kΩ, 5%, 1/16W	2	R12, R13
R8201CS00SC	SM0603	Res., 8.2 kΩ, 5%, 1/16W	7	R3, R9, R81, R103, R106, R117, R118
RI100S09SC	SM3216	Res.Block, 10Ωx4, iso., 5%, 1/16W	5	RP29, RP34, RP69, RP71, RP72
RI102S09SC	SM3216	Res.Block, 1 kΩx4, iso., 5%, 1/16W	7	RP1, RP2, RP3, RP4, RP6, RP18, RP44
RI103S09SC	SM3216	Res.Block, 10 kΩx4, iso., 5%, 1/16W	22	RP5, RP7, RP11, RP13, RP14, RP17, RP19, RP22, RP24, RP25, RP26, RP28, RP33, RP36, RP39, RP42, RP45, _RP47, RP48, RP49, RP55, RP67
RI272S09SC	SM3216	Res.Block, 2.7 kΩx4, iso., 5%, 1/16W	6	RP9, RP30, RP31, RP37, RP40, RP41
RI330S09SC	SM3216	Res.Block, 33Ωx4, iso., 5%, 1/16W	16	RP10, RP12, RP15, RP50, RP51, RP52, RP53, RP54, RP56, RP57, RP59, RP60, RP61, RP63, RP64, RP65
RI331S09SC	SM3216	Res.Block, 330Ωx4, iso., 5%, 1/16W	2	RP8, RP27

Table 6-20. Bill Of Materials (Continued)

Part Number	Package Type	Description	Qty	Reference Design
RI472S09SC	SM3216	Res.Block, 4.7 kΩx4, iso., 5%, 1/16W	7	RP20, RP21, RP23, RP32, RP35, RP38, RP43
RI562S09SC	SM3216	Res.Block, 5.6 kΩx4, iso., 5%, 1/16W	2	RP16, RP46
RI822S09SC	SM3216	Res.Block, 8.2 kΩx4, iso., 5%, 1/16W	5	RP58, RP62, RP66, RP68, RP70
SCREW-4-40	HDWR	4-40 Panhead Screw, 1/3"	2	HS1, HS2
SHUNTS		Jumper shunts	5	J1, J6, J7, J17, J18
SI9933DYS	SOP8	Dual P-Channel Enhancement-Mode MOSFET	1	Q1
SK168DIMVLTB	TH	Socket, 168-pin Dimm, unbuffered, 3V, w/tabs	2	U5, U6
SK321PGAZIF	PGA321	ZIF Socket for Pentium® (socket 7)	1	U14
SK40TSO	TSOP40	Socket, 40 pin, TSOP	1	U3
Y14318186B2G-18	TH	Crystal, 14.31818 MHz, ATS-49 pkg, 18 pF, 20 ppm	1	Y3
Y32768003B2F-12	TH	Xtal, 32.768 KHz, 12.5 pF, 20 ppm	1	Y1
ZVN4206SOT223	SOT223	MOSFET	1	Q3