

FEATURES

- A single chip JPEG processor which integrates all the modules needed for JPEG encoding and decoding:
 - ⇒ Raster to block and block to raster conversion
 - ⇒ Strip buffer
 - ⇒ JPEG encoder/decoder
- Two speed grades available: 27 MHz for CCIR resolutions and 30 MHz for Square pixel resolutions.
- Motion video compression/expansion capability of up to 25 frames/sec square pixel PAL and up to 30 frames/sec CCIR NTSC
- Three modes of Bit Rate Control (BRC):
 - ⇒ Still images- guarantees file size close to and below a prescribed value.
 - ⇒ Motion video- keeps the file size approximately fixed.
 - ⇒ No BRC- uses fixed quantization tables.
- Glue-less interface to common video decoders (e.g., Philips, Brooktree, ITT, Samsung)
- Supports video interface of 8 and 16 bits YUV 4:2:2
- Support for master and slave video synchronization
- Pixel enables function to support non-contiguous transfer of pixels (e.g. for still operation).
- Flexible, cost effective interface to a variety of host controllers ranging from the dedicated high performance ZR36067 to a generic low-cost MCU:
 - ⇒ 8 bits master supports transfer of up to 30 Mbytes/sec.
 - ⇒ 16 bits slave supports transfer of up to 16.7 Mbytes/sec.
 - ⇒ 8 bits slave supports transfer of up to 8.3 Mbytes/sec.
- On chip video processing including:
 - ⇒ Support for mixing of two video sources
 - ⇒ Up/down horizontal and vertical scaling of 1:2 & 1:4
 - ⇒ Support for cropping and programmable background color
- 3.3V power supply with 5V tolerant I/O
- Low power consumption
 - ⇒ 850 mW at 30 MHz operating frequency
 - ⇒ Power down (sleep) mode for very low power consumption (<20mW).
- 100 pin PQFP package

APPLICATIONS

- Desk-top video editing sub-systems
- Security and industrial surveillance
- Full-motion video capture
- Digital still cameras
- JPEG based video conferencing systems

DESCRIPTION

The ZR36060 is an integrated JPEG codec targeted to video capture and editing applications in desktop and laptop computers. It integrates the functionality of a JPEG codec (e.g., the ZR36050), a Raster-to-Block (e.g., the ZR36015) and the strip buffer (32Kx8 SRAM), as well as additional functionality into a single device. The ZR36060 is based on the field proven fully compliant Zoran JPEG devices. It incorporates the patented Zoran Bit Rate Control (BRC) mechanism to maintain a constant bit rate. In compression the ZR36060 captures digital video (YUV 4:2:2 format), optionally performs cropping and down scaling on it, encodes it into Baseline JPEG bit-stream, and outputs the compressed data to a host controller. In decompression it receives JPEG compressed data, decodes it back to YUV 4:2:2 video format, up-scales it if needed, and outputs the reconstructed video to the video encoder. The ZR36060 provides both in compression and expansion, hardware support for mixing two rectangular areas of video into a unified video stream. The ZR36060 video interface can operate as a sync master or slave, in 8-bit or 16-bit YUV 4:2:2. This flexibility makes it compatible with a large variety of video decoders and

encoders. Support for non-contiguous transfer of pixels makes the ZR36060 applicable for still picture applications. The code interface of the ZR36060 can be either 8-bit master, 8- or 16-bit slave. The ZR36060 can cost-effectively interface a variety of host controllers, ranging from the dedicated, high performance ZR36067 PCI controller to generic, low cost micro-controllers. The ZR36060 is a CMOS device that requires a 3.3V power supply. It can be connected to 3V or 5V signal level devices (the ZR36060 inputs are 5V tolerant). A power-down ("SLEEP") mode limits the current consumption of the ZR36060 to 20mA. When active, the current consumption is limited to 260mA. This makes the ZR36060 compliant with PCMCIA and CardBus restrictions.

Reference Designs

- Video Inlet - USB Video Capture Peripheral (see fig. 1)
- Instant Replay (H33)- Integrated PCI-based Video Capture Editing Board (see fig. 2)

Figure 1. Block Diagram of a USB video capture peripheral using the ZR36060

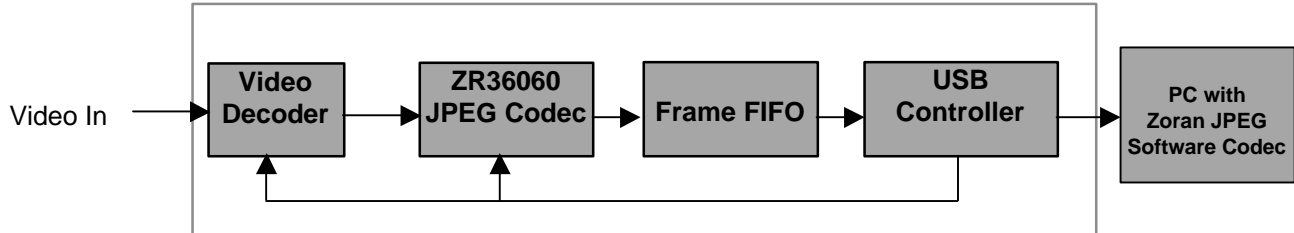
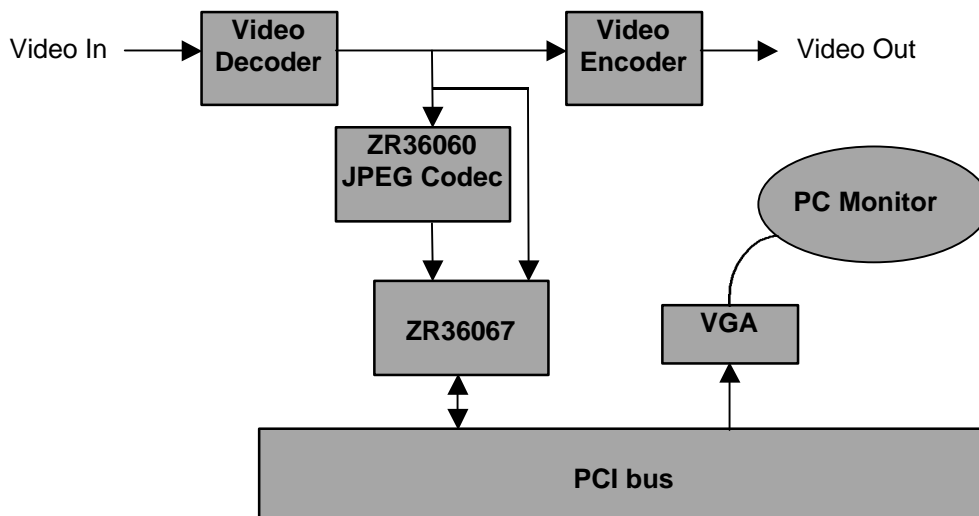


Figure 2: Block Diagram of a desktop video editing system using the ZR36060



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