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WINBOND I/O

GENERAL DESCRIPTION

The W83877AF is an enhanced version from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, IDE interface, configurable plug-and-play registers for the whole chip --- adding powerful features: IrDA 1.1 (MIR for 1.152M bps or FIR for 4M bps), TV remote IR. In addition to the function enhancement, W83877AF is pin-to-pin compatible to W83877F.

The disk drive adapter functions of the W83877AF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, interrupt and DMA logic. The wide range of functions integrated onto the W83877AF greatly reduces the number of components required for interfacing with floppy disk drives. The W83877AF supports up to 4 Three-mode Floppy Disk Drives (FDD) of formats 360K, 720K, 1.2M, 1.44M, or 2.88M, and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83877AF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. One of UART supports infrared (IR) includes 32-byte FIFO, serial IR (115,200 bps), MIR (1.152M bps or 0.576M bps), FIR (4M bps), and TV remote IR (supported NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83877AF supports one PC-compatible printer port (SPP), bi-directional Printer Port (BPP), and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be attached. Especially in the application of notebook computer, this feature is very useful.

The Extension Adapter Mode of the W83877AF also allows pocket devices to be installed through the printer interface pins in notebook computer applications according to a protocol set by Winbond, but with upgraded performance. The JOYSTICK mode allows a joystick to be connected to a parallel port with a signal switching cable.

The W83877AF supports two embedded hard disk drive (IDE AT bus) interfaces and a game port with decoded read/write output.

The configuration registers support mode selection, function enable/disable, and power down function selection. Moreover, the configurable PnP registers are compatible with the plug-and-play feature in Windows 95™, which makes system resource allocation more efficient than ever.

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FEATURES

General:

- Plug & Play 1.0A Compliant
- Support 8 IRQs, 4 DMA channels, 480 re-locatable addresses

FDC:

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track select-able capability
- DMA enable logic
- Supports floppy disk drives and tape drives
- Detects all over-run and under-run conditions
- Data rate and drive control registers
- Built-in address mark detection circuit to simplify the read electronics
- IBM PC system address decoder
- 24 MHz crystal input (48 Mhz when for 2 Mbps fast tape drive)
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Supports up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077/ 765A
- Supports 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Supports perpendicular recording format

  Support 3-mode FDD, and its Win95 driver
- 16-byte data FIFOs

UART:

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - 5, 6, 7 or 8-bit characters
  - Even, odd or no parity bit generation/detection
  - 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate is up to 911.6 (8 times of 115.2K bps) for 1.8461M Hz and 1.5M bps for 24M Hz

Infrared:

- Supports IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Supports SHARP ASK-IR protocol with maximum baud rate up to 57600 bps
- Supports IrDA version 1.1 MIR (1.152M bps) and FIR (4M bps) protocol
  - Two DMA channel for transmitter and receiver
  - 32-byte FIFO is supported in the TX/RX terminal
  - 8-byte status FIFO is supported to store received frame status (such as overrun, CRC error, etc.)
- Supports auto-config SIR and FIR

Parallel Port:

- Compatible with IBM parallel port
- Supports parallel port with bi-directional lines
- Supports Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Supports Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Extension Adapter Mode supports pocket devices through parallel port
- JOYSTICK mode supports joystick through parallel port

IDE:

- Supports up to two embedded hard disk drives (IDE AT BUS)

Others:

- Programmable configuration settings
- Immediate or automatic power-down mode for power management
- All hardware power-on settings have internal pull-up or pull-down resistors as default value

Package:

- 100-pin QFP (W83877AF), and 100-pin TQFP (W83877AD)

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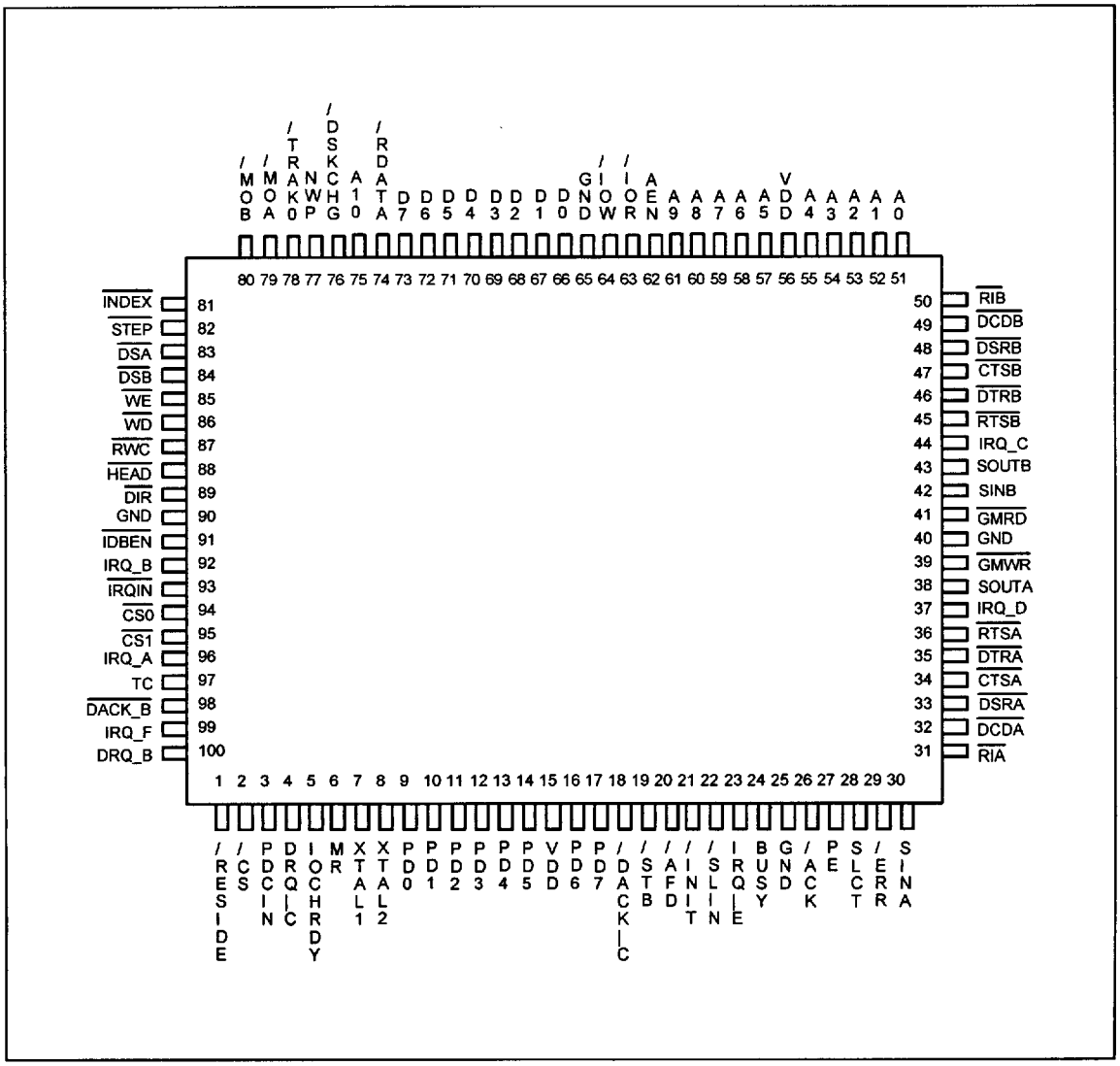
1. PIN CONFIGURATION



1.0 PIN DESCRIPTION

(Note: Refer to section 9.2 DC CHARACTERISTICS for details.)

I/O8tc - TTL level output pin with 8 mA source-sink capability; CMOS level input voltage

I/O12t - TTL level bi-directional pin with 12 mA source-sink capability

I/O24t - TTL level bi-directional pin with 24 mA source-sink capability

OUT8t - TTL level output pin with 8 mA source-sink capability

OUT12t - TTL level output pin with 12 mA source-sink capability

OD12 - Open-drain output pin with 12 mA sink capability

OD24 - Open-drain output pin with 24 mA sink capability

INt - TTL level input pin

INts - TTL level Schmitt-triggered input pin

INc - CMOS level input pin

INcs - CMOS level Schmitt-triggered input pin

1.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
D0–D7	66-73	I/O_{24t}	System data bus bits 0-7
A0–A9	51-55 57-61	IN_t	System address bus bits 0-9
A10	75	IN_t	In ECP Mode, this pin is the A10 address input.
IOCHRDY	5	OD_{24}	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	6	IN_{ts}	Master Reset. Active high. MR is low during normal operations.
$\overline{CS}$	2	IN_t	Active low chip select signal.
$\overline{DACK\_N}$		IN_t	DMA acknowledge signal D.
IRSL1		OUT_{12t}	IR module mode select 1.
IRSL2		OUT_{12t}	IR module mode select 2.
AEN	62	IN_t	System address bus enable
$\overline{IOR}$	63	IN_{ts}	CPU I/O read signal
$\overline{IOW}$	64	IN_{ts}	CPU I/O write signal
DRQ_B	100	OUT_{12t}	DMA request signal B
$\overline{DACK\_B}$	98	IN_{ts}	DMA Acknowledge signal B
DRQ_C	4	OUT_{12t}	DMA request signal C
$\overline{DACK\_C}$	18	IN_{ts}	DMA Acknowledge signal C

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
TC	97	IN_{ts}	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQIN	93	IN_t	Interrupt request input.
DRQ_D		OUT_{12t}	DMA request signal D.
IRSL2		OUT_{12t}	IR module mode selection 2.
IRRXH/IRSL0		I/O_{12t}	When input, act as a function of high speed IR receiving terminal. When output selected, act as a IR module mode selection 0.
IRQ_A	96	OUT_{12t}	When CR16 Bit 4 (GOIQSEL) = 0: Interrupt request signal A;
GIO1		I/O_{12t}	When CR16 Bit 4 (GOIQSEL) = 1: General Purpose I/O port 1.
IRQ_B	92	OUT_{12t}	When CR16 Bit 4 (GOIQSEL) = 0: Interrupt request signal B;
GIO0		I/O_{12t}	When CR16 Bit 4 (GOIQSEL) = 1: General Purpose I/O port 0.
IRQ_C	44	OUT_{12t}	Interrupt request signal C
IRQ_D	37	OUT_{12t}	Interrupt request signal D
IRQ_E	23	OUT_{12t}	Interrupt request signal E
IRQ_F	99	OUT_{12t}	Interrupt request signal F
XTAL1	7	CLK IN	XTAL oscillator input
XTAL2	8	CLK OUT	XTAL oscillator output

1.2 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{CTSA}$	34	IN_t	Clear To Send is the modem control input.
$\overline{CTSB}$	47	IN_t	The function of these pins can be tested by reading Bit 4 of the handshake status register.
$\overline{DSRA}$	33	IN_t	Data Set Ready. An active low indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{DSRB}$	48	IN_t	
$\overline{DCDA}$	32	IN_t	Data Carrier Detect. An active low indicates the modem or data set has detected a data carrier.
$\overline{DCDB}$	49	IN_t	
$\overline{RIA}$	31	IN_t	Ring Indicator. An active low indicates that a ring signal is being received by the modem or data set.
$\overline{RIB}$	50	IN_t	

1.2 Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
SINA SINB/IRRX1	30 42	IN_t IN_t	Serial Input. Used to receive serial data from the communication link.
SOUTA PIN2IPSEL	38	O_{8tc} I_{8tc}	UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled up internally and is defined as PIN2IPSEL, which provides the power-on value for CR16 bit 1 (PIN2IPSEL). A 4.7 kΩ is recommended when intends to pull down at power-on reset.
SOUTB IRTX1 PGMDRQ	43	O_{8tc} O_{8tc} I_{8tc}	UART B Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PGMDRQ, which provides the power-on value for CR16 bit 3 (GMDRQ). A 4.7 kΩ is recommended when intends to pull up at power-on reset.
$\overline{\text{DTRA}}$ PHEFRAS	35	O_{8tc} I_{8tc}	UART A Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PHEFRAS, which provides the power-on value for CR16 bit 0 (HEFRAS). A 4.7 kΩ is recommended when intends to pull up at power-on reset.
$\overline{\text{DTRB}}$	46	O_{8t}	UART B Data Terminal Ready. An active low informs the modem or data set that controller is ready to communicate.
$\overline{\text{RTSA}}$ PPNPCVS	36	O_{8tc} I_{8tc}	UART A Request To Send. An active low informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled up internally and is defined as PPNPCVS, which provides the power-on value for CR16 bit 2 (PNPCVS). A 4.7 kΩ is recommended when intends to pull down at power-on reset.
$\overline{\text{RTSB}}$ PGOIQSEL	45	O_{8tc} I_{8tc}	UART B Request To Send. An active low informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as PGOIQSEL, which provides the power-on value for CR16 bit 4 (GOIQSEL). A 4.7 kΩ is recommended when intends to pull up at power-on reset.

1.3 Game Port/Power Down Interface

If Bit 3 of CR16 (GMDRQ) is 1, Bit 4 of CR3 (GMODS0) determines whether the game port is in Adapter mode or Portable mode (default is Adapter mode). If Bit 3 of CR16 is 0, pin 39 and 41 are used for DMA A operation.

SYMBOL	PIN	I/O	FUNCTION
$\overline{GMRD}$	41	OUT_{8t}	When CR16 Bit 3 (GMDRQ) = 1, Adapter mode: Game port read control signal.
PFDCEN		OUT_{8t}	Portable mode: When parallel port is selected as Extension FDD/Extension 2FDD mode, this pin will be active. The active state is dependent on bit 7 of CRA (PFDCACT), and default is low active.
$\overline{DACK\_A}$		IN_t	When CR16 Bit 3 (GMDRQ) = 0, DMA acknowledge signal A.
$\overline{GMWR}$	39	OUT_{8t}	When CR16 Bit 3 (GMDRQ) = 1, Adapter mode: Game port write control signal.
PEXTEN		OUT_{8t}	Portable mode: When a particular extended mode is selected for the parallel port, this pin will be active. The extended modes include Extension Adapter mode, EPP mode, ECP mode, and ECP/EPP mode, which are selected using bit 3 - bit 0 of CRA. The active state is dependent on bit 6 of CRA (PEXTACT); the default is low active.
DRQ_A		OUT_{8t}	When CR16 Bit 3 (GMDRQ) = 0: DMA request signal A.
PDCIN	3	IN_t	This input pin controls the chip power down. When this pin is active, the clock supply to the chip will be inhibited and the output pins will be tri-stated as defined in CR4 and CR6. The PDCIN is pulled down internally. Its active state is defined by bit 4 of CRA (PDCHACT). Default is high active.
$\overline{DACK\_N}$		IN_t	DMA acknowledge signal D.
IRSL1		OUT_{12t}	IR module mode select 1.
IRRXH/IRSL0		I/O_{12t}	When input pin, high speed IR received terminal. When as output pin, IR module mode select 0. Input or output are definied in high speed IR register.

1.4 Multi-Mode Parallel Port

The following pins have eight functions, which are controlled by bits PRTMOD0, PRTMOD1, and PRTMOD2 of CR0 and CR9. (refer to section 8.0, Extended Functions).

SYMBOL	PIN	I/O	FUNCTION
BUSY	24	IN_t	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{MOB}$ pin.
		IN_t	EXTENSION ADAPTER MODE: XIRQ This pin is an interrupt request generated by the Extension Adapter and is an active high input.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD A and B; the function of this pin is the same as that of the $\overline{MOB}$ pin.
		–	JOYSTICK MODE: NC pin.
$\overline{ACK}$	26	IN_t	PRINTER MODE: $\overline{ACK}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DSB2}$ This pin is for the Extension FDD B; its functions are the same as those of the $\overline{DSB}$ pin.
		IN_t	EXTENSION ADAPTER MODE: XDRQ DMA request generated by the Extension Adapter. An active high input.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DSB2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{DSB}$ pin.
		–	JOYSTICK MODE: NC pin.

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PE	27	IN_t	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WD2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{WD}$ pin.
		OUT_{12t}	EXTENSION ADAPTER MODE: XA0 This pin is system address A0 for the Extension Adapter
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WD2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WD}$ pin.
		–	JOYSTICK MODE: NC pin.
SLCT	28	IN_t	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WE2 This pin is for Extension FDD B; its functions are the same as those of the $\overline{WE}$ pin.
		OUT_{12t}	EXTENSION ADAPTER MODE: XA1 This pin is system address A1 for the Extension Adapter.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WE2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WE}$ pin.
		–	JOYSTICK MODE: NC pin.

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{ERR}$	29	IN_t	PRINTER MODE: $\overline{ERR}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{HEAD}$ pin.
		OUT_{12t}	EXTENSION ADAPTER MODE: XA2 This pin is system address A2 for the Extension Adapter.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{HEAD}$ pin.
		–	JOYSTICK MODE: NC pin.
$\overline{SLIN}$	22	OD_{12}	PRINTER MODE: $\overline{SLIN}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{STEP}$ pin.
		OUT_{12t}	EXTENSION ADAPTER MODE: XTC This pin is the DMA terminal count for the Extension Adapter. The count is sent by TC directly.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{STEP}$ pin.
		OUT_{12t}	JOYSTICK MODE: V_{DD} for joystick.

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{INIT}$	21	OD_{12}	PRINTER MODE: $\overline{INIT}$ Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{DIR}$ pin.
		OUT_{12t}	EXTENSION ADAPTER MODE: $\overline{XDACK}$ This pin is the DMA acknowledge output for the Extension Adapter; the output is sent directly from $\overline{PDACKX}$.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{DIR}$ pin.
		OUT_{12t}	JOYSTICK MODE: V_{DD} for joystick.
$\overline{AFD}$	20	OD_{12}	PRINTER MODE: $\overline{AFD}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{RWC2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{RWC}$ pin.
		OUT_{12t}	EXTENSION ADAPTER MODE: $\overline{XRD}$ This pin is the I/O read command for the Extension Adapter. When the Extension Adapter base address is written to the Extension Adapter address register, $\overline{XRD}$ and $\overline{XWR}$ go low simultaneously so that the command register on the Extension Adapter can latch the same base address.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{RWC2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{RWC}$ pin.
		OUT_{12t}	JOYSTICK MODE: V_{DD} for joystick.

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{STB}$	19	OD_{12}	PRINTER MODE: $\overline{STB}$
			An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OUT_{12t}	EXTENSION ADAPTER MODE: $\overline{XWR}$
			This pin is the I/O write command for the Extension Adapter. When the Extension Adapter base address is written to the Extension Adapter address register, $\overline{XRD}$ and $\overline{XWR}$ go low simultaneously so that the command register on the Extension Adapter can latch the same base address.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
		OUT_{12t}	JOYSTICK MODE: V_{DD} for joystick.
PD0	9	I/O_{24t}	PRINTER MODE: PD0
			Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{INDEX2}$
			This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{INDEX}$ pin. This pin is pulled high internally.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD0
			This pin is system data bus D0 for the Extension Adapter.
		IN_t	EXTENSION 2FDD MODE: $\overline{INDEX2}$
			This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{INDEX}$ pin. This pin is pulled high internally.
		I/O_{24t}	JOYSTICK MODE: JP0
			This pin is the paddle 0 input for joystick.

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD1	10	I/O_{24t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{TRAK0}$ pin. This pin is pulled high internally.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD1 This pin is system data bus D1 for the Extension Adapter.
		IN_t	EXTENSION. 2FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{TRAK0}$ pin. This pin is pulled high internally.
		I/O_{24t}	JOYSTICK MODE: JP1 This pin is the paddle 1 input for joystick.
PD2	11	I/O_{24t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{WP2}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{WP}$ pin. This pin is pulled high internally.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD2 This pin is system data bus D2 for the Extension Adapter.
		IN_t	EXTENSION. 2FDD MODE: $\overline{WP2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WP}$ pin. This pin is pulled high internally.
		-	JOYSTICK MODE: NC pin

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD3	12	I/O_{24t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{RDATA2}$ Motor on B for Extension FDD B; the function of this pin is the same as that of the $\overline{RDATA}$ pin. This pin is pulled high internally.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD3 This pin is system data bus D3 for the Extension Adapter.
		IN_t	EXTENSION 2FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD A and B; function of this pin is the same as that of the $\overline{RDATA}$ pin. This pin is pulled high internally.
		-	JOYSTICK MODE: NC pin
PD4	13	I/O_{24t}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{DSKCHG2}$ Drive select B for Extension FDD B; the function of this pin is the same as that of $\overline{DSKCHG}$ pin. This pin is pulled high internally.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD4 This pin is system data bus D4 for the Extension Adapter.
		IN_t	EXTENSION 2FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{DSKCHG}$ pin. This pin is pulled high internally.
		IN_t	JOYSTICK MODE: JB0 This pin is the button 0 input for the joystick.
PD5	14	I/O_{24t}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD5 This pin is system data bus D5 for the Extension Adapter.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
		IN_t	JOYSTICK MODE: JB1 This pin is the button 1 input for the joystick.

1.4 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD6	16	I/O_{24t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD6 This pin is system data bus D6 for the Extension Adapter.
		OD_{24}	EXTENSION. 2FDD MODE: $\overline{MOA2}$ This pin is for Extension FDD A; its function is the same as that of the $\overline{MOA}$ pin.
		-	JOYSTICK MODE: NC pin
PD7	17	I/O_{24t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		I/O_{24t}	EXTENSION ADAPTER MODE: XD7 This pin is system data bus D7 for the Extension Adapter.
		OD_{24}	EXTENSION 2FDD MODE: $\overline{DSA2}$ This pin is for Extension FDD A; its function is the same as that of the $\overline{DSA}$ pin.
		-	JOYSTICK MODE: NC pin

1.5 IDE and FDC Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{RESIDE}}$	1	OUT_{12t}	When CR16 Bit 1 (IRIDE) = 0: Active low reset signal for IDE;
IRQ_G		OUT_{12t}	When CR16 Bit 1 (IRIDE) = 1: Interrupt request signal G.
DRQ_D		OUT_{12t}	DMA request signal.
IRSL2		OUT_{12t}	IR module mode select 2.
$\overline{\text{IDBEN}}$	91	OUT_{12t}	When CR16 Bit 1 (IRIDE) = 0: Active low enable signal for IDE;
IRQ_H		OUT_{12t}	When CR16 Bit 1 (IRIDE) = 1: Interrupt request signal H.
IRSL2		OUT_{12t}	IR module mode selection 2.
$\overline{\text{DACK\_N}}$		IN_t	DMA acknowledge signal D.
IRRXH/IRSL0		I/O_{12t}	When input selected, act as high speed IR receiving terminal. When output selected, act as IR module mode selection 0.
$\overline{\text{CS1}}$	95	OUT_{12t}	When CR16 Bit 1 (IRIDE) = 0: This pin is used to select the IDE controller. $\overline{\text{CS1}}$ decodes the HDC addresses specified in CR22.
IRTX2		OUT_{12t}	When CR16 Bit 1 (IRIDE) = 1: Function as a InfraRed transmission data line.
$\overline{\text{CS0}}$	94	OUT_{12t}	When CR16 Bit 1 (IRIDE) = 0: This pin is used to select the IDE controller. $\overline{\text{CS0}}$ decodes HDC addresses specified in CR21.
IRRX2		IN_t	When CR16 Bit 1 (IRIDE) = 1: Function as a InfraRed receiving line.
$\overline{\text{WE}}$	85	OD_{24}	Write enable. An open drain output.
$\overline{\text{DIR}}$	89	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
$\overline{\text{HEAD}}$	88	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
$\overline{\text{RWC}}$	87	OD_{24}	Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. An open drain output. Logic 0 = 250 Kb/s Logic 1 = 500 Kb/s When bit 5 of CR9 (EN3MODE) is set to high, the three-mode FDD function is enabled, and the pin will have a different definition. Refer to the EN3MODE bit in CR9.
$\overline{\text{WD}}$	86	OD_{24}	Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output.

1.5 IDE and FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{STEP}$	82	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
$\overline{INDEX}$	81	IN_{cs}	This schmitt input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{TRAK0}$	78	IN_{cs}	Track 0. This schmitt input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{WP}$	77	IN_{cs}	Write protected. This active low schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{RDATA}$	74	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{DSKCHG}$	76	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{MOA}$	79	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{MOB}$	80	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{DSA}$	83	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{DSB}$	84	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
V_{DD}	15, 56		+5 Volt power supply for the digital circuitry
GND	25, 40, 65, 90		Ground

2.0 FDC FUNCTIONAL DESCRIPTION

2.1 W83877AF FDC

The floppy disk controller of the W83877AF integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to data rate 1 M bits/sec. (2 M bits/sec for fast tape drive with 48 MHz crystal in)

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

2.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

2.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD × (1/Data Rate) *8 - 1.5 µS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 × 16 µS - 1.5 µS = 14.5 µS
2 Byte	2 × 16 µS - 1.5 µS = 30.5 µS
8 Byte	8 × 16 µS - 1.5 µS = 6.5 µS
15 Byte	15 × 16 µS - 1.5 µS = 238.5 µS
FIFO THRESHOLD	**MAXIMUM DELAY TO SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 × 8 µS - 1.5 µS = 6.5 µS
2 Byte	2 × 8 µS - 1.5 µS = 14.5 µS
8 Byte	8 × 8 µS - 1.5 µS = 62.5 µS
15 Byte	15 × 8 µS - 1.5 µS = 118.5 µS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.••

2.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

2.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

2.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

2.1.6 Tape Drive

The W83877AF supports standard tape drives (1 Mbps, 500 Kbps, 250 Kbps) and new fast tape drive (2M bps). When working at 2 M bps, you need to change the crystal to 48 MHz.

2.1.7 FDC Core

The W83877AF FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

2.1.8 FDC Commands

Command Symbol Descriptions:

C:	Cylinder number 0 - 256
D:	Data Pattern
DIR:	Step Direction
	DIR = 0, step out
	DIR = 1, step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EOT:	End of Track
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of track
FIFOTHR:	FIFO Threshold
GAP:	Gap length selection
GPL:	Gap Length
H:	Head number
HDS:	Head number select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset

MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number
R:	Record
RCN:	Relative Cylinder Number
R/W:	Read/Write
SC:	Sector/per cylinder
SK:	Skip deleted data address mark
SRT:	Step Rate Time
ST0:	Status Register 0
ST1:	Status Register 1
ST2:	Status Register 2
ST3:	Status Register 3
WG:	Write gate alters timing of WE

2.1.9 FDC Instruction Sets

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command codes
Result	W	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes/Sector
	W	---------- SC ----------								Sectors/Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector Repeat:	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| --------SRT ---------- | -------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	| ------ FIFOTHR ----|					
	W	| ----------PRETRK ---------- |								
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	| ---------- RCN ---------- |								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	-------SRT ---------- | --------- HUT --------								
	R	---------- HLT ----------| ND								
	R	---------- SC/EOT ----------								
	R	LOCK 0 D3 D2 D1 D0 GAP WG								
	R	0 EIS EFIFO POLL | --- FIFOTHR ---- |								
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation - FDC goes into standby state)
Result	R	---------- ST0 ----------								ST0 = 80H

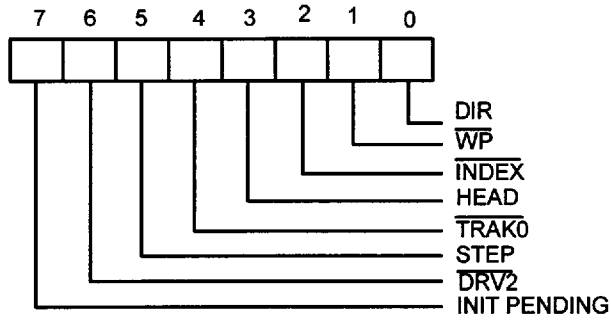
2.2 Register Descriptions

There are several status, data, and control registers in W83877AF. These registers are defined below:

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

2.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

$\overline{\text{DRV2}}$ (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of $\overline{\text{STEP}}$ output.

$\overline{\text{TRAK0}}$ (Bit 4):

This bit indicates the value of $\overline{\text{TRAK0}}$ input.

HEAD (Bit 3):

This bit indicates the complement of $\overline{\text{HEAD}}$ output.

0 side 0

1 side 1

$\overline{\text{INDEX}}$ (Bit 2):

This bit indicates the value of $\overline{\text{INDEX}}$ output.

$\overline{\text{WP}}$ (Bit 1):

0disk is write-protected

1disk is not write-protected

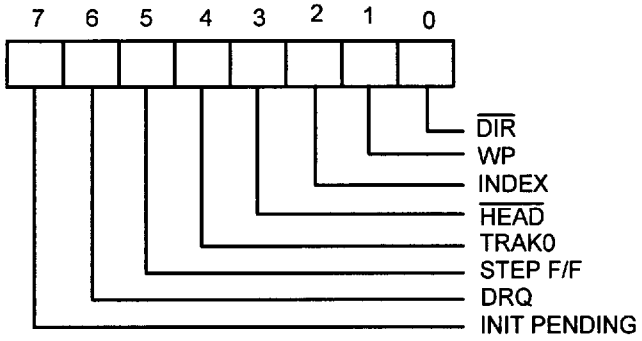
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched $\overline{\text{STEP}}$ output.

TRAK0 (Bit 4):

This bit indicates the complement of $\overline{\text{TRAK0}}$ input.

$\overline{\text{HEAD}}$ (Bit 3):

This bit indicates the value of $\overline{\text{HEAD}}$ output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of $\overline{\text{INDEX}}$ output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

$\overline{\text{DIR}}$ (Bit 0)

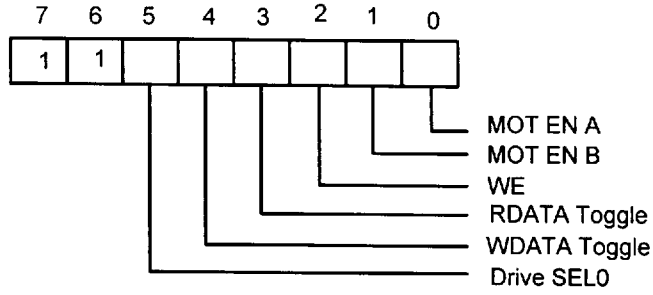
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

2.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the $\overline{WD}$ output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the $\overline{RDATA}$ output pin.

WE (Bit 2):

This bit indicates the complement of the $\overline{WE}$ output pin.

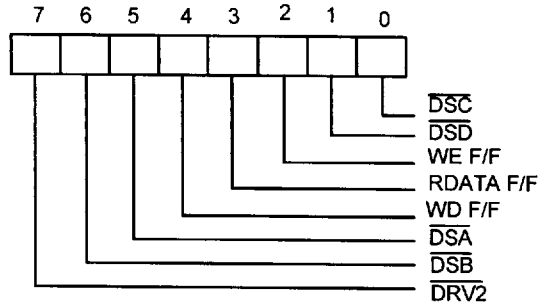
MOT EN B (Bit 1)

This bit indicates the complement of the $\overline{MOB}$ output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the $\overline{MOA}$ output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



$\overline{DRV2}$ (Bit 7):

0 A second drive has been installed

1 A second drive has not been installed

$\overline{DSB}$ (Bit 6):

This bit indicates the status of $\overline{DSB}$ output pin.

$\overline{DSA}$ (Bit 5):

This bit indicates the status of $\overline{DSA}$ output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched $\overline{WD}$ output pin at every rising edge of the $\overline{WD}$ output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched $\overline{RDATA}$ output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched $\overline{WE}$ output pin.

$\overline{DSD}$ (Bit 1):

0 Drive D has been selected

1 Drive D has not been selected

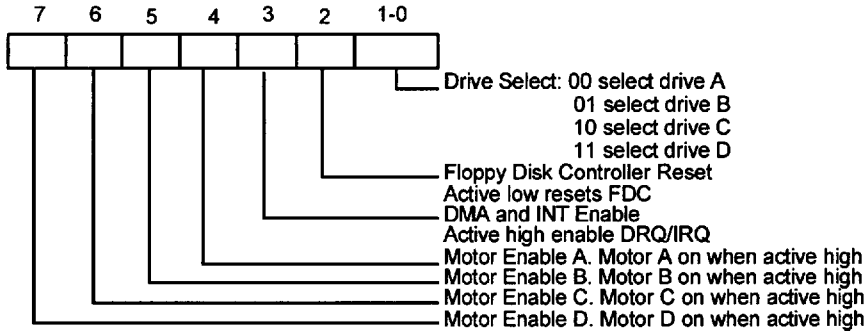
$\overline{DSC}$ (Bit 0):

0 Drive C has been selected

1 Drive C has not been selected

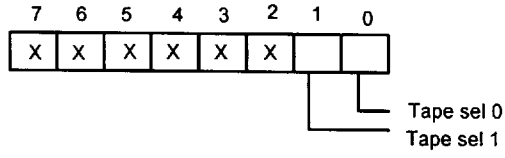
2.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

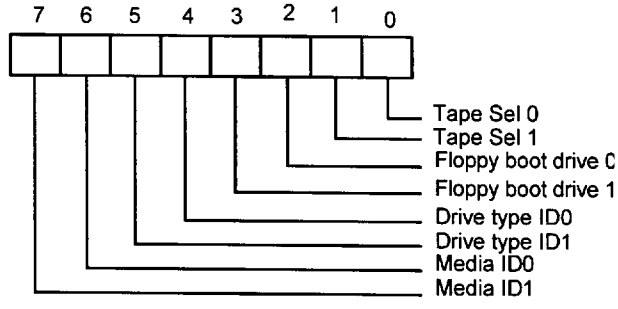


2.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:



If three mode FDD function is enabled (EN3MODE = 1 in CR9), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of CR8 bit 3, 2.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of CR7. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of CR8 bit 1, 0.

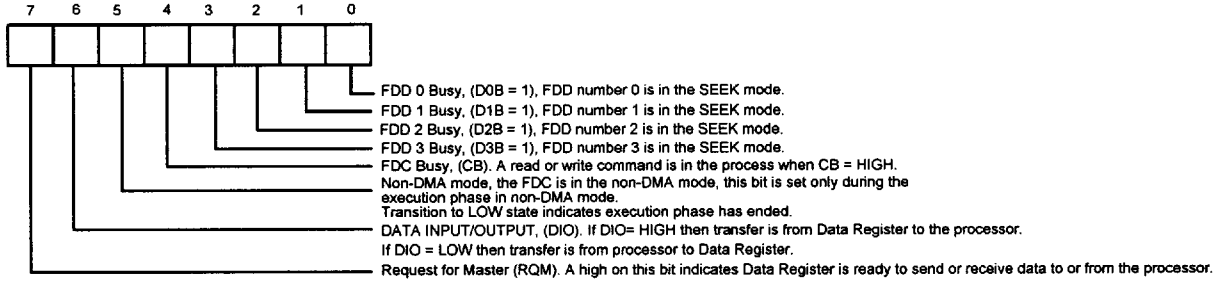
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

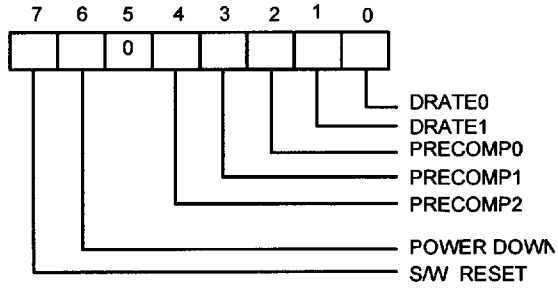
2.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



2.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode

1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

PRECOM 2 1 0	PRECOMPENSATION DELAY
0 0 0	Default Delays
0 0 1	41.67 nS
0 1 0	83.34 nS
0 1 1	125.00 nS
1 0 0	166.67 nS
1 0 1	208.33 nS
1 1 0	250.00 nS
1 1 1	0.00 nS (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 nS
300 KB/S	125 nS
500 KB/S	125 nS
1 MB/S	41.67 nS

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC and reduced write current control.

00 500 KB/S (MFM), 250 KB/S (FM), $\overline{RWC}$ = 1.

01 300 KB/S (MFM), 150 KB/S (FM), $\overline{RWC}$ = 0.

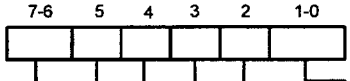
10 250 KB/S (MFM), 125 KB/S (FM), $\overline{RWC}$ = 0.

11 1 MB/S (MFM), Illegal (FM), $\overline{RWC}$ = 1.

2.2.7 FIFO Register (R/W base address + 5)

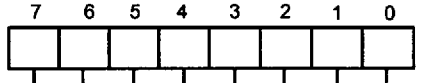
The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83877AF, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

Status Register 0 (ST0)



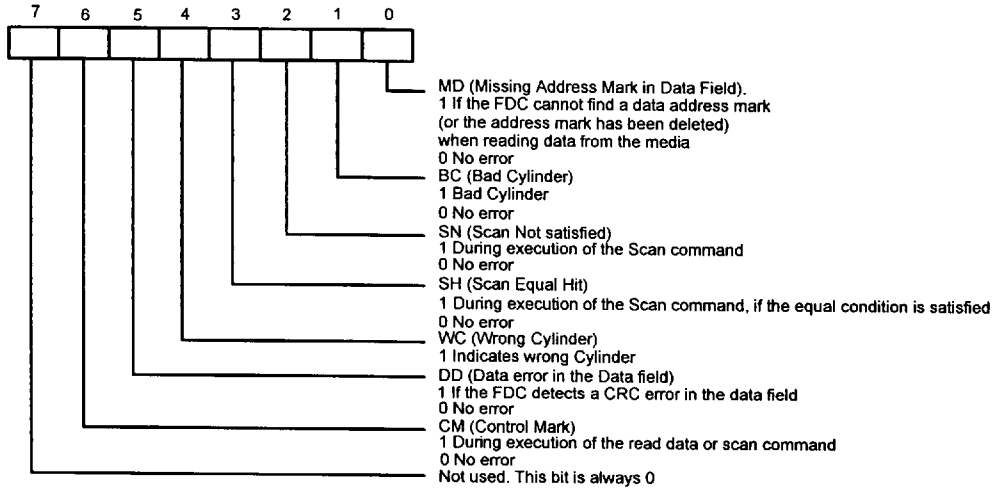
US1, US0 Drive Select:
00 Drive A selected
01 Drive B selected
10 Drive C selected
11 Drive D selected
HD Head address:
1 Head selected
0 Head selected
NR Not Ready:
1 Drive is not ready
0 Drive is ready
EC Equipment Check:
1 When a fault signal is received from the FDD or the track
0 signal fails to occur after 77 step pulses
0 No error
SE Seek end:
1 seek end
0 seek error
IC Interrupt Code:
00 Normal termination of command
01 Abnormal termination of command
10 Invalid command issue
11 Abnormal termination because the ready signal from FDD changed state during command executi

Status Register 1 (ST1)

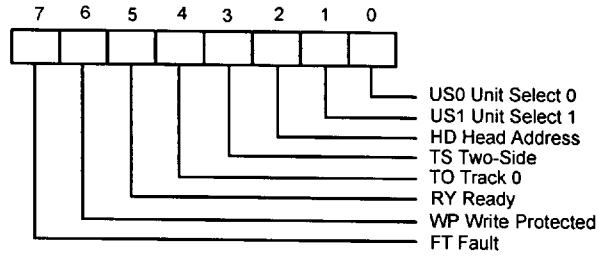


Missing Address Mark. 1 When the FDC cannot detect the data address mark or the data address mark has been deleted.
NW (Not Writable). 1 If a write Protect signal is detected from the diskette drive during execution of write data.
ND (No DATA). 1 If specified sector cannot be found during execution of a read, write or verify data.
Not used. This bit is always 0.
OR (Over Rum). 1 If the FDC is not serviced by the host system within a certain time interval during data transfer.
DE (data Error).1 When the FDC detects a CRC error in either the ID field or the data field.
Not used. This bit is always 0.
EN (End of track). 1 When the FDC tries to access a sector beyond the final sector of a cylinder.

Status Register 2 (ST2)

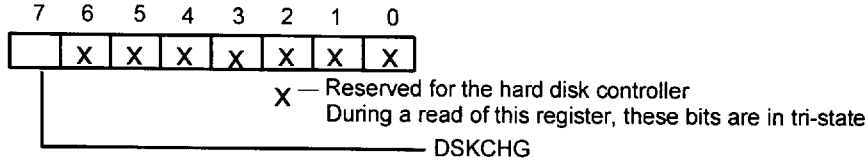


Status Register 3 (ST3)

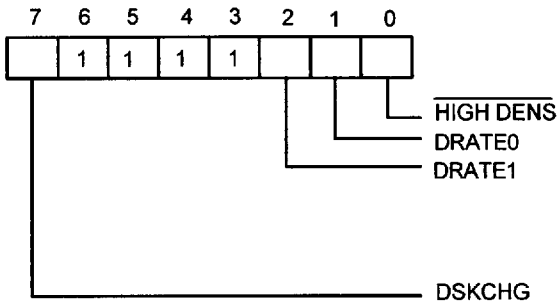


2.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of $\overline{\text{DSKCHG}}$, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



In the PS/2 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the complement of the $\overline{\text{DSKCHG}}$ input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):

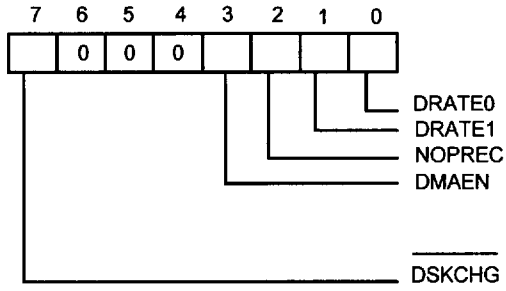
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

$\overline{\text{HIGH DENS}}$ (Bit 0):

0 500 KB/S or 1 MB/S data rate (high density FDD)

1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the status of $\overline{\text{DSKCHG}}$ input.

Bit 6-4: These bits are always a logic 1 during a read.

DMAEN (Bit 3):

This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):

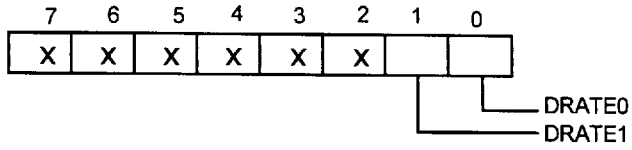
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

2.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



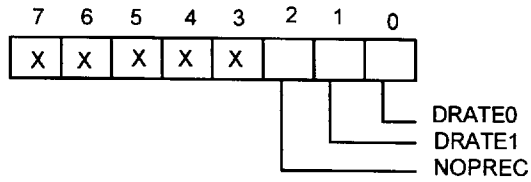
X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

In the PS/2 Model 30 mode, the bit definitions are as follows:



X : Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):

This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

3.0 IDE

The IDE interface is essentially the AT bus ported to the hard disk drive. The hard disk controller resides on the IDE hard disk drive. So the IDE interface provides only chip select signals and AT bus signals between the IDE hard disk drive and ISA slot. Table 3-1 shows the IDE registers and their ISA addresses.

Table 3-1

I/O ADDRESS OFFSET	REGISTERS	
	READ	WRITE
$\overline{CS0}$ base address + 0	Data Register	Data Register
$\overline{CS0}$ base address + 1	Error Register	Write-Precomp
$\overline{CS0}$ base address + 2	Sector Count	Sector Count
$\overline{CS0}$ base address + 3	Sector Number	Sector Number
$\overline{CS0}$ base address + 4	Cylinder LOW	Cylinder LOW
$\overline{CS0}$ base address + 5	Cylinder HIGH	Cylinder HIGH
$\overline{CS0}$ base address + 6	SDH Register	SDH Register
$\overline{CS0}$ base address + 7	Status Register	Command Register
$\overline{CS1}$ base address + 6	Alternate Status	Fixed Disk Control

3.1 IDE Decode Description

When the processor selects the addresses which match the ones specified in CR 21, the chip system enables $\overline{CS0}$ = LOW; otherwise, $\overline{CS0}$ = HIGH. When the processor selects the address which matches the one specified in CR22, the chip system enables $\overline{CS1}$ = LOW; otherwise, $\overline{CS1}$ = HIGH.

4.0 UART PORT

4.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

4.2 Register Address

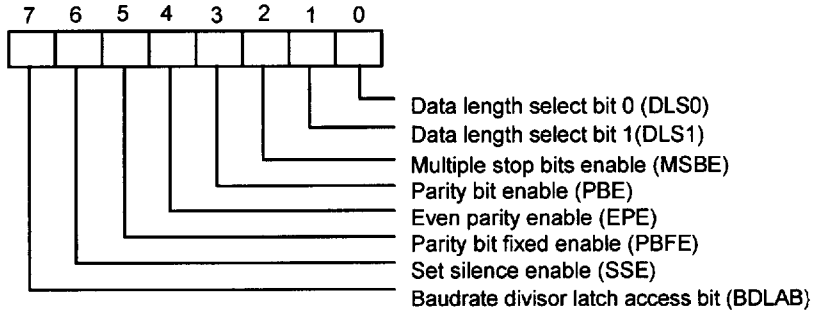
TABLE 4-1 UART Register Bit Map

Register Address Base			Bit Number							
			0	1	2	3	4	5	6	7
8 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
8 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
9 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
A	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
A	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
B	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baud rate Divisor Latch Access Bit (BDLAB)
C	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
D	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
E	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
F	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
8 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
9 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 mode.

4.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.



Bit 7: BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud rate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.

Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only SOUT is affected by this bit; the transmitter is not affected.

Bit 5: PBFE. When PBE and PBFE of UCR are both set to a logical 1,

(1) if EPE is a logical 1, the parity bit is fixed as a logical 0 to transmit and check.

(2) if EPE is a logical 0, the parity bit is fixed as a logical 1 to transmit and check.

Bit 4: EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.

Bit 3: PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.

Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to a logical 0, one stop bit is sent and checked.

(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.

(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.

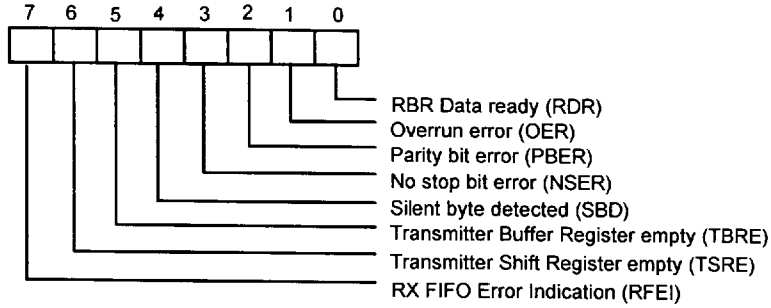
Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 4-2 WORD LENGTH DEFINITION

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

4.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.



Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other than these two cases, this bit will be reset to a logical 0.

Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.

Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

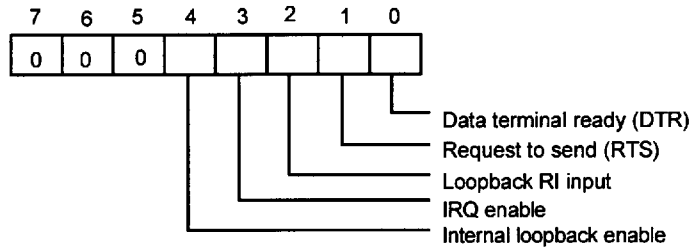
Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

4.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

(1) SOUT is forced to a logical 1, and SIN is isolated from the communication link instead of the TSR.

(2) Modem output pins are set to their inactive state.

(3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) → $\overline{DSR}$, RTS (bit 1 of HCR) → $\overline{CTS}$, Loopback RI input (bit 2 of HCR) → $\overline{RI}$ and IRQ enable (bit 3 of HCR) → $\overline{DCD}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input $\overline{DCD}$.

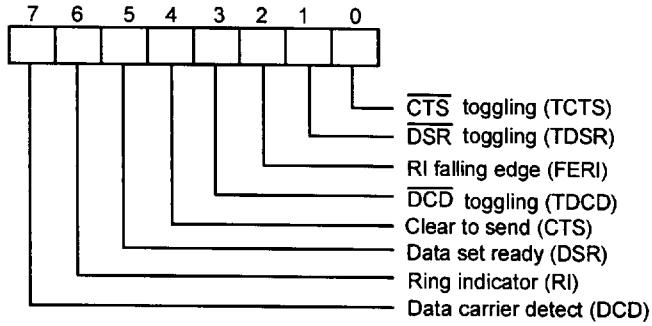
Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input $\overline{RI}$.

Bit 1: This bit controls the $\overline{RTS}$ output. The value of this bit is inverted and output to $\overline{RTS}$.

Bit 0: This bit controls the $\overline{DTR}$ output. The value of this bit is inverted and output to $\overline{DTR}$.

4.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.



Bit 7: This bit is the opposite of the $\overline{DCD}$ input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6: This bit is the opposite of the $\overline{RI}$ input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5: This bit is the opposite of the $\overline{DSR}$ input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4: This bit is the opposite of the $\overline{CTS}$ input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3: TDCD. This bit indicates that the $\overline{DCD}$ pin has changed state after HSR was read by the CPU.

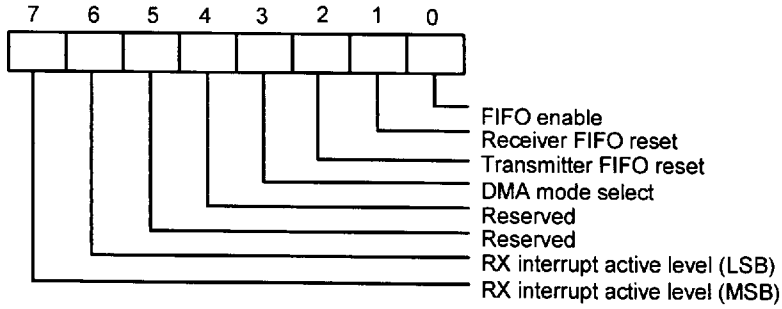
Bit 2: FERI. This bit indicates that the $\overline{RI}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the $\overline{DSR}$ pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the $\overline{CTS}$ pin has changed state after HSR was read by the CPU.

4.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 4-3 FIFO TRIGGER LEVEL

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

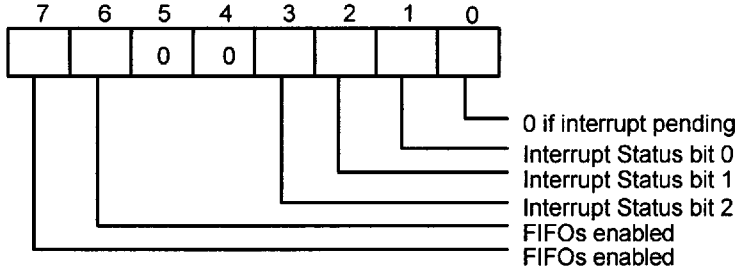
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

4.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

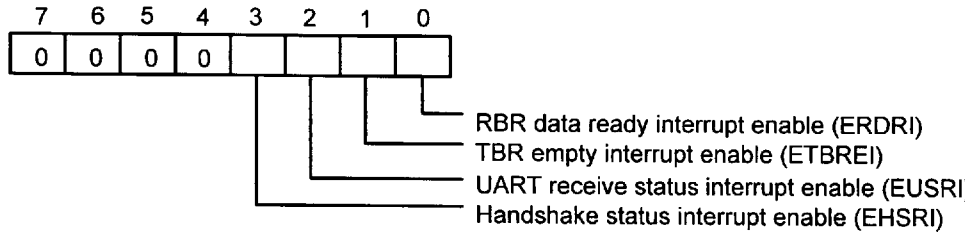
TABLE 4-4 INTERRUPT CONTROL FUNCTION

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

4.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.



Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

4.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to 2^{16}-1. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

4.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 4-5 BAUD RATE TABLE

BAUD RATE USING 24 MHZ TO GENERATE 1.8461 MHZ		
Desired Baud Rate	Decimal divisor used to generate 16X clock	Percent error difference between desired and actual
50	2304	**
75	1536	**
110	1047	0.18%
134.5	857	0.099%
150	768	**
300	384	**
600	192	**
1200	96	**
1800	64	**
2000	58	0.53%
2400	48	**
3600	32	**
4800	24	**
7200	16	**
9600	12	**
19200	6	**
38400	3	**
57600	2	**
115200	1	**
1.5M	1*	0%

* Only use in high speed mode (refer CR0C bit7 and CR0C bit6).

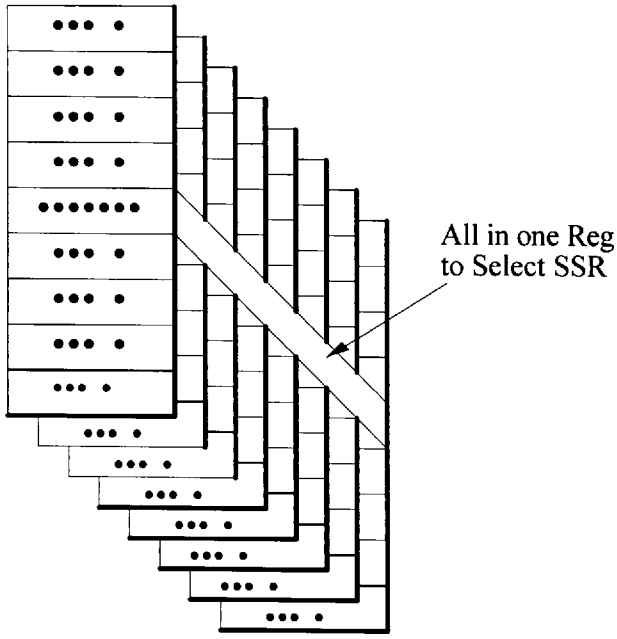
** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

4.3 IR Port

In the W83877AF includes two serial ports, that is UART A and UART B. The second serial port, UART B, also has built in the Infrared (IR) functions which include IrDA 1.0 SIR, IrDA 1.1 MIR (1.152M bps), IrDA FIR (4M bps), SHARP ASK-IR, and remote control (that support NEC, RC-5, advanced RC-5, and RECS-80 protocol).

4.3.1 Advanced UART B Register Description

When bank select enable bit (ENBNKSEL, in CR2C.bit3) is set, UART B will be switched to Advanced UART B, and eight Register Sets can be accessed. These Register Sets control enhanced UART B, IR function switching such as SIR, MIR, or FIR. Also a superior traditional UART B function can be use such as 32-byte transmitter/receiver FIFO, non-encoding IRQ identify status register, and automatic flow control. The MIR/FIR and remote control registers are also defined in these Register Sets. Structure of he Register Sets is shown as follows.



*Set 0, 1 are legacy/Advanced UART Registers
*Set 2~7 are Advanced UART Registers

All Set•s registers have a common register which is *Sets Select Register* (SSR) in order to switch to any *Set* when config this register. The summary description of these *Sets* is shown in the following.

Set	UART	IR Mode	Sets Description
0	••	••	Legacy/Advanced UART Control and Status Registers.
1	••	••	Legacy Baud Rate Divisor Register.
2		••	Advanced UART Control and Status Registers.
3		••	Version ID *and* Mapped Control Registers.
4		••	Transmitter/Receiver/Timer Counter Registers *and* IR Control Registers.
5		••	Flow Control *and* IR Control *and* Frame Status FIFO Registers.
6		••	IR Physical Layer Control Registers
7		••	Remote Control *and* IR front-end Module Selection Registers.

4.3.2 Set0-Legacy/Advanced UART Control and Status Registers

Address Offset	Register Name	Register Description
0	**RBR/TBR**	Receiver/Transmitter Buffer Registers
1	**ICR**	Interrupt Control Register
2	**ISR/UFR**	Interrupt Status *or* UART FIFO Control Register
3	**UCR/SSR**	UART Control *or* Sets Select Register
4	**HCR**	Handshake Control Register
5	**USR**	UART Status Register
6	**HSR**	Handshake Status Register
7	**UDR/ESCR**	User Defined Register

4.3.2.1 Set0.Reg0 - Receiver/Transmitter Buffer Registers (RBR/TBR) (Read/Write)

Receiver Buffer Register is read only and Transmitter Buffer Register is write only. These registers are described same as legacy UART.

In the legacy UART, this port only supports PIO mode. In the advanced UART, if setup to MIR/FIR/Remote IR, this port will support DMA handshake function. Two DMA channel can be used, that is one TX DMA channel and another RX DMA channel. Therefore, single DMA channel is also supported when set the bit of D_CHSW (DMA Channel Swap, in Set2.Reg2.Bit3) and the TX/RX DMA channel is swapped. Note that two DMA channel are defined in config register CR2A which select DMA channel or disable DMA channel. If enable RX DMA channel and disable TX DMA channel, then the single DMA channel will be selected.

4.3.2.2 Set0.Reg1 - Interrupt Control Register (ICR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
UART	0	0	0	0	EHSRI	EUSRI	ETBREI	ERDRI
Advanced UART	ETMRI	EFSFI	ETXTHI	EDMAI	EHSRI	EUSRI/ TXURI	ETBREI	ERXTHI

Where UART is used to Legacy UART, and the functions for these bits are defined in the previous UART, nevertheless the traditional SIR or ASK-IR based on the legacy UART also have same definitions. The advanced UART functions included Advanced SIR/ASK-IR, MIR, FIR, or Remote IR are described as follows.

Bit 7: **ETMRI - Enable Timer Interrupt**

Write to 1, enable timer interrupt.

Bit 6: *MIR, FIR mode:*

EFSFI - Enable Frame Status FIFO Interrupt

Write to 1, enable frame status FIFO interrupt.

Advanced SIR/ASK-IR, Remote IR:

Not used.

Bit 5: *Advanced SIR/ASK-IR, MIR, FIR, Remote IR:*

ETXTHI - Enable Transmitter Threshold Interrupt

Write to 1, enable transmitter threshold interrupt.

Bit 4: *MIR, FIR, Remote IR:*

EDMAI - Enable DMA Interrupt.

Write to 1, enable DMA interrupt.

Bit 3: *Advanced UART/SIR/ASK-IR, MIR, FIR, Remote IR:*

EHSRI - Enable HSR (Handshake Status Register) Interrupt

Write to 1, enable handshake status register interrupt. Note that the bit IRHSSL (Infrared Handshake Select) should be set to 1, then this bit EHSRI is effective.

Bit 2: *Advanced SIR/ASK-IR:*

EUSRI - Enable USR (UART Status Register) Interrupt

Write to 1, enable UART status register interrupt.

MIR, FIR, Remote Controller:

EHSRI/ETXURI - Enable USR Interrupt *or* Enable Transmitter Underrun Interrupt

Write to 1, enable USR interrupt or enable transmitter underrun interrupt.

Bit 1: **ETBREI - Enable TBR (Transmitter Buffer Register) Empty Interrupt**

Write to 1, enable transmitter buffer register empty interrupt.

Bit 0: **ERBRI - Enable RDR (Receiver Buffer Register) Interrupt**

Write to 1, enable receiver buffer register interrupt.

4.3.2.3 Set0.Reg2 - Interrupt Status Register/UART FIFO Control Register (ISR/UFR)

(1) Interrupt Status Register: (Write Only)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy UART	FIFO Enable	FIFO Enable	0	0	IID2	IID1	IID0	IP
Advanced UART	TMR_I	FSF_I	TXTH_I	DMA_I	HS_I	USR_I/ FEND_I	TXEMP_I	RXTH_I
Reset Value	0	0	1	0	0	0	1	0

Legacy UART: Same as previous register defined.

Advanced UART:

Bit 7: **TMR_I - Timer Interrupt.**

Set to 1 when timer count to 0. This bit will be affected by (1) the timer registers are defined in Set4.Reg0 and Set4.Reg1, (2) EN_TMR(Enable Timer, in Set4.Reg2.Bit0) should be set to 1, (3) ENTMR_I (Enable Timer Interrupt, in Set0.Reg1.Bit7) should be set to 1.

Bit 6: *MIR, FIR modes:*

FSF_I - Frame Status FIFO Interrupt.

Set to 1 when Frame Status FIFO is equal or larger than the threshold level *or* Frame Status FIFO time-out occurs. Clear to 0 when Frame Status FIFO is below the threshold level.

Advanced UART/SIR/ASK-IR, Remote IR modes:

Not used.

Bit 5: **TXTH_I - Transmitter Threshold Interrupt.**

Set to 1 if the TBR (Transmitter Buffer Register) FIFO is below the threshold level. Clear to 0 if the TBR (Transmitter Buffer Register) FIFO is below the threshold level.

Bit 4: *MIR, FIR, Remote IR modes:*

DMA_I - DMA Interrupt.

Set to 1 if the DMA controller 8237A sends a TC (Terminal Count) to I/O device which that may be a Transmitter TC or a Receiver TC. Clear to 0 when this register is read.

Bit 3: **HS_I - Handshake Status Interrupt.**

Set to 1 when the Handshake Status Register has a toggle. Clear to 0 when Handshake Status Register (HSR) is read. Note that in all IR modes included SIR, ASK-IR, MIR, FIR, and Remote Control IR are defaulted to inactive except set IR Handshake Status Enable (IRHS_EN) to 1.

Bit 2: *Advanced UART/SIR/ASK-IR modes:*

USR_I - UART Status Interrupt.

Set to 1 when overrun, or parity bit, or stop bit, or silent byte detected error in the UART Status Register (USR) sets to 1. Clear to 0 when USR is read.

MIR, FIR modes:

FEND_I - Frame End Interrupt.

Set to 1 when (1) a frame have a grace end to be detected where the frame signal is defined in the physical layer of IrDA version 1.1 (2) abort signal or illegal signal has been detected during receiving valid data. Clear to 0 when this register is read.

Remote Controller mode:

Not used.

Bit 1: **TXEMP_I - Transmitter Empty.**

Set to 1 when transmitter (or, say, FIFO + Transmitter) is empty. Clear to 0 when this register is read.

Bit 0: **RXTH_I - Receiver Threshold Interrupt.**

Set to 1 when (1) the Receiver Buffer Register (RBR) is equal *or* larger than the threshold level, (2) RBR occurs time-out if the receiver buffer register has valid data and below the threshold level. Clear to 0 when RBR is less than threshold level from reading RBR.

(2) UART FIFO Control Register (UFR):

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Legacy UART	RXFTL1 (MSB)	RXFTL0 (LSB)	0	0	0	TXF_RST	RXF_RST	EN_FIFO
Advanced UART	RXFTL1 (MSB)	RXFTL0 (LSB)	TXFTL1 (MSB)	TXFTL0 (LSB)	0	TXF_RST	RXF_RST	EN_FIFO
Reset Value	0	0	0	0	0	0	0	0

Legacy UART: The definition of this register is same as Legacy UART mode.

Advanced UART:

Bit 7, 6: **RXFTL1, 0 - Receiver FIFO Threshold Level**

Definition is same as Legacy UART, that is to determine the RXTH_I to become 1 when the Receiver FIFO Threshold Level is equal or larger than the defined value shown as follow.

RXFTL1, 0 (Bit 7, 6)	RX FIFO Threshold Level (FIFO Size: ***16-byte***)	RX FIFO Threshold Level (FIFO Size: ***32-byte***)
00	1	1
01	4	4
10	8	16
11	14	26

Note that the FIFO Size is referred to SET2.Reg4.

Bit 5, 4: **TXFTL1, 0 - Transmitter FIFO Threshold Level**

To determine the TXTH_I (Transmitter Threshold Level Interrupt) is set to 1 when the Transmitter Threshold Level is less than the programmed value shown as follows.

TXFTL1, 0 (Bit 5, 4)	TX FIFO Threshold Level (FIFO Size: *16-byte*)	TX FIFO Threshold Level (FIFO Size: *32-byte*)
00	1	1
01	3	7
10	9	17
11	13	25

Bit 3 ~0 **Same Legacy UART mode**

4.3.2.4 Set0.Reg3 - UART Control Register/Set Select Register (UCR/SSR):

These two registers are shared same address. In any Set, *Set Select Register (SSR)* can be programmed to desired Set, but UART Control Register can be programmed only in Set 0 and Set 1, that is, in other Sets will not affect when program this register. The mapping of entry Set and programming value is shown as follows.

SSR Bits									Selected
7	6	5	4	3	2	1	0	Hex Value	Set
0	••	••	••	••	••	••	••	••	**Set 0**
1	Any value but not used in SET 2~7							••	**Set1**
1	1	1	0	0	0	0	0	**0xE0**	**Set 2**
1	1	1	0	0	1	0	0	**0xE4**	**Set 3**
1	1	1	0	1	0	0	0	**0xE8**	**Set 4**
1	1	1	1	1	1	0	0	**0xEC**	**Set 5**
1	1	1	1	0	0	0	0	**0xF0**	**Set 6**
1	1	1	1	0	1	0	0	**0xF4**	**Set 7**

UART Control Register: Defined legacy UART.

4.3.2.5 Set0.Reg4 - Handshake Control Register (HCR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy UART	0	0	0	XLOOP	EN_IRQ	LP_RI	RTS	DTR
Advanced UART	AD_MD2	AD_MD1	AD_MD0	SIR_PLS	TX_WT	EN_DMA	RTS	DTR
Reset Value	0	0	0	0	0	0	0	0

Legacy UART Register: These registers are defined same as previous description.

Advanced UART Register:

Bit 7~5 *Advanced UART/SIR/ASK-IR, MIR, FIR, Remote Controller modes:*

AD_MD2~0 - Advanced UART/Infrared mode Select.

These registers are active when Advanced UART Select (ADV_SL, in Set2.Reg2.Bit0) is set to 1. Operational mode selection is defined as follows. When the backward operation occurs these register will be reset to 0 and backward legacy UART mode.

AD_MD2~0 (Bit 7, 6, 5)	Selected Mode
000	Advanced **UART**
001	Low speed **MIR** (0.576M bps)
010	Advanced **ASK-IR**
011	Advanced **SIR**
100	High Speed **MIR** (1.152M bps)
101	**FIR** (4M bps)
110	**Consumer IR**
111	**Reserved**

Bit 4: *MIR, FIR modes:*

SIR_PLS - Send Infrared Pulse

Write to 1 then automatic send a 2 μs infrared pulse after physical frame end. In order to talk to SIR that the high speed infrared is still in process when sends this pulse. This bit will be automatically cleared by hardware.

Other modes:

Not used.

Bit 3: *MIR, FIR modes:*

TX_WT - Transmission Waiting

If this bit sets to 1, the transmitter will wait for TX FIFO reaching to threshold level or transmitter time-out which avoid short data bytes to want to transmit, then begins to transmit data from TX FIFO. That is in order to avoid Underrun.

Other modes:

Not used.

Bit 2: *MIR, FIR modes:*

EN_DMA - Enable DMA

Enable DMA function to transmission or receiving. Before using this, the DMA channel should be select. If set RX DMA channel and disable TX DMA channel then the single DMA channel is used. In the single channel system, the bit of D_CHSW (DMA channel swap, in Set 2.Reg2.Bit3) will determine RX DMA channel or TX DMA channel.

Other modes:

Not used.

Bit 1, 0: **RTS, DTR**

Functional definitions is same as legacy UART mode.

4.3.2.6 Set0.Reg5 - UART Status Register (USR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy UART	RFEI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
Advanced UART	LB_INFR	TSRE	TBRE	MX_LEX	PHY_ERR	CRC_ERR	OER	RDR
Reset Value	0	0	0	0	0	0	0	0

Legacy UART Register: These registers are defined same as previous description.

Advanced UART Register:

Bit 7: *MIR, FIR modes:*

LB_INFR - Last Byte In Frame End

Set to 1 when a last byte of a frame is in the FIFO bottom. This bit indicates that separate one frame from another frame when RX FIFO has more than one frame.

Bit 6, 5: Same as legacy UART description.

Bit 4: *MIR, FIR modes:*

MX_LEX - Maximum Frame Length Exceed

Set to 1 when frame length from the receiver has exceeded the programmed frame length which is in SET4.Reg6 and Reg5.If this bit is set to 1, the receiver will not receive any data to RX FIFO.

Bit 3: *MIR, FIR modes:*

PHY_ERR - Physical Layer Error

Set to 1 when an illegal data symbol is received. Where the illegal data symbol is defined in physical layer of IrDA version 1.1. When this bit is set to 1, the decoder of receiver will be aborted and a frame end signal is set to 1.

Bit 2: *MIR, FIR modes:*

CRC_ERR - CRC Error

Set to 1 when an attached CRC is error.

Bit 1, 0: **OER - Overrun Error, RDR - RBR Data Ready**

Definitions are same as legacy UART.

4.3.2.7 Set0.Reg6 - Handshake Status Register (HSR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy UART	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
Advanced UART	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
Reset Value	0	0	0	0	0	0	0	0

Legacy/Advanced UART Register: These registers are defined same as previous description.

4.3.2.8 Set0.Reg7 - User Defined Register (UDR/AUDR)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Legacy UART	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced UART	FLC_ACT	UNDRN	RX_BSY/ RX_IP	LST_FE/ RX_PD	S_FEND	0	LB_SF	RX_TO
Reset Value	0	0	0	0	0	0	0	0

Legacy UART Register: These registers are defined same as previous description.

Advanced UART Register:

Bit 7 *MIR, FIR modes:*

FLC_ACT - Flow Control Active

Set to 1 when the flow control occurs. Clear to 0 when this register is read. Note that this will be affected by Set5.Reg2 which control the SIR mode switches to MIR/FIR mode *or* MIR/FIR mode operated in DMA function switches to SIR mode.

Bit 6 *MIR, FIR modes:*

UNDRN - Underrun

Set to 1 when transmitter is empty *and* not set S_FEND (in this register bit 3) operated in PIO mode or not TC (Terminal Count) operated in DMA mode. Clear to 0 when write to 1.

Bit 5 *MIR, FIR modes:*

RX_BSY - Receiver Busy

Set to 1 when receiver is busy or active in process.

Remote IR mode:

RX_IP - Receiver in Process

Set to 1 when receiver is in process.

Bit 4: *MIR, FIR modes:*

LST_FE - Lost Frame End

Set to 1 when a frame end in a entire frame is lost. Clear to 0 when read this register.

Remote IR modes:

RX_PD - Receiver Pulse Detected

Set to 1 when one or more than one remote pulses are detected. Clear to 0 when read this register.

Bit 3 *MIR, FIR modes:*

S_FEND - Set a Frame End

Write to 1 when want to terminal the frame, that is, the procedure of PIO command is

An Entire Frame = Write Frame Data (First) + Write S_FEND (Last)

This bit should be set to 1, if use in PIO mode, to avoid transmitter underrun. Note that this bit S_FEND is set to 1 that is equivalent to TC (Terminal Count) in DMA mode. So that this bit should be set to 0 in DMA mode.

Bit 2: Reserved.

Bit 1: *MIR, FIR modes:*

LB_SF - Last Byte Stay in FIFO

Set to 1 that indicates one or more than one frame end still stay in receiver FIFO.

Bit 0: *MIR, FIR, Remote IR modes:*

RX_TO - Receiver FIFO or Frame Status FIFO time-out

Set to 1 when receiver FIFO *or* frame status FIFO occurs time-out

4.3.3 Set1 - Legacy Baud Rate Divisor Register

Address Offset	Register Name	Register Description
0	BLL	Baud Rate Divisor Latch (Low Byte)
1	BHL	Baud Rate Divisor Latch (High Byte)
2	ISR/UFR	Interrupt Status *or* UART FIFO Control Register
3	UCR/SSR	UART Control *or* Sets Select Register
4	HCR	Handshake Control Register
5	USR	UART Status Register
6	HSR	Handshake Status Register
7	UDR/ESCR	User Defined Register

4.3.3.1 Set1.Reg0~1 - Baud Rate Divisor Latch (BLL/BHL)

The two registers of BLL and BHL are baud rate divisor latch in the legacy UART/SIR/ASK-IR mode. Read/Write these registers, if set in Advanced UART mode, will occur backward operation, that is, will go to legacy UART mode and clear some register values shown table as follows.

Set & Register	Advanced Mode DIS_BACK=••	Legacy Mode DIS_BACK=0
Set 0.Reg 4	Bit 7~5	-
Set 2.Reg 2	Bit 0, 5, 7	Bit 5, 7
Set 4.Reg 3	Bit 2, 3	-

Note that DIS_BACK=1 (Disable Backward operation) in legacy UART/SIR/ASK-IR mode will not affect any register which that can operate legacy SIR/ASK-IR.

4.3.3.2 Set1.Reg 2~7

This registers is defined as same as Set 0 registers.

4.3.4 Set2 - Interrupt Status *or* UART FIFO Control Register (ISR/UFR)

These registers are only used in advanced modes.

Address Offset	Register Name	Register Description
0	ABLL	Advanced Baud Rate Divisor Latch (Low Byte)
1	ABHL	Advanced Baud Rate Divisor Latch (High Byte)
2	ADCR1	Advanced UART Control Register 1
3	SSR	Sets Select Register
4	ADCR2	Advanced UART Control Register 2
5	Reserved	-
6	TXFDTH	Transmitter FIFO Depth
7	RXFDTH	Receiver FIFO Depth

4.3.4.1 Reg0, 1 - Advanced Baud Rate Divisor Latch (ABLL/ABHL)

The two registers are same as legacy UART baud rate divisor latch in SET 1. Reg0~1. When use advanced UART/SIR/ASK-IR mode operation, should program these registers to set baud rate. That is to avoid to backward operation occurred.

4.3.4.2 Reg2 - Advanced UART Control Register 1 (ADCR1)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced UART	BR_OUT	-	EN_LOUT	D_CHSW	ALOOP	DMATHL	DMA_F	ADV_SL
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **BR_OUT - Baud Rate Clock Output**

Write to 1 then the programmed baud rate clock will output to DTR pin. This bit is only test baud rate divisor.

Bit 6: **Reserved,** write 0.

Bit 5: **EN_LOUT - Enable Loopback Output**

Write to 1, enable output transmitter data to IRTX pin during doing loopback operation. Setting this bit can check output data with internal data.

Bit 4: **D_CHSW - DMA TX/RX Channel Swap**

If use signal DMA channel in MIR/FIR mode, then the DMA channel can be swapped.

D_CHSW	DMA Channel Selected
0	Receiver (Default)
1	Transmitter

Write to 1, then enable output data during the ALOOP=1.

Bit 3: **ALOOP - All mode Loopback**

Write to 1, then enable loopback in all modes.

Bit 2: **DMATHL - DMA Threshold Level**

Set DMA threshold level as shown below table.

DMATHL	TX FIFO Threshold		RX FIFO Threshold (16/32-Byte)
	16-Byte	32-Byte	
0	13	13	4
1	23	7	10

Bit 1: **DMA_F - DMA Fairness**

DMA_F	Function Description
0	DMA request (DREQ) is forced inactive after 10.5us
1	No effect DMA request.

Bit 0: **ADV_SL - Advanced mode Select**

Write to 1, then advanced mode is selected.

4.3.4.3 Reg3 - Sets Select Register (SSR)

Read this register that returns $E0_{16}$. Write it to select other register Set.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
default Value	1	1	1	0	0	0	0	0

4.3.4.4 Reg4 - Advanced UART Control Register 2 (ADCR2)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced UART	DIS_BACK	-	PR_DIV1	PR_DIV0	RX_FSZ1	RX_FSZ0	TX_FSZ1	TXFSZ0
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **DIS_BACK - Disable Backward Operation**

Write to 1, read *or* write BLL or BHL (Baud rate Divisor Latch Register, in Set1.Reg0~1) will is disable backward legacy UART mode. When use legacy SIR/ASK-IR mode, this bit should be set to 1 to avoid backward operation.

Bit 6: **Reserved,** write 0.

Bit 5, 4: **PR_DIV1~0 - Pre-Divisor 1~0.**

These bits select pre-divisor for external input clock 24M Hz. The clock through the pre-divisor then input to baud rate divisor of UART.

PR_DIV1~0	Pre-divisor	Max. Baud Rate
00	13.0	**115.2K** bps
01	1.625	**921.6K** bps
10	6.5	**230.4K** bps
11	1	**1.5M** bps

Bit 3, 2: **RX_FSZ1~0 - Receiver FIFO Size 1~0**

These bits setup receiver FIFO size when FIFO is enable.

RX_FSZ1~0	RX FIFO Size
00	**16**-Byte
01	**32**-Byte
1X	Reserved

Bit 2, 0: **TX_FSZ1~0 - Transmitter FIFO Size 1~0**

These bits setup transmitter FIFO size when FIFO is enable.

TX_FSZ1~0	TX FIFO Size
00	**16**-Byte
01	**32**-Byte
1X	Reserved

4.3.4.5 Reg6 - Transmitter FIFO Depth (TXFDTH) (Read Only)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced UART	0	0	TXFD5	TXFD4	TXFD3	TXFD2	TXFD1	TXFD1
Reset Value	0	0	0	0	0	0	0	0

Bit 7~6: **Reserved,** Read 0.

Bit 5~0: Read these bits will return the current transmitter FIFO depth, that is, how many bytes are there in the transmitter FIFO.

4.3.4.6 Reg7 - Receiver FIFO Depth (RXFDTH) (Read Only)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced UART	0	0	RXFD5	RXFD4	RXFD3	RXFD2	RXFD1	RXFD1
Reset Value	0	0	0	0	0	0	0	0

Bit 7~6: **Reserved,** Read 0.

Bit 5~0: Read these bits will return the current receiver FIFO depth, that is, how many bytes are there in the receiver FIFO.

4.3.5 Set3 - Version ID *and* Mapped Control Registers

Address Offset	Register Name	Register Description
0	AUID	Advanced UART ID
1	MP_UCR	Mapped UART Control Register
2	MP_UFR	Mapped UART FIFO Control Register
3	SSR	Sets Select Register
4	Reversed	-
5	Reserved	-
6	Reserved	-
7	Reserved	-

4.3.5.1 Reg0 - Advanced UART ID (AUID)

This register is read only. Indicate that advanced UART version ID. Read it and return $1X_{16}$.

4.3.5.2 Reg1 - Mapped UART Control Register (MP_UCR)

Read only. Read this register that returns UART Control Register value of Set 0.

4.3.5.3 Reg2 - Mapped UART FIFO Control Register (MP_UFR)

Read only. Read this register that returns UART FIFO Control Register (UFR) value of SET 0.

4.3.5.4 Reg3 - Sets Select Register (SSR)

Read this register that returns $E4_{16}$. Write it to select other register Set.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
default Value	1	1	1	0	0	1	0	0

4.3.6 Set4 - TX/RX/Timer counter registers *and* IR control registers.

Address Offset	Register Name	Register Description
0	TMRL	Timer Value Low Byte
1	TMRH	Timer Value High Byte
2	IR_MSL	Infrared mode Select
3	SSR	Sets Select Register
4	TFRLL	Transmitter Frame Length Low Byte
5	TFRLH	Transmitter Frame Length High Byte
6	RFRLL	Receiver Frame Length Low Byte
7	RFRLH	Receiver Frame Length High Byte

4.3.6.1 Set4.Reg0, 1 - Timer Value Register (TMRL/TMRH)

This is a 12-bit timer which resolution is 1 ms, that is, the programmed maximum time is 2^{12}-1 ms. The timer is a down-counter. The timer start down count when the bit EN_TMR (Enable Timer) of Set4.Reg2. is set to 1. When the timer down count to *zero* and EN_TMR=1, the TMR_I is set to 1. When the counter down count to zero, a new initial value will be re-loaded into timer counter.

4.3.6.2 Set4.Reg2 - Infrared mode Select (IR_MSL)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced UART	-	-	-	-	IR_MSL1	IR_MSL0	TMR_TST	EN_TMR
Reset Value	0	0	0	0	0	0	0	0

Bit 7~4: **Reserved**, write to 0.

Bit 3, 2: **IR_MSL1, 0 - Infrared mode Select**

Select legacy UART or SIR or ASK-IR mode. Note that using legacy SIR/ASK-IR should set DIS_BACK=1 to avoid backward when program baud rate. Below is shown mode selected. Note that to avoid legacy backward operation, the bit of DIS_BACK (Disable Backward, in Set2.Reg4. Bit7) should be set to 1 when legacy ASK-IR mode or legacy SIR mode is selected.

IR_MSL1, 0	Operation Mode Selected
00	Legacy **UART**
01	Reserved
10	Legacy **ASK-IR**
11	Legacy **SIR**

Bit 1: **TMR_TST - Timer Test**

Write to 1, then reading the TMRL/TMRH will return the programmed values of TMRL/TMRH, that is, does not return down count counter value. This bit is for test timer register.

Bit 0: **EN_TMR - Enable Timer**

Write to 1, enable the timer.

4.3.6.3 Set4.Reg3 - Set Select Register (SSR)

Read this register returns $E8_{16}$. Write this register to select other Set.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
default Value	1	1	1	1	1	0	0	0

4.3.6.4 Set4.Reg4, 5 - Transmitter Frame Length (TFRLL/TFRLH)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TFRLL	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
Reset Value	0	0	0	0	0	0	0	0
TFRLH	-	-	-	bit 12	bit 11	bit 10	bit 9	bit 8
Reset Value	-	-	-	0	0	0	0	0

These are 13-bit registers. Write these registers then the transmitter frame length of a package will be programmed. These registers are only used in APM=1 (automatic package mode, Set5.Reg4.bit5). When APM=1, the physical layer will split data stream to a programmed frame length if the transmitted data is larger than the programmed frame length. When read these registers, they will return the number of bytes which is not transmitted from a frame length programmed.

4.3.6.5 Set4.Reg6, 7 - Receiver Frame Length (RFRLL/RFRLH)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFRLL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reset Value	0	0	0	0	0	0	0	0
RFRLH	-	-	-	bit 12	bit 11	bit 10	bit 9	bit 8
Reset Value	-	-	-	0	0	0	0	0

These are 13-bit registers and combined a 13-bit up counter. Program these registers, then the receiver frame length will be limited to the programmed frame length. If the received frame length is larger than the programmed receiver frame length, the bit of MX_LEX (Maximum Length Exceed) will be set to 1. Simultaneously, the receiver will not receive any data to RX FIFO until the next start flag in the next frame, which is defined in the physical layer IrDA 1.1, is reached and then the received data begin to write to RX FIFO. Read these registers will return the number of received data bytes from the receiver for a frame.

4.3.7 Set 5 - Flow control *and* IR control *and* Frame Status FIFO registers

Address Offset	Register Name	Register Description
0	**FCBLL**	Flow Control Baud Rate Divisor Latch Register (Low Byte)
1	**FCBHL**	Flow Control Baud Rate Divisor Latch Register (High Byte)
2	**FC_MD**	Flow Control Mode Operation
3	**SSR**	Sets Select Register
4	**IRCFG1**	Infrared Config Register
5	**FS_FO**	Frame Status FIFO Register
6	**RFRLFL**	Receiver Frame Length FIFO Low Byte
7	**RFRLFH**	Receiver Frame Length FIFO High Byte

4.3.7.1 Set5.Reg0, 1 - Flow Control Baud Rate Divisor Latch Register (FCDLL/ FCDHL)

If occurs flow control from MIR/FIR mode change to SIR mode, then the pre-programming baud rate of FCBLL/FCBHL are loaded to advanced baud rate divisor latch (ADBLL/ADBHL).

4.3.7.2 Set5.Reg2 - Flow Control mode Operation (FC_MD)

These registers control flow control mode operation as shown below table.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FC_MD	FC_MD2	FC_MD1	FC_MD0	-	FC_DSW	EN_FD	EN_BRFC	EN_FC
Reset Value	0	0	0	0	0	0	0	0

Bit 7~5 **FC_MD2 - Flow Control mode**

When occurs flow control state, these bits will be loaded to AD_MD2~0 of advanced HSR (Handshake Status Register). These three bits defined are same as AD_MD2~0.

Bit 4: **Reserved**, write 0.

Bit 3: **FC_DSW - Flow Control DMA Channel Swap**

Write to 1, when occurs flow control state, enable to swap DMA channel of both transmitter and receiver.

FC_DSW	Next Mode After Flow Control Occurred
0	Receiver Channel
1	Transmitter Channel

Bit 2: **EN_FD - Enable Flow DMA Control**

Write to 1, then enable to use DMA channel when flow control is occurred.

Bit 1: **EN_BRFC - Enable Baud Rate Flow Control**

Write to 1 then enable FC_BLL/FC_BHL (Flow Control Baud Rate Divider Latch, in Set5.Reg1~0) to be loaded to advanced baud rate divisor latch (ADBLL/ADBHL, in Set2.Reg1~0).

Bit 0: **EN_FC - Enable Flow Control**

Write to 1 then can use flow control function and bit 7~1 of this register can be activated.

4.3.7.3 Set5.Reg3 - Sets Select Register (SSR)

Write this register then change Set of register. Read this register will return EC_{16}.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
default Value	1	1	1	0	1	1	0	0

4.3.7.4 Set5.Reg4 - Infrared Config Register 1 (IRCFG1)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRCFG1	-	FSF_TH	FEND_M	AUX_RX	-	-	IRHSSL	IR_FULL
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved**, write 0.

Bit 6: **FSF_TH - Frame Status FIFO Threshold**

Set this bit to determine the frame status FIFO threshold level and to generate the FSF_I. The threshold level values are defined as follows.

FSF_TH	Status FIFO Threshold Level
0	2
1	4

Bit 5: **FEND_MD - Frame End mode**

Write to 1 then enable hardware automatically to split same length frame defined Set4.Reg4 and Set4.Reg5, i.e., TFRLL/TFRLH.

Bit 4: **AUX_RX - Auxiliary Receiver Pin**

Write to 1, select IRRX input pin. (Refer to Set7.Reg7.Bit5)

Bit 3~2: **Reserved**, write 0.

Bit 1: **IRHSSL - Infrared Handshake Status Select**

Write to 0, then the HSR (Handshake Status Register) is normal operation as same as UART. Write to 1, then HSR will be disable, and read HSR will return 30_{16}.

Bit 0: **IR_FULL - Infrared Full Duplex Operation**

Write to 0, then IR function is operated in half duplex. Write to 1, then IR function is operated in full duplex.

4.3.7.5 Set5.Reg5 - Frame Status FIFO Register (FS_FO)

This register are indicated the FIFO bottom of frame status.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FS_FO	FSFDR	LST_FR	-	MX_LEX	PHY_ERR	CRC_ERR	RX_OV	FSF_OV
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **FSFDR - Frame Status FIFO Data Ready**

Indicated that have a valid data in frame status FIFO bottom.

Bit 6: **LST_FR - Lost Frame**

Set to 1 when one or more than one frame has been lost.

Bit 5: **Reserved.**

Bit 4: **MX_LEX - Maximum Frame Length Exceed**

Set to 1 when exceed programmed maximum frame length defined Set4.Reg6 and Set4.Reg7. This bit is frame status FIFO bottom. To read this bit will return a valid value when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 3: **PHY_ERR - Physical Error**

During receiving data, any physical layer error, defined IrDA 1.1, will be set to 1 in this bit. This bit is frame status FIFO bottom. To read this bit will return a valid value when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 2: **CRC_ERR - CRC Error**

Set to 1 when receive a bad CRC in a frame. This CRC belongs to physical layer defined in IrDA 1.1. This bit is frame status FIFO bottom. To read this bit will return a valid value when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 1: **RX_OV - Received Data Overrun**

Set to 1 when Received data in FIFO occur overrun.

Bit 0: **FSF_OV - Frame Status FIFO Overrun**

Set to 1 When frame status FIFO occur overrun.

4.3.7.5 Set5.Reg6, 7 - Receiver Frame Length FIFO (RFLFL/RFLFH) or Lost Frame Number (LST_NU)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFLFL/ LST_NU	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Value	0	0	0	0	0	0	0	0
RFLFH	-	-	-	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset Value	0	0	0	0	0	0	0	0

Receiver Frame Length FIFO (RFLFL/RFLFH):

These registers are 13-bit. Read these registers will return received frame length. When read the register of *RFLFH* will pop-up another frame status and frame length if FSFDR=1 (Set5.Reg4.Bit7).

Lost Frame Number (LST_NU):

When LST_FR=1 (Set5.Reg4. Bit6), Reg6 is replaced to LST_NU, that is 8-bit register and read RFLFH will return 0. When read the register of *RFLFH* will pop-up another frame status and frame length if FSFDR=1 (Set5.Reg4.Bit7).

4.3.8 Set6 - IR Physical Layer Control Registers

Address Offset	Register Name	Register Description
0	IR_CFG2	Infrared Config Register 2
1	MIR_PW	MIR (1.152M bps or 0.576M bps) Pulse Width
2	SIR_PW	SIR Pulse Width
3	SSR	Sets Select Register
4	HIR_FNU	High Speed Infrared Flag Number
5	Reserved	-
6	Reserved	-
7	Reserved	-

4.3.8.1 Set6.Reg0 - Infrared Config Register 2 (IR_CFG2)

This register config ASK-IR, MIR, FIR operation function.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IR_CFG2	SHMD_N	SHDM_N	FIR_CRC	MIR_CRC	-	INV_CRC	DIS_CRC	-
Reset Value	0	0	1	0	0	0	0	0

Bit 7: **SHMD_N - ASK-IR Modulation Disable**

SHMD_N	Modulation Mode
0	SOUT modulate 500K Hz Square Wave
1	Re-rout SOUT

Bit 6: **SHDM_N - ASK-IR Demodulation Disable**

SHDM_N	Demodulation Mode
0	Demodulation 500K Hz
1	Re-rout SIN

Bit 5: **FIR_CRC - FIR (4M bps) CRC Type**

FIR_CRC	CRC Type
0	16-bit CRC
1	32-bit CRC

Note that the 16/32-bit CRC are defined in IrDA 1.1 physical layer.

Bit 4: **MIR_CRC - MIR (1.152M/0.576M bps) CRC Type**

MIR_CRC	CRC Type
0	16-bit CRC
1	32-bit CRC

Bit 2: **INV_CRC - Inverting CRC**

Write to 1 then the CRC is inverted output in physical layer.

Bit 1: **DIS_CRC - Disable CRC**

Write to 1 then the transmitter does not transmit CRC in physical layer.

Bit 0: **Reserved**, write 1.

4.3.8.2 Set6.Reg1 - MIR (1.152M/0.576M bps) Pulse Width

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIR_PW	-	-	-	M_PW4	M_PW3	M_PW2	M_PW1	M_PW0
Reset Value	0	0	0	0	1	0	1	0

This 5-bit register is set MIR output pulse width.

M_PW4~0	MIR Pulse Width (1.152M bps)	MIR Output Width (0.576M bps)
00000	**0** ns	**0** ns
00001	**20.83** ns	**41.66** ns
00010	**41.66** (==20.83*2) ns	**83.32** (==41.66*2) ns
...	...	...
k_{10}	**20.83*k_{10}** ns	**41.66*k_{10}** ns
...	...	...
11111	**645** ns	**1290** ns

4.3.8.3 Set6.Reg2 - SIR Pulse Width

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIR_PW	-	-	-	S_PW4	S_PW3	S_PW2	S_PW1	S_PW0
Reset Value	0	0	0	0	0	0	0	0

This 5-bit register is set SIR output pulse width.

S_PW4~0	SIR Output Pulse Width
00000	**3/16 bit time** of UART
01101	**1.6** us
Others	**1.6** us

4.3.8.4 Set6.Reg3 - Set Select Register

Write this register then go to other Set. Read this register then return $F0_{16}$.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
default Value	1	1	1	1	0	0	0	0

4.3.8.5 Set6.Reg4 - High Speed Infrared Beginning Flag Number (HIR_FNU)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HIR_FNU	M_FG3	M_FG2	M_FG1	M_FG0	F_FL3	F_FL2	F_FL1	F_FL0
Reset Value	0	0	1	0	1	0	1	0

Bit 7~4: **M_FG3~0 - MIR beginning Flag Number**

These bits define the number of transmitter *Start Flag* of MIR. Note that the number of MIR start flag should be equal or more than *two* which is defined in IrDA 1.1 physical layer. The default value is 2.

M_FG3~0	Beginning Flag Number
0000	Reserved
0001	1
0010	2 (Default)
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16
1011	20
1100	24
1101	28
1110	32
1111	Reserved

Bit 3~0: **F_FG3~0 - FIR Beginning Flag Number**

These bits define the number of transmitter *Preamble Flag* in FIR. Note that the number of FIR start flag should be equal to *sixteen* which is defined in IrDA 1.1 physical layer. The default value is 16.

M_FG3~0	Beginning Flag Number
0000	Reserved
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	**16** (Default)
1011	20
1100	24
1101	28
1110	32
1111	Reserved

4.3.9 Set7 - Remote control *and* IR module selection registers

Address Offset	Register Name	Register Description
0	**RIR_RXC**	Remote Infrared Receiver Control
1	**RIR_TXC**	Remote Infrared Transmitter Control
2	**RIR_CFG**	Remote Infrared Config Register
3	**SSR**	Sets Select Register
4	**IRM_SL1**	Infrared Module (Front End) Select 1
5	**IRM_SL2**	Infrared Module Select 2
6	**IRM_SL3**	Infrared Module Select 3
7	**IRM_CR**	Infrared Module Control Register

4.3.9.1 Set7.Reg0 - Remote Infrared Receiver Control (RIR_RXC)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIR_RXC	RX_FR2	RX_FR1	RX_FR0	RX_FSL4	RX_FSL3	RX_FSL2	RX_FSL1	RX_FSL0
default Value	0	0	1	0	1	0	0	1

This register defines frequency ranges of remote IR of receiver.

Bit 7~5: **RX_FR2~0 - Receiver Frequency Range 2~0.**

These bits select the input frequency of the receiver ranges. For the input signal, that is through a band pass filter, i.e., the frequency of the input signal is located at this defined range then the signal will be received.

Bit 4~0: **RX_FSL4~0 - Receiver Frequency Select 4~0.**

Select the receiver operation frequency.

Table: Low Frequency range select of receiver.

	RX_FR2~0 (Low Frequency)					
	001		010		011	
RX_FSL4~0	Min.	Max.	Min.	Max.	Min.	Max.
00010	26.1	29.6	24.7	31.7	23.4	34.2
00011	28.2	32.0	26.7	34.3	25.3	36.9
00100	29.4	33.3	27.8	35.7	26.3	38.4
00101	30.0	34.0	28.4	36.5	26.9	39.3
00110	31.4	35.6	29.6	38.1	28.1	41.0
00111	32.1	36.4	30.3	39.0	28.7	42.0
01000	32.8	37.2	31.0	39.8	29.4	42.9
01001	***33.6****	***38.1****	31.7	40.8	30.1	44.0
01011	34.4	39.0	32.5	41.8	30.8	45.0
01100	36.2	41.0	34.2	44.0	32.4	47.3
01101	37.2	42.1	35.1	45.1	33.2	48.6
01111	38.2	43.2	36.0	46.3	34.1	49.9
10000	40.3	45.7	38.1	49.0	36.1	52n.7
10010	41.5	47.1	39.2	50.4	37.2	54.3
10011	42.8	48.5	40.4	51.9	38.3	56.0
10101	44.1	50.0	41.7	53.6	39.5	57.7
10111	45.5	51.6	43.0	55.3	40.7	59.6
11010	48.7	55.2	46.0	59.1	43.6	63.7
11011	50.4	57.1	47.6	61.2	45.1	65.9
11101	54.3	61.5	51.3	65.9	48.6	71.0

Note that the other non-defined values are reserved.

Table: High Frequency range select of receiver

	RX_FR2~0 (High Frequency)	
	001	
RX_FSL4~0	Min.	Max.
00011	355.6	457.1
01000	380.1	489.8
01011	410.3	527.4

Note that the other non-defined values are reserved.

Table: SHARP ASK-IR receiver frequency range select.

RX_FSL4~0 (SHARP ASK-IR)												
RX_FR2~0	001		010		011		100		101		110	
-	***480.0****	***533.3****	457.1	564.7	436.4	600.0	417.4	640.0	400.0	685.6	384.0	738.5

Note that the other non-defined values are reserved.

4.3.9.1 Set7.Reg1 - Remote Infrared Transmitter Control (RIR_TXC)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIR_TXC	TX_PW2	TX_PW1	TX_PW0	TX_FSL4	TX_FSL3	TX_FSL2	TX_FSL1	TX_FSL0
default Value	0	1	1	0	1	0	0	1

This Register is defined the transmitter frequency and pulse width of remote IR.

Bit 7~5: **TX_PW2~0 - Transmitter Pulse Width 2~ 0.**

Select the transmission pulse width.

TX_PW2~0	Low Frequency	High Frequency
010	6 μs	0.7 μs
011	7 μs	0.8 μs
100	9 μs	0.9 μs
101	10.6 μs	1.0 μs

Note that the other non-defined TX_PW are reserved.

Bit 4~0: **TX_FSL4~0 - Transmitter Frequency Select 4~0.**

Select the transmission frequency.

Table: Low frequency selected.

TX_FSL4~0	Low Frequency
00011	30K Hz
00100	31K HZ
...	...
11101	56K Hz

Note that the other non-defined TX_FSL4~0 are reserved.

Table: High frequency selected.

TX_FSL4~0	High Frequency
00011	400K Hz
01000	450K Hz
01011	480K Hz

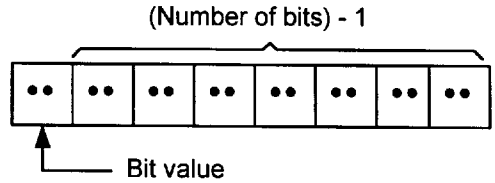
Note that the other non-defined TX_FSL4~0 are reserved.

4.3.9.2 Set7.Reg2 - Remote Infrared Config Register (RIR_CFG)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIR_CFG	P_PNB	SMP_M	RXCFS	-	TX_CFS	RX_DM	TX_MM1	TX_MM0
default Value	0	0	0	0	0	0	0	0

Bit 7: **P_PNB: Programming Pulse Number Coding.**

Write to 1 then programming pulse number coding is selected. The code format is defined as follows.



The bit value is set to 0, then the high pulse will be transmitted/received. The bit value is set to 1, then no energy will be transmitted/received.

Bit 6: **SMP_M - Sampling mode.**

To choose receiver sampling mode.

Write to 0 then uses T-period sampling, that the T-period is programmed UART baud rate.

Write to 1 then directly use programmed baud rate to do over-sampling.

Bit 5: **RXCFS - Receiver Carry Frequency Select**

RXCFS	Selected Frequency
0	30K ~ 56K Hz
1	400K ~ 480K Hz

Bit 4: **Reserved,** write 0.

Bit 3: **TX_CFS - Transmitter Carry Frequency Select.**

Setting low speed or high speed transmitter carry frequency.

TX_FCS	Selected Frequency
0	30K ~ 56K Hz
1	400K ~ 480K Hz

Bit 2: **RX_DM - Receiver Demodulation mode.**

RX_DM	Demodulation Mode
0	Enable internal decoder
1	Disable internal decoder

Bit 1~0: **TX_MM1~0 - Transmitter Modulation mode 1~0**

TX_MM1~0	TX Modulation Mode
00	Continuously send pulse for logic 0
01	**8 pulses** for logic 0 and no pulse for logic 1.
10	**6 pulses** for logic 0 and no pulse for logic 1
11	Reserved.

4.3.9.3 Set7.Reg3 - Sets Select Register (SSR)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
default Value	1	1	1	1	0	1	0	0

Read this register and return $F4_{16}$. Write this register then switch to other Set.

4.3.9.4 Set7.Reg4 - Infrared Module (Front End) Select 1 (IRM_SL1)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_SL1	IR_MSP	SIR_SL2	SIR_SL1	SIR_SL0	-	AIR_SL2	AIR_SL1	AIR_SL0
default Value	0	0	0	0	0	0	0	0

Bit 7: **IR_MSP - IR mode Select Pulse**

Write to 1, the transmitter (IRTX) will send a 64 μs pulse to setup a special IR front-end operational mode. When IR front-end module uses *mode select pin (MD)* and *transmitter IR pulse (IRTX)* to switch high speed IR (such as FIR or MIR) or low speed IR (SIR or ASK-IR), this bit should be used.

Bit 6~4: **SIR_SL2~0 - SIR (Serial IR) mode select.**

These bits are to program the operational mode of the SIR front-end module. These values of SIR_SL2~0 will automatically load to pins of IR_SL2~0, respectively, when (1) AM_FMT=1 (Automatic Format, in Set7.Reg7.Bit7), (2) the mode of Advanced UART is set to SIR (AD_MD2~0, in Set0.Reg4.Bit7~0).

Bit 3: **Reserved,** write 0.

Bit 2~0: **AIR_SL2~0 - ASK-IR mode Select.**

These bits will setup the operational mode of ASK-IR front-end module when AM_FMT=1 *and* AD_MD2~0 are set to ASK-IR mode. These values will automatically load to IR_SL2~0, respectively.

4.3.9.5 Set7.Reg5 - Infrared module (Front End) Select 2 (IRM_SL2)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_SL2	-	FIR_SL2	FIR_SL1	FIR_SL0	-	MIR_SL2	MIR_SL1	MIR_SL0
default Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved,** write 0.

Bit 6~4: **FIR_SL2~0 - FIR mode select.**

These bits setup the operational mode of FIR front-end module when AM_FMT=1 and AD_MD2~0 set to FIR mode. These values will automatically load to IR_SL2~0, respectively.

Bit 3: **Reserved,** write 0.

Bit 2~0: **MIR_SL2~0 - MIR mode Select.**

These bits setup the MIR operational mode when AM_FMT=1 *and* AD_MD2~0 set to MIR mode. These values will be automatically loaded to IR_SL2~0, respectively.

4.3.9.6 Set7.Reg6 - Infrared module (Front End) Select 3 (IRM_SL3)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_SL3	-	LRC_SL2	LRC_SL1	LRC_SL0	-	HRC_SL2	HRC_SL1	HRC_SL0
default Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved,** write 0.

Bit 6~4: **LRC_SL2~0 - Low Speed Remote IR mode select.**

These bits setup the operational mode of *low speed* remote IR front-end module when AM_FMT=1 and AD_MD2~0 set to Remote IR mode. These values will automatically load to IR_SL2~0, respectively.

Bit 3: **Reserved,** write 0.

Bit 2~0: **HRC_SL2~0 - High Speed Remote IR Mode Select.**

These bits setup the operational mode of *high speed* remote IR front-end module when AM_FMT=1 and .AD_MD2~0 set to Remote IR mode. These values will automatically load to IR_SL2~0, respectively.

4.3.9.7 Set7.Reg7 - Infrared module Control Register (IRM_CR)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_CR	AM_FMT	IRX_MSL	IRSL0D	RXINV	TXINV	-	-	-
default Value	0	0	0	0	0	0	0	0

Bit 7: **AM_FMT - Automatic Format**

Write to 1, enable automatic format IR front-end module. These bit will affect the output of IR_SL2~0 which is referred by IR front-end module selection (Set7.Reg4~6)

Bit 6: **IRX_MSL - IR Receiver module Select**

Select the receiver input path from the IR front end module if IR module has the separated high speed and low speed receiver path. If the IR module is only one receiving path, then this bit should be set to 0.

IRX_MSL	Receiver Pin selected
0	IRRX (Low/High Speed)
1	IRRXH (High Speed)

Bit 5: **IRSL0D - Direction of IRSL0 Pin**

Select function for IRRXH or IRSL0 because they are common pin and different input/output direction.

IRSL0_D	Function
0	IRRXH (I/P)
1	IRSL0 (O/P)

Table: IR receiver input pin selection

IRSL0D	IRX_MSL	AUX_RX	High Speed IR	Selected IR Pin
0	0	0	X	**IRRX**
0	0	1	X	**IRRXH**
0	1	X	0	**IRRX**
0	1	X	1	**IRRXH**
1	0	0	X	**IRRX**
1	0	1	X	Reserved
1	1	X	0	**IRRX**
1	1	X	1	Reserved

Note that (1) AUX_RX is defined in Set5.Reg4.Bit4, (2) high speed IR includes MIR (1.152M or 0.576M bps) and FIR (4M bps), (3) IRRX is the input of the low speed or high speed IR receiver, IRRXH is the input of the high speed IR receiver.

Bit 4: **RXINV - Receiving Signal Invert**

Write to 1, Invert the receiving signal.

Bit 3: **TXINV - Transmitting Signal Invert**

Write to 1, Invert the transmitting signal.

Bit 2~0: **Reserved,** write 0.

5.0 PARALLEL PORT

5.1 Printer Interface Logic

The parallel port of the W83877AF makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The W83877AF supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), Extension 2FDD mode (EXT2FDD), Extension Adapter mode (EXTADP), and JOYSTICK mode on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation.

Table 5-1 shows the pin definitions for different modes of the parallel port.

TABLE 5-1-A Parallel Port Connnector and Pin Definition for SPP/EPP/ECP Modes

HOST CONNECTOR	PIN NUMBER OF W83877AF	PIN ATTRIBUTE	SPP	EPP	ECP
1	19	O	nSTB	nWrite	nSTB, HostClk
2-9	9-14,16-17	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	26	I	nACK	Intr	nACK, PeriphClk
11	24	I	BUSY	nWait	BUSY, PeriphAck[2]
12	27	I	PE	PE	PEerror, nAckReverse[2]
13	28	I	SLCT	Select	SLCT, Xflag
14	20	O	nAFD	nDStrb	nAFD, HostAck[2]
15	29	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	21	O	nINIT	nInit	nINIT[1], nReverseRqst[2]
17	22	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, refer to the IEEE 1284 standard.

TABLE 5-1-B Parallel Port Connector and Pin Definition for EXTFDD and EXT2FDD Modes

HOST CONNECTOR	PIN NUMBER OF W83877A	PIN ATTRIBUTE	SPP	PIN ATTRIBUTE	EXT2FDD	PIN ATTRIBUTE	EXTFDD
1	19	O	nSTB	---	---	---	---
2	9	I/O	PD0	I	$\overline{\text{INDEX2}}$	I	$\overline{\text{INDEX2}}$
3	10	I/O	PD1	I	$\overline{\text{TRAK02}}$	I	
4	11	I/O	PD2	I	$\overline{\text{WP2}}$	I	
5	12	I/O	PD3	I	$\overline{\text{RDATA2}}$	I	$\overline{\text{RDATA2}}$

TABLE 5-1-B, continued

HOST CONNECTOR	PIN NUMBER OF W83877A	PIN ATTRIBUTE	SPP	PIN ATTRIBUTE	EXT2FDD	PIN ATTRIBUTE	EXTFDD
6	13	I/O	PD4	I	$\overline{\text{DSKCHG2}}$	I	$\overline{\text{DSKCHG2}}$
7	14	I/O	PD5	---	---	---	---
8	15	I/O	PD6	OD	$\overline{\text{MOA2}}$	---	---
9	16	I/O	PD7	OD	$\overline{\text{DSA2}}$	---	---
10	26	I	nACK	OD	$\overline{\text{DSB2}}$	OD	
11	24	I	BUSY	OD	$\overline{\text{MOB2}}$	OD	
12	27	I	PE	OD	$\overline{\text{WD2}}$	OD	$\overline{\text{WD2}}$
13	28	I	SLCT	OD	$\overline{\text{WE2}}$	OD	$\overline{\text{WE2}}$
14	20	O	nAFD	OD	$\overline{\text{RWC2}}$	OD	$\overline{\text{RWC2}}$
15	29	I	nERR	OD	$\overline{\text{NERR2}}$	OD	
16	21	O	nINIT	OD	$\overline{\text{DIR2}}$	OD	$\overline{\text{DIR2}}$
17	22	O	nSLIN	OD	$\overline{\text{STEP2}}$	OD	

TABLE 5-1-C Parallel Port Connector and Pin Definition for EXTADP Mode

HOST CONNECTOR	PIN NUMBER OF W83877A	PIN ATTRIBUTE	SPP	PIN ATTRIBUTE	EXTADP MODE	PIN ATTRIBUTE	JOYSTIC K MODE
1	19	O	nSTB	O	$\overline{\text{XWR}}$	O	VDD
2	9	I/O	PD0	I/O	XD0	I	JP0
3	10	I/O	PD1	I/O	XD1	I	JP1
4	11	I/O	PD2	I/O	XD2	I	---
5	12	I/O	PD3	I/O	XD3	I	---
6	13	I/O	PD4	I/O	XD4	I	JB0
7	14	I/O	PD5	I/O	XD5	I	JB1
8	15	I/O	PD6	I/O	XD6	I	---
9	16	I/O	PD7	I/O	XD7	I	---
10	26	I	nACK	I	XDRQ	I	---
11	24	I	BUSY	I	XIRQ	I	---
12	27	I	PE	O	XA0	I	---
13	28	I	SLCT	O	XA1	I	---
14	20	O	nAFD	O	$\overline{\text{XRD}}$	O	VDD
15	29	I	nERR	O	XA2	I	---
16	21	O	nINIT	O	$\overline{\text{XDACK}}$	O	VDD
17	22	O	nSLIN	O	TC	O	VDD

5.2 Enhanced Parallel Port (EPP)

TABLE 5-2 PRINTER MODE AND EPP REGISTER ADDRESS

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

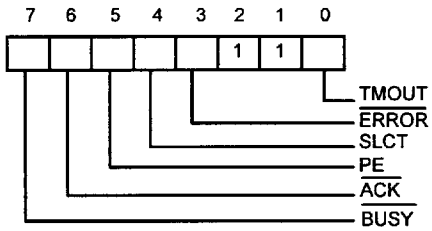
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

5.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

5.2.2 Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:



Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's $\overline{ACK}$ signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{BUSY}$ stops.

Bit 5: A 1 means the printer has detected the end of paper.

Bit 4: A 1 means the printer is selected.

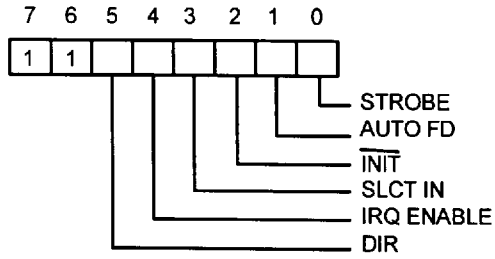
Bit 3: A 0 means the printer has encountered an error condition.

Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.

Bit 0: This bit is valid in EPP mode only. It indicates that a 10 μS time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

5.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



Bit 7, 6: These two bits are a logic one during a read. They can be written.

Bit 5: Direction control bit

When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4: A 1 in this position allows an interrupt to occur when $\overline{ACK}$ changes from low to high.

Bit 3: A 1 in this bit position selects the printer.

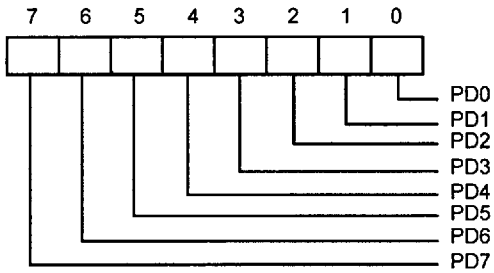
Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

5.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

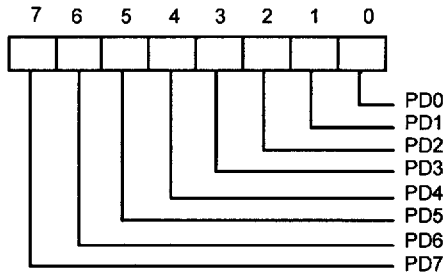


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of $\overline{IOW}$ causes an EPP address write cycle to be performed, and the trailing edge of $\overline{IOW}$ latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of $\overline{IOR}$ causes an EPP address read cycle to be performed and the data to be output to the host CPU.

5.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of $\overline{IOW}$ causes an EPP data write cycle to be performed, and the trailing edge of $\overline{IOW}$ latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of $\overline{IOR}$ causes an EPP read cycle to be performed and the data to be output to the host CPU.

5.2.6 Bit Map of Parallel Port and EPP Registers

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	$\overline{\text{BUSY}}$	$\overline{\text{ACK}}$	PE	SLCT	$\overline{\text{ERROR}}$	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	$\overline{\text{INIT}}$	$\overline{\text{AUTOFD}}$	$\overline{\text{STROBE}}$
Control Latch (Write)	1	1	DIR	IRQ	SLIN	$\overline{\text{INIT}}$	$\overline{\text{AUTOFD}}$	$\overline{\text{STROBE}}$
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

5.2.7 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
nWrite	O	Denotes an address or data read or write operation.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
nWait	I	Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer selected status; same as SPP mode.
nDStrb	O	This signal is active low. It denotes a data read or write operation.
nError	I	Error; same as SPP mode.
nInits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
nAStrb	O	This signal is active low. It denotes an address read or write operation.

5.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time $\overline{WAIT}$ is de-asserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

5.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

5.3.1 ECP Register and Mode Definitions

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR23, which are determined by configuration register or hardware setting.

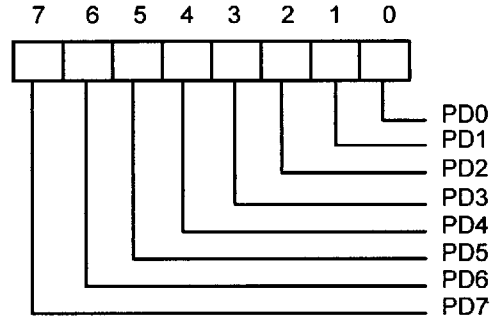
MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

5.3.2 Data and ecpAFifo Port

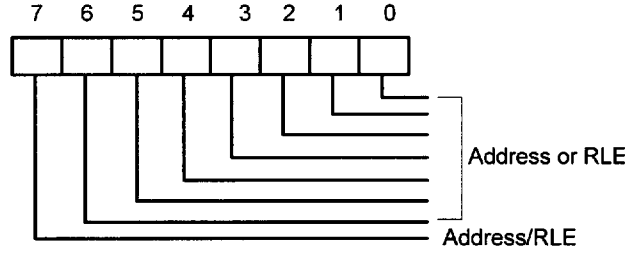
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a wite operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



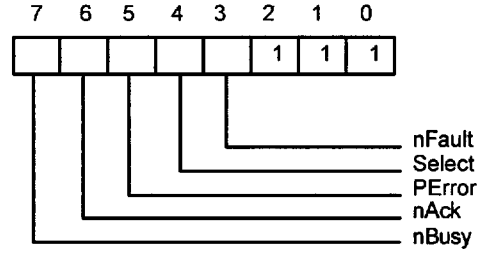
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:



5.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:



Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

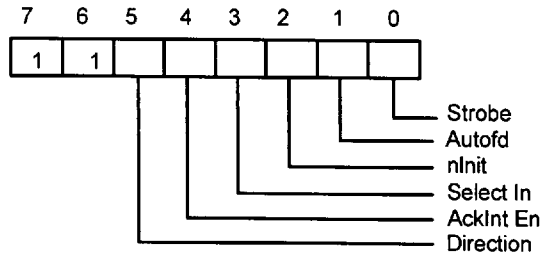
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logic one during a read.

5.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Bit 6, 7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0 the parallel port is in output mode.

1 the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the $\overline{ACK}$ input.

Bit 3: This bit is inverted and output to the $\overline{SLIN}$ output.

0 The printer is not selected.

1 The printer is selected.

Bit 2: This bit is output to the $\overline{INIT}$ output.

Bit 1: This bit is inverted and output to the $\overline{AFD}$ output.

Bit 0: This bit is inverted and output to the $\overline{STB}$ output.

5.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

5.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

5.3.7 tFifo (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction.

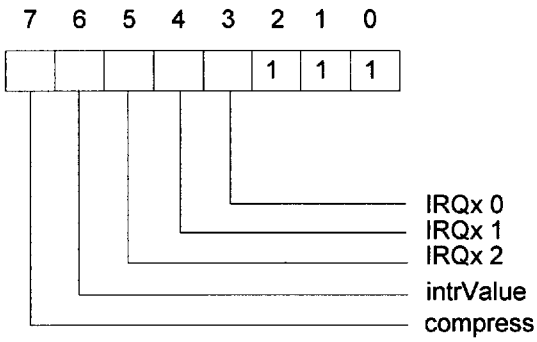
Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

5.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

5.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

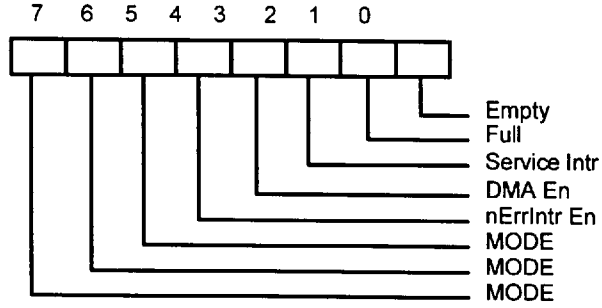
Bit 5-3: Reflect the IRQ resource assigned for ECP port.

cnfgB[5:3]	IRQ resource
000	reflect other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

Bit 2-0: These five bits are at high level during a read and can be written.

5.3.11 ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: These bits are read/write and select the mode.

000 Standard Parallel Port mode. The FIFO is reset in this mode.

001 PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.

010 Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.

011 ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. When the direction is 1 (reverse direction) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.

100 Selects EPP Mode. In this mode, EPP is active if the EPP supported option is selected.

101 Reserved.

110 Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.

111 Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

1 Disables the interrupt generated on the asserting edge of nFault.

0 Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

1 Enables DMA.

0 Disables DMA unconditionally.

Bit 2: Read/Write

1 Disables DMA and all of the service interrupts.

0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.

(a) dmaEn = 1:

During DMA this bit is set to a 1 when terminal count is reached.

(b) dmaEn = 0 direction = 0:

This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.

(c) dmaEn = 0 direction = 1:

This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0 The FIFO has at least 1 free byte.

1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

0 The FIFO contains at least 1 byte of data.

1 The FIFO is completely empty.

5.3.11 Bit Map of ECP Port Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
dcr	1	1	Directio	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

5.3.12 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe (HostClk)	O	The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contains address or data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutofd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low.
nFault (nPeriphRequest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

5.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

Mode Switching

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

Data Compression

The W83877AF supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

5.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

5.3.15 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, which will disable the DMA.

5.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. The host must set the direction, state, dmaEn = 0 and serviceIntr = 0 in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

5.4 Extension FDD Mode (EXTFDD)

In this mode, the W83877AF changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 5-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOB}}$ and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

5.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83877AF changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table 5-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOA}}$, $\overline{\text{DSA}}$, $\overline{\text{MOB}}$, and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, and $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

5.6 Extension Adapter Mode (EXTADP) (Patent pending)

In this mode, the W83877AF redefines the printer interface pins for use as an extension adapter, allowing a pocket peripheral adapter card to be installed through the DB-25 printer connector. The pin assignments for the extension adapter are shown in table 5-1.

XD0-XD7 are the system data bus for the extension adapter.

XA0-XA2 are the system address bus.

$\overline{XWR}$ and $\overline{XRD}$ are the I/O read/write commands with address comparing match or in DMA access mode.

$\overline{XDACK}$, XTC, and XDRQ are used in conjunction with $\overline{PDACKX}$, TC, and PDRQX to execute a DMA cycle.

The extension adapter can issue a DMA request by setting pin XDRQ high, thus sending the W83877AF output to the host system by pin PDRQX. The DMA controller should recognize the DMA request and output a relative $\overline{DACK}$ to pin $\overline{PDACKX}$ of the W83877AF, which will output the DACK without any change from pin $\overline{XDACK}$ to the extension adapter. Once the DMA transfer is completed, a terminal count (TC) should be issued from the DMA controller to pin TC of W83877AF and output to the extension adapter via pin XTC. XIRQ is the interrupt request of the extension adapter. The value of XIRQ coming from the extension adapter will directly pass through pin IRQ7 to the host system.

XIRQ and IRQ7, $\overline{XDACK}$ and $\overline{PDACKX}$, and XDRQ and PDRQX are three input/output pairs of W83877AF pins. Although these pins are defined as DMA and interrupt functions, they can be redefined by users for other specific functions.

5.6.1 Operation

The idea behind EXTADP mode is to treat the parallel port DB-25 connector as an ISA slot, except that its addresses are not issued to the extension adapter. The operation of EXTADP mode is described below:

1. Set the W83877AF to EXTADP mode by programming bit 7 of CR7 as low and bit 3 and bit 2 of CR0 as high and low, respectively.
2. The W83877AF CR2 is an address register that records the address of the extension adapter. When the desired address is written into CR2, pins $\overline{XWR}$ and $\overline{XRD}$ of the W83877AF will simultaneously go low and the desired address will also appear on the printer data bus PD7-PD0. Users can logically OR these two signals as an initial reset.
3. After the above two steps, every time the host system issues an IOR or IOW command, the W83877AF will compare the I/O address with the CR2 register. If the comparison matches, the data, low bits addresses (XA2-XA0), and $\overline{XWR}$/$\overline{XRD}$ will be presented on the parallel port DB-25 connector.
4. DMA operations are handled in the same way as item 3, except that the relevant $\overline{PDACKX}$, PDRQX will be active on the DB-25 connector.

5.7 Joystick Mode (Patent pending)

The joystick mode allows users to plug a joystick into the parallel port DB-25 connector. The pin definitions are shown in Table 5-1.

Pins $\overline{NSTB}$, $\overline{AFD}$, $\overline{NSLIN}$, and $\overline{INIT}$ output high as a voltage supply to the joystick.

Pins PD5 and PD4 are the button input of the joystick.

Pins PD1 and PD0 are the X/Y axis paddle input of the joystick.

There are two one-shot timers (556) inside the W83877AF for use with the joystick.

6.0 GAME PORT DECODER

The W83877AF provides $\overline{GMRD}$ and $\overline{GMWR}$ pins that decode game port address as specified in CR1E and I/O read/write commands.

If the host issues $\overline{IOR}$ and the specified address, the $\overline{GMRD}$ pin is low active; if it issues $\overline{IOW}$ and the specified address, the $\overline{GMWR}$ pin is low active.

7.0 PLUG AND PLAY CONFIGURATION

A powerful new plug-and-play function has been built into the W83877AF to help simplify the task of setting up a computer environment. With appropriate support from BIOS manufacturers, the system designer can freely allocate Winbond I/O devices (i.e., the FDC, PRT, UART, IDE, and game port) in the PC's I/O space (100H - 3FFH). In addition, the W83877AF also provides 8 interrupt requests and 3 DMA pairs for designers to assign in interfacing FDCs, UARTs, and PRTs. Hence this powerful I/O chip offers greater flexibility for system designers.

The PnP feature is implemented through a set of Extended Function Registers (CR1E and CR20 to 29). Details on configuring these registers are given in Section 8. The default values of these PnP-related registers set the system to a configuration compatible with environments designed with previous Winbond I/O chips.

8.0 EXTENDED FUNCTION REGISTERS

The W83877AF provides many configuration registers for setting up different types of configurations. After power-on reset, the state of the hardware setting of each pin will be latched by the relevant configuration register to allow the W83877AF to enter the proper operating configuration. To protect the chip from invalid reads or writes, the configuration registers cannot be accessed by the user.

There are four ways to enable the configuration registers to be read or written. HEFERE (CR0C bit 5) and HEFRAS (CR16 bit 0) can be used to select one out of these four methods of entering the Extended Function mode as follows:

HEFRAS	HEFERE	address and value
0	0	write 88H to the location 250H
0	1	write 89H to the location 250H (power-on default)
1	0	write 86H to the location 3F0H twice
1	1	write 87H to the location 3F0H twice

First, a specific value must be written once (88H/89H) or twice (86H/87H) to the Extended Functions Enable Register (I/O port address 250H or 3F0H). Second, an index value (00H-17H, 1EH, 20H-29H) must be written to the Extended Functions Index Register (I/O port address 251H or 3F0H) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 252H or 3F1H).

After programming of the configuration register is finished, an additional value should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. In the case of EFER at 250H, this additional value can be any value other than 88H if HEFERE = 0 and 89H if HEFERE = 1. While EFER is at 3F0H, this additional value must be AAH. The designer can also set bit 6 of CR9 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

8.1 Extended Functions Enable Registers (EFERs)

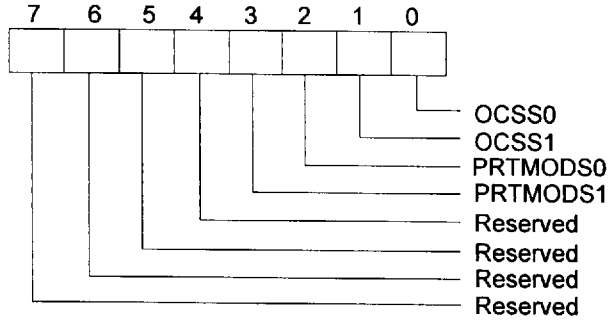
After a power-on reset, the W83877AF enters the default operating mode. Before the W83877AF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 250H or 3F0H (as described in the above section).

8.2 Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (0H, 1H, 2H, ..., or 29H) to access Configuration Register 0 (CR0), Configuration Register 1 (CR1), Configuration Register 2 (CR2), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 251H or 3F0H (as described in section 8.0) on PC/AT systems; the EFDRs are read/write registers with port address 252H or 3F1H (as described in section 8.0) on PC/AT systems. The function of each configuration register is described below.

8.2.1 Configuration Register 0 (CR0), default = 00H

When the device is in Extended Function mode and EFIR is 0H, the CR0 register can be accessed through EFDR. The bit definitions for CR0 are as follows:



Bit 7-Bit 4: Reserved.

PRTMOD1 PRTMOD0 (Bit 3, Bit 2):

These two bits and PRTMOD2 (CR9 bit7) determine the parallel port mode of the W83877A (as shown following Table).

Table:

PRTMODS2 (BIT 7 OF CR9)	PRTMOD1 (BIT 3 OF CR0)	PRTMODS0 (BIT 2 OF CR0)	
0	0	0	SPP
0	0	1	EXTFDC
0	1	0	EXTADP
0	1	1	EXT2FDD
1	0	0	JOYSTICK
1	0	1	EPP/SPP
1	1	0	ECP
1	1	1	ECP/EPP

00 SPP Mode (Default), PRTMOD2 = 0; Standard and Bi-directional Modes
01 Extension FDD Mode (EXTFDD), PRTMOD2 = 0
10 Extension Adapter Mode (EXTADP), PRTMOD2 = 0
11 Extension 2FDD Mode (EXT2FDD), PRTMOD2 = 0
00 JOYSTICK Mode, PRTMOD2 = 1
01 EPP Mode and SPP Mode, PRTMOD2 = 1
10 ECP Mode, PRTMOD2 = 1
11 ECP Mode and EPP Mode, PRTMOD2 = 1

OSCS1, OSCS0 (Bit 1, Bit 0):

These two bits and OSCS2 (CR6 bit 6) are used to select one of the W83877AF's power-down functions. These bits may be programmed in four different ways:

00 Default power-on state after power-on reset (OSCS2 = 0).

00 OSC on, 24 MHz clock is stopped internally (OSCS2 = 1). Clock can be restarted by clearing OSCS2.

01 Immediate power-down (IPD) state, OSCS2 = 0

When bit 0 is 1 and bit 1 is set to 0, the W83877AF will stop its oscillator and enter power-down mode immediately. The W83877AF will not leave the power-down mode until either a system power-on reset from the MR pin or these two bits are used to program the chip back to power-on state. After leaving the power-down mode, the W83877AF must wait 128 mS for the oscillator to stabilize.

10 Standby for automatic power-down (APD), OSCS2 = 0

When bit 1 is set to 1 and bit 0 is set to 0, the W83877AF will stand by for automatic power-down. A power-down will occur when the following conditions obtain:

- FDC not busy
- FDD motor off
- Interrupt source of line status, modem status, and data ready is inactive (neglecting IER enable/disable)
- Master Reset inactive
- SOUTA and SOUTB in idle state
- SINA and SINB in idle state
- No register read or write to chip

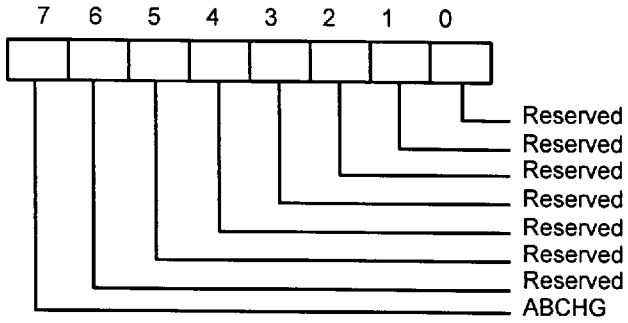
If all of these conditions are met, a counter begins to count down. While the timer is counting down, the W83877AF remains in normal operating mode, and if any of the above conditions changes, the counter will be reset. If the set time (set by bit 7 and bit 6 of CR8) elapses without a change in any of the above conditions, bits 1 and 0 will be set to (1, 1) and the chip will enter automatic power-down mode. The oscillator of the W83877AF will remain running, but the internal clock will be disabled to save power. Once the above conditions are no longer met, the internal clock will be re-supplied and the chip will return to normal operation.

11 Automatic power-down (ADP) state, OSCS2 = 0

The W83877AF enters this state automatically after the counter described above has counted down. If there is a change in any of the conditions listed above, the W83877AF 's clock will be restarted and bits 1 and 0 will be set to (1, 0), i.e., standby for automatic power-down. When the clock is restarted, the chip is ready for normal operation, with no need to wait for the oscillator to stabilize.

8.2.2 Configuration Register 1 (CR1), default = 00H

When the device is in Extended Function mode and EFIR is 01H, the CR1 register can be accessed through EFDR. The bit definitions are as follows:



Bit 0-bit 6: Reserved.

ABCHG (Bit 7):

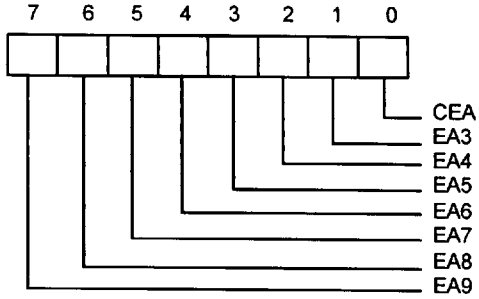
This bit enables the FDC AB Change Mode. Default to be enabled at power-on reset.

0 Drives A and B assigned as usual

1 Drive A and drive B assignments exchanged

8.2.3 Configuration Register 2 (CR2), default = 00H

When the device is in Extended Function mode and EFIR is 02H, the CR2 register can be accessed through EFDR. The bit definitions are as follows:

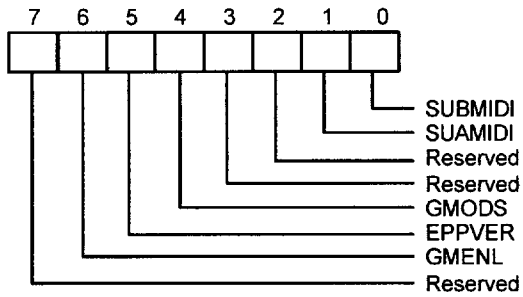


When the W83877AF is programmed into extension adapter mode, the contents of this register are a base address for the extension adapter. When base addresses EA3-EA9 are written into CR2, both the $\overline{XRD}$ and $\overline{XWR}$ pins will be active low simultaneously and an adapter connected to the parallel port can latch the same base address through pins XD1-XD7. After the base address is latched into CR2, a subsequent read/write cycle to this same base address will generate an $\overline{XRD}$ or $\overline{XWR}$ signal.

If CEA is set to 0, then the W83877AF will compare system addresses SA9-SA3 with EA9-EA3 to generate a compare-equal signal for this read/write command to access the Extension adapter. If CEA is set to 1, then only EA9-EA4 are used in this comparison.

8.2.4 Configuration Register 3 (CR3), default = 30H

When the device is in Extended Function mode and EFIR is 03H, the CR3 register can be accessed through EFDR. The bit definitions are as follows:



SUBMIDI (Bit 0):

This bit selects the clock divide rate of UART B.

0 disables MIDI support, UART B clock = 24 MHz divided by 13 (default)

1 enables MIDI support, UART B clock = 24 MHz divided by 12

SUAMIDI (Bit 1):

This bit selects the clock divide rate of UART A.

0 Disables MIDI support, UART A clock = 24 MHz divided by 13 (default)

1 Enables MIDI support, UART A clock = 24 MHz divided by 12

Bit 2-bit 3: Reserved.

GMODS (Bit 4):

This bit selects the adapter mode or portable mode.

0 Selects the portable mode. Pins 41 and 39 will function as PFDCEN and PEXTEN

1 Selects the adapter mode. Pins 41 and 39 will function as $\overline{\text{GMRD}}$ and $\overline{\text{GMWR}}$

Note: GMDRQ (CR16 bit 3) has higher precedence over this bit. That is, GMODS selection is only valid when GMGRQ = 1.

EPPVER (Bit 5):

This bit selects the EPP version of parallel port:

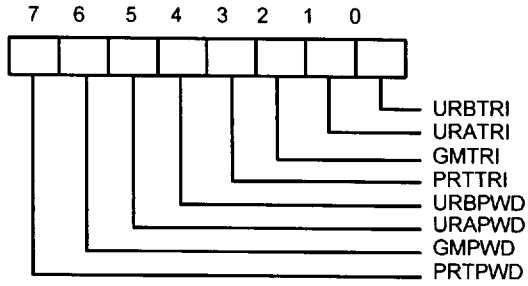
0 Selects the EPP 1.9 version

1 Selects the EPP 1.7 version (default)

Bit 7-bit 6: Reserved.

8.2.5 Configuration Register 4 (CR4), default = 00H

When the device is in Extended Function mode and EFIR is 04H, the CR4 register can be accessed through EFDR. The bit definitions are as follows:



PRTPWD (Bit 7):

0 Supplies power to the parallel port (default)

1 Puts the parallel port in power-down mode

GMPWD (Bit 6):

0 Supplies power to the game port (default)

1 Puts the game port in power-down mode

URAPWD (Bit 5):

0 Supplies power to COMA (default)

1 Puts COMA in power-down mode

URBPWD (Bit 4):

0 Supplies power to COMB (default)

1 Puts COMB in power-down mode

PRTTRI (Bit 3):

This bit enables or disables the tri-state outputs of parallel port in power-down mode.

0 The output pins of the parallel port will not be tri-stated when parallel port is in power-down mode. (default)

1 The output pins of the parallel port will be tri-stated when parallel port is in power-down mode.

GMTRI (Bit 2):

This bit enables or disables the tri-state outputs of the game port in power-down mode.

0 The output pins of the game port will not be tri-stated when game port is in power-down mode. (default)

1 The output pins of the game port will be tri-stated when game port is in power-down mode.

URATRI (Bit 1):

This bit enables or disables the tri-state outputs of UART A in power-down mode.

0 The output pins of UART A will not be tri-stated when UART A is in power-down mode.

1 The output pins of UART A will be tri-stated when UART A is in power-down mode.

URBTRI (Bit 0):

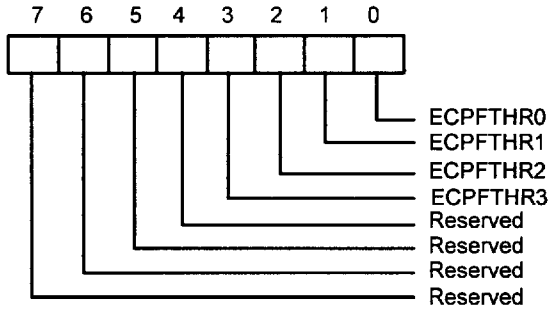
This bit enables or disables the tri-state outputs of UART B in power-down mode.

0 The output pins of UART B will not be tri-stated when UART B is in power-down mode.

1 The output pins of UART B will be tri-stated when UART B is in power-down mode.

8.2.6 Configuration Register 5 (CR5), default = 00H

When the device is in Extended Function mode and EFIR is 05H, the CR5 register can be accessed through EFDR. The bit definitions are as follows:

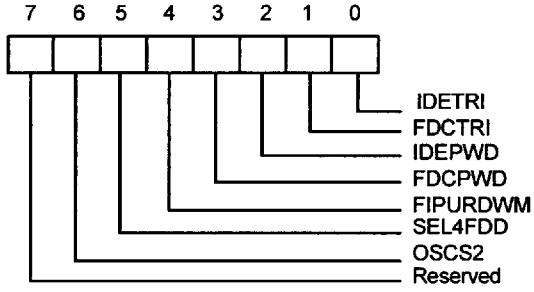


Bit 7-4: Reserved

ECPFTHR3-0 (bit 3-0): These four bits define the FIFO threshold for the ECP mode parallel port. The default value is 0000 after power-up.

8.2.7 Configuration Register 6 (CR6), default = 00H

When the device is in Extended Function mode and EFIR is 06H, the CR6 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7: Reserved

OSCS2 (Bit 6): This bit and OSCS1, OSCS0 (bit 1, 0 of CR0) select one of the W83877AF's power-down functions. Refer to descriptions of CR0. (Default to be 0)

SEL4FDD (Bit 5): Selects four FDD mode

0 Selects two FDD mode (default, see Table 8-2)

1 Selects four FDD mode

$\overline{DSA}$, $\overline{DSB}$, $\overline{MOA}$ and $\overline{MOB}$ output pins are encoded as show in Table 8-3 to select four drives.

Table 8-2

DO REGISTER (3F2H)						$\overline{MOB}$	$\overline{MOA}$	$\overline{DSB}$	$\overline{DSA}$	DRIVE
Bit 7	Bit 6	Bit 5	Bit 4	Bit 1	Bit 0					SELECTED
0	0	0	0	0	0	1	1	1	1	--
0	0	0	1	0	0	1	0	1	0	FDD A
0	0	1	0	0	1	0	1	0	1	FDD B
0	1	0	0	0	1	1	1	1	1	--
1	0	0	0	1	1	1	1	1	1	--

Table 8-3

DO REGISTER (3F2H)						$\overline{MOB}$	$\overline{MOA}$	$\overline{DSB}$	$\overline{DSA}$	DRIVE
Bit 7	Bit 6	Bit 5	Bit 4	Bit 1	Bit 0					SELECTED
0	0	0	0	X	X	1	1	x	x	--
0	0	0	1	0	0	0	0	0	0	FDD A
0	0	1	0	0	1	0	0	0	1	FDD B
0	1	0	0	1	0	0	0	1	0	FDD C
1	0	0	0	1	1	0	0	1	1	FDD D

FIPURDWN (Bit 4):

This bit controls the internal pull-up resistors of the FDC input pins $\overline{RDATA}$, $\overline{INDEX}$, $\overline{TRAK0}$, $\overline{DSKCHG}$, and $\overline{WP}$.

0 The internal pull-up resistors of FDC are turned on. (default)

1 The internal pull-up resistors of FDC are turned off.

FDCPWD (Bit 3):

This bit controls the power to the FDC.

0 Power is supplied to the FDC. (default)

1 Puts the FDC in power-down mode.

IDEPWD (Bit 2):

This bit controls the power of the IDE.

0 Power is supplied to the IDE. (default)

1 Puts the IDE in power-down mode.

FDCTRI (Bit 1):

This bit enables or disables the tri-state outputs of the FDC in power-down mode.

0 The output pins of the FDC will not be tri-stated when FDC is in power-down mode.

1 The output pins of the FDC will be tri-stated when FDC is in power-down mode.

IDETRI (Bit 0):

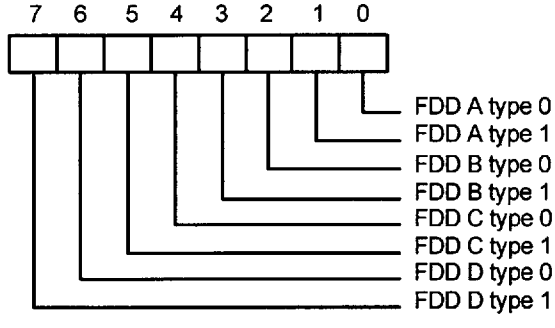
This bit enables or disables the tri-state outputs of the IDE in power-down mode.

0 The output pins of the IDE will not be tri-stated when IDE is in power-down mode.

1 The output pins of the IDE will be tri-stated when IDE is in power-down mode.

8.2.8 Configuration Register 7 (CR7), default = 00H

When the device is in Extended Function mode and EFIR is 07H, the CR7 register can be accessed through EFDR. The bit definitions are as follows:



FDD A type 1, 0 (Bit 1, 0):

These two bits select the type of FDD A.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$= 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1; Bit 5 of CR9 = 1):

01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

FDD B type 1, 0 (Bit 3, 2):

These two bits select the type of FDD B.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$= 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

FDD C type 1, 0 (Bit 5, 4):

These two bits select the type of FDD C.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$ = 1, he data transfer rate is 500 Kb/s.

Three mode FDD select (EN 3 MODE = 1):

01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

FDD D type 1, 0 (Bit 7, 6):

These two bits select the type of FDD D.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$ = 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

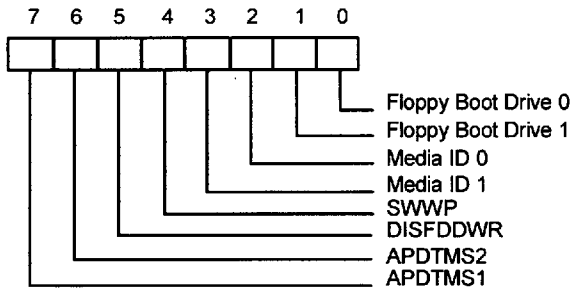
01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

8.2.9 Configuration Register 8 (CR8), default = 00H

When the device is in Extended Function mode and EFIR is 08H, the CR8 register can be accessed through EFDR. The bit definitions are as follows:



APDTMS2 APDTMS1 (Bit 6, 7):

These two bits select the count-down time of the automatic power-down mode counter.

00	4 seconds
01	32 seconds
10	64 seconds
11	4 minutes

DISFDDWR (Bit 5):

This bit enables or disables FDD write data.

0	Enables FDD write
1	Disables FDD write (forces pins $\overline{WE}$, $\overline{WD}$ to stay high)

Once this bit is set high, the FDC operates normally, but because pin $\overline{WE}$ is inactive, the FDD will not write data to diskettes. For example, if a diskette is formatted with DISFDDWR = 1, after the format command has been executed, messages will be displayed that appear to indicate that the format is complete. If the diskette is removed from the disk drive and inserted again, however, typing the DIR command will reveal that the contents of the diskette have not been modified and the diskette was not actually reformatted.

This is because as the operating system (e.g., DOS) reads the diskette files, it keeps the files in memory. If there is a write operation, DOS will write data to the diskette and memory simultaneously. When DOS wants to read the diskette, it will first search the files in memory. If DOS finds the file in memory, it will not issue a read command to read the diskette. When DISFDDWR = 1, DOS still writes data to the diskette and memory, but only the data in memory are updated. If a read operation is performed, data are read from memory first, and not from the diskette. The action of removing the diskette from the drive and inserting it again forces the $\overline{DSKCHG}$ pin active. DOS will then read the contents of the diskette and will show that the contents have not been modified. The same holds true with write commands.

The disable FDD write function allows users to protect diskettes against computer viruses by ensuring that no data are written to the diskette.

SWWP (Bit 4):

0	Normal, use $\overline{WP}$ to determine whether the FDD is write-protected or not
1	FDD is always write-protected

Media ID 1 Media ID 0 (Bit 3, 2):

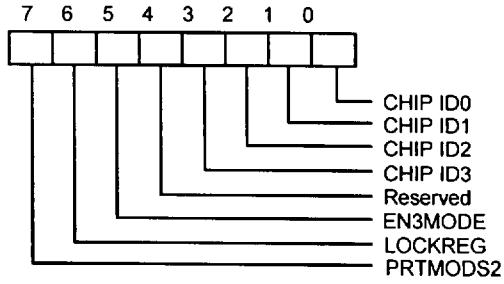
These two bits hold the media ID bit 1, 0 for three mode

Floppy Boot Drive 1 Floppy Boot Drive 0 (bit 1, 0)

These two bits hold the value of floppy boot drive 1 and drive 0 for three mode

8.2.10 Configuration Register 9 (CR9), default = 0AH

When the device is in Extended Function mode and EFIR is 09H, the CR9 register can be accessed through EFDR. The bit definitions are as follows:



PRTMODS2 (Bit 7):

This bit and PRTMODS1, PRTMODS0 (bits 3, 2 of CR0) select the operating mode of the W83877AF. Refer to the descriptions of CR0.

LOCKREG (Bit 6):

This bit enables or disables the reading and writing of all configuration registers.

0 Enables the reading and writing of CR0-CR29

1 Disables the reading and writing of CR0-CR29 (locks W83877AF extension functions)

EN3MODE (Bit 5):

This bit enables or disables three mode FDD selection. When this bit is high, it enables the read/write 3F3H register.

0 Disables 3 mode FDD selection

1 Enables 3 mode FDD selection

When three mode FDD function is enabled, the value of $\overline{RWC}$ depends on bit 5 and bit 4 of TDR(3F3H). The values of $\overline{RWC}$ and their meaning are shown in Table 8-4.

Table 8-4

BIT 5 OF TDR	BIT 4 OF TDR	$\overline{RWC}$	$\overline{RWC}$ = 0	$\overline{RWC}$ = 1
0	0	Normal	250K bps	500K bps
0	1	0	1.2 M FDD	X
1	0	1	X	1.4M FDD
1	1	X	X	X

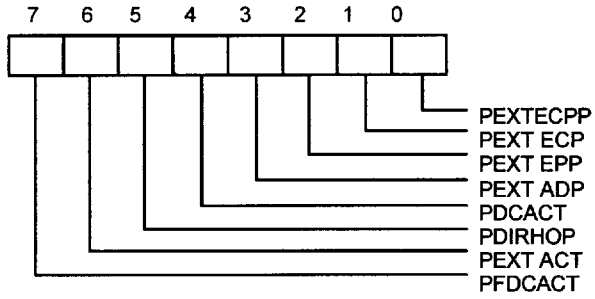
Bit 4: Reserved.

CHIP ID 3, CHIP ID 2, CHIP ID 1, CHIP ID 0 (Bit 3-0):

These four bits are read-only bits that contain chip identification information. The value is 0BH for W83877AF during a read.

8.2.11 Configuration Register A (CRA), default = 1FH

When the device is in Extended Function mode and EFIR is 0AH, the CRA register can be accessed through EFDR. The bit definitions are as follows:



PFDCACT (Bit 7):

This bit controls whether PFDCEN (pin 41) is active high or low in portable mode.

0 PFDCEN is active low

1 PFDCEN is active high

PEXTACT (Bit 6):

This bit controls whether PEXTEN (pin 39) is active high or low in portable mode. This pin can also reflect the mode of the parallel port: EXTADP mode, EPP mode, ECP mode, or ECP/EPP mode, or any combination of these modes.

0 PEXTEN is active low

1 PEXTEN is active high

Bit 5: Reserved.

PDCACT (Bit 4):

This bit controls whether the PDCIN pin is active high or low.

0 PDCIN is active low

1 PDCIN is active high

PEXTADP (Bit 3):

This bit controls whether the PEXTEN pin is active in EXTADP mode.

0 PEXTEN is not active in EXTADP mode

1 PEXTEN is active in EXTADP mode

PEXTEPP (Bit 2):

This bit controls whether the PEXTEN pin is active in EPP mode.

0 PEXTEN is not active in EPP mode

1 PEXTEN is active in EPP mode

PEXTECP (Bit 1):

This bit controls whether the PEXTEN pin is active in ECP mode.

0 PEXTEN is not active in ECP mode

1 PEXTEN is active in ECP mode

PEXTECPP (Bit 0):

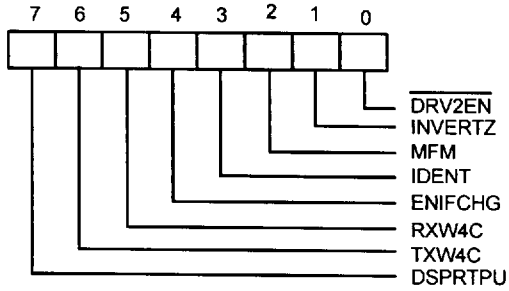
This bit controls whether the PEXTEN pin is active in ECP/EPP mode.

0 PEXTEN is not active in ECP/EPP mode

1 PEXTEN is active in ECP/EPP mode

8.2.12 Configuration Register B (CR0B), default = 0CH

When the device is in Extended Function mode and EFIR is 0BH, the CRB register can be accessed through EFDR. The bit definitions are as follows:



Bit 7: DSPRTPU

0 Enable parallel port pull-up resister.

1 Disable parallel port pull-up resister.

TXW4C (Bit 6):

This bit is active high. When active, the IR controller will wait for 4-character period of time from the end of last receiving before it can start transmitting data.

RXW4C (Bit 5):

This bit is active high. When active, the IR controller will wait for 4-character period of time from the end of last transmitting before it can start receiving data.

ENIFCHG (Bit 4):

This bit is active high. When active, it enables host interface mode change, which is determined by IDENT (Bit 3) and MFM (Bit 2).

IDENT (Bit 3):

This bit indicates the type of drive being accessed and changes the level on $\overline{RWC}$ (pin 87).

0 $\overline{RWC}$ will be active low for high data rates (typically used for 3.5" drives)

1 $\overline{RWC}$ will be active high for high data rates (typically used for 5.25" drives)

When hardware reset or ENIFCHG is a logic 1, IDENT and MFM select one of three interface modes, as shown in Table 8-5.

Table 8- 5

IDENT	MFM	INTERFACE
0	0	Model 30 mode
0	1	PS/2 mode
1	0	AT mode
1	1	AT mode

MFM (Bit 2):

This bit and IDENT select one of the three interface modes (PS/2 mode, Model 30, or PC/AT mode).

INTVERTZ (Bit 1):

This bit determines the polarity of all FDD interface signals.

0 FDD interface signals are active low

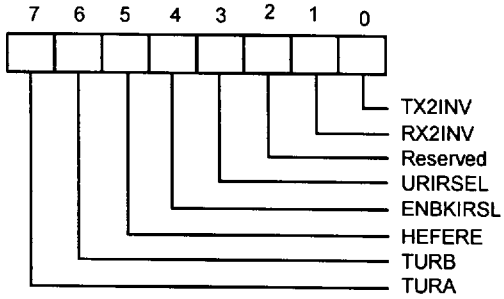
1 FDD interface signals are active high

$\overline{DRV2EN}$ (Bit 0): PS/2 mode only

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

8.2.13 Configuration Register C (CR0C), default = 28H

When the device is in Extended Function mode and EFIR is 0CH, the CR0C register can be accessed through EFDR. The bit definitions are as follows:



TURA (bit 7):

0 the clock source of UART A is 1.8462 MHz (24 MHz divide 13) (default)

1 the clock source of UART A is 24 MHz, it can make the baud rate of UART A up to 1.5 MHz

TURB (bit 6):

0 the clock source of UART B is 1.8462 MHz (24 MHz divide 13) (default)

1 the clock source of UART B is 24 MHz, it can make the baud rate of UART A up to 1.5 MHz

HEFERE (bit 5): this bit combines with HEFRAS (CR16 bit 0) to define how to enable Extended Function Registers.

HEFRAS	HEFERE	address and value
0	0	write 88H to the location 250H
0	1	write 89H to the location 250H (default)
1	0	write 86H to the location 3F0H twice
1	1	write 87H to the location 3F0H twice

The default value of HEFERE is 1.

Bit 4: ENBKIRSL - Enable Bank IR Function Select.

0 IR selection of configuration register is higher priority.

1 IR selection of bank of UART B is higher priority.

URIRSEL (bit 3):

0 select UART B as IR function.

1 select UART B as normal function.

The default value of URIRSEL is 1.

Bit 2: Reserved.

RX2INV (bit 1):

0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.

1 inverse the SINB pin of UART B function or IRRX pin of IR function

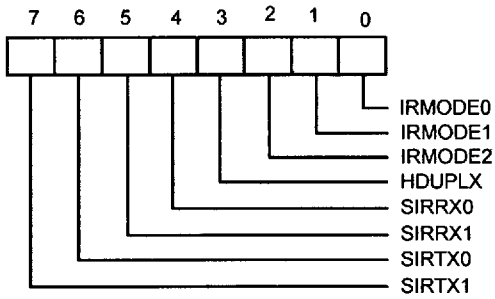
TX2INV (bit 0):

0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

8.2.14 Configuration Register D (CR0D), default = A3H

When the device is in Extended Function mode and EFIR is 0DH, the CR0D register can be accessed through EFDR. The bit definitions are as follows:



SIRTX1 (bit 7): IRTX pin selection bit 1

SIRTX0 (bit 6): IRTX pin selection bit 0

SIRTX1	SIRTX0	IRTX output on pin
0	0	disabled
0	1	IRTX1 (pin 43)
1	0	IRTX2 (pin 95)
1	1	disabled

SIRRX1 (bit 5): IRRX pin selection bit 1

SIRRX0 (bit 4): IRRX pin selection bit 0

SIRRX1	SIRRX0	IRRX input on pin
0	0	disabled
0	1	IRRX1 (pin 42)
1	0	IRRX2 (pin 94)
1	1	disabled

HDUPLX (bit 3):

0 The IR function is Full Duplex.

1 The IR function is Half Duplex.

IRMODE2 (bit 2): IR function mode selection bit 2

IRMODE1 (bit 1): IR function mode selection bit 1

IRMODE0 (bit 0): IR function mode selection bit 0

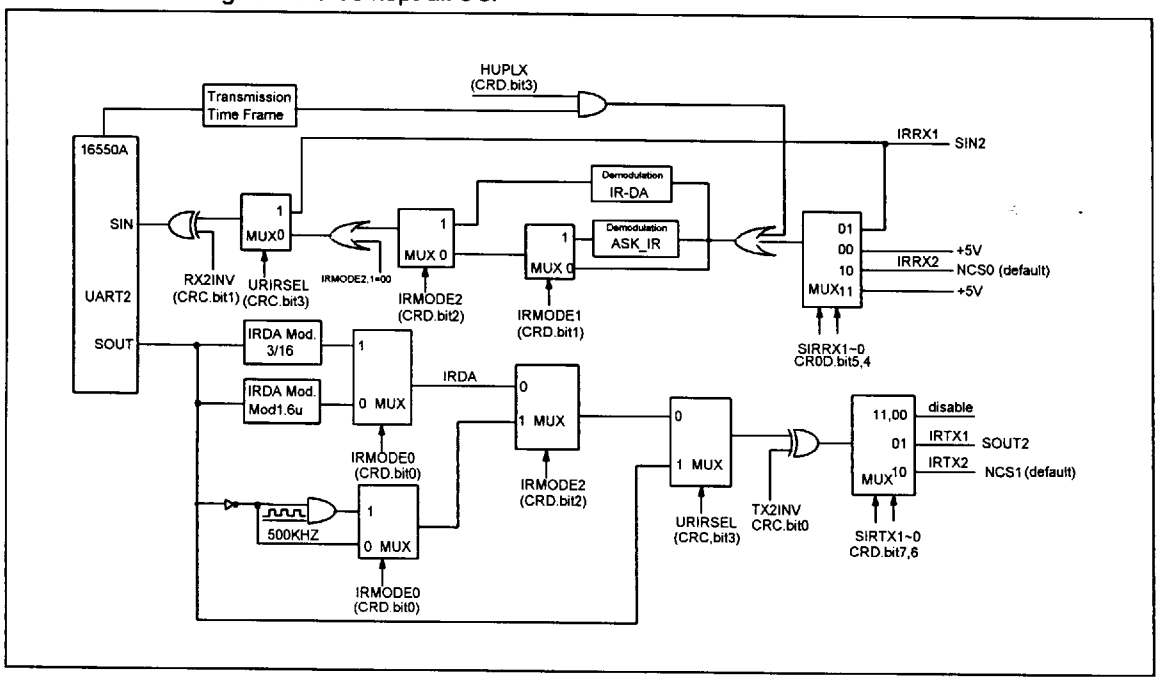
IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB
100	ASK-IR	Inverting IRTX pin	routed to SINB
101	ASK-IR	Inverting IRTX & 500 KHz clock	routed to SINB
110	ASK-IR	Inverting IRTX	Demodulation into SINB
111*	ASK-IR	Inverting IRTX & 500 KHz clock	Demodulation into SINB

Note: The notation is normal mode in the IR function.

The SIR schematic diagram for registers CRC and CRD is shown below.

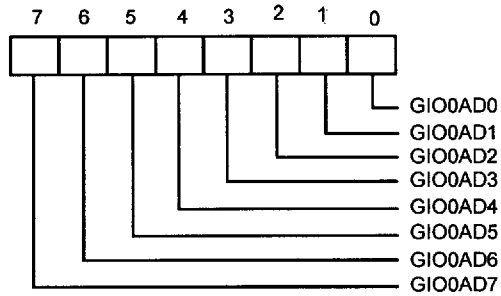
8.2.15 Configuration Register E (CR0E), Configuration Register F (CR0F)

Reserved for testing. Should be kept all 0's.



8.2.16 Configuration Register 10 (CR10), default = 00H

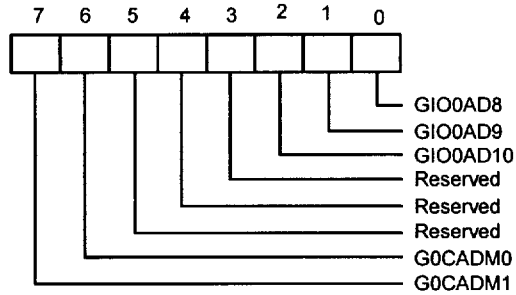
When the device is in Extended Function mode and EFIR is 10H, the CR10 register can be accessed through EFDR. The bit definitions are as follows:



GIO0AD7-GIO0AD0 (bit 7-bit 0): GIOP0 (pin 92) address bit 7 - bit 0.

8.2.17 Configuration Register 11 (CR11), default = 00H

When the device is in Extended Function mode and EFIR is 11H, the CR11 register can be accessed through EFDR. The bit definitions are as follows:



G0CADM1-G0CADM0 (bit 7-bit 6): GIOP0 address bit compare mode selection

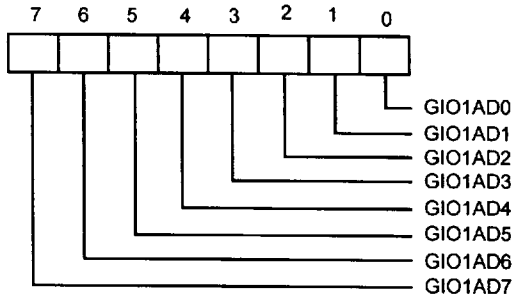
G0CADM1	G0CADM0	GIOP0 pin
0	0	compare GIO0AD10-GIO0AD0 with SA10-SA0
0	1	compare GIO0AD10-GIO0AD1 with SA10-SA1
1	0	compare GIO0AD10-GIO0AD2 with SA10-SA2
1	1	compare GIO0AD10-GIO0AD3 with SA10-SA3

Bit 5-bit 3: Reserved

GIO0AD10-GIO0AD8 (bit 2-bit 0): GIOP0 (pin 92) address bit 10-bit 8

8.2.18 Configuration Register 12 (CR12), default = 00H

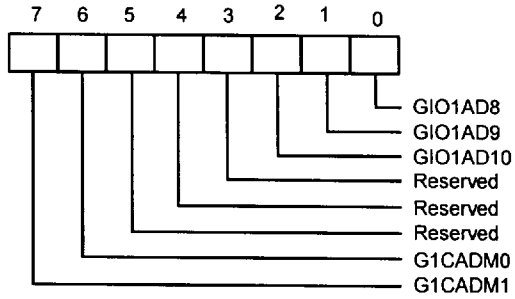
When the device is in Extended Function mode and EFIR is 12H, the CR12 register can be accessed through EFDR. The bit definitions are as follows:



GIO1AD7-GIO1AD0 (bit 7-bit 0): GIOP1 (pin 96) address bit 7-bit 0.

8.2.19 Configuration Register 13 (CR13), default = 00H

When the device is in Extended Function mode and EFIR is 13H, the CR13 register can be accessed through EFDR. The bit definitions are as follows:



G1CADM1-G1CADM0 (bit 7-bit 6): GIOP1 address bit compare mode selection

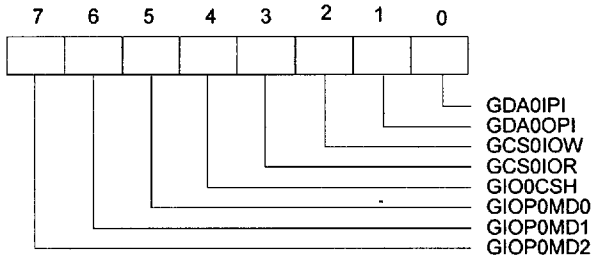
G1CADM1	G1CADM0	GIOP1 pin
0	0	compare GIO1AD10-GIO1AD0 with SA10-SA0
0	1	compare GIO1AD10-GIO1AD1 with SA10-SA1
1	0	compare GIO1AD10-GIO1AD2 with SA10-SA2
1	1	compare GIO1AD10-GIO1AD3 with SA10-SA3

Bit 5- bit 3: Reserved

GIO1AD10-GIO1AD8 (bit 2-it 0): GIOP1 (pin 96) address bit 10-bit 8

8.2.20 Configuration Register 14 (CR14), default = 00H

When the device is in Extended Function mode and EFIR is 14H, the CR14 register can be accessed through EFDR. The bit definitions are as follows:



GIOP0MD2-GIOP0MD0 (bit 7-bit 5): GIOP0 pin mode selection

GIOP0MD2	GIOP0MD1	GIOP0MD0	GIOP0 pin
0	0	0	inactive (tri-state)
0	0	1	as a data output pin (SD0→GIOP0), when (AEN = L) AND (nIOW = L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will be present on GIOP0
0	1	0	as a data input pin (GIOP0→SD0), when (AEN = L) AND (nIOR = L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will be present on SD0
0	1	1	as a data input/output pin (GIOP0↔SD0). When (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will be present on GIOP0 When (AEN = L) AND (nIOR = L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will be present on SD0
1	X	X	as a Chip Select pin, the pin will be active at (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (nIOR = L) OR (nIOW = L)

GIO0CSH(bit 4):

0 the Chip Select pin will be active LOW when (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (nIOR = L) OR (nIOW = L)

1 the Chip Select pin will be active HIGH when (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (nIOR = L) OR (nIOW = L)

GCS0IOR (bit 3): See below.

GCS0IOW (bit 2): See below.

GCS0IOR	GCS0IOW	
0	0	GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0)
0	1	GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (nIOW = L)
1	0	GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (nIOR = L)
1	1	GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (nIOW = L OR nIOR = L)

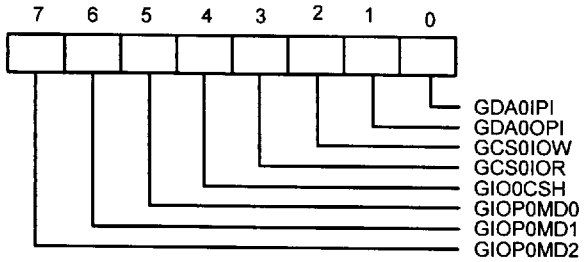
GDA0OPI (bit 1): See below.

GDA0IPI (bit 0): See below.

GDA0OPI	GDA0IPI	
0	0	GIOP0 functions as a data pin, and GIOP0→SD0, SD0→GIOP0
0	1	GIOP0 functions as a data pin, and inverse GIOP0→SD0, SD0→GIOP0
1	0	GIOP0 functions as a data pin, and GIOP0→SD0, inverse SD0→GIOP0
1	1	GIOP0 functions as a data pin, and inverse GIOP0→SD0, inverse SD0→GIOP0

8.2.21 Configuration Register 15 (CR15), default = 00H

When the device is in Extended Function mode and EFIR is 15H, the CR15 register can be accessed through EFDR. The bit definitions are as follows:



GIOP1MD2-GIOP1MD0 (bit 7-bit 5): GIOP1 pin mode selection

GIOP1MD2	GIOP1MD1	GIOP1MD0	GIOP1 pin
0	0	0	inactive (tri-state)
0	0	1	as a data output pin (SD1→GIOP1), when (AEN = L) AND (nIOW = L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will be present on GIOP1
0	1	0	as a data input pin (GIOP1→SD1), when (AEN = L) AND (nIOR = L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will be present on SD1
0	1	1	as a data input/output pin (GIOP1↔SD1). When (AEN = L) AND (nIOW = L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will be present on GIOP1 When (AEN = L) AND (nIOR = L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will be present on SD1
1	X	X	as a Chip Select pin, the pin will be active at (AEN = L) AND (SA10-0 = GIO1AD10-0) OR (nIOR = L) OR (nIOW = L)

GIO1CSH (bit 4):

0	the Chip Select pin will active LOW when (AEN = L) AND (SA10-0 = GIOAD10-0) OR (nIOR = L) OR (nIOW = L)
1	the Chip Select pin will active HIGH when (AEN = L) AND (SA10-0 = GIOAD10-0) OR (nIOR = L) OR (nIOW = L)

GCS1IOR (bit 3): See below.

GCS1IOW (bit 2): See below.

GCS1IOR	GCS1IOW	
0	0	GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0)
0	1	GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (nIOW = L)
1	0	GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (nIOR = L)
1	1	GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (nIOW = L OR nIOR = L)

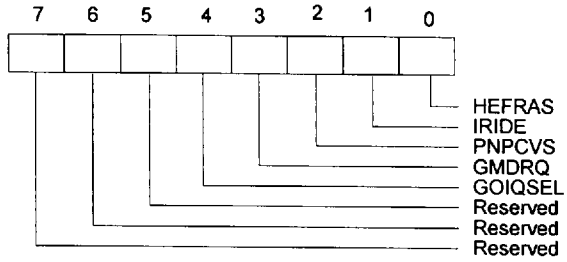
GDA0OPI (bit 1): See below.

GDA1IPI (bit 0): See below.

GDA1OPI	GDA1IPI	
0	0	GIOP1 functions as a data pin, and GIOP1→SD1, SD1→GIOP1
0	1	GIOP1 functions as a data pin, and inverse GIOP1→SD1, SD1→GIOP1
1	0	GIOP1 functions as a data pin, and GIOP1→SD1, inverse SD1→GIOP1
1	1	GIOP1 functions as a data pin, and inverse GIOP1→ SD1, inverse SD1→GIOP1

8.2.22 Configuration Register 16 (CR16), default = 0EH

When the device is in Extended Function mode and EFIR is 16H, the CR16 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7-bit 4: Reserved.

G1QASEL (bit 5):

0 pin 96 function as IRQ_A.

1 pin 96 function as GIO1.

The corresponding power-on setting pin is nRTSB (pin 45).

G0QBSEL (bit 4):

0 pins 92 function as IRQ_B.

1 pins 92 function as GIO0.

The corresponding power-on setting pin is nRTSB (pin 45).

GMDRQ (bit 3):

0 pins 39, 41 function as DRQ_A, nDACK_A, respectively.

1 pins 39, 41 function as nGMWR, nGMRD, respectively.

The corresponding power-on setting pin is SOUTB (pin 43).

PNPCVS (bit 2):

0 PnP-related registers (CR1E, CR20-29) reset to be all 0s.

1 default settings for these registers.

The corresponding power-on setting pin is nRTSA (pin 36).

PnP register	PNPCVS = 1	PNPCVS = 0
CR1E	81H	00H
CR20	FCH	00H
CR21	7CH	00H
CR22	FDH	00H
CR23	DEH	00H
CR24	FEH	00H
CR25	BEH	00H
CR26	23H	00H
CR27	05H	00H
CR28	43H	00H
CR29	60H	00H

Note: The new value of PNPCVS must be complementary to the old one to make an effective change. For example, the user must set PNPCVS to 1 first and then reset it to 0 to reset these PnP registers if the present value of PNPCVS is 0.

IRIDE (bit 1):

0 pins 1, 91, 94, 95 function as IDE ports.

1 pins 1, 91, 94, 95 function as IR ports.

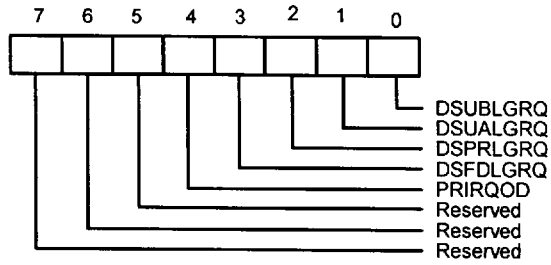
The corresponding power-on setting pin is SOUTA (pin 38).

pin	IRIDE = 0	IRIDE = 1
1	nRSTIDE	IRQ_G
91	nIDBEN	IRQ_H
94	nCS0	IRRX2
95	nCS1	IRTX2

HEFRAS (bit 0): combines with HEFERE (CR0C bit 5) to define how to access Extended Function Registers (refer to CR0C bit 5 description). The corresponding power-on setting pin is nDTRA (pin 35).

8.2.23 Configuration Register 17 (CR17), default = 00H

When the device is in Extended Function mode and EFIR is 17H, the CR17 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7-bit 5: Reserved.

PRIRQOD (bit4):

0 printer IRQ ports are totem-poles in SPP mode and open-drains in ECP/EPP mode.

1 printer IRQ ports are totem-poles in all modes.

DSFDLGRQ (bit 3):

0 enable FDC legacy mode on IRQ and DRQ selections. DO register bit 3 has effect on selecting IRQ.

1 disable FDC legacy mode on IRQ and DRQ selections. DO register bit 3 has no effect on selecting IRQ.

DSPRLGRQ (bit 2):

0 enable PRT legacy mode on IRQ and DRQ selections. DCR bit 4 has effect on selecting IRQ.

1 disable PRT legacy mode on IRQ and DRQ selections. DCR bit 4 has no effect on selecting IRQ.

DSUALGRQ (bit 1):

0 enable UART A legacy mode on IRQ selection. MCR bit 3 has effect on selecting IRQ.

1 disable UART A legacy mode on IRQ selection. MCR bit 3 has no effect on selecting IRQ.

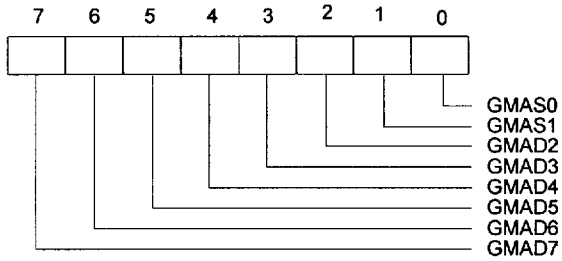
DSUBLGRQ (bit 0):

0 enable UART B legacy mode on IRQ selection. MCR bit 3 has effect on selecting IRQ.

1 disable UART B legacy mode on IRQ selection. MCR bit 3 has no effect on selecting IRQ.

8.2.24 Configuration Register 1E (CR1E)

When the device is in Extended Function mode and EFIR is 1EH, the CR1E register can be accessed through EFDR. Default = 81H if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



This register is used to select the base address of Game Chip Select Decoder (GAMECS) from 100H-3F0H on 16-byte boundaries. nCS = 0 and A10 = 0 are required to qualify the GAMECS output.

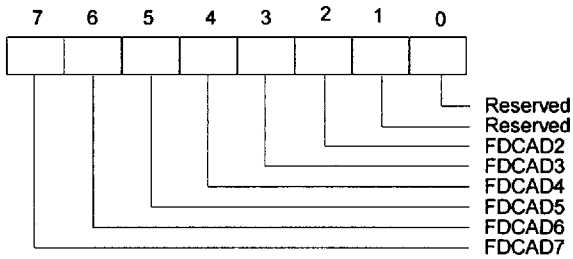
GMAD7-GMAD2 (bit 7-bit 2): match A[9:4].

GMAS1-GMAS0 (bit 1-bit 0): CAMECS configuration.

00	GAMECS disable
01	1-byte decode, A[3:0] = 0001b
10	8-byte decode, A[3:0] = 0xxxb
11	16-byte decode, A[3:0] = xxxxb

8.2.25 Configuration Register 20 (CR20)

When the device is in Extended Function mode and EFIR is 20H, the CR20 register can be accessed through EFDR. Default = FCH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



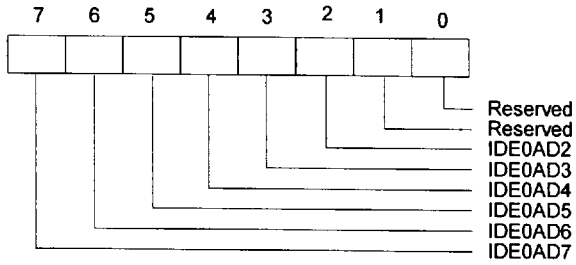
This register is used to select the base address of the Floppy Disk Controller (FDC) from 100H-3F0H on 16-byte boundaries. nCS = 0 and A10 = 0 are required to access the FDC registers. A[3:0] are always decoded as 0xxxb.

FDCAD7-FDCAD2 (bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 1-bit 0: Reserved, fixed at zero.

8.2.26 Configuration Register 21 (CR21)

When the device is in Extended Function mode and EFIR is 21H, the CR21 register can be accessed through EFDR. Default = 7CH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



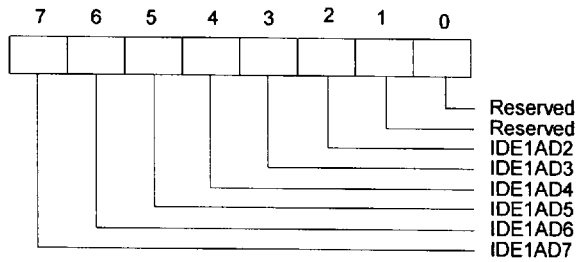
This register is used to select the base address of the IDE Interface Control Registers from 100H-3F0H on 16-byte boundaries. nCS = 0 and A10 = 0 are required to access the IDE registers. A[3:0] are always decoded as 0xxxb.

IDE0AD7-IDE0AD2 (bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 1-bit 0: Reserved, fixed at zero.

8.2.27 Configuration Register 22 (CR22)

When the device is in Extended Function mode and EFIR is 22H, the CR22 register can be accessed through EFDR. Default = FDH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



This register is used to select the base address of the IDE Interface Alternate Status Register from 106H-3F6H on 16-byte boundaries + 6. nCS = 0 and A10 = 0 are required to access the IDE Alternate Status register. A[3:0] must be 0110b.

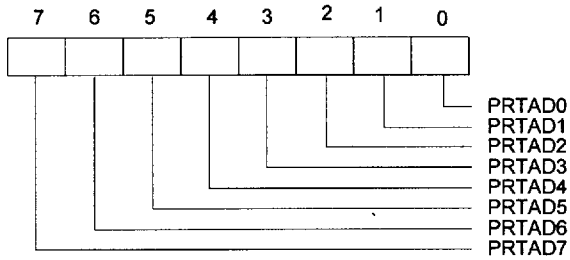
IDE1AD7-IDE1AD2 (bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 1: Reserved, fixed at zero.

Bit 0: Reserved, fixed at one.

8.2.28 Configuration Register 23 (CR23)

When the device is in Extended Function mode and EFIR is 23H, the CR23 register can be accessed through EFDR. Default = DEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

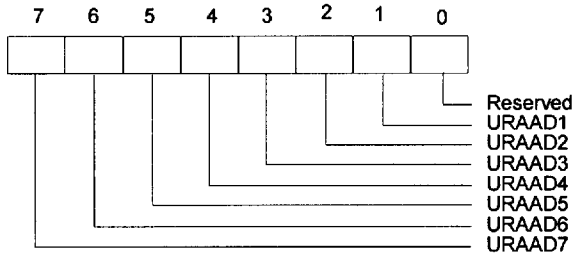


This register is used to select the base address of the parallel port. If EPP is disable, the parallel port can be set from 100H-3FCH on 4-byte boundaries. If EPP is enable, the parallel port can be set from 100H-3F8H on 8-byte boundaries. nCS = 0 and A10 = 0 are required to access the parallel port when in compatible, bi-directional, or EPP modes. A10 is active in ECP mode.

PRTAD7-PRTAD0 (bit 7-bit 0): match A[9:2]. Bit 7 = 0 and bit 6 = 0 disable this decode.

8.2.29 Configuration Register 24 (CR24)

When the device is in Extended Function mode and EFIR is 24H, the CR24 register can be accessed through EFDR. Default = FEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



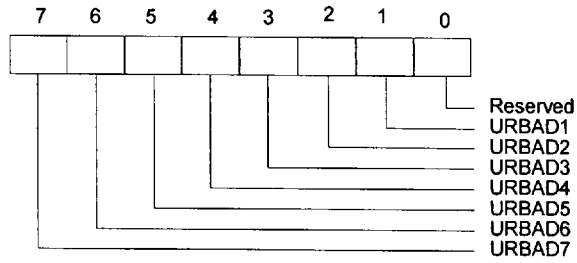
This register is used to select the base address of the UART A from 100H-3F8H on 8-byte boundaries. nCS = 0 and A10 = 0 are required to access the UART A registers. A[2:0] are don't-care conditions.

URAAD7-URAAD1 (bit 7-bit 1): match A[9:3]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 0: Reserved, fixed at zero.

8.2.30 Configuration Register 25 (CR25)

When the device is in Extended Function mode and EFIR is 25H, the CR25 register can be accessed through EFDR. Default = BEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



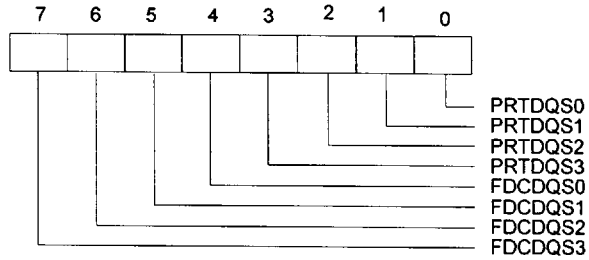
This register is used to select the base address of the UART B from 100H-3F8H on 8-byte boundaries. nCS = 0 and A10 = 0 are required to access the UART B registers. A[2:0] are don't-care conditions.

URBAD7-URBAD1 (bit 7-bit 1): match A[9:3]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 0: Reserved, fixed at zero.

8.2.31 Configuration Register 26 (CR26)

When the device is in Extended Function mode and EFIR is 26H, the CR26 register can be accessed through EFDR. Default = 23H if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



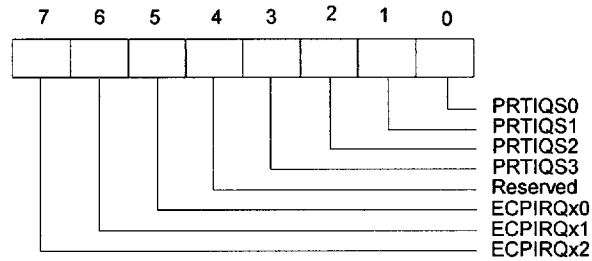
FDCDQS3-FDCDQS0 (bit 7-bit 4): Allocate DMA resource for FDC.

PRTDQS3-PRTDQS0 (bit 3-bit 0): Allocate DMA resource for PRT.

bit 7- bit4, bit 3 - bit 0	DMA selected
0000	None
0001	DMA_A
0010	DMA_B
0011	DMA_C

8.2.32 Configuration Register 27 (CR27)

When the device is in Extended Function mode and EFIR is 27, the CR27 register can be accessed through EFDR. Default = 05H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



ECPIRQx2-ECPIRQx0 (bit7-bit 5): These bits are configurable equivalents to bit[5:3] of cnfgB register in ECP mode except that cnfgB[5:3] are read-only bits. They indicate the IRQ resource assigned for the ECP printer port. It is the software designer's responsibility to ensure that CR27[7:5] and CR27[3:0] are consistent. For example, CR27[7:5] should be filled with 001 (select IRQ 7) if CR27[3:0] are to be programmed as 0101 (select IRQ_E) while IRQ_E is connected to IRQ 7.

CR27[7:5]	IRQ resource
000	reflect other IRQ resources selected by CR27[3:0] (default)
001	IRQ 7
010	IRQ 9
011	IRQ 10
100	IRQ 11
101	IRQ 14
110	IRQ 15
111	IRQ 5

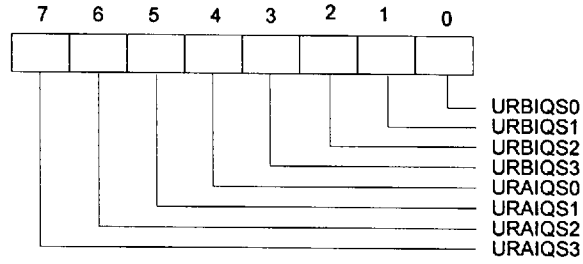
Bit 4: Reserved.

PRTIQS3-PRTIQS0 (bit 3-bit 0): Select IRQ resource for the parallel port. Any unselected IRQ is in tristate.

CR27[3:0]	IRQ selected
0000	None
0001	IRQ_A
0010	IRQ_B
0011	IRQ_C
0100	IRQ_D
0101	IRQ_E
0110	IRQ_F
0111	IRQ_G
1000	IRQ_H

8.2.33 Configuration Register 28 (CR28)

When the device is in Extended Function mode and EFIR is 28, the CR28 register can be accessed through EFDR. Default = 43H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

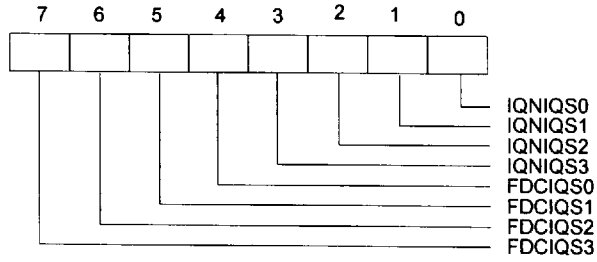


URAIQS3-URAIQS0 (bit 7-bit 4): Allocate interrupt resource for UART A.

URBIQS3-URBIQS0 (bit 3-bit 0): Allocate interrupt resource for UART B.

8.2.34 Configuration Register 29 (CR29)

When the device is in Extended Function mode and EFIR is 29, the CR29 register can be accessed through EFDR. Default = 62H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

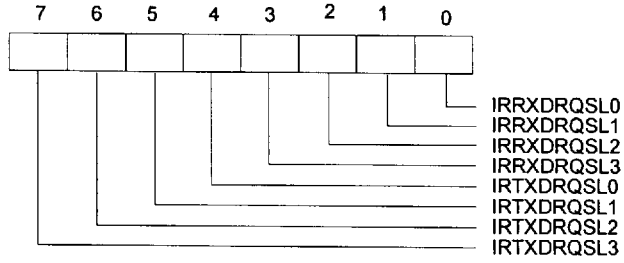


FDCIQS3-FDCIQS0 (bit 7-bit 4): Allocate interrupt resource for FDC.

IQNIQS3-IQNIQS0 (bit 3-bit 0): Allocate interrupt resource for IRQIN.

8.2.35 Configuration Registers (CR2A)

When the device is in Extended Function mode and EFIR is 2AH, the CR2A register can be accessed through EFDR. This register default value is 00_{16}. The bit definitions are as follows:

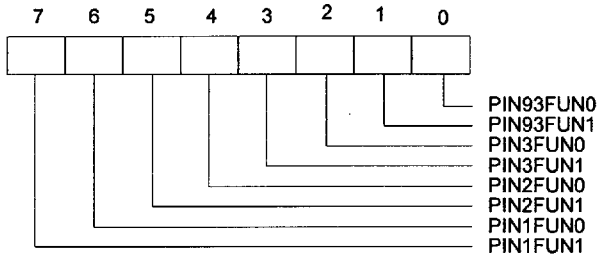


IRTXDRQSL (bit 7-bit 4): Transmitter DMA channel A through D selection when high speed infrared (FIR/MIR) is used and enable DMA channel. Note that these bits is used in two DMA channels.

IRRXDRQSL(bit 3-bit 0): Receiver or Transmitter DMA channel A through selection when high speed infrared (FIR/MIR) is used and enable DMA channel. Note that these bits act as RX DMA channel selection if two DMA channel is used, or these bits act as RX/TX DMA channel selection if single DMA channel is used.

8.2.36 Configuration Registers (CR2B)

When the device is in Extended Function mode and EFIR is 2BH, the CR2B register can be accessed through EFDR. This register default value is 00_{16}. The bit definitions are as follows:



Bit 7~6: PIN1FUN1~0 - Pin 1 function select.

PIN1FUN1	PIN1FUN0	Pin 1
0	0	IRQ_G
0	1	nRESIDE
1	0	DRQ_D
1	1	IRSL2

Bit 5-4: PIN2FUN1~0 - Pin 2 function select.

PIN2FUN1	PIN2FUN0	Pin 2
0	0	nCS
0	1	nDACK_D
1	0	IRSL1
1	1	IRSL2

Bit 3-2: PIN3FUN1~0 - Pin 3 function select.

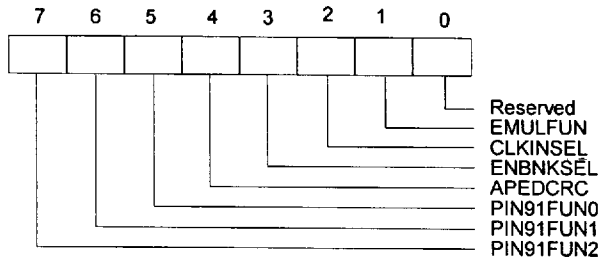
PIN3FUN1	PIN3FUN0	Pin 3
0	0	PDCIN
0	1	nDACK_D
1	0	IRSL1
1	1	IRRXH/IRSL0

Bit 1-0: PIN93FUN1~0 - Pin 93 function select.

PIN93FUN1	PIN93FUN0	Pin 93
0	0	IRQIN
0	1	DRQ_D
1	0	IRSL2
1	1	IRRXH/IRSL0

8.2.37 Configuration Registers (CR2C)

When the device is in Extended Function mode and EFIR is 2CH, the CR2C register can be accessed through EFDR. This register default value is 10_{16}. The bit definitions are as follows:



Bit 7-5 : PIN91FUN2~0 - Pin 91 function select.

PIN91FUN(CR2C.7)	PIN91FUN(CR2C.6)	PIN91FUN(CR2C.5)	Pin 91
0	0	0	IRQ_H
0	0	1	nDBENL
0	1	0	IRSL2
0	1	1	IRRXH/IRSL0
1	0	0	DACK_D

Note: The IRSL0/IRRXH selection is determined by Bit 5(IRSL0 Mode selection) of Register 7 of Bank 7. When setting Bit 5 to logical 1, IRSL0 is selected; When setting Bit 5 to logical 0, IRRXH is selected.

Bit 4 :APEDCRC - Append CRC to receiver when a frame is end.

= 0 No append hardware CRC value as data in FIR/MIR mode

= 1 Append hardware CRC value as data in FIR/MIR mode

Bit 3 :ENBNKSEL - Bank select enable

= 0 Disable UART B bank selection

= 1 Enable UART B bank selection

Bit 2 :CLKINSEL - Clock input selection

= 0 The clock on pin XTAL1/XTAL2 is 24 MHz

= 1 The clock on pin XTAL1/XTAL2 is 48 MHz

Bit 1:EMULFUN - Emulate internal defined function

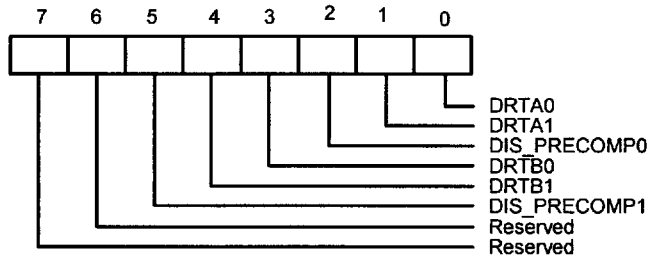
= 0 Disable emulation mode

= 1 Enable emulation mode

Bit 0: Reserved.

8.2.37 Configuration Registers (CR2D)

When the device is in Extended Function mode and EFIR is $2D_{16}$, the CR2D register can be accessed through EFDR. This register default value is 00_{16}. The bit definitions are as follows:



This register controls the data rate selection for FDC. It also controls if pre-compensation is enabled.

DRTA1, DRTA0 (bit 1 - bit 0):

These two bits combining with data rate selection bits in Data Rate Register select the operational data rate for FDD A as follows:

Drive Rate Table		Data Rate		Operational Data Rate	
DRTA1	DRTA0	DRATE1	DRATE0	MFM	FM
0	0	1	1	1M	---
0	0	0	0	500K	250K
0	0	0	1	300K	150K
0	0	1	0	250K	125K
0	1	1	1	1M	---
0	1	0	0	500K	250K
0	1	0	1	500K	250K
0	1	1	0	250K	125K
1	0	1	1	1M	---
1	0	0	0	500K	250K
1	0	0	1	2M	---
1	0	1	0	250K	125K

DIS_PRECOMP0 (bit 2):

This bit controls if pre-compensation is enabled for FDD A.

0 enable pre-compensation for FDD A

1 disable pre-compensation for FDD A

DRTB1, DRTB0 (bit 4 - bit 3):

These two bits combining with data rate selection bits in Data Rate Register select the operational data rate for FDD B as shown in last table.

DIS_PRECOMP1 (bit 5):

This bit controls if precompensation is enabled for FDD B.

0 enable precompensation for FDD B

1 disable precompensation for FDD B

Bit 7 - bit 6: Reserved.

8.3 Bit Map Configuration Registers

Table: Bit Map of Configuration Registers

Register	Power-on Reset Value	D7	D6	D5	D4	D3	D2	D1	D0
CR0	0000 0000	0	0	0	0	PRTMODS1	PRTMODS0	OSCS1	OSCS0
CR1	0000 0000	ABCHG	0	0	0	0	0	0	0
CR2	0000 0000	RA9	RA8	RA7	RA6	RA5	RA4	RA3	CEA
CR3	0011 0000	0	GMENL	EPPVER	GMODS	0	0	SUAMIDI	SUBMIDI
CR4	0000 0000	PRTPWD	GMPWD	URAPWD	URBPWD	PRTTRI	GMTRI	URATRI	URBTRI
CR5	0000 0000	0	0	0	0	ECPFTHR3	ECPFTHR2	ECPFTHR1	ECPFTHR0
CR6	0000 0000	0	OSCS2	SEL4FDD	FIPURDWN	FDCPWD	IDEPWD	FDCTRI	IDETRI
CR7	0000 0000	FDD D T1	FDD D T0	FDD C T1	FDD C T0	FDD B T1	FDD B T0	FDD A T1	FDD A T0
CR8	0000 0000	APDTMS1	APDTMS0	DISFDDWR	SWWP	MEDIA 1	MEDIA 0	BOOT 1	BOOT 0
CR9	0000 1011	PRTMODS2	LOCKREG	EN3MODE	0	CHIP ID 3	CHIP ID 2	CHIP ID 1	CHIP ID 0
CRA	0001 1111	PFDCACT	PEXTACT	PDIRHISOP	PDCHACT	PEXTADP	PEXTEPP	PEXTECP	PEXTECPP
CRB	0000 0000	0	Tx4WC	Rx4WC	ENIFCHG	IDENT	MFM	INVERTZ	DRV2EN
CRC	0010 1000	TURA	TURB	HEFERE	ENBKIRSL	URIRSEL	0	RX2INV	TX2INV
CRD	1010 0011	SIRTX1	SIRTX0	SIRRX1	SIRRX0	HDUPLX	IRMODE2	IRMODE1	IRMODE0
CR10	0000 0000	GIO0AD7	GIO0AD6	GIO0AD5	GIO0AD4	GIO0AD3	GIO0AD2	GIO0AD1	GIO0AD0
CR11	0000 0000	0	0	0	0	0	GIO0AD10	GIO0AD9	GIO0AD8
CR12	0000 0000	GIO1AD7	GIO1AD6	GIO1AD5	GIO1AD4	GIO1AD3	GIO1AD2	GIO1AD1	GIO1AD0
CR13	0000 0000	0	0	0	0	0	GIO1AD10	GIO1AD9	GIO1AD8
CR14	0000 0000	GIOP0MD2	GIOP0MD1	GIOP0MD0	GIO0CSH	GCS0IOR	GCS0IOW	GDA0OPI	GDA0IPI
CR15	0000 0000	GIOP1MD2	GIOP1MD1	GIOP1MD0	GIO1CSH	GCS1IOR	GCS1IOW	GDA1OPI	GDA1IPI
CR16	000s ssss[1]	0	0	G1QASEL	G0QBSEL	GMDRQ	PNPCVS	IRIDE	HEFRAS
CR17	0000 0000	0	0	0	PRIRQOD	DSFDLGRQ	DSPRLGRQ	DSUALGRQ	DSUBLGRQ
CR1E	1000 0001[2]	GMAD7	GMAD6	GMAD5	GMAD4	GMAD3	GMAD2	GMAS1	GMAS0
CR20	1111 1100[2]	FDCAD7	FDCAD6	FDCAD5	FDCAD4	FDCAD3	FDCAD2	0	0
CR21	0111 1100[2]	IDE0AD7	IDE0AD6	IDE0AD5	IDE0AD4	IDE0AD3	IDE0AD2	0	0
CR22	1111 1101[2]	IDE1AD7	IDE1AD6	IDE1AD5	IDE1AD4	IDE1AD3	IDE1AD2	0	1
CR23	1101 1110[2]	PRTAD7	PRTAD6	PRTAD5	PRTAD4	PRTAD3	PRTAD2	PRTAD1	PRTAD0
CR24	1111 1110[2]	URAAD7	URAAD6	URAAD5	URAAD4	URAAD3	URAAD2	URAAD1	0
CR25	1011 1110[2]	URBAD7	URBAD6	URBAD5	URBAD4	URBAD3	URBAD2	URBAD1	0
CR26	0010 0011[2]	FDCDQS3	FDCDQS2	FDCDQS1	FDCDQS0	PRTDQS3	PRTDQS2	PRTDQS1	PRTDQS0
CR27	0000 0101[2]	ECPIRQx2	ECPIRQx1	ECPIRQx0	0	PRTIQS3	PRTIQS2	PRTIQS1	PRTIQS0
CR28	0100 0011[2]	URAIQS3	URAIQS2	URAIQS1	URAIQS0	URBIQS3	URBIQS2	URBIQS1	URBIQS0
CR29	0110 0000[2]	FDCIQS3	FDCIQS2	FDCIQS1	FDCIQS0	IQNIQS3	IQNIQS2	IQNIQS1	IQNIQS0
CR2A	0000 0000	IRTXDSL3	IRTXDSL2	IRTXDSL1	IRTXDSL0	IRRXDSL3	IRRXDSL2	IRRXDSL1	IRRXDSL0
CR2B	0000 0000	PIN1FUN1	PIN1FUN0	PIN2FUN1	PIN2FUN0	PIN3FUN1	PIN3FUN0	PIN93FN1	PIN93FN0
CR2C	0001 0000	PIN91FN2	PIN91FN1	PIN91FN0	APEDCRC	ENBNKSL	CLKINSL	0	0

Notes:

1. 's' means its value depends on corresponding power-on setting pin.
2. These default values are valid when CR16 bit 2 is 1 during power-on reset; They will be all 0's if CR16 bit 2 is 0.

9.0 SPECIFICATIONS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNI	CONDITIONS
I/O_{8tc} - TTL level output pin with source-sink capabilities of 8 mA; CMOS level input voltage						
Input Low Voltage	V_{IL}	-0.5		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}+0.5	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with source-sink capabilities of 12 mA						
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{DD}+0.5	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24t} - TTL level bi-directional pin with source-sink capabilities of 24 mA						
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{DD}+0.5	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

9.2 DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{8t} - TTL level output pin with source-sink capabilities of 8 mA						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = -8 mA
OUT_{12t} - TTL level output pin with source-sink capabilities of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD_{12} - Open-drain output pin with sink capabilities of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD_{24} - Open-drain output pin with sink capabilities of 24 mA						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
IN_t - TTL level input pin						
Input Low Voltage	VIL			0.8	V	VDD = 5 V
Input High Voltage	VIH	2.0			V	VDD = 5 V
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0V
IN_{ts} - TTL level input pin Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hysteresis (Vt+ - Vt-)	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0V
IN_c- CMOS level input pin						
Input Low Voltage	VIL			0.3xVDD	V	VDD = 5 V
Input High Voltage	VIH	0.7xVDD			V	VDD = 5 V
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0V
IN_{cs} - CMOS level schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	VDD = 5 V
Input High Threshold Voltage	Vt+	3..2	3.5	3.8	V	VDD = 5 V
Hysteresis (Vt+ - Vt-)	VTH	1.5	2		V	VDD = 5 V
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0V

9.3 AC Characteristics

9.3.1 FDC: Data rate = 1 MB/500 KB/300 KB/250 KB/sec.

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
SA9-SA0, AEN, $\overline{DACK}$, $\overline{CS}$, setup time to $\overline{IOR}$••	TAR		25			nS
SA9-SA0, AEN, $\overline{DACK}$, hold time for $\overline{IOR}$••	TAR		0			nS
$\overline{IOR}$ width	TRR		80			nS
Data access time from $\overline{IOR}$••	TFD	CL = 100 pf			80	nS
Data hold from $\overline{IOR}$••	TDH	CL = 100 pf	10			nS
SD to from $\overline{IOR}$ ••	TDF	CL = 100 pf	10		50	nS
IRQ delay from $\overline{IOR}$••	TRI				360/570 /675	nS
SA9-SA0, AEN, $\overline{DACK}$, setup time to $\overline{IOW}$••	TAW		25			nS
SA9-SA0, AEN, $\overline{DACK}$, hold time for $\overline{IOW}$••	TWA		0			nS
$\overline{IOW}$ width	TWW		60			nS
Data setup time to $\overline{IOW}$••	TDW		60			nS
Data hold time from $\overline{IOW}$••	TWD		0			nS
IRQ delay from $\overline{IOW}$••	TWI				360/570 /675	nS
DRQ cycle time	TMCY		27			µS
DRQ delay time $\overline{DACK}$••	TAM				50	nS
DRQ to $\overline{DACK}$ delay	TMA		0			nS
$\overline{DACK}$ width	TAA		260/430 /510			nS
$\overline{IOR}$ delay from $\overline{DRQ}$	TMR		0			nS
$\overline{IOW}$ delay from $\overline{DRQ}$	TMW		0			nS

9.3 AC Characteristics, FDC continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
$\overline{IOW}$ or $\overline{IOR}$ response time from DRQ	TMRW			6/12 /20/24		µS
TC width	TTC		135/220 /260			nS
RESET width	TRST		1.8/3/3. 5			µS
$\overline{INDEX}$ width	TIDX		0.5/0.9 /1.0			µS
$\overline{DIR}$ setup time to $\overline{STEP}$	TDST		1.0/1.6 /2.0			µS
$\overline{DIR}$ hold time from $\overline{STEP}$	TSTD		24/40/48			µS
$\overline{STEP}$ pulse width	TSTP		6.8/11.5 /13.8	7/11.7 /14	7.2/11.9 /14.2	µS
$\overline{STEP}$ cycle width	TSC		Note 2	Note 2	Note 2	µS
$\overline{WD}$ pulse width	TWDD		100/185 /225	125/210 /250	150/235 /275	µS
Write precompensation	TWPC		100/138 /225	125/210 /250	150/235 /275	µS

Notes:

1. Typical values for T = 25C and normal supply voltage.

2. Programmable from 2 mS through 32 mS in 2 mS increments.

9.3.2 IDE

PARAMETER	SYMBOL	MAX.	UNIT
$\overline{CS0}$, $\overline{CS1}$ delay from SA valid	T1	50	nS
DBENL, DBENH delay from AEN, IOCS16, SA	T2	50	nS
IDED7 to D7 delay (read cycle)	T4	50	nS
D7 to IDED7 delay (write cycle)	T3	50	nS

9.3.3 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT	100 pF Loading		1	µS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR	100 pF Loading		175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			1/2	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR	100 pF Loading		250	nS
Delay from $\overline{IOR}$ to Output	TMWO	100 pF Loading		200	nS
Set Interrupt Delay from Modem Input	TSIM			250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM			250	nS
Interrupt Active Delay	TIAD	100 pF Loading		25	nS
Interrupt Inactive Delay	TIID	100 pF Loading		30	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

9.3.4 Extension Adapter Mode

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{XRD}$, $\overline{XWR}$ Delay from $\overline{IOR}$, $\overline{IOW}$	tx1				50	nS
XA<0:2> Delay from SA<0:2>	tx2				50	nS
XD<0:7> Setup time	tx3		50			nS
XD<0:7> Hold time	tx4		0			nS
IRQ & Delay from XIRQ	tx5				50	nS
DRQX Delay from XDRQ	tx6				50	nS
$\overline{XDACK}$ Delay from $\overline{DACKX}$	tx7				50	nS
XTC Delay from TC	tx8				50	nS

9.3.5 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, INDEX, STROBE, AUTOFD Delay from IOW	t1			100	nS
IRQ Delay from ACK, nFAULT	t2			60	nS
IRQ Delay from IOW	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
ERROR Active to IRQ Active	t5			105	nS

9.3.6 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to IOR Asserted	t1	40		nS
IOCHRDY Deasserted to IOR Deasserted	t2	0		nS
IOR Deasserted to Ax Valid	t3	10	10	nS
IOR Deasserted to IOW or IOR Asserted	t4	40		
IOR Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
IOR Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
WAIT Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
WRITE Deasserted to IOR Asserted	t13	0		nS
WAIT Asserted to WRITE Deasserted	t14	0	185	nS
Deasserted to WRITE Modified	t15	60	190	nS
IOR Asserted to PD Hi-Z	t16	0	50	nS
WAIT Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
WAIT Deasserted to PD Drive	t20	60	190	nS
WRITE Deasserted to Command	t21	1		nS

9.3.6 EPP Data or Address Read Cycle Timing Parameters, continued

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

9.3.7 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS

9.3.7 EPP Data or Address Write Cycle Timing Parameters, continued

PARAMETER	SYM.	MIN.	MAX.	UNIT
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS

9.3.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

9.3.9 ECP Parallel Port Forward Timing Parameters

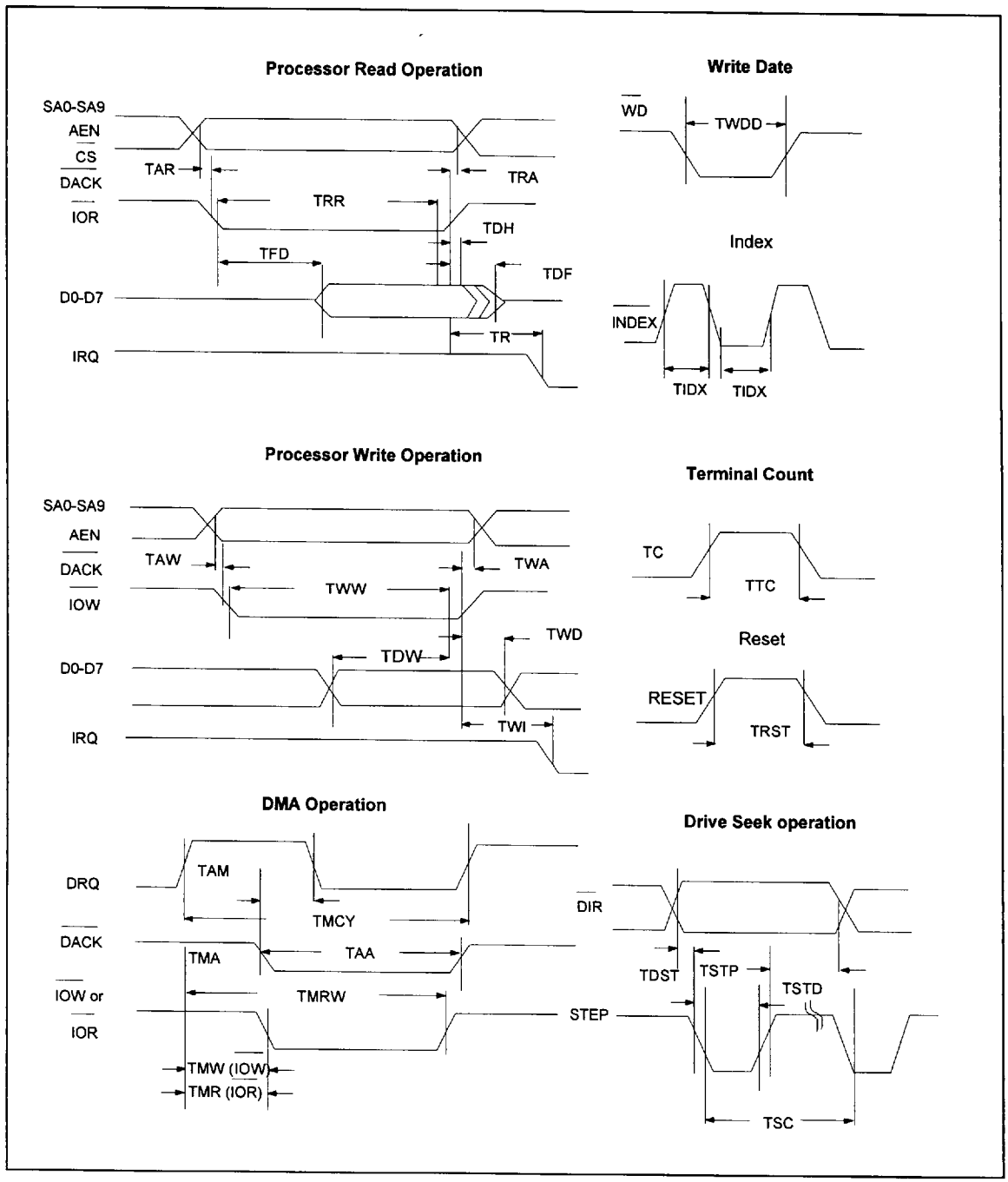
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

9.3.10 ECP Parallel Port Reverse Timing Parameters

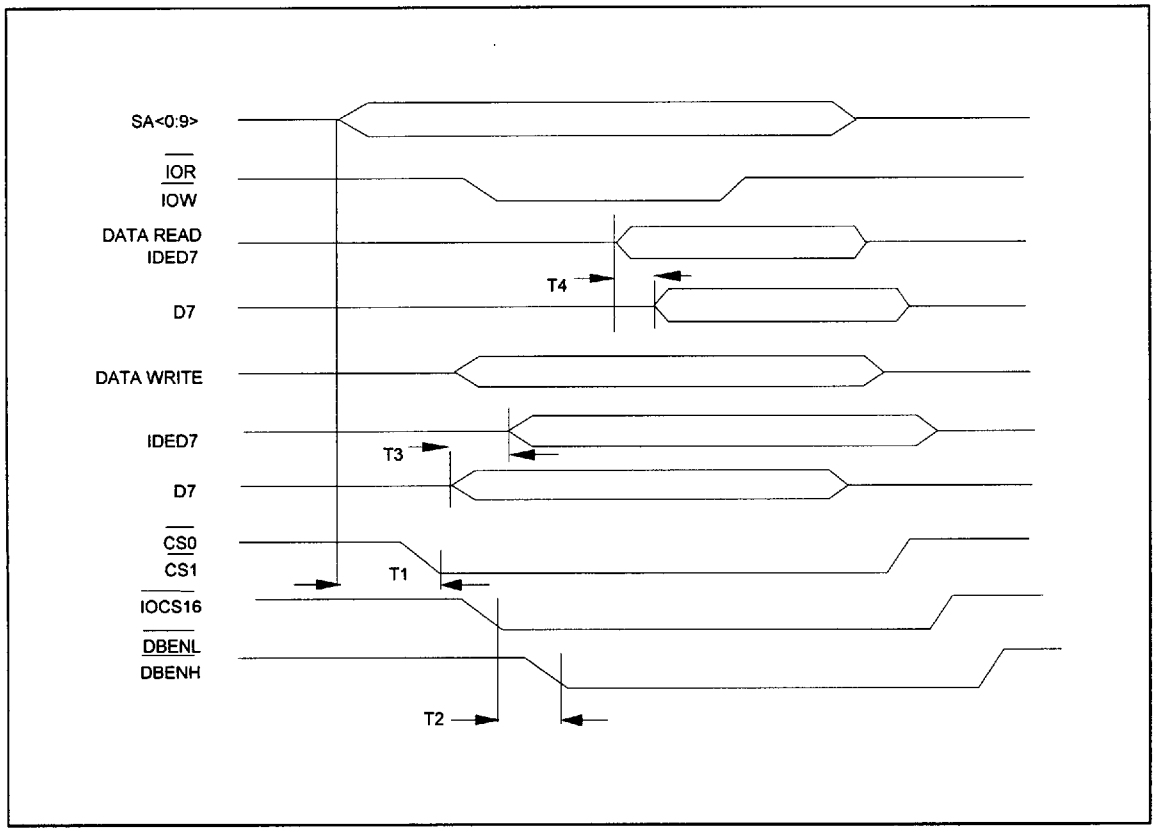
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

10.0 TIMING WAVEFORMS

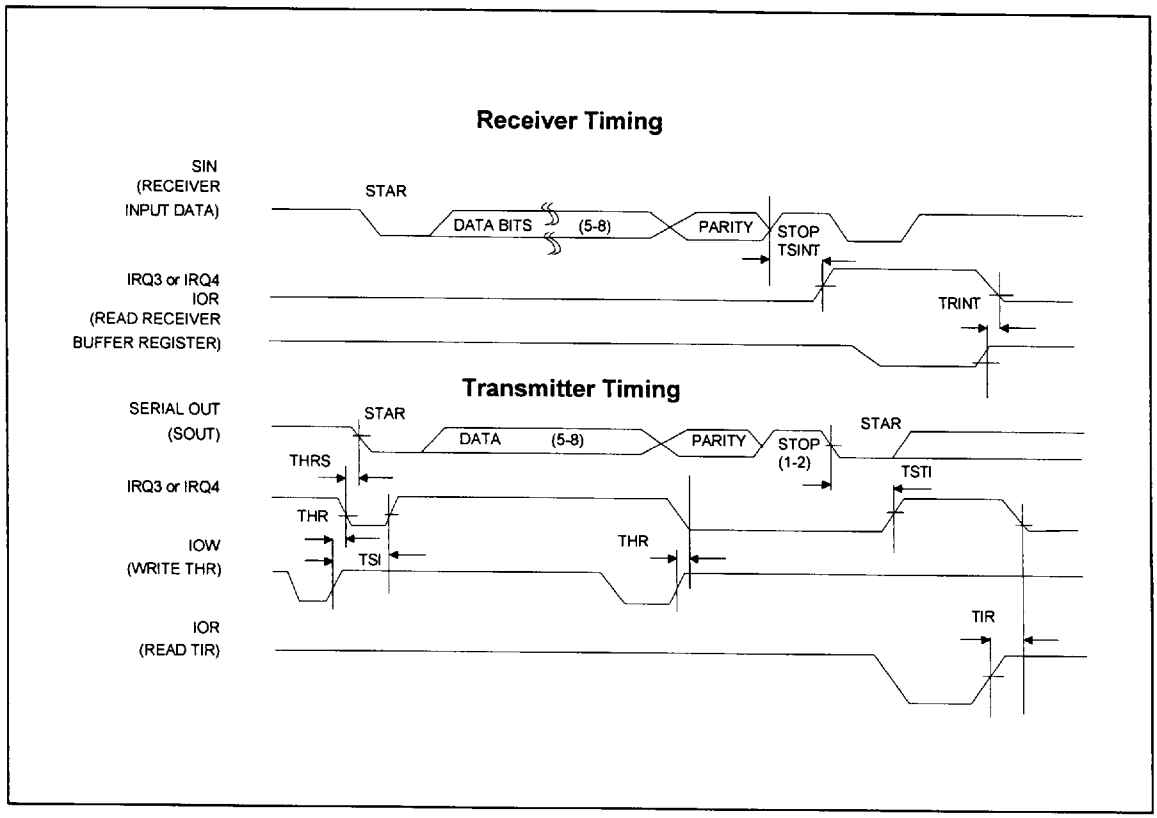
10.1 FDC



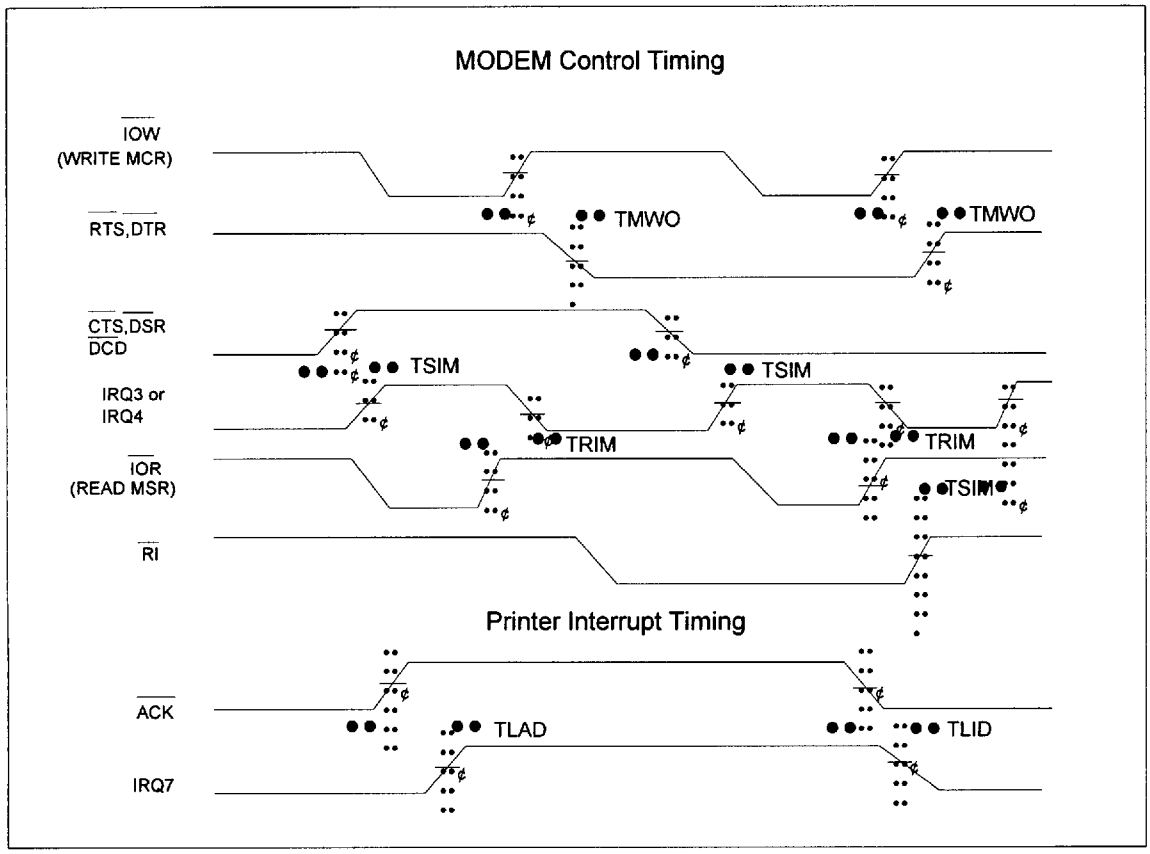
10.2 IDE



10.3 UART/Parallel

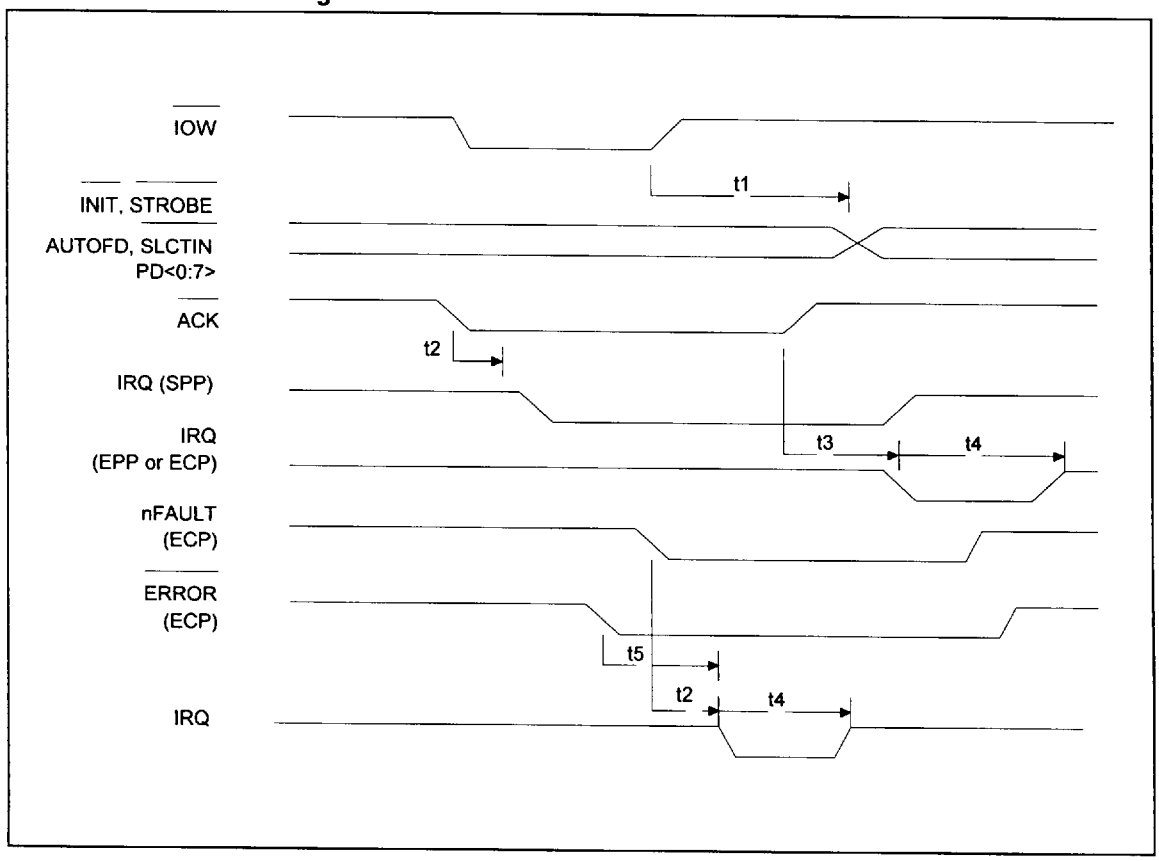


10.3.1 Modem Control Timing



10.4 Parallel Port

10.4.1 Parallel Port Timing



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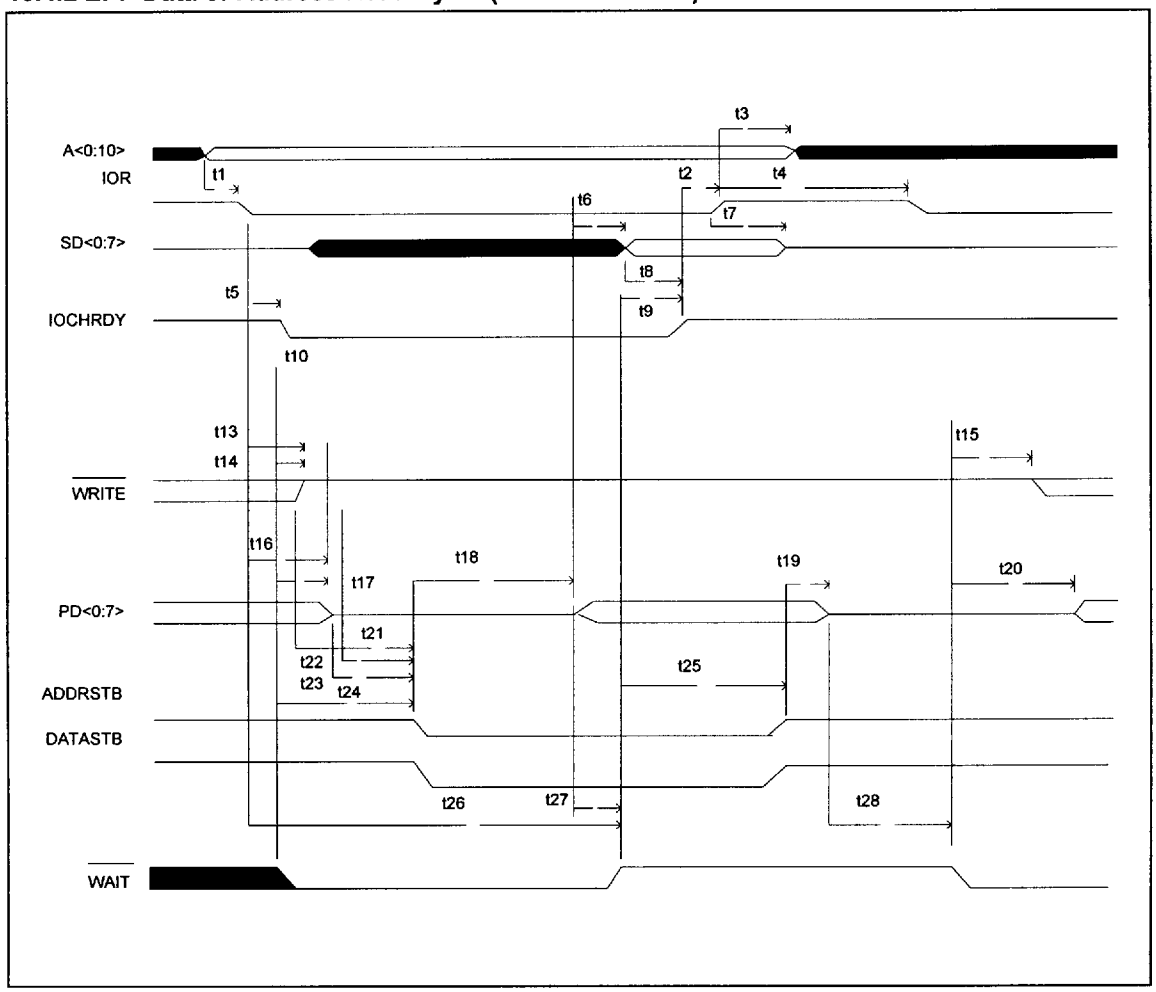
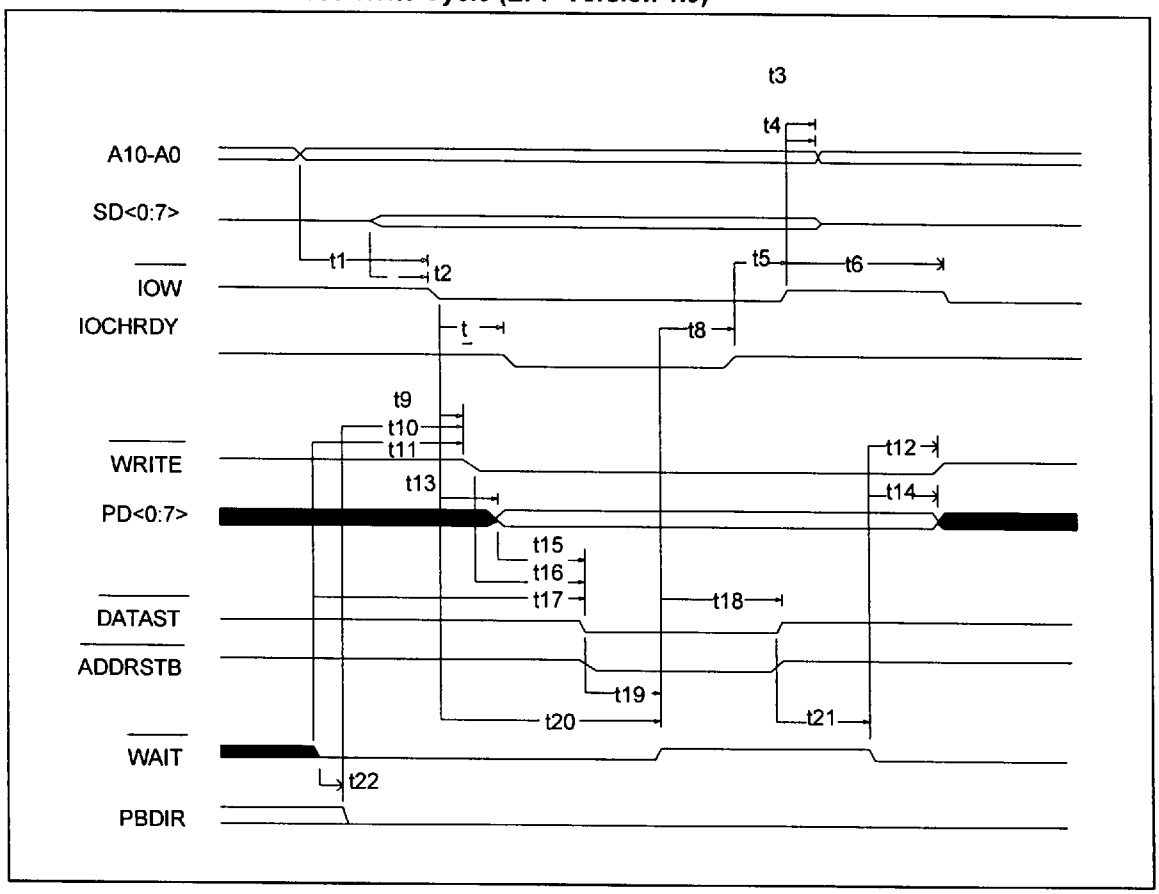
10.4.2 EPP Data or Address Read Cycle (EPP Version 1.9)

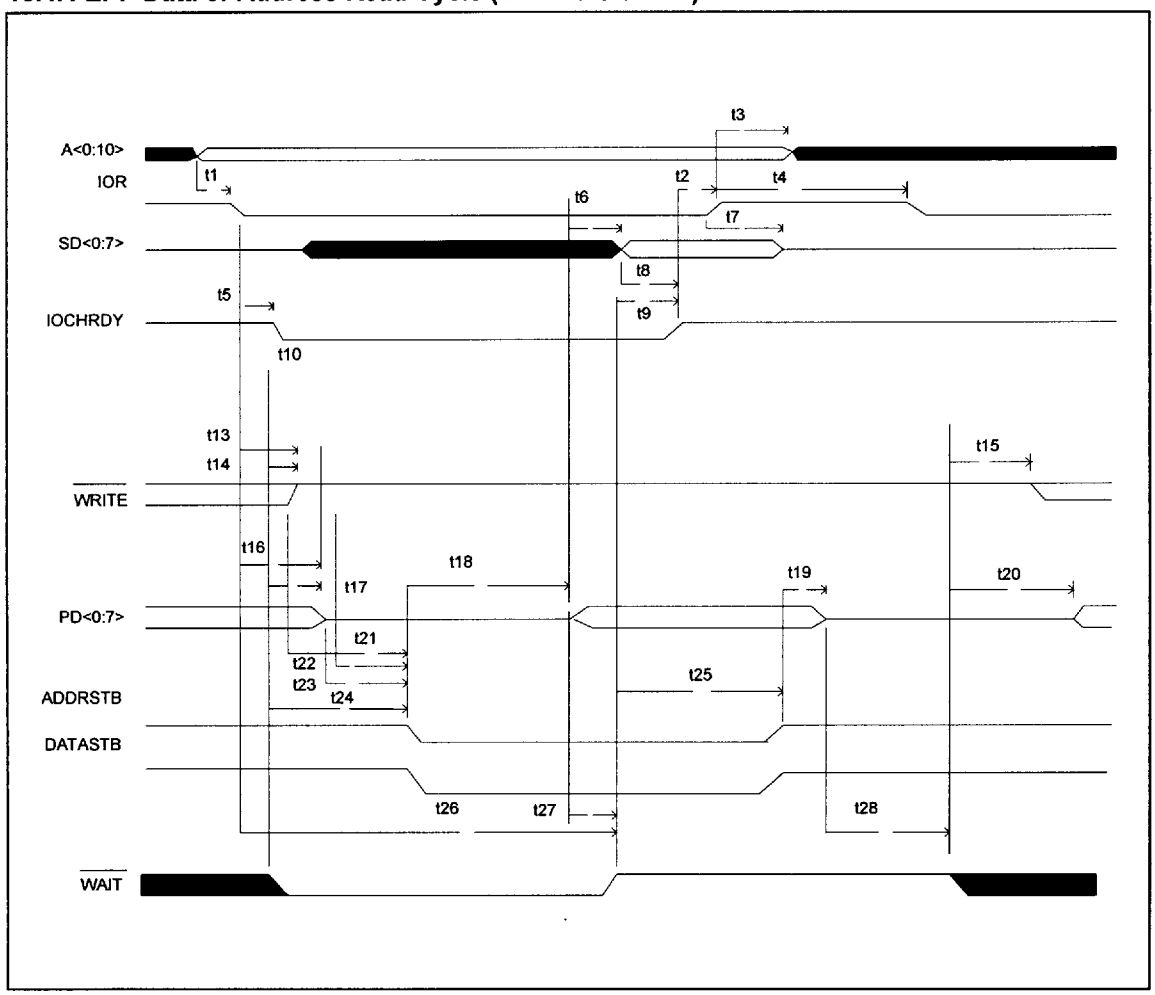


Publication Release Date: Sep. 1996
Preliminary Version 0.50

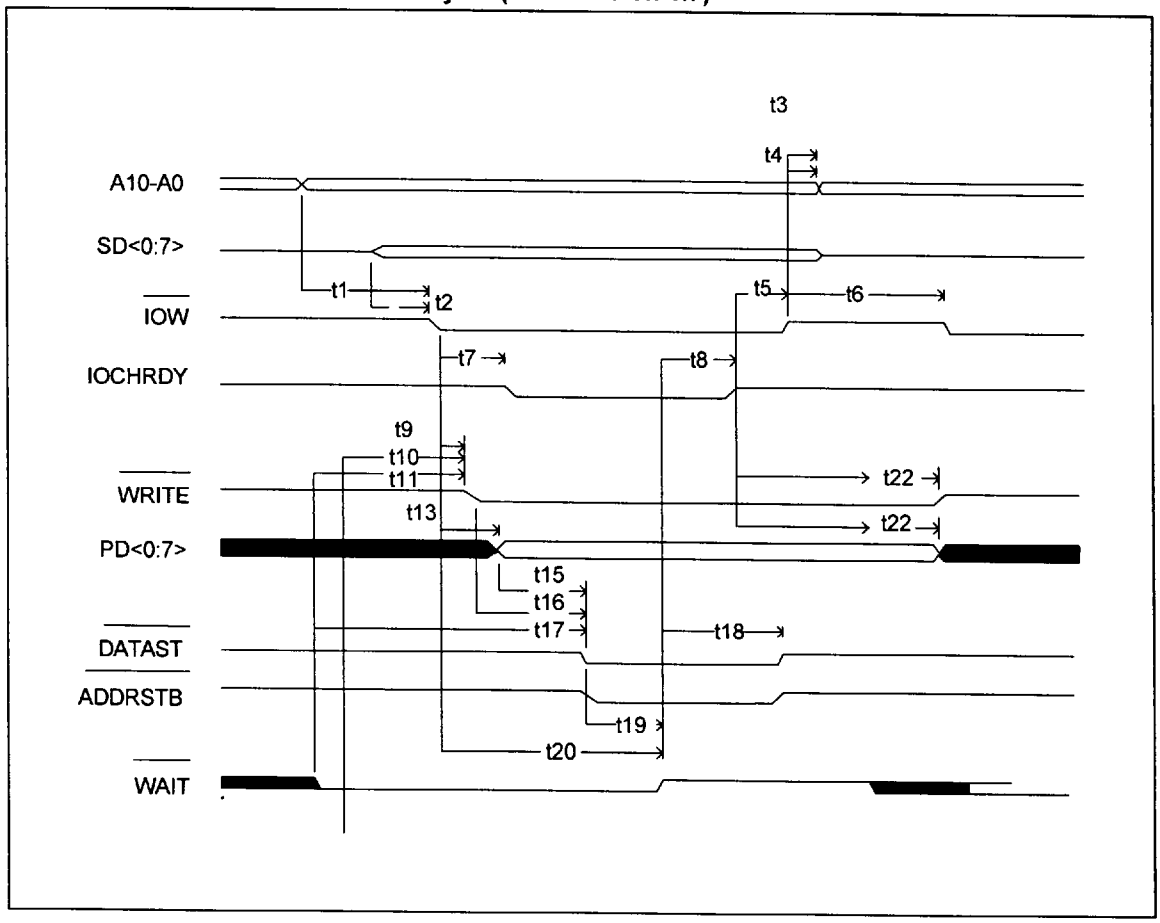
10.4.3 EPP Data or Address Write Cycle (EPP Version 1.9)



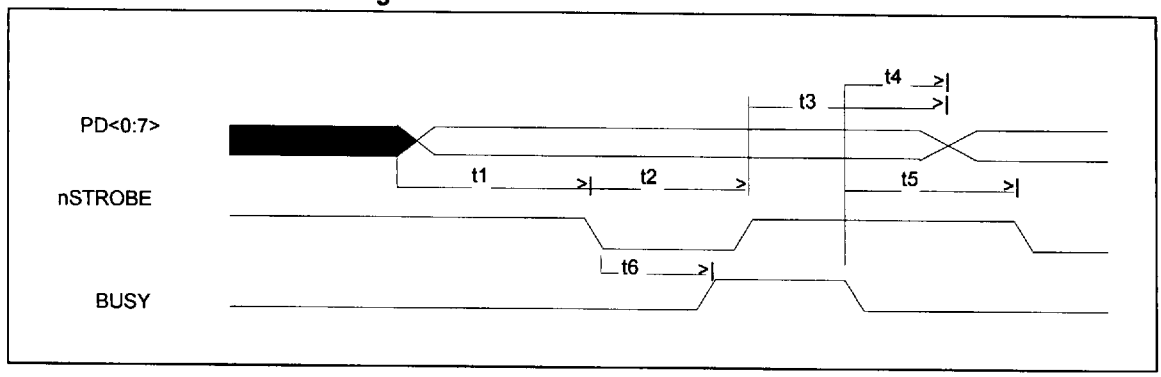
10.4.4 EPP Data or Address Read Cycle (EPP Version 1.7)



10.4.5 EPP Data or Address Write Cycle (EPP Version 1.7)



10.4.6 Parallel Port FIFO Timing



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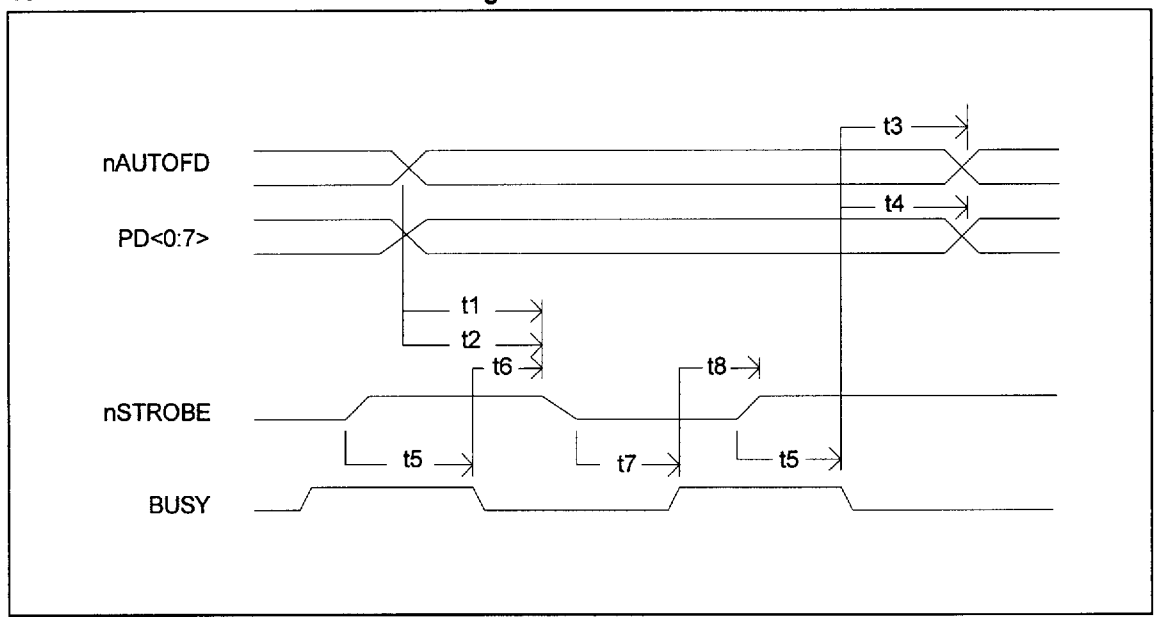
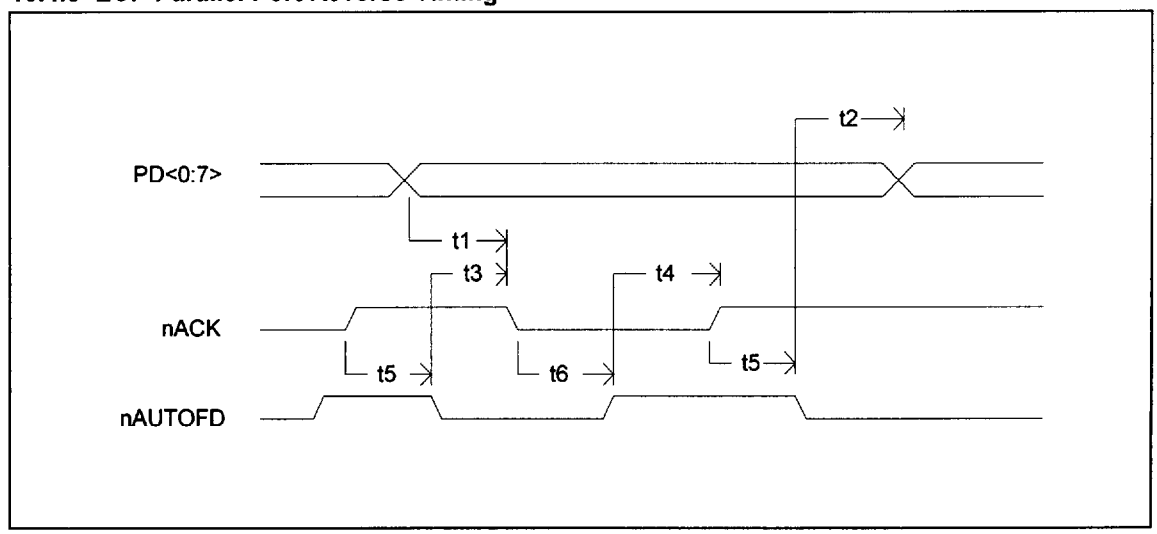
10.4.7 ECP Parallel Port Forward Timing

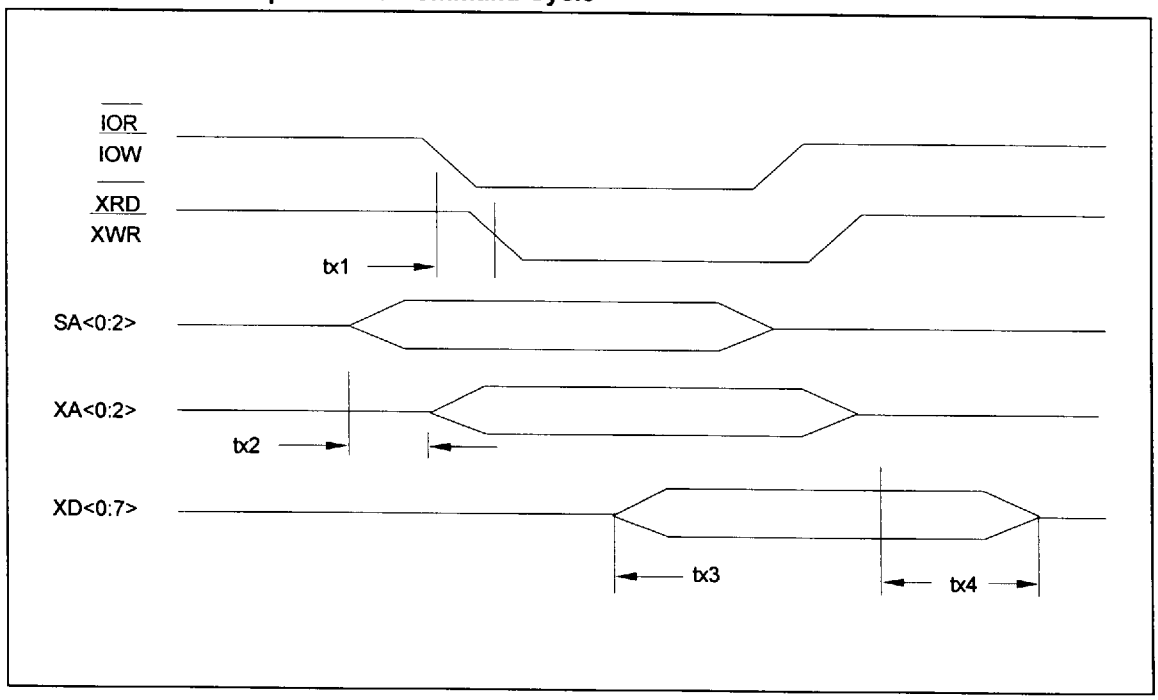


10.4.8 ECP Parallel Port Reverse Timing

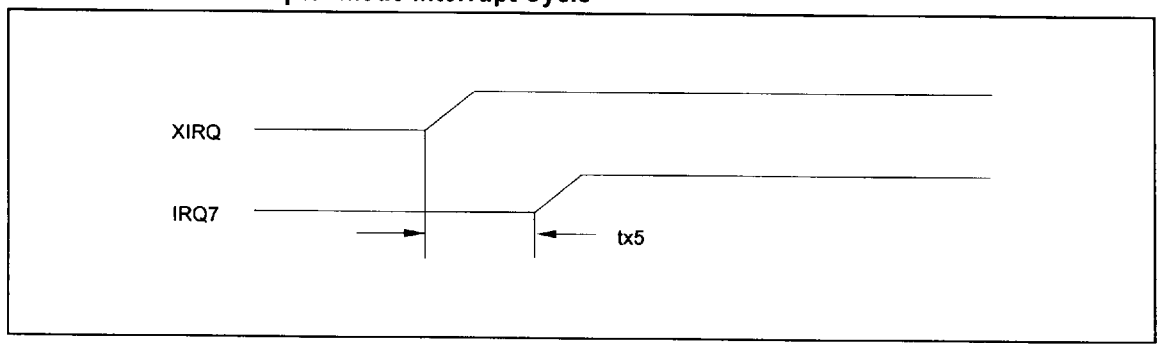


Publication Release Date: Sep. 1996
Preliminary Version 0.50

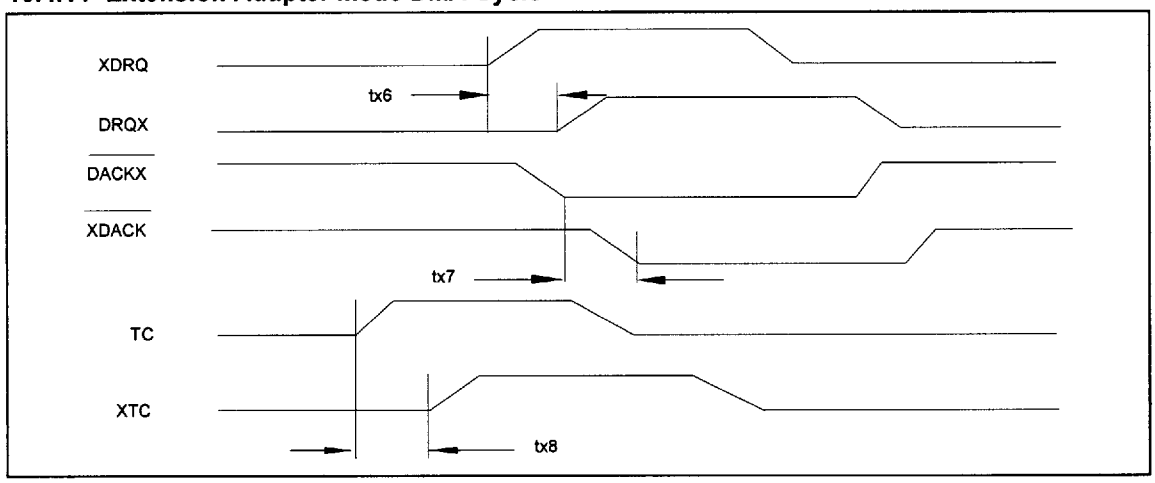
10.4.9 Extension Adapter Mode Command Cycle



10.4.10 Extension Adapter Mode Interrupt Cycle

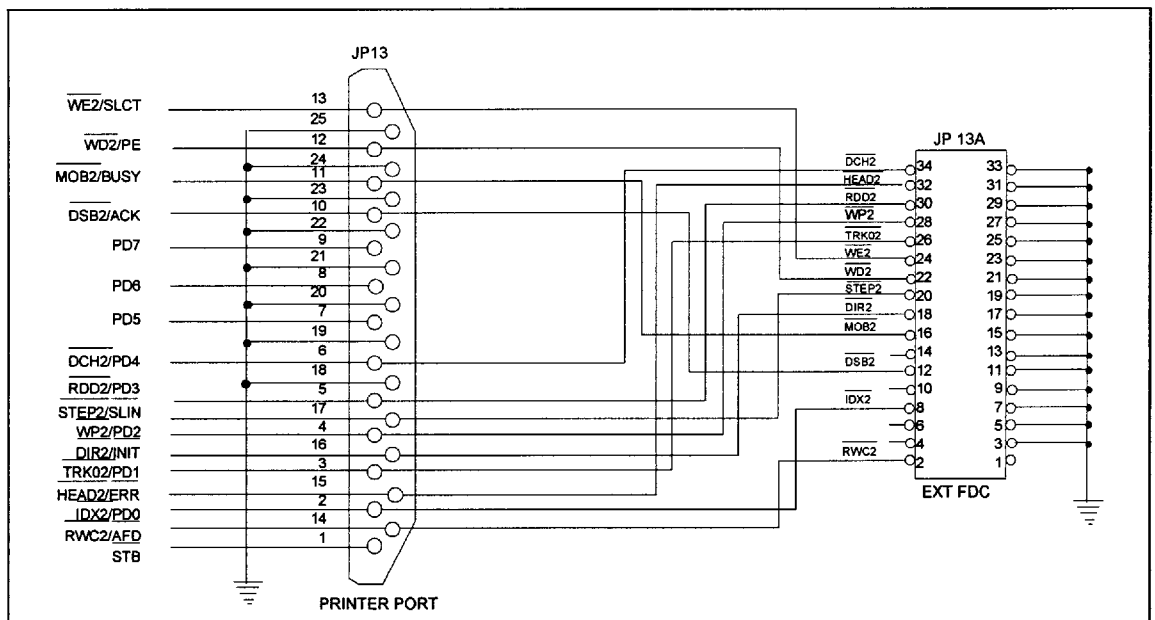


10.4.11 Extension Adapter Mode DMA Cycle



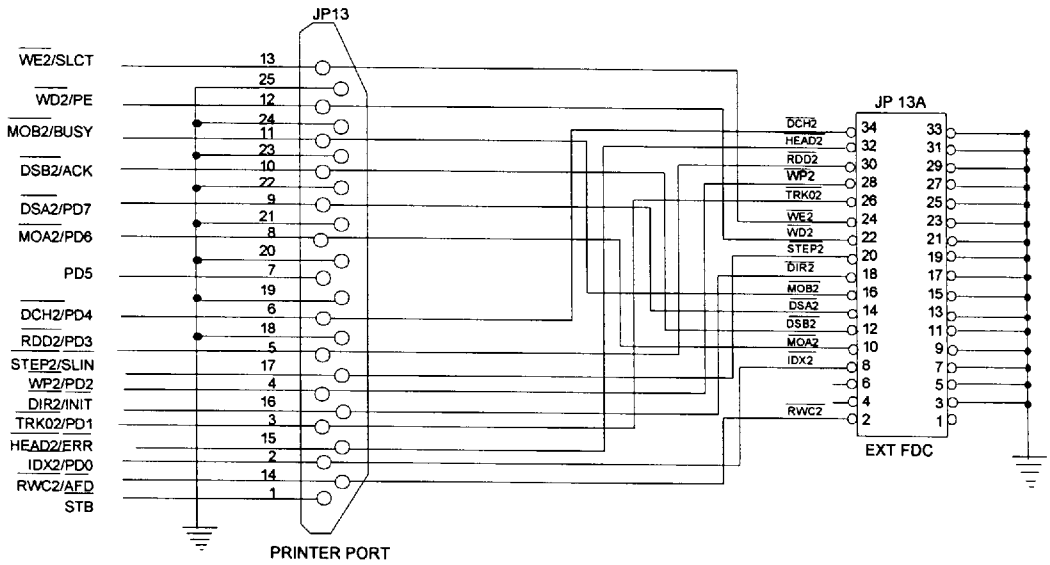
11.0 APPLICATION CIRCUITS

11.1 Parallel Port Extension FDD



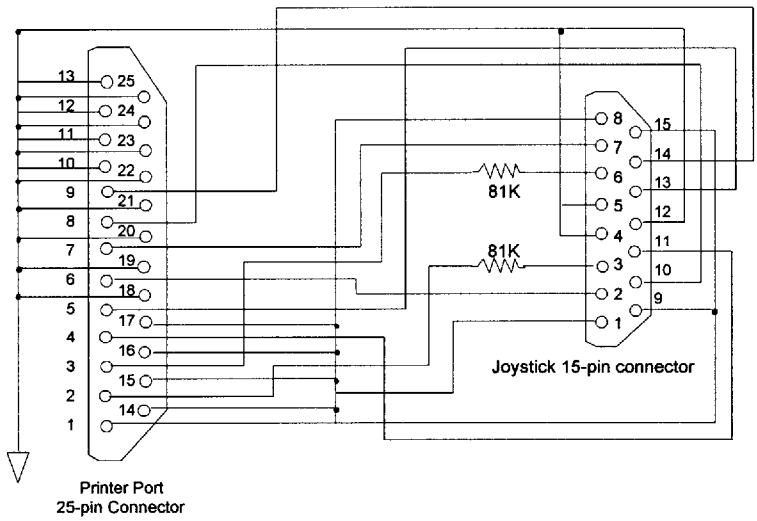
Parallel Port Extension FDD Mode Connection Diagram

11.2 Parallel Port Extension 2FDD



Parallel Port Extension 2FDD Connection Diagram

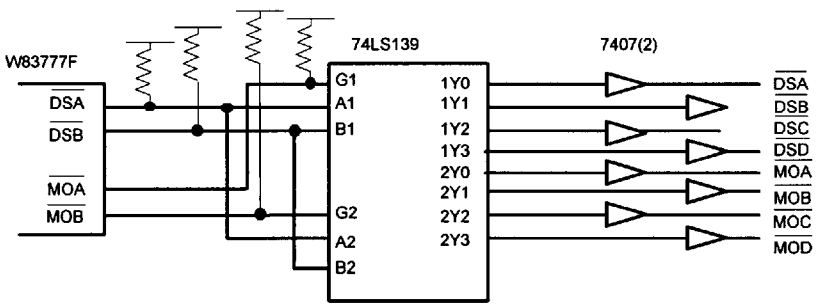
11.3 Parallel Port Joystick Mode



Signal	Joystick 15-pin Connector	Printer Port 25-pin Connector
VDD	1,8,9,15	1,14,15,16,17
GND	4,5,12	18~25
D0	3	2
D1	6	3
D2	NC	4
D3	NC	5
D4	2	6
D5	7	7
D6	NC	8
D7	NC	9

Parallel Port Joystick Mode Connection Diagram

11.4 Four FDD Mode

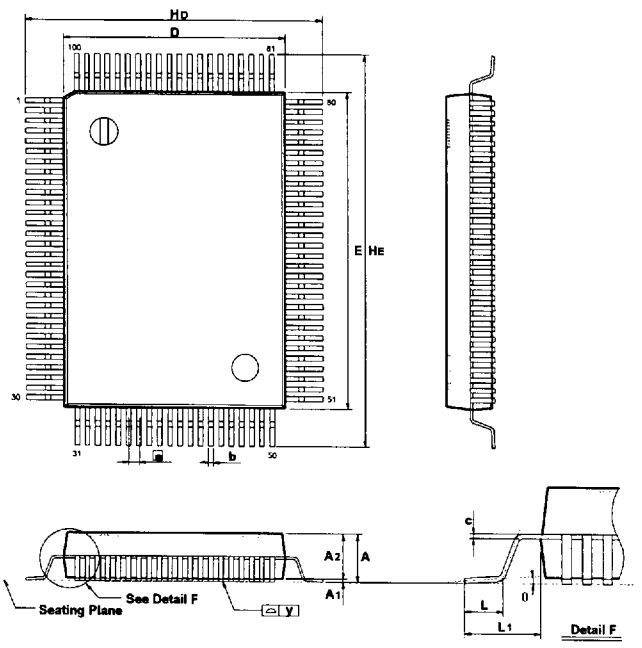


12.0 ORDERING INFORMATION

Part No.	Package
W83877AF	100-pin QFP
W83877AD	100-pin TQFP

13.0 PACKAGE DIMENSIONS

W83877AF (100-pin QFP)



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.010	0.012	0.016	0.25	0.30	0.40
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.50	0.65	0.80
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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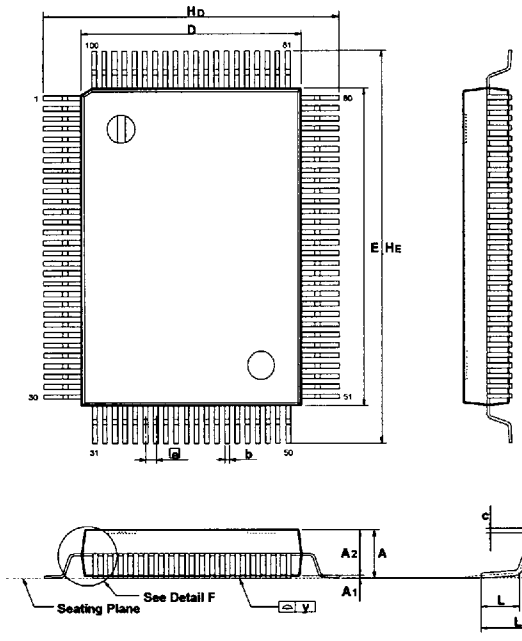
W83877AD (100-pin TQFP)



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.009	0.013	0.015	0.22	0.32	0.38
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		0.039			1.00	
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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Note: All data and specifications are subject to change without notice.