Winbond IPMI Solution

- IPMI BMC (W83910F)
- IPMI Sensor

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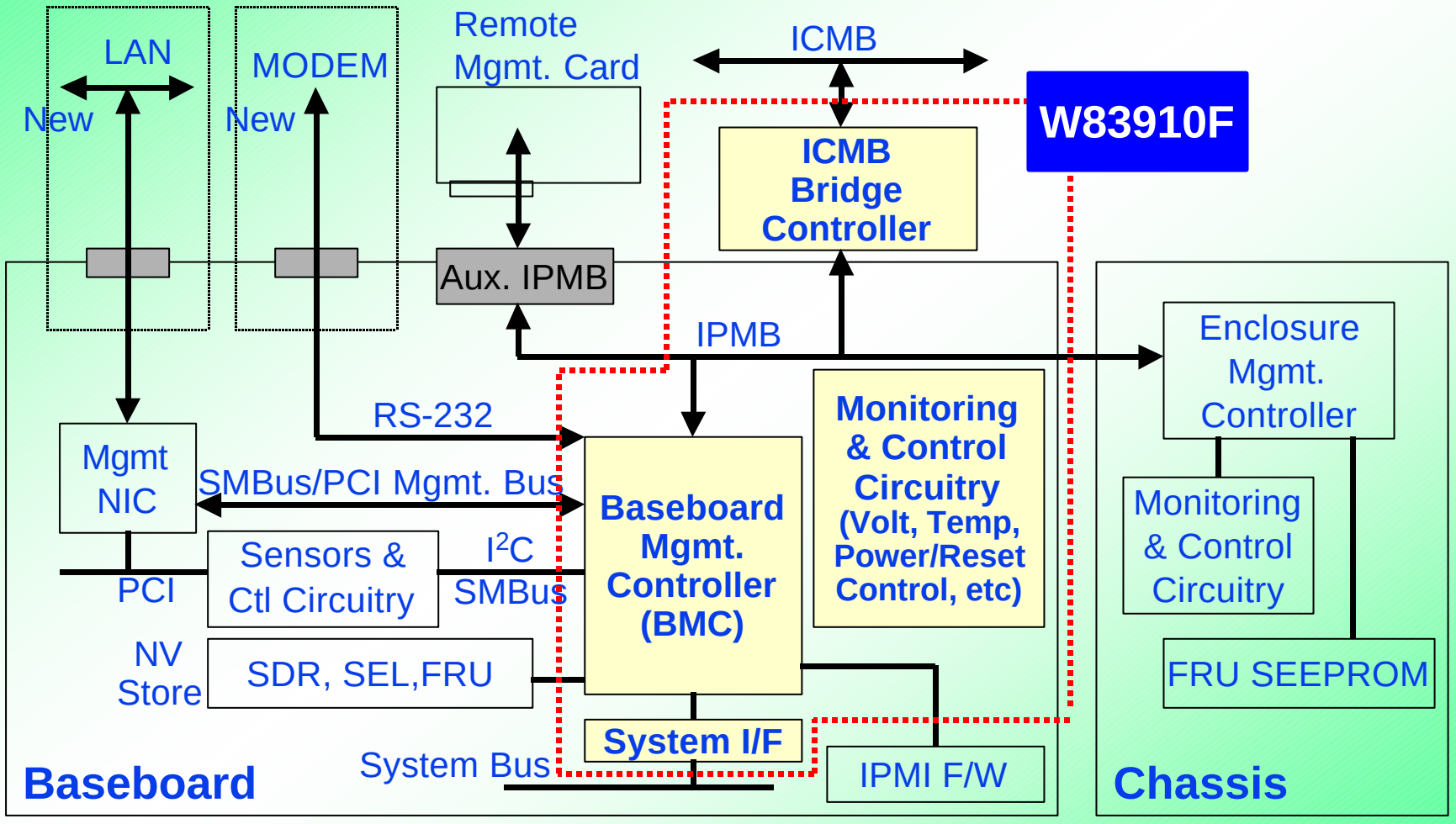
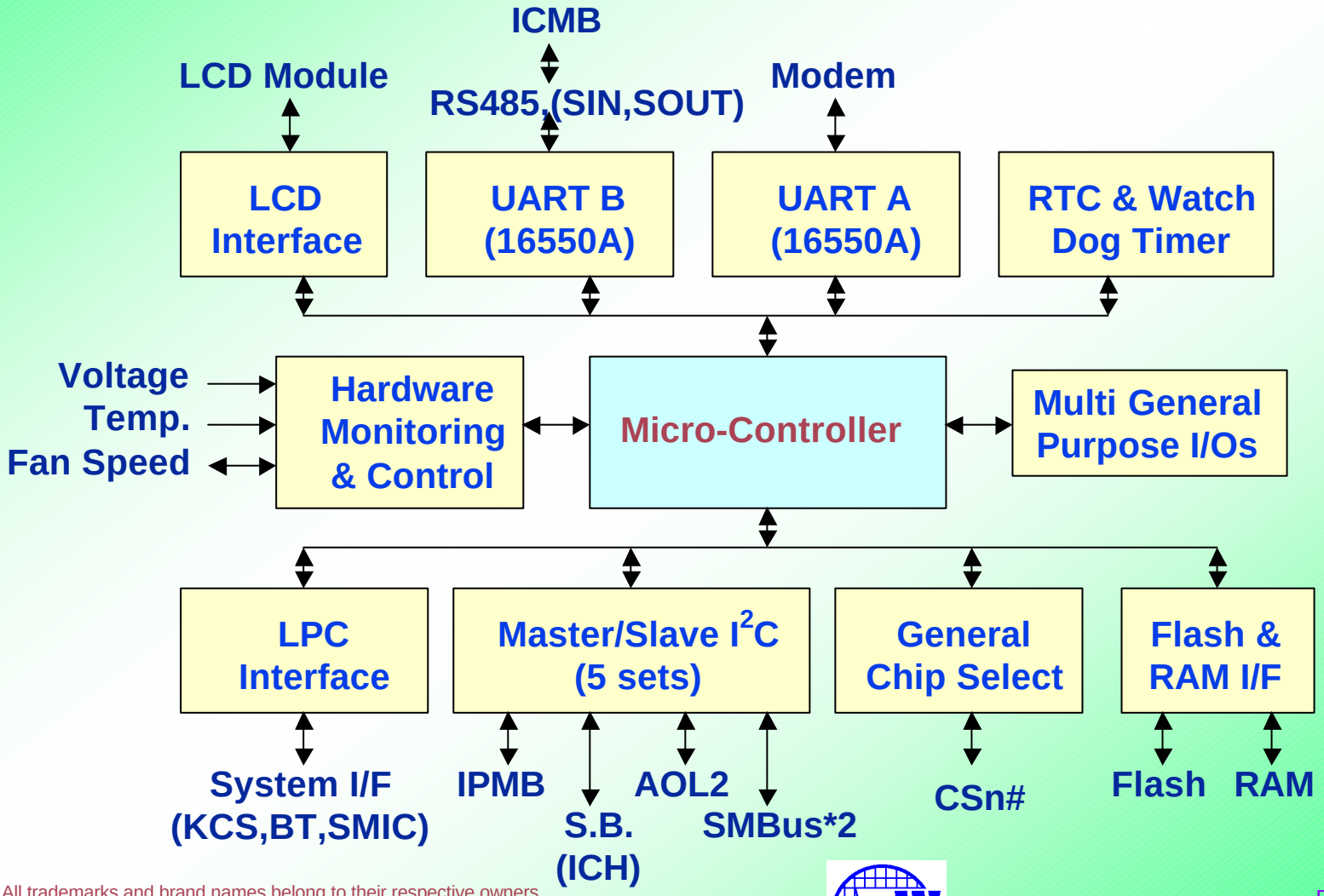
W83910F & IPMI 1.5 Block Diagram



W83910F Block Diagram



W83910F Features (I)

IPMI BMC

- **Micro-Controller**
  - ⇨ 8032 Micro-Controller Based
  - ⇨ Enhanced Peripheral Devices
- **Interface and Connection**
  - ⇨ LPC Interface for System Bus with 3 Physical Protocols
    - ✓ Keyboard Control Style (KCS)
    - ✓ Block Transfer (BT)
    - ✓ Server Management Interface Chip (SMIC)
  - ⇨ 5 Sets of I^2C Controller with 16-Bytes Transfer/Receive FIFOs
    - ✓ All of the 5 Sets Support Master/Slave Mode
  - ⇨ Two 16550A UARTs with 16-Bytes Send/Receive FIFOs
    - ✓ One for Remote Modem Connection
    - ✓ The other for ICMB Connection
  - ⇨ ISA Bus with Companion Chip

W83910F Features (II)
IPMI BMC

❑ Built-In Basic Hardware Monitoring (Sensor)

⇨ 3 Thermal, 7 Voltages, 3 Fan Speed in Standard Mode

✓ 3 Thermal Inputs Optionally for
- Remote Thermistors
- 2N3904 NPN-type Transistors
- Intel™ CPU Thermal Diode Interface

✓ 7 Voltage Inputs

✓ 3 Sets of Fan Control
- Fan Speed Monitoring
- PWM (Pulse Width Modulation) Outputs for Fan Control

⇨ 8 Thermal, 12 Voltages, 8 Fan Speed in Multiplex Mode

W83910F Features (III)

IPMI BMC

- **Memory and Extra I/O Ports Support/Control**
  - ⇨ **Provide/Support 1KB Internal SRAM**
  - ⇨ **Support up to 128KB External Flash Memory**
    - ✓ **Rewriteable I/F for 64KB Flash Memory (Default)**
    - ✓ **PSENHIGH Pin for Extra 2 Bank 64KB Flash Memory Switch**
  - ⇨ **Support up to 128KB External SRAM**
    - ✓ **Interface for 64KB SRAM (Default)**
    - ✓ **4 Chip Select Pins for Extra 64KB SRAM, Every Pin Control 16KB**
  - ⇨ **Support Extra I/O Ports by 4 Chip Select Pins (The Same Pins as the Above Item)**
    - ✓ **Interface for Informative LCD Module**

W83910F Features (IV)

IPMI BMC

- **Others**
  - ⇨ Real Time Clock
  - ⇨ Watch Dog Timer
  - ⇨ 40 Programmable General Purpose I/O Pins
- **Power Supply**
  - ⇨ 5V Vcc for Legacy Devices; 5V AVcc for Analog Vcc (H/W Monitor); 3.3V Vcc for LPC Interface; 5V Vsb; Vbat
  - ⇨ Separate Vss for Digital and Analog Devices
- **128-PQFP**
  - ⇨ More Economic for Cost
  - ⇨ More Flexible for Layout

W83910F Features (V)

Debugger and Firmware

- **Debugger**
  - ⇨ System Side Emulator
    - ✓ Interface with W83910F via LPC Bus
  - ⇨ Windows 2000, NT 4.0 Based
  - ⇨ Perform Like Standard 80C32 Emulator
  - ⇨ Friendly to Develop W83910F Firmware
  - ⇨ On-line Flash (BMC Firmware) Burning
  - ⇨ Direct Control to the Devices Monitor by W83910F
- **BMC Firmware**
  - ⇨ Support IPMI, IPMB, ICMB Commands
  - ⇨ Pass Intel ICTS (IPMI Conformance Test Suite)
- **Others**
  - ⇨ Driver Supports SMIC, KCS, BT Interface and Dynamics Switch
  - ⇨ Provide Snap-in to Support MMC (Microsoft Management Console) on Windows 2000

Winbond Hardware Monitor (Sensor) Overall Introduction

- W83781D --- 7 Voltage, 3 Fan On/Off, 3 Temp. Sensor (Thermistor)
- W83782D --- 9 Voltage, 3 Fan PWM Control, 3 Temp. Sensor (Thermistor, Thermal Diode, 2N3904)
- W83783S --- 5 Voltage, 2 Fan PWM Control, 2 Temp. Sensor (Thermistor, Thermal Diode, 2N3904)
- W83L784R --- 5 Voltage, 2 Smart Fan™ Control, 2 Temp. Sensor (Thermistor, Thermal Diode, 2N3904)
- W83L785R --- 4 Voltage, 2 Fan PWM Control, 2 Temp. Sensor, 9 GPIO (Thermistor, Thermal Diode, 2N3904)
- W83791D --- Most Features of W83782D + Speech + ASF Sensor Spec.

W83791D Features

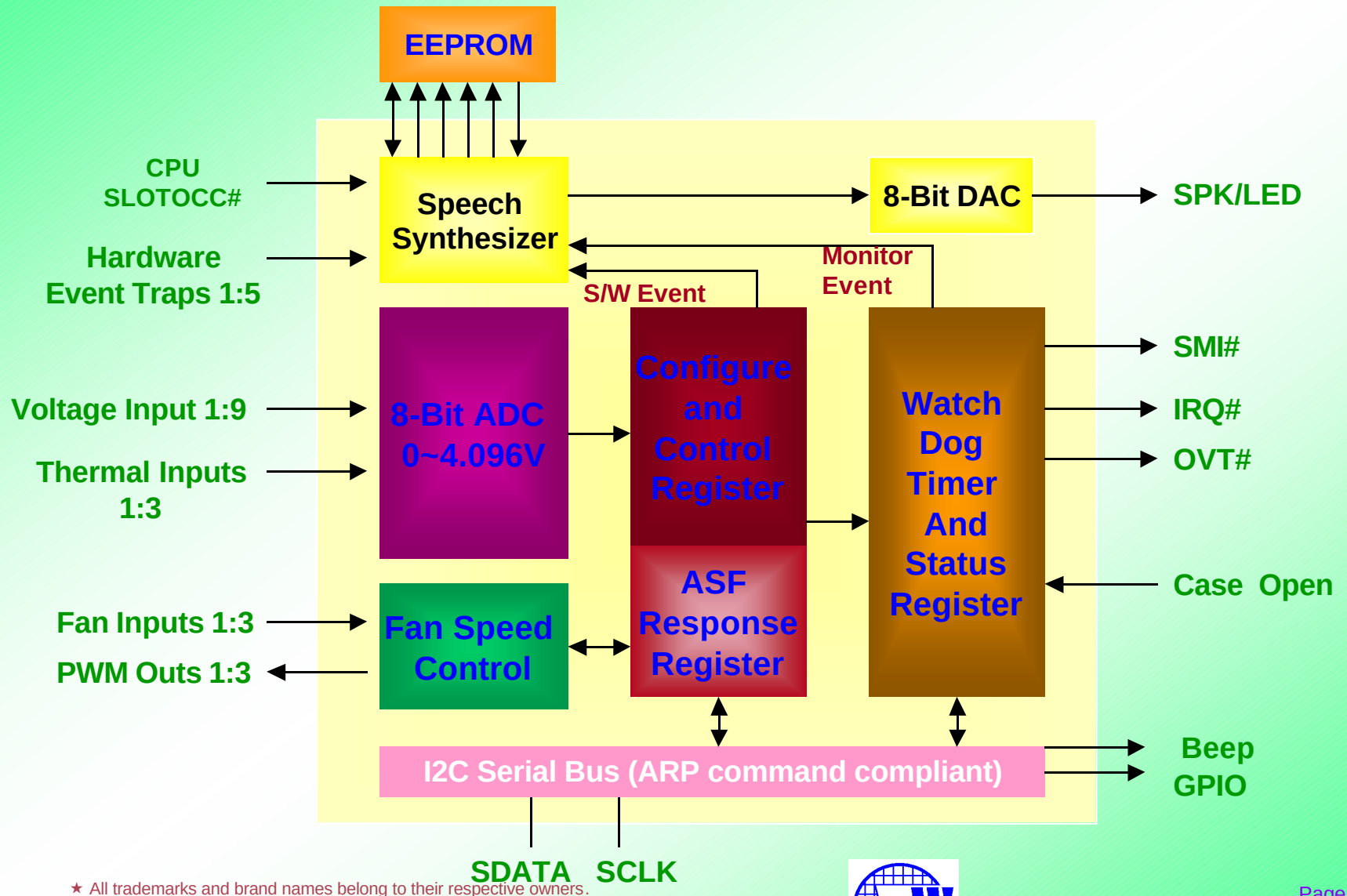
IPMI and ASF Sensor

❑ Unique Functions

- ⇨ Speech Function with Winbond Flash EEPROM W55FXX
- ⇨ SMBus 2.0 ARP Command Compliant
- ⇨ ASF Sensor Spec. Compatible
- ⇨ Intel CPU VID Table Selection --- VRM 8.4 and VRM 9.0 Compliant
- ⇨ 5 VID Input/Output Pins for CPU VID Control
- ⇨ Powered By 5VSB
- ⇨ 3 Sets of Smart Fan Control and 2 Sets of PWM Fan Control (Optional with Speech Function Pins)

- Internal Clock Oscillation
- Most Features of W83782D
- 2 Address Setting Pins for Multiple Devices Support (up to 4 Devices)
- I2C Serial Bus Interface Only
- 48-LQFP

W83791D Block Diagram



ASF(Alert Standard Forum) Spec. Introduction

- **Goal**
  - To Enable Remote System Access and Control for Network Management in Both OS-present and OS-absent Environment
- **Implementation**
  - LAN and Sensor Devices Are Powered by VSB
  - Standard I/F of Alerting Solutions for Different System and Chip Vendors
- **Importance & Advantage**
  - ASF Will Be a Network Management Standard Spec. Boosted by Intel, 3Com, Gateway, Dell, Compaq ..etc.
  - Real Client PCs Management even None OS
  - To Reduce Network Maintain and Service Cost of MIS People

W83910F
Winbond IPMI
BMC

Winbond Electronics Corp.

PRELIMINARY

1. GENERAL DESCRIPTION

W83910F is a management controller of Intelligent Platform Management Interface (IPMI). The management controller is based on the micro-controller 80C32 and enhances the peripheral device in the micro-controller, that including full function UART 16550A, System Management Bus (SMBus), system hardware monitor, PWM Control, and GPIO. LPC interface is supported to communicate with system management software (SMS). There are three physical protocols, which are SMIC (Server Management Interface Chip), and KCS (Keyboard Controller Style), and BT (Block Transfer), between the management controller W83910F and the system host.

Micro-controller 80C32 is built inside the W83910F. The maximum 64K-byte flash memory interface signals are including 8-bit Address/Data Bus, one address latch signal ALE, 8-bit high address bus, and external data memory control signal that can record the System Event Log (SEL) data. Two programming Chip Selects (CSA#, CSB#) are provided to select different memory ranges or I/O port ranges. The W83910F provides two UART ports that are fully compatible with 16550A. One UART port supports full MODEM connection signals which that can use external machine to communicate the management controller. Another UART port only supports 3-wire connection signals which can communicate with the Intelligent Chassis Management Bus (ICMB). There are 5-set System Management Buses (SMBus) in the W83910F, which support 16 bytes Transfer/Receive FIFO and provide master/slave mode. One of SMBus is connected to Intelligent Management Platform Bus (IPMB) to access/control chassis management controller or Field Replaceable Unit (FRU) SEEPROM or AUX/Management-card connector. The others can be severed as private I^2C to access FRU SEEPROM on the memory or processor board.

An 8-bit analog-to-digital converter (ADC) was built inside W83910F. The W83910F can monitor 7 analog voltage inputs , 3 fan tachometer inputs, 3 temperature sensors or remote temperature sensors. The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ CPU with thermal diode output. The W83910F provides 3 PWM (pulse width modulation) outputs to support fan speed control .

The system management software (SMS) can communicate with W83910F through the LPC interface. There are three physical interfaces (SMIC, KCS, and BT) in the W83910F to request/response the IPMI messages. GPIO pins are supported to control/detect the external signal. The grouped interrupt and interrupt status are supported to give micro-controller as a service pointer when the GPIO input signal has a edge transition.

For the spacing saving consideration of the Baseboard Management Controller system, W83910F is in the package of 128-pin PQFP.

1. FEATURES

1.1 Micro-Controller Peripheral

- Two compatible 16550A UART port

--- One supports full MODEM connection signals

--- One supports 3-wire connection signals

- Five sets system management Bus or master/slave I^2C interface
- Hardware monitor
  - 7 voltages, 3 fan speed, 3 temperature (Standard mode)
  - 12 voltages, 8 fan speed, 8 temperature (with Multiplexer mode)
- GPIO pins
- Three system management software interface using LPC

--- Server Management Interface Chip (SMIC) interface

--- Keyboard Control Style (KCS) interface

--- Block Transfer (BT) interface

- Two system watch-dog timer

--- Watch-dog Timer is supported to restart system

--- Restart event record

1.2 UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- Fully programmable serial-interface characteristics:

--- 5, 6, 7 or 8-bit characters

--- Even, odd or no parity bit generation/detection

--- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:

--- Loop-back controls for communications link fault isolation

--- Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz by 1 to (2^{16}-1)

1.3 Hardware Monitoring Items

- 3 thermal inputs from remote thermistors or 2N3904 NPN-type transistors or PII /PIII) thermal diode output
- 7 voltage inputs and one internal power voltage
- 3sets of fan speed control and fan speed monitoring input

--- PWM (pulse width modulation) outputs for fan speed control

1.4 Real Time Clock

- 27 bytes of clock, and control/status register (14 bytes in Bank 0 and 13 bytes in Bank 2); 242 bytes of general purpose RAM
- BCD or Binary representation of time, calendar, and alarm registers
- Counts seconds, minutes, hours, days of week, days of month, month, year, and century
- 12-hour/ 24-hour clock with AM/PM in 12-hour mode
- Daylight saving time option; automatic leap-year adjustment

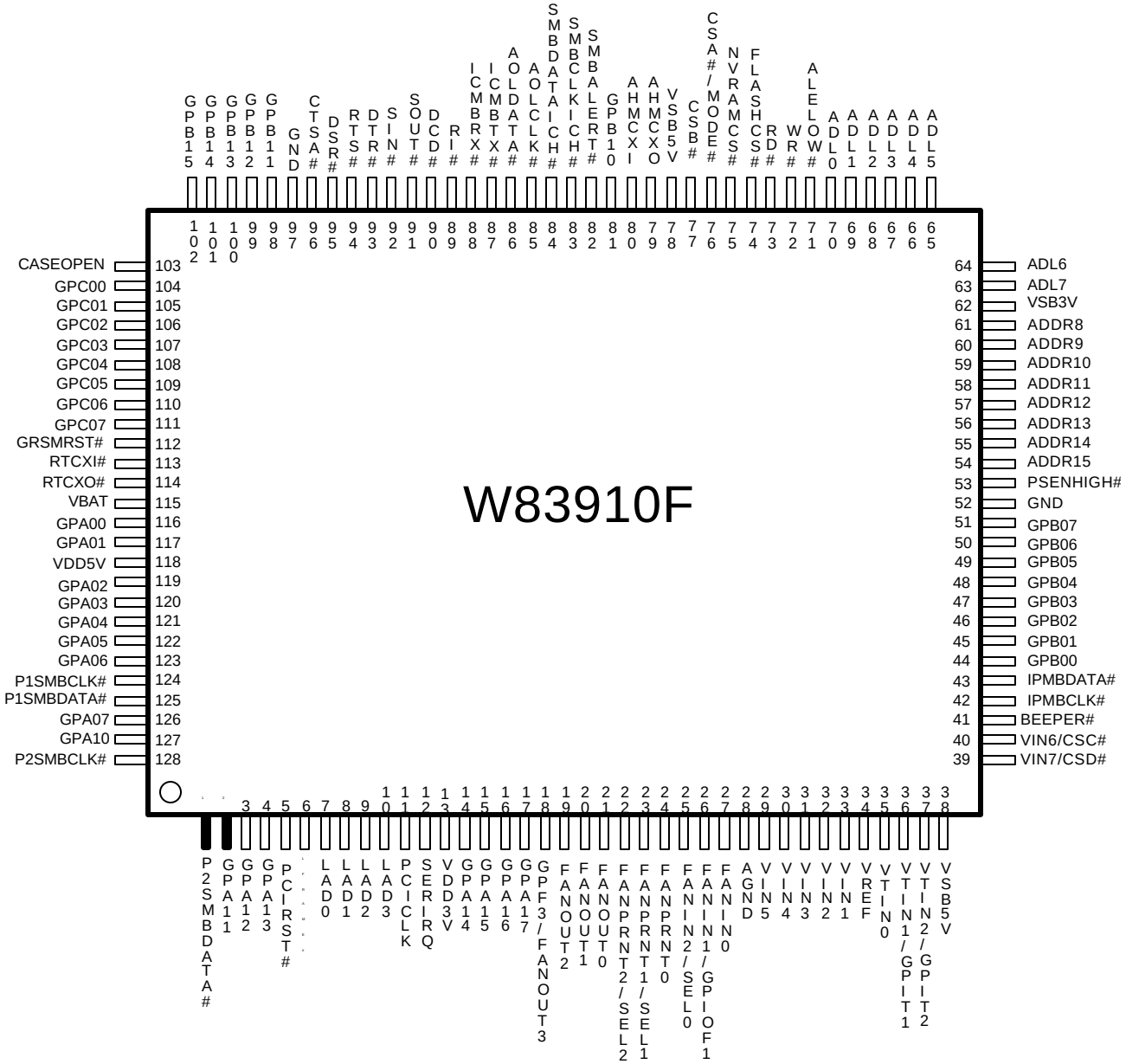
1.5 General

- LPC Interface with Serial IRQ
- I^2C^{TM} serial bus interface
- 5V VDD or VSB operation

1.6 Package

- 128-pin PQFP

2. PIN CONFIGURATION



3. PIN DESCRIPTION

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12tp3} - 3.3V TTL level bi-directional pin with 12 mA source-sink capability

I/OD_{12t} - TTL level bi-directional pin open drain output with 12 mA sink capability

I/O_{24t} - TTL level bi-directional pin with 24 mA source-sink capability

OUT_{12t} - output pin with 12 mA source-sink capability

OUT_{12tp3} - 3.3V TTL level output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

IN_{cs} - CMOS level Schmitt-trigger input pin

IN_{t} - TTL level input pin

IN_{td} - TTL level input pin with internal pull down resistor

IN_{ts} - TTL level Schmitt-trigger input pin

IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin

A_{IN} - Analog input

A_{OUT} - Analog output

Pin No.	Pin name	Type	Description
LPC Interface .			
5	PCIRST#	IN_{tsp3}	LPC interface reset signal (PCIRST#)
6	LFRAME#	IN_{tsp3}	Indicates start of a new cycle, termination of broken cycle.
10,9,8,7	LAD[3:0]	I/O_{12tp3}	Multiplexed Command, Address, and Data bus
11	PCICLK	IN_{tsp3}	33M Hz clock input for LPC bus
12	SERIRQ	I/OD_{12t}	This signal implements the serial interrupt protocol
System I2C Interface.			
124	P1SMBCLK#	I/OD_{12st}	Private I^2C^{TM} bus 1 clock
125	P1SMBDATA#	I/OD_{12st}	Private I^2C^{TM} bus 1 data.
128	P2SMBCLK#	I/OD_{12st}	Private I^2C^{TM} bus 2 clock
1	P2SMBDATA#	I/OD_{12st}	Private I^2C^{TM} bus 2 data.
IPMB Interface.			
42	IPMBCLK#	I/OD_{20st}	IPMB clock
43	IPMBDATA#	I/OD_{20st}	IPMB data
RS-232 serial interface to connect to MODEM.			
96	CTS#	IN_{t}	Clear To Send
95	DSR#	IN_{t}	Data Set Ready
94	RTS#	OUT_{8}	Request To Send

93	DTR#	OUT_8	Data Terminal Ready
92	SIN	IN_t	Receiver Data Input
91	SOUT	OUT_8	Transmitter Data Output
90	DCD#	IN_t	Data Carrier Detect
89	RI#	IN_t	Ring Indicator
Serial interface to connect ICMB			
88	ICMBRX#	IN_t	ICMB Receiver Data Input
87	ICMBTX#	OUT_8	ICMB Transmitter Data Output
Flash ROM & NVRAM interface			
71	ALE	OUT_{12}	Address Latch enable
63-70	ADL[7:0]	I/O_{12t}	ADDR/Data Bus
53-61	ADDR[16:8]	OUT_{12}	Address bus
72	WD#	OUT_{12}	Write Command
73	RD#	OUT_{12}	Read Command
74	FLASHCS#	I/O_{12st}	Flash rom chip select
75	NVRAMCS#	OUT_{12t}	Non-volatile ram chip select
76	CSA# / MODE#	O_{12t} / I_{ts}	General Purpose Chip Select# / Standard or Multiplex mode trapping
77	CSB#	O_{12t}	General Purpose Chip Select#
Private I2C interface			
82	SMBALERT#	I/OD_{6st}	SMBus alert
83	SMBCLKICH#	I/OD_{6st}	I2C bus Clock signal
84	SMBDATAICH#	I/OD_{6st}	I2C bus Data signal
85	AOLCLK#	I/OD_{6st}	I2C bus Clock signal/AOL-II
86	AOLDATA#	I/OD_{6st}	I2C bus Data signal/AOL-II
112	GRSMRST#	I_{ts}	Resume reset from standby power good.
BMC & RTC crystal			
80	BMCXI	XI	40MHz Crystal/Clock input for BMC
79	BMCXO	XO	Crystal output from BMC
113	RTCXI	XI	32.768KHz Crystal input for RTC
114	RTCXO	XO	Crystal output for RTC
Hardware monitor sensor input			
33	VIN1	AIN	Voltage sensor 1
32	VIN2	AIN	Voltage sensor 2
31	VIN3(+5V)	AIN	Voltage sensor 3
30	VIN4(+12V)	AIN	Voltage sensor 4
29	VIN5(+3V)	AIN	Voltage sensor 5
40	VIN6 / CSC#	AIN	Voltage sensor 6 / General Purpose Chip Select#

39	VIN7 / CSD#	AIN	Voltage sensor 7 / General Purpose Chip Select#
34	VREF	AOUT	Reference voltage output
35	VTIN0	AIN	Thermal sensor input 0
36	VTIN1 / GPIT1	AIN	Thermal sensor input 1 / When at Multiplex mode, this pin is GPI function.
37	VTIN2 / GPIT2	AIN	Thermal sensor input 2 / When at Multiplex mode, this pin is GPO function.
27	FANIN0	I_{ts}	Fan tachometer input 0
26	FANIN1 / GPIOF1	I_{ts}	Fan tachometer input 1 / When at Multiplex mode, this pin is GPIO function
25	FANIN2 / SEL0	I_{ts} / OUT_{12}	Fan tachometer input 2 / Multiplex mode select output 0
24	FANPRNT0	I_{ts}	Fan present input 0
23	FANPRNT1 / SEL1	I_{ts} / OUT_{12}	Fan present input 1 / Multiplex mode select output 1
22	FANPRNT2 / SEL2	I_{ts} / OUT_{12}	Fan present input 2 / Multiplex mode select output 2
21	FANOUT0	OUT_{12}	Fan PWM output 0 to control fan speed
20	FANOUT1	OUT_{12}	Fan PWM output 1 to control fan speed
19	FANOUT2	OUT_{12}	Fan PWM output 2 to control fan speed
18	GPF3 / FANOUT3	I_{ts} / OUT_{12}	General Purpose Output / Fan PWM output 3 to control fan speed in Multiplex mode
41	BEEPER#	OUT_{12}	Alarm sound output
103	Caseopen	I/OD_6	Chassis intrude indicator. An active high input from an external circuit which latches a Case Open event..
Power and ground			
28	AGND	Ground	Analog ground
52,97	GND	Ground	Ground
115	VBAT	Power	Battery Power
38,78	VSB5V	Power	5V standby power
62	VSB3V	Power	3V standby power
13	VDD3V	Power	3V power
118	VDD5v	Power	5V power
General Purpose I/O pins			
2,3,4,14,15 ,16,17, 116,117, 126,127, 119~123	GPA00 ~ GPA07, GPA10~GPA17	I/OD_{12st}	General Purpose I/O with VCC power
44~51,81, 98~102	GPB00~GPB07, GPB10~GPB15	I/OD_{12st}	General Purpose I/O with VSB power
104~111	GPC00~GPC07	I_{ts}	General Purpose I/O with VBAT power