Chapter 6. Specifications

These specifications are subject to change without notice.
Please contact your sales office for the latest specifications.

6.1. Absolute Maximum Ratings

Supply Voltage	–0.3 to 7.0 V	Storage Temperature Range	–40 °C to 125 °C
Input Voltage	–0.3 V to V_{CC}	Lead Temperature (10 seconds)	300 °C
Output Voltage	–0.3 V to V_{CC}	Junction Temperature	175 °C

Figure 64. Absolute maximum ratings

6.2. Recommended Operating Conditions

PARAMETER		COMMERCIAL			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
T_A	Operating ambient temperature	0		70	°C

Figure 65. Recommended operating conditions

6.3. DC Specifications

Parameter		Test Conditions	Commercial		UNIT
			MIN	MAX	
V_{IH}	High-level input voltage		2.0		V
V_{IHC}	High-level input voltage for CLK only		2.0		V
V_{IL}	Low-level input voltage			0.8	V
V_{ILC}	Low-level input voltage for CLK only			0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –1.0 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 4.0 mA		0.4	V
I_{LI}	Input leakage current	V_{CC} = MAX, V_{IN} = 0–V_{CC}		±10	µA
I_{LO}	Output leakage current (Output disabled)	V_{CC} = MAX, V_{IN} = 0–V_{CC}		±10	µA
I_{CC}	Standby current	V_{CC} = MAX, DC conditions TTL inputs		75	mA
I_{DD}	Switching current	V_{CC} = MAX, T_{CY} = MIN, TTL inputs		200	mA
C_{IN}	Input capacitance*	$_{TA}$ = 255C		2	pF
C_{CLK}	Clock capacitance*	f = 1 MHz		4	pF
C_{OUT}	Output capacitance*	V_{CC} = 5.0 V		4	pF

*Capacitance not tested

6.4. AC Specifications

Param.	Description	Edge	MIN	MAX	Unit	Loading	Notes
Clocks							
T_{MCY}	MEMCLK period		20		ns		50.0 MHz
T_{MCH}	MEMCLK high		6.6		ns		
T_{MCL}	MEMCLK low		6.6		ns		
T_{PCY}	PIXCLK period		12.5		ns		80.0 MHz
T_{PHC}	PIXCLK period (16-bit mode)		20		ns		50.0 MHz
T_{PCH}	PIXCLK high		5		ns		
T_{PCL}	PIXCLK low		5		ns		
T_{PHH}	PIXCLK high (16-bit mode)				ns		
T_{PHL}	PIXCLK low (16-bit mode)				ns		
Reset Parameters							
T_{RST}	Reset pulse width		175		ns		7 MEMCLKs
T_{MS}	Mode setup		10		ns		
T_{MH}	Mode hold		10		ns		
T_{REV}	Reset disabled to SE enabled		15		ns	50 pF	
Host Bus Interface							
T_{ACS}	Address to command setup		5		ns		
T_{ACH}	Address from command hold		5		ns		
T_{BCS}	BHEN to command setup		5		ns		
T_{BCH}	BHEN to command hold		5		ns		
T_{MRP}	MEMR pulse width		5M		ns		
T_{MWP}	MEMW pulse width		5M		ns		
T_{IRP}	IORD pulse width		5M		ns		
T_{IWP}	IOWR pulse width		5M		ns		
T_{BPW}	BALE pulse width		30		ns		
T_{ATC}	AEN valid to command		100		ns		
T_{BTC}	BALE to command		30		ns		
T_{CTA}	Command to AEN invalid		30		ns		
T_{RCS}	REFRESH to command setup		5		ns		
T_{CRH}	Command to REFRESH hold		5		ns		
T_{DCS}	Write data to command setup				ns		
T_{CTM}	Command to MISCWR– active				ns	30 pF	
T_{MTC}	MISCWR– to command inactive		20		ns	30 pF	
T_{MPW}	MISCWR– pulse width		20		ns	30 pF	
T_{AVB}	Address valid to BALE inactive				ns		

Figure 66. Switching characteristics over the operating range. (These specifications are subject to change without notice. Please contact your sales office for the latest specifications.)

6.4. AC Specifications, continued

Param.	Description	Edge	MIN	MAX	Unit	Loading	Notes
Host Bus Interface, continued							
T_{BAH}	BALE inactive to address hold		15		ns		
T_{CZD}	Command to ZEROWS delay				ns	30 pF	
T_{ZPW}	ZEROWS pulse width				ns	30 pF	
T_{CZI}	Command inactive to ZEROWS inactive				ns	30 pF	
T_{AVM}	Address valid to MEMCS16 active			50	ns	30 pF	
T_{AMH}	Address invalid to MEMCS16 hold		0		ns	30 pF	
T_{BED}	BUSOUT– enable delay			15	ns	30 pF	
T_{BDD}	BUSOUT– disable delay			15	ns	30 pF	
T_{CDR}	Command to DACRD–				ns	30 pF	
T_{DRC}	Command inactive to DACRD– inactive				ns	30 pF	
T_{CDW}	Command to DACWR–				ns	30 pF	
T_{DRW}	DACRD– pulse width		50		ns	30 pF	
T_{WPW}	DACWR– pulse width		50		ns	30 pF	
T_{DWC}	DACWR– to command inactive				ns	30 pF	
T_{RDH}	Read data hold		0		ns	30 pF	
T_{CAD}	Command to ACK delay				ns	30 pF	
T_{ATD}	ACK to data			0	ns	30 pF	
T_{APW}	ACK pulse width		120		ns	30 pF	
T_{CDH}	Write command inactive to data hold		0		ns		
T_{ICI}	Inter command idle time				ns		
BIOS ROM, DAC							
T_{CRE}	Command to ROMEN–		50		ns	30 pF	
T_{RPW}	ROMEN– pulse width		5M–4		ns	30 pF	
T_{RS}	ROMEN– data setup		10		ns	30 pF	
T_{IRW}	Inter ROMEN– width		60		ns	30 pF	
T_{RRH}	ROMEN– high to ROMA0 high		5	20	ns	30 pF	
T_{RRL}	ROMEN– high to ROMA0 low		5	20	ns	30 pF	
T_{RAD}	ROM ACK to data			50	ns	30 pF	
T_{BRV}	BHEN to ROMA0 valid		20		ns	30 pF	
T_{ARV}	Address to ROMA0 valid		20		ns	30 pF	
T_{RH}	ROMEN– data hold		5		ns	30 pF	

Figure 66, continued. Switching characteristics over the operating range. (These specifications are subject to change without notice. Please contact your sales office for the latest specifications.)

6.4. AC Specifications, continued

Param.	Description	Edge	MIN	MAX	Unit	Loading	Notes
Video							
T_{HS}	HSYNC output delay	VIDOUTCLK+	10	24	ns	30 pF	
T_{VS}	VSYNC output delay	VIDOUTCLK+	12	32	ns	30 pF	
T_{BK}	BLANK– output delay	VIDOUTCLK+	4	8	ns	15 pF	
T_{VOD}	VIDOUT[7..0]– output delay	VIDOUTCLK+		8	ns	15 pF	
T_{VOV}	VIDOUT[7..0]– valid	VIDOUTCLK+	3		ns	15 pF	
T_{RVD}	VIDOUTCLK rising edge to data	VIDOUTCLK+			ns	15 pF	
T_{FVD}	VIDOUTCLK falling edge to data	VIDOUTCLK+			ns	15 pF	
T_{RDI}	VIDOUTCLK rising edge to data invalid	VIDOUTCLK+			ns	15 pF	
T_{FDI}	VIDOUTCLK falling edge to data invalid	VIDOUTCLK+			ns	15 pF	
VRAM Serial Read							
T_{PVL}	PIXCLK to VIDOUTCLK low		3	12	ns	15 pF	
T_{PVH}	PIXCLK to VIDOUTCLK high		3	12	ns	15 pF	
T_{VOH}	VIDOUTCLK high		5		ns	15 pF	
T_{VOL}	VIDOUTCLK low		5		ns	15 pF	
T_{HVH}	VIDOUTCLK high (16-bit mode)				ns	15 pF	
T_{HVL}	VIDOUTCLK low (16-bit mode)				ns	15 pF	
T_{VSD}	VIDOUTCLK to SERCLK delay		0	1	ns	15 pF	
T_{SVS}	Serial video setup		4		ns	15 pF	
T_{SVH}	Serial video hold		0		ns	15 pF	
T_{SSE}	SERCLK to SE1B–/SE2B– valid		0		ns	50 pF	On SE1B–/SE2B–
						80 pF	On SERCLK
T_{SCP}	SERCLK precharge time		10		ns	80pF	
Frame Buffer							
T_{MRD}	MEMCLK to RASxx delay		6	21	ns	30 pF	
T_{RC}	RAS cycle time		7M		ns	30 pF	
T_{PC}	Page-mode cycle time		5M		ns	30 pF	
T_{RAS}	RAS pulse width		4M–5	4M–1	ns	30 pF	
T_{CAS}	CAS pulse width		4M–5	4M–1	ns	50 pF	
T_{RASP}	RAS page-mode pulse width			64M	ns	30 pF	
T_{CASP}	CAS page-mode pulse width		3M–5	3M–1	ns	50 pF	
T_{ASR}	Address setup to RAS		4		ns	100 pF	On address lines
T_{RAH}	Row address hold		1M–5		ns	100 pF	On address lines
T_{RCD}	RAS to CAS delay		1M+1		ns	50 pF	On CAS

Figure 66, continued. Switching characteristics over the operating range. (These specifications are subject to change without notice. Please contact your sales office for the latest specifications.)

6.4. AC Specifications, continued

Param.	Description	Edge	MIN	MAX	Unit	Loading	Notes
Frame Buffer, continued							
T_{RP}	RAS precharge		3M+1		ns	30 pF	
T_{ASC}	Address setup to CAS		1.5		ns	100 pF	On address lines
T_{CAH}	Column address hold		2M–8		ns	100 pF	On address lines
T_{CPN}	CAS precharge, non-page-mode		3M+1		ns	50 pF	
T_{CP}	CAS precharge, page-mode		2M+1		ns	50 pF	
T_{ROE}	RAS to output enable		15	2M	ns	50 pF	On TRG01–/TRG23–
T_{COE}	CAS to output enable			1M	ns	50 pF	On TRG01–/TRG23–
T_{OEW}	Output enable pulse width		3M–2		ns	50 pF	
T_{OWP}	Output enable pulse width, page mode				ns	50 pF	
T_{CRD}	CAS to read delay, non–page mode			3M	ns	50 pF	On data lines
T_{CRV}	CAS to read valid		0		ns	50 pF	On data lines
T_{RWE}	RAS to write enable		15	2M+1	ns	50 pF	On WE[0..3]–
T_{CWE}	CAS to write enable			1M+1	ns	30 pF	On WE[0..3]–
T_{WP}	Write enable pulse width		3M–4		ns	30 pF	
T_{DWD}	Data to write delay		8		ns	50 pF	On data lines
T_{WDV}	Write to data valid		–3		ns	50 pF	On data lines
T_{PPRS}	Plane-to-plane RAS skew			3M–1	ns	30 pF	
T_{PPCS}	Plane-to-plane CAS skew			3M–1	ns	30 pF	
T_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle			typ 1M		50 pF	
T_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle			typ 6M		50 pF	
Read Transfer Cycle							
T_{TLS}	TR low setup		1M–8		ns	50 pF	
T_{TLH}	TR low hold		3M		ns	50 pF	
T_{DRS}	DSF to RAS setup		1M–8		ns	50 pF	
T_{DRH}	DSF to RAS hold		3M		ns	50 pF	
T_{SRS}	Split read setup		60		ns	50 pF	
T_{SRH}	Split read hold		30		ns	50 pF	
T_{TSD}	TR to first SERCLK delay		25P		ns	50 pF	P=PIXCLK period

Figure 66, continued. Switching characteristics over the operating range. (These specifications are subject to change without notice. Please contact your sales office for the latest specifications.)

6.5. Timing Diagrams

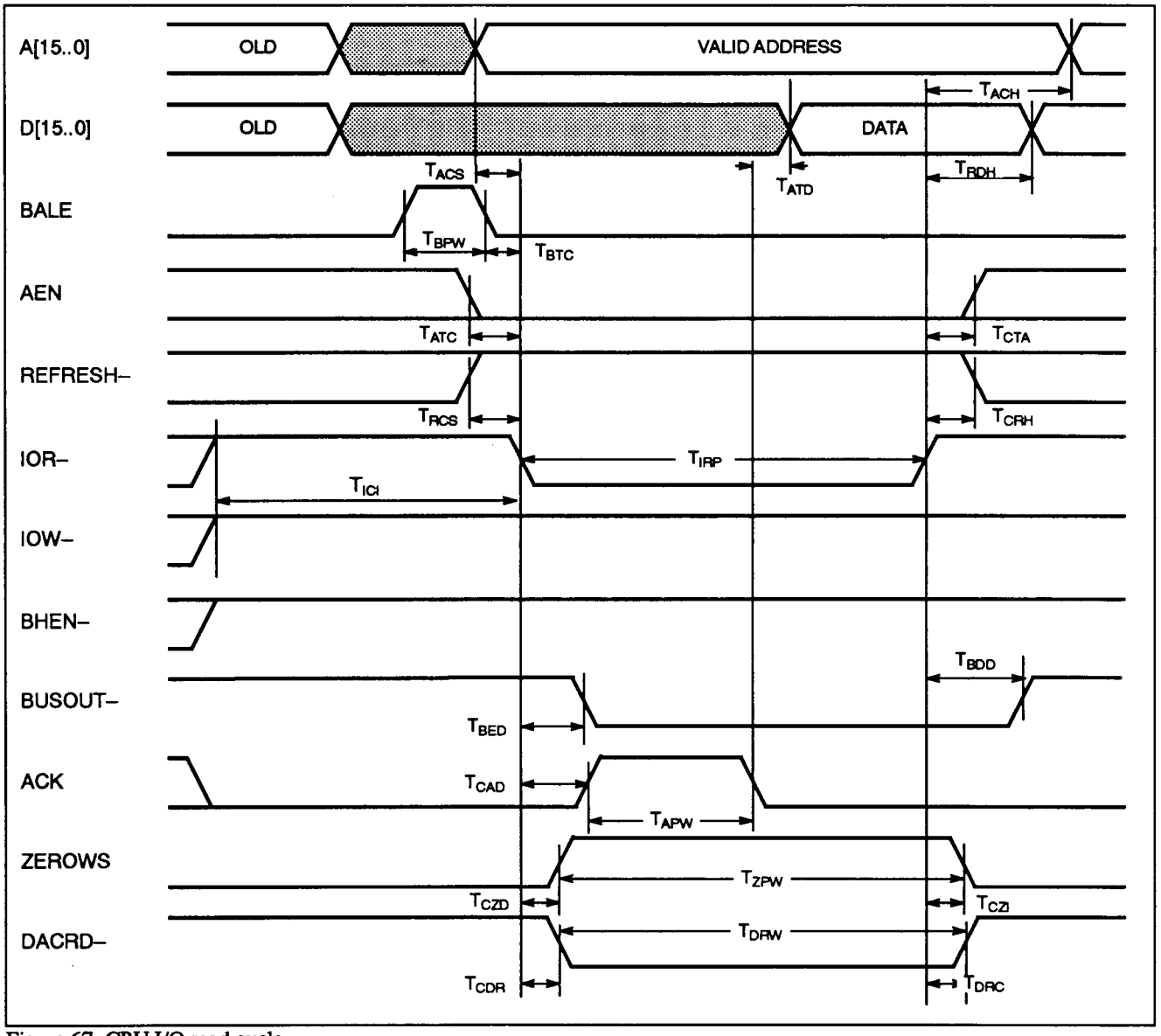


Figure 67. CPU I/O read cycle

6.5. Timing Diagrams, continued

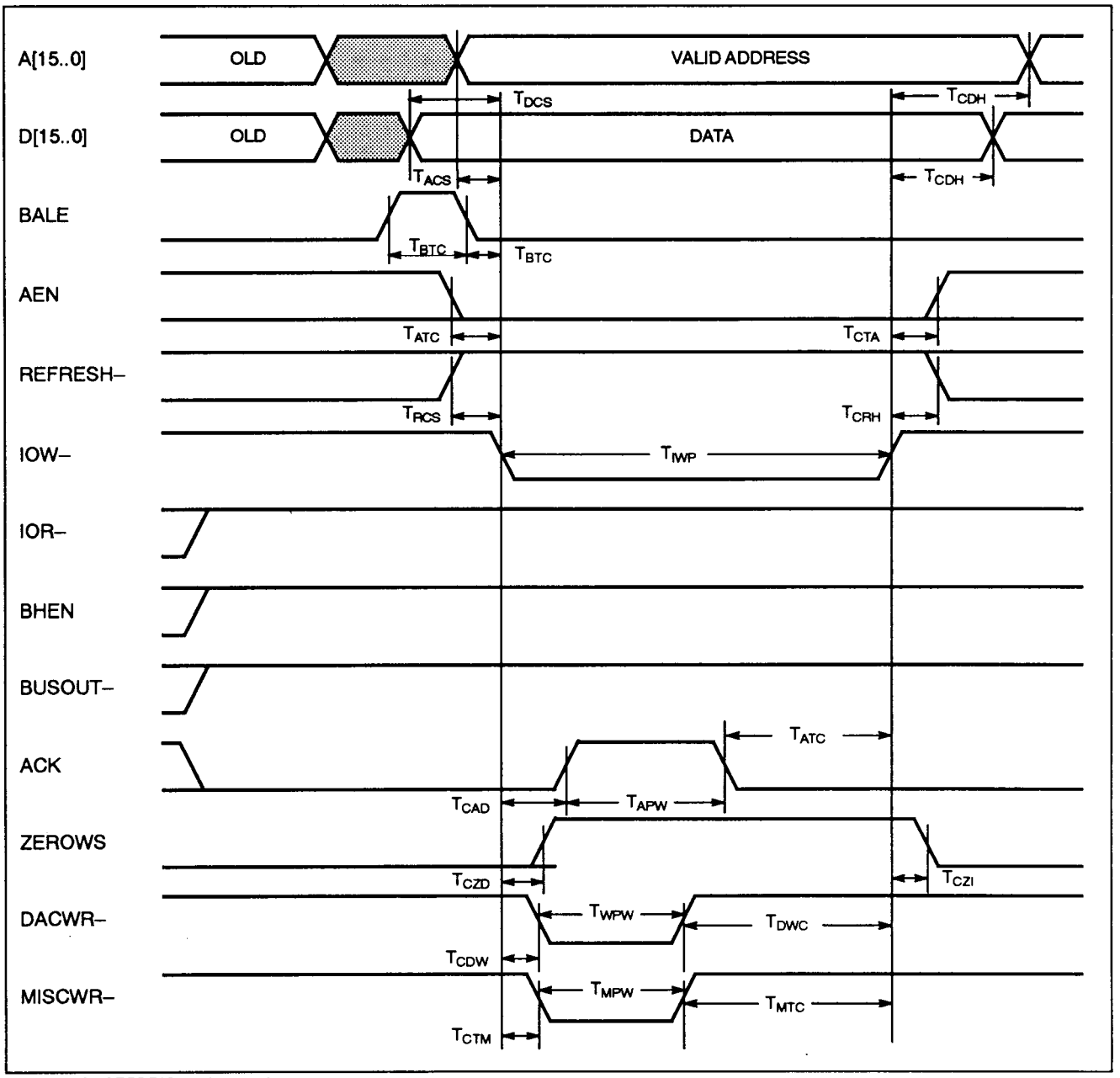


Figure 68. CPU I/O write cycle

6.5. Timing Diagrams, continued

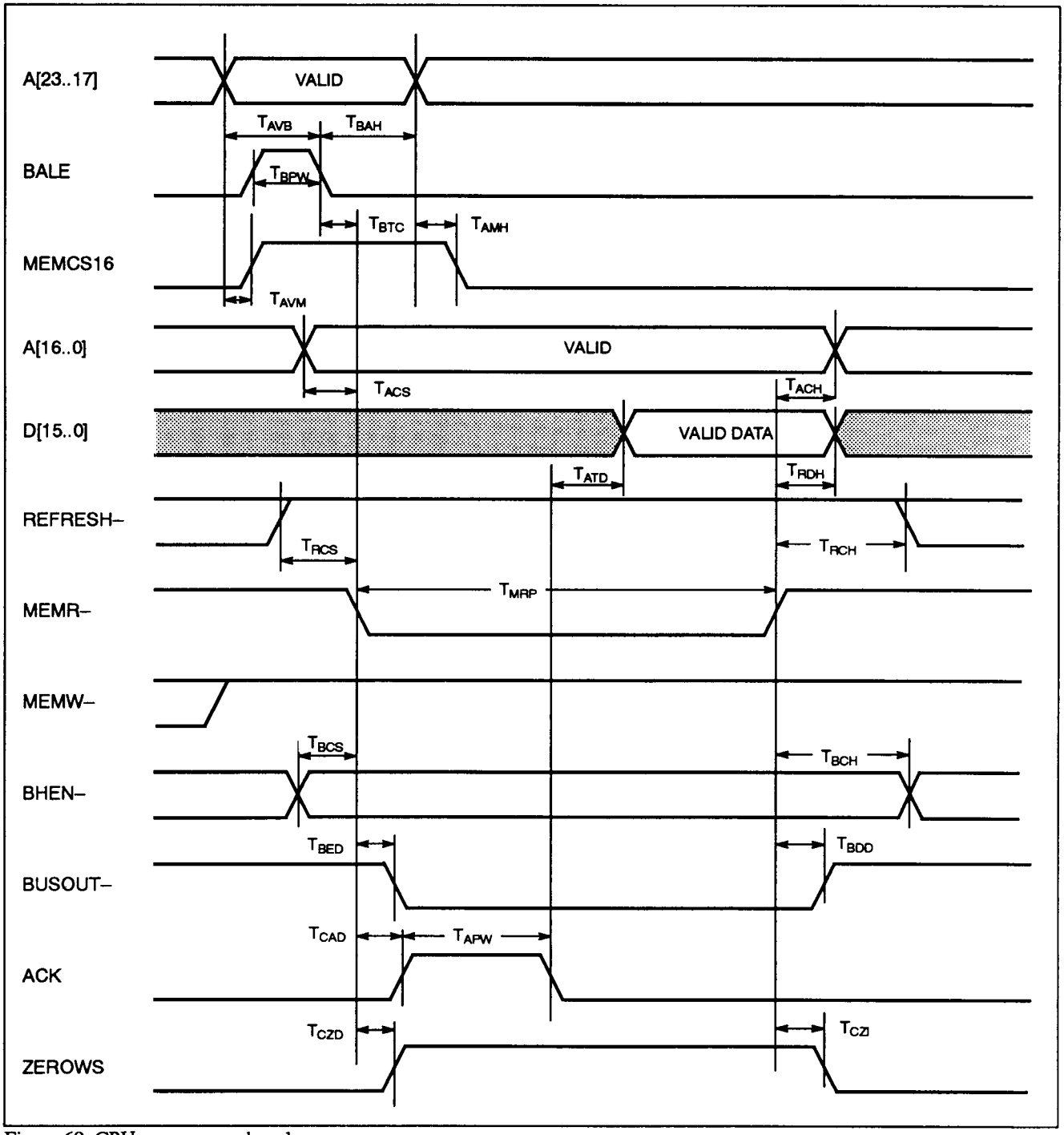


Figure 69. CPU memory read cycle

6.5. Timing Diagrams, continued

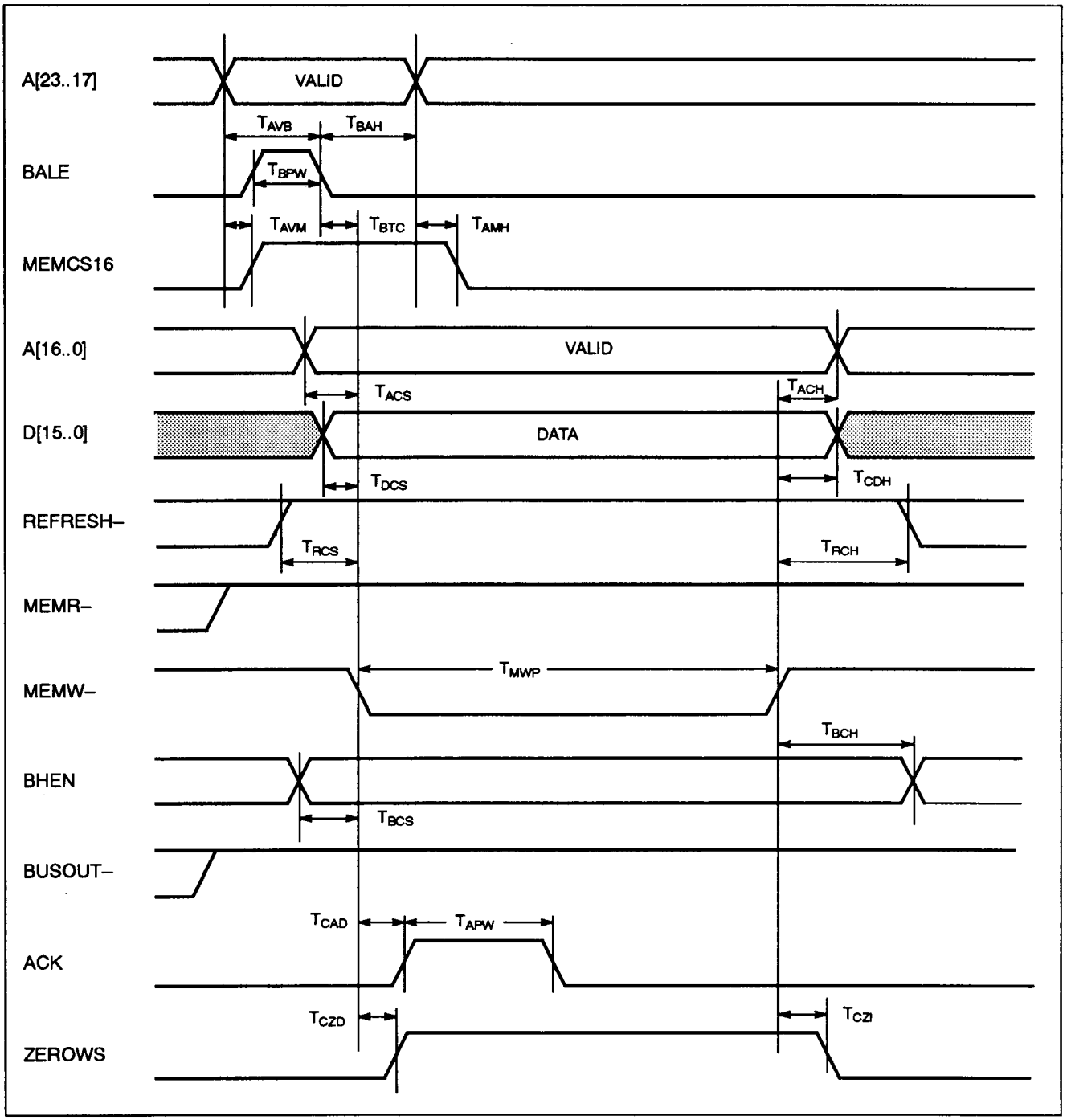


Figure 70. CPU memory write cycle

6.5. Timing Diagrams, continued

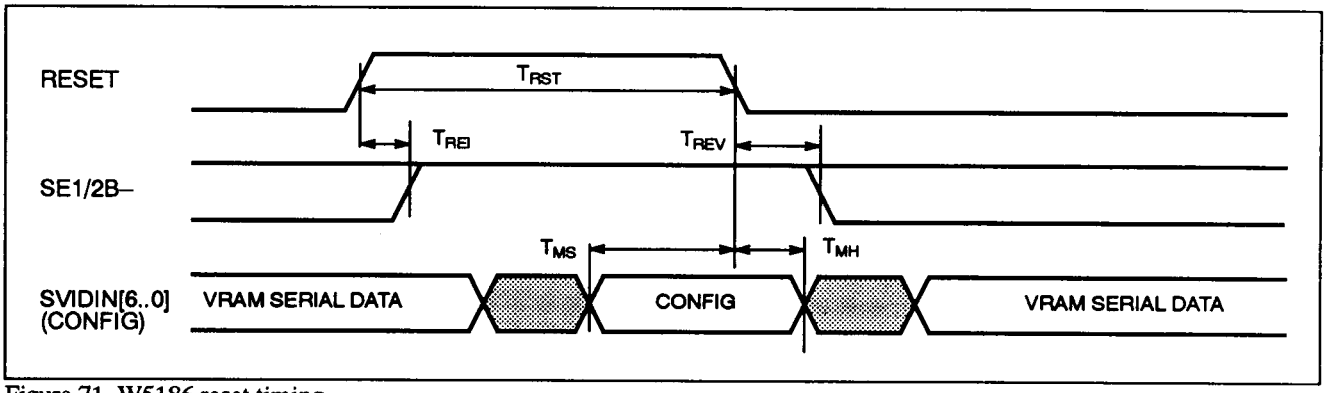


Figure 71. W5186 reset timing

6.5. Timing Diagrams, continued

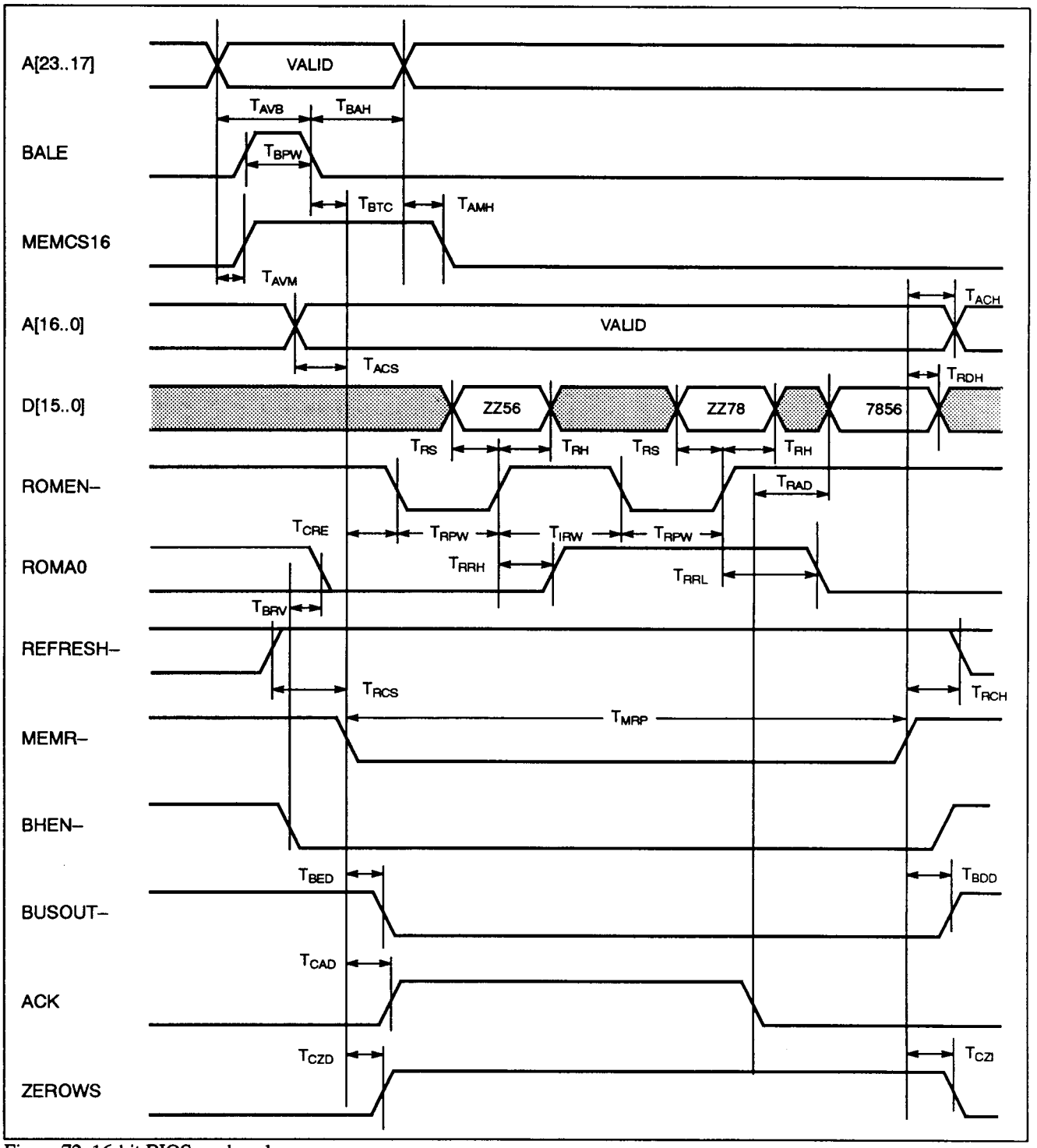


Figure 72. 16-bit BIOS read cycle

6.5. Timing Diagrams, continued

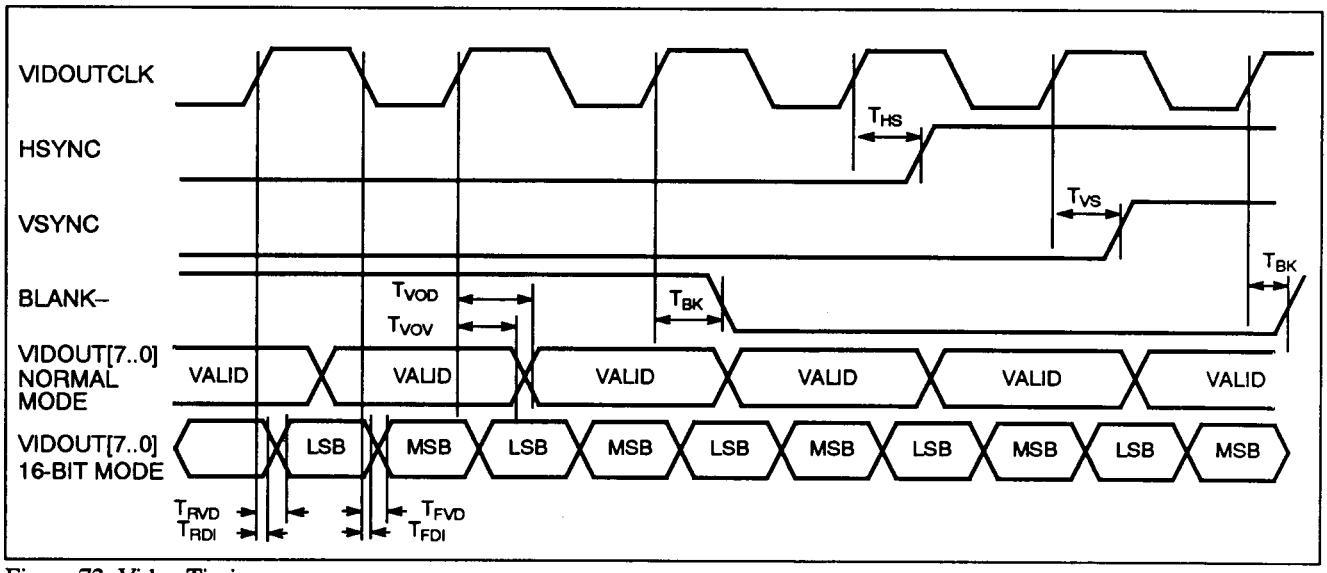


Figure 73. Video Timing

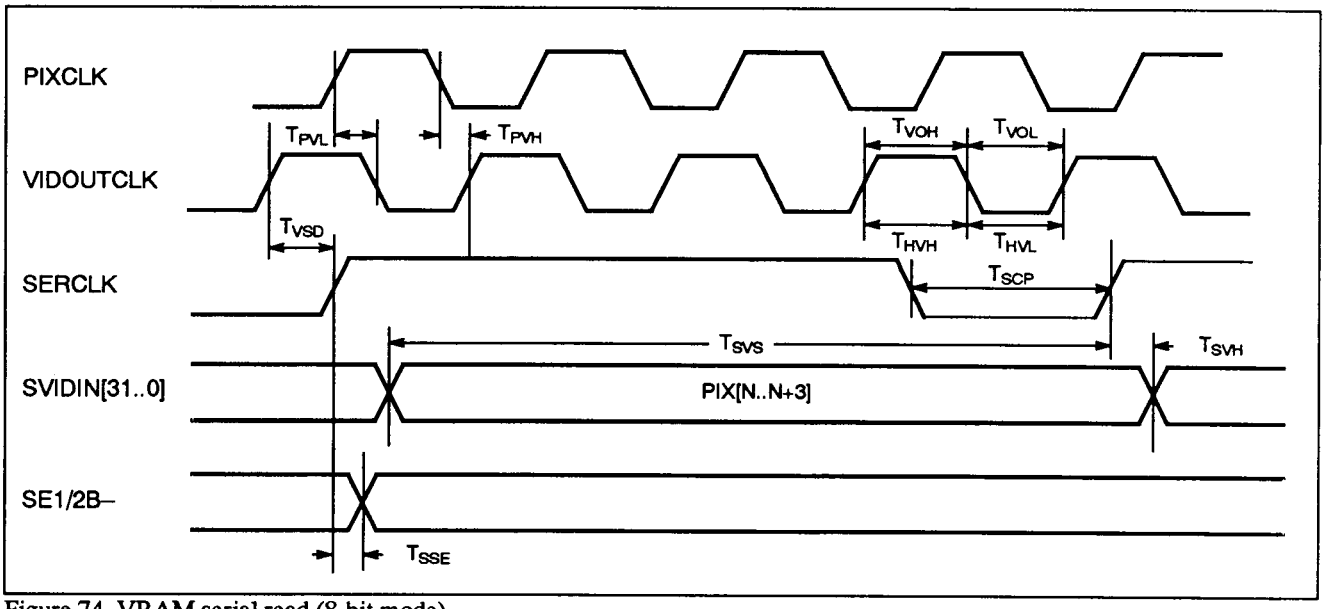


Figure 74. VRAM serial read (8-bit mode)

6.5. Timing Diagrams, continued

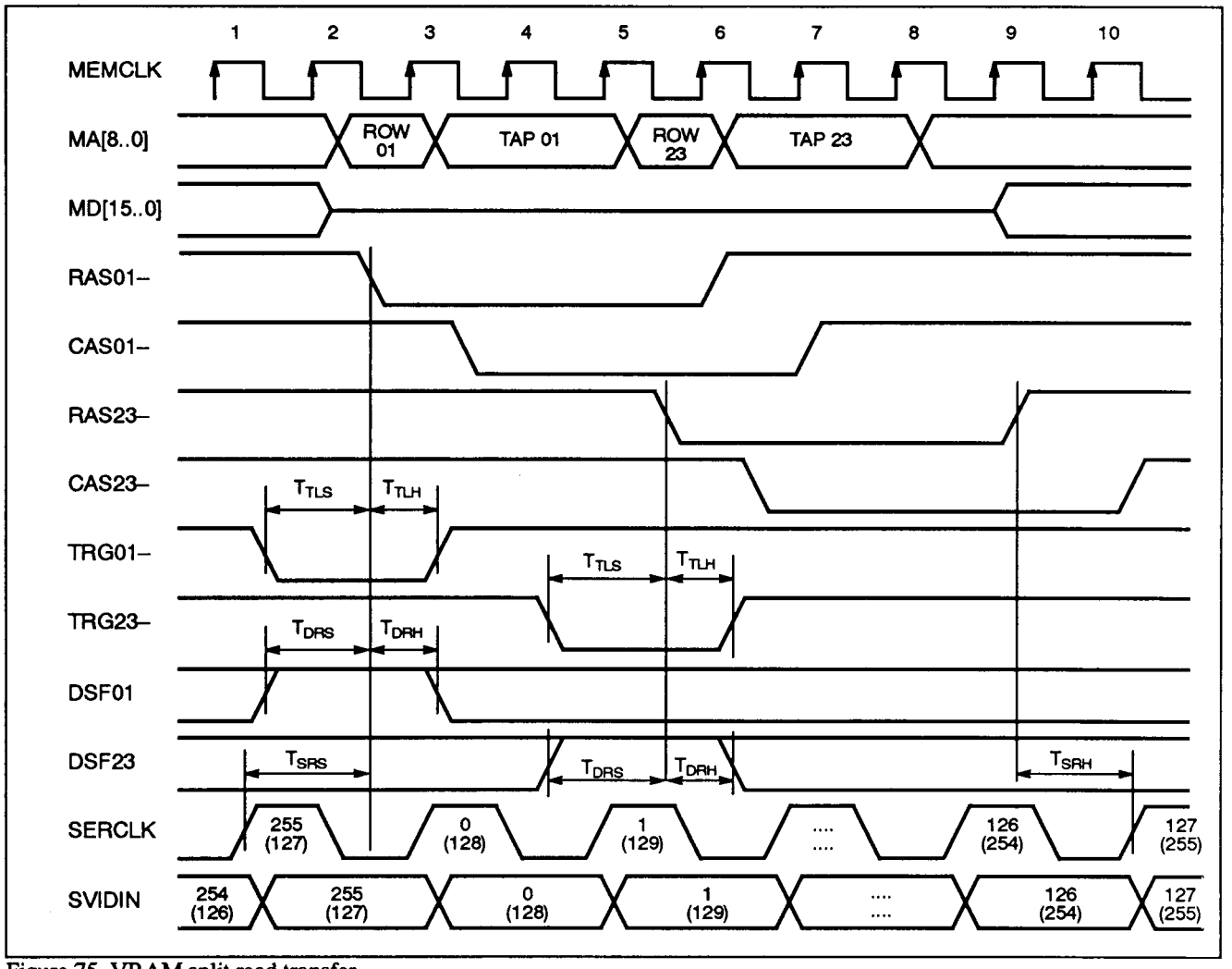


Figure 75. VRAM split read transfer

6.5. Timing Diagrams, continued

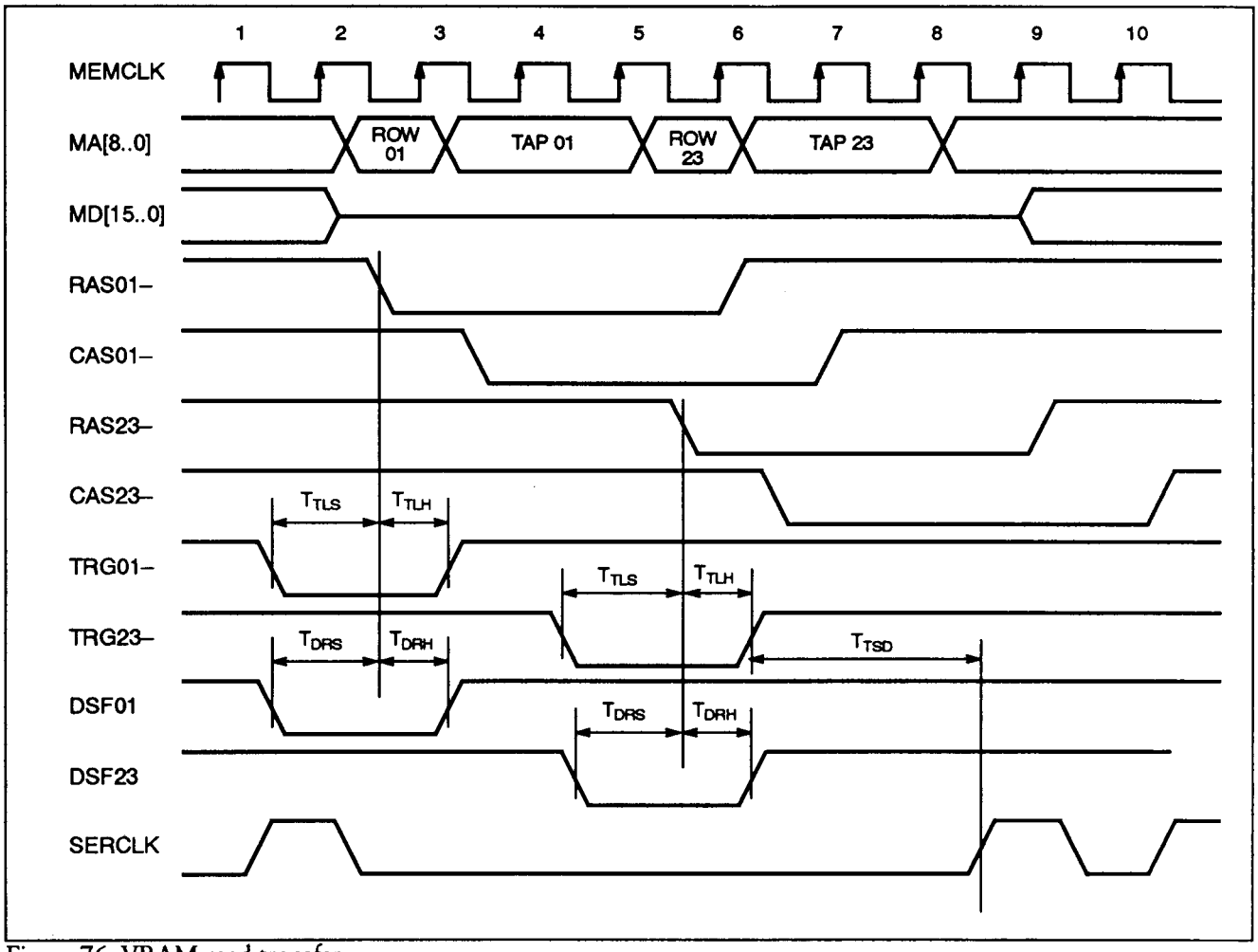


Figure 76. VRAM read transfer

6.5. Timing Diagrams, continued

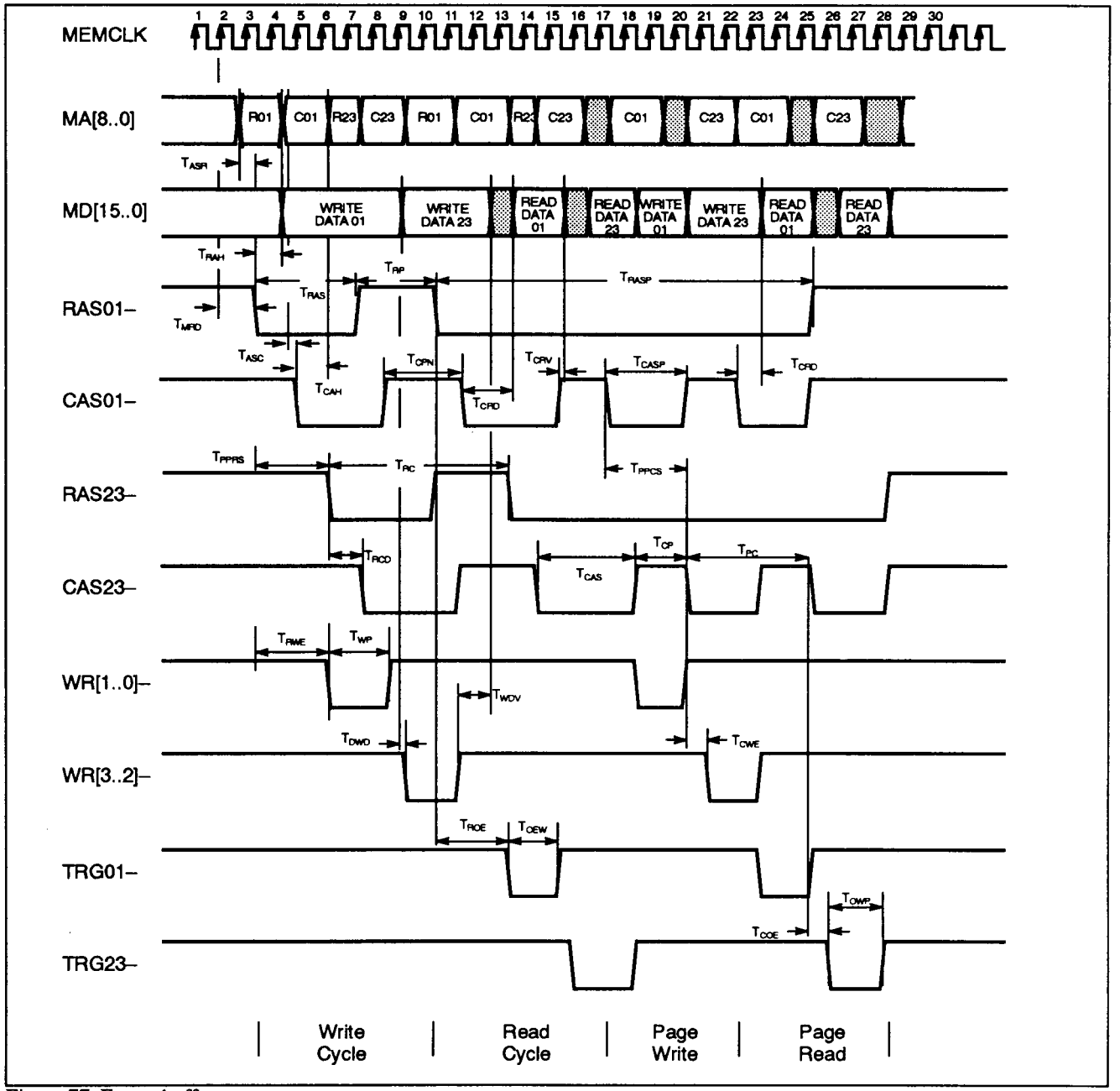


Figure 77. Frame buffer

6.5. Timing Diagrams, continued

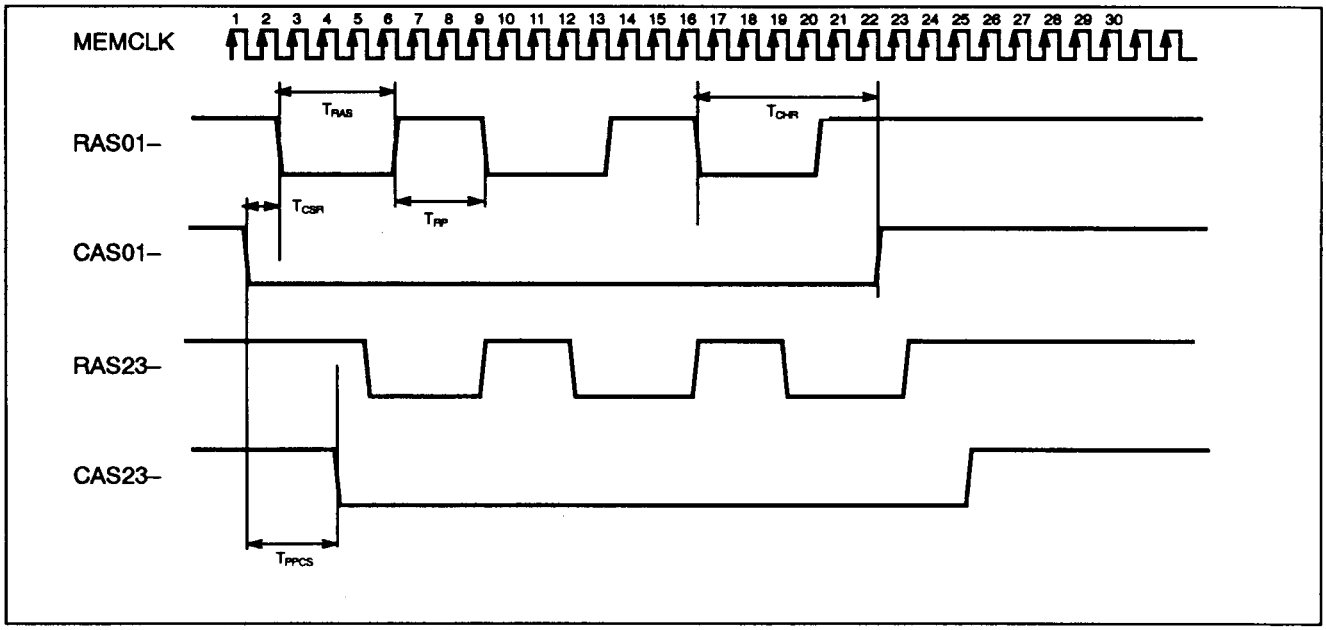


Figure 78. Frame buffer refresh timing (3 RAS cycle)

6.6. Pin Configuration

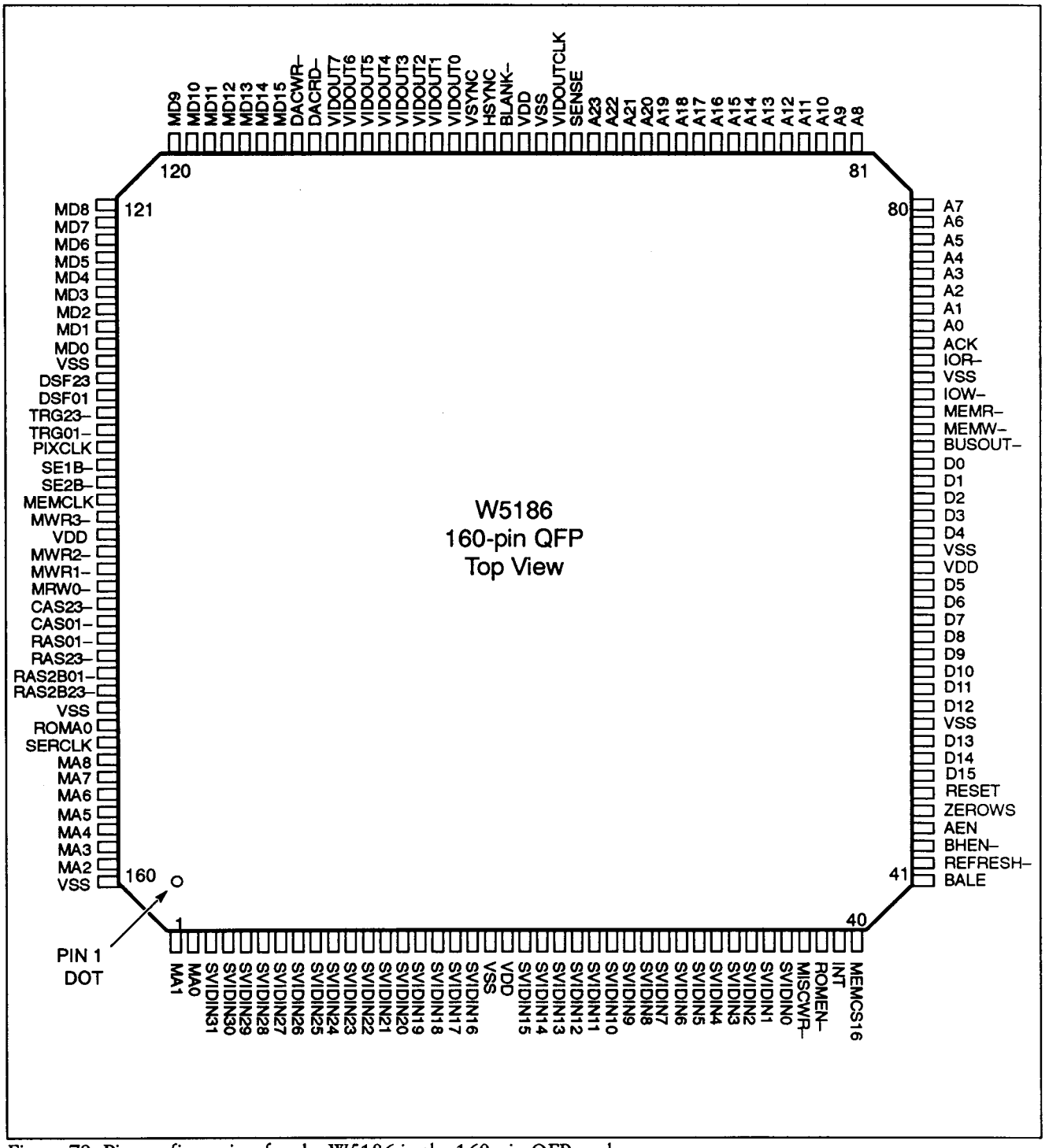
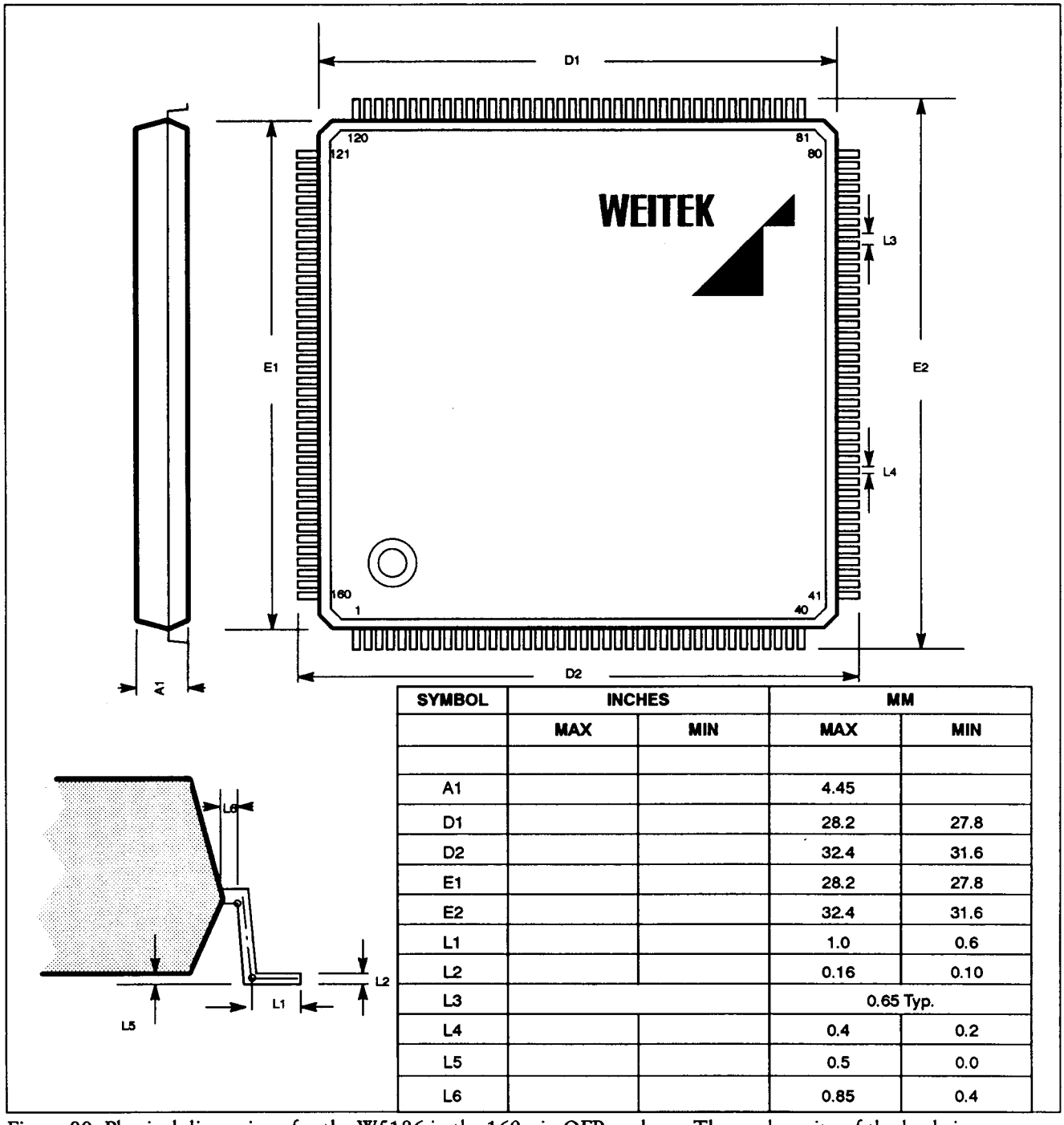


Figure 79. Pin configuration for the W5186 in the 160-pin QFP package.

6.7. Physical Dimensions



SYMBOL	INCHES		MM	
	MAX	MIN	MAX	MIN
A1			4.45	
D1			28.2	27.8
D2			32.4	31.6
E1			28.2	27.8
E2			32.4	31.6
L1			1.0	0.6
L2			0.16	0.10
L3			0.65 Typ.	
L4			0.4	0.2
L5			0.5	0.0
L6			0.85	0.4

Figure 80. Physical dimensions for the W5186 in the 160-pin QFP package. The coplanarity of the leads is 0.15 mm (0.006 in.) maximum

6.8. I/O Characteristics

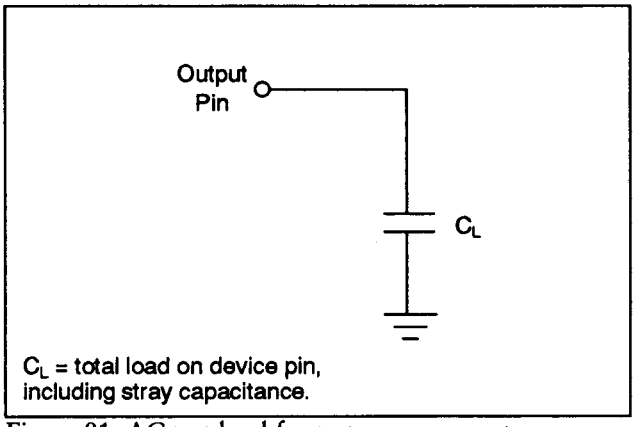


Figure 81. AC test load for test measurement

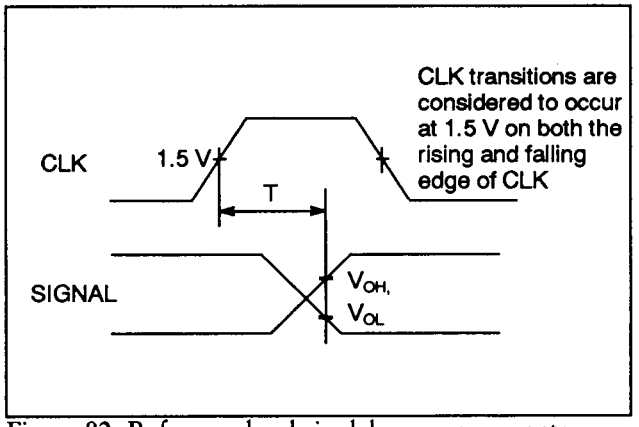


Figure 82. Reference levels in delay measurements

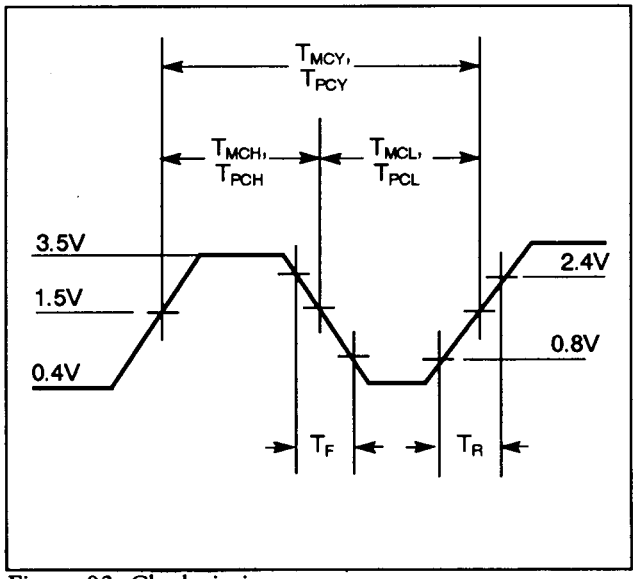


Figure 83. Clock timing

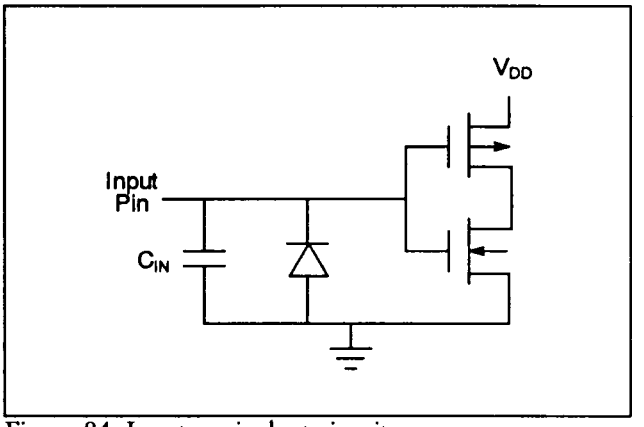


Figure 84. Input equivalent circuits

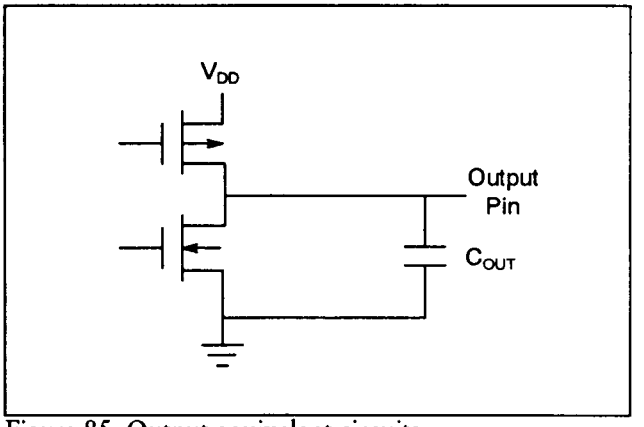


Figure 85. Output equivalent circuits

6.9. Physical Considerations

6.9.1. PC BOARD LAYOUT

Since the W5186 controls DRAMs directly, it is important to pay careful attention to the PC board layout. Power and ground planes are essential for good impedance control, cross-talk reduction, and to reduce ground bounce. It is vital to put the W5186 as close as possible to the memory array to reduce the ringing and undershoot caused by transmission line effects.

Be certain to provide ample capacitive decoupling: since the entire DRAM array is being driven by the W5186, decoupling is especially vital near the processor.

Pay close attention to the length of ISA bus signal traces from the ISA bus connector to the W5186 itself for best system reliability. Signals that should be as short as possible include: MEMR–, MEMW–, IOR– and IOW–.

6.9.2. LOADING AND TERMINATION

The AC specifications listed give the maximum capacitive loading permitted on each of the output and bidirectional signals. Exceeding these will result in additional propagation delay, and may prevent the system from working properly.

The W5186 was designed to drive an unterminated memory array: do not use series damping resistors on the frame buffer memory.

6.10. Related Documents

Programming the GHA. Information on GHA programming.

W5186 BIOS Designer's Guide. Information about creating a custom (non–Phoenix) BIOS.

W5186 Video Performance. Information on determining optimum use of modes and resolutions.

6.11. Ordering Information

Package Type	Speed Grade	Temperature Range (Ambient)	Order Number
160-pin plastic QFP	80 MHz	0-70°C	W5186–80–PFP

Figure 86. Ordering information