PRELIMINARY

W167B

133-MHz Spread Spectrum FTG for Pentium® II Platforms

Features

- **Maximized EMI Suppression using Cypress's Spread Spectrum technology**
- **Three copies of CPU outputs selectable frequency**
- **Three copies of 3V66 selectable frequency output at 3.3V**
- **Ten copies of PCI clocks (selectable frequency), 3.3V**
- **One double strength 14.318-MHz reference output at 3.3V**
- **One copy of 48-MHz USB clock**
- **One copy of selectable 24-/48-MHz for SIO**
- **One copy of CPU-divide-by-2 output as reference input to Direct Rambus™ Clock Generator (Cypress W134)**
- **Three copies of IOAPIC**
- **Available in 48-pin SSOP (300 mils)**

Key Specifications

Supply Voltages: ..... V_{DDQ2} = 2.5V±5%
V_{DDQ3} = 3.3V±5%

CPU, CPUdiv2 Output Jitter:..... 250 ps

CPU, CPUdiv2 Output Skew:..... 175 ps

IOAPIC, 3V66 Output Skew:..... 250 ps

PCI0:8 Pin to Pin Skew:..... 500 ps

Duty Cycle:..... 45/55%

Spread Spectrum Modulation:..... ±0.25%

CPU to 3V66 Output Offset:..... 0.0–1.5 ns (CPU leads)

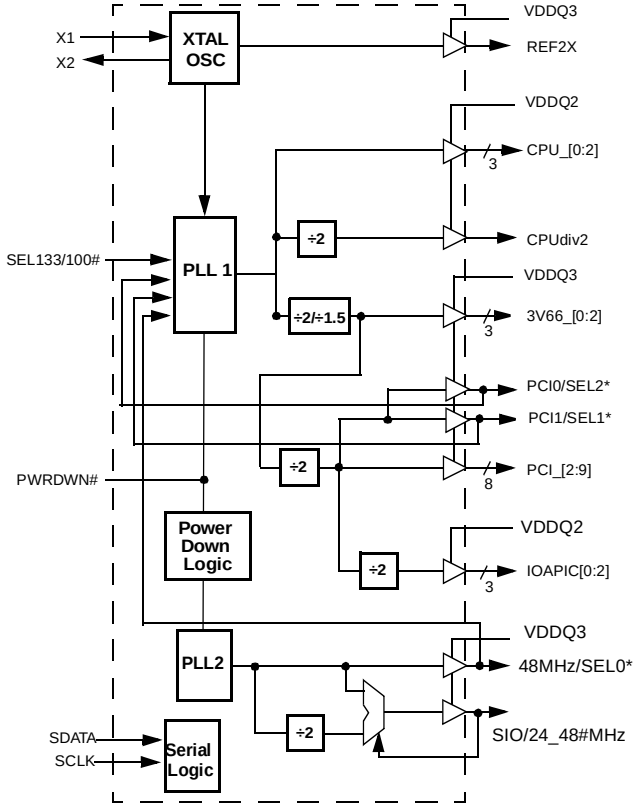
3V66 to PCI Output Offset:..... 1.5–4.0 ns (3V66 leads)

CPU to IOAPIC Output Offset: ..... 1.5–4.0 ns (CPU leads)

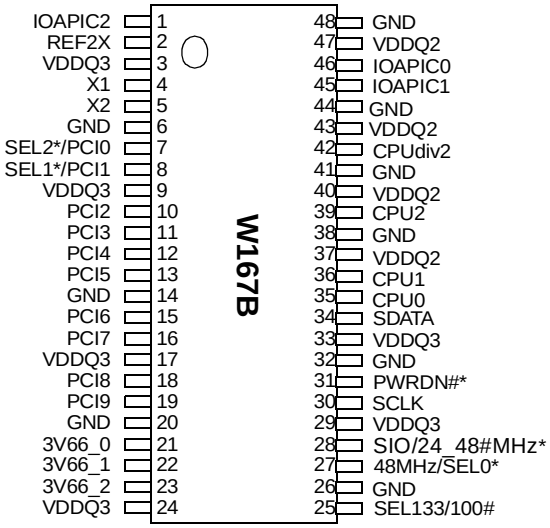
Table 1. Pin Selectable Frequency

SEL133/ 100#	SEL2	SEL1	SEL0	CPU MHz	3V66 MHz	PCI MHz	IOAPIC MHz
1	1	1	1	133.3	66.7	33.3	16.7
1	1	1	0	138	69	34.5	17.3
1	1	0	1	143	71.5	35.8	17.9
1	1	0	0	148	74	37	18.5
1	0	1	1	150	75	37.5	18.8
1	0	1	0	152.5	76.3	38.1	19.1
1	0	0	1	155	77.5	38.8	19.4
1	0	0	0	160	80	40	20
0	1	1	1	100.2	66.8	33.4	16.7
0	1	1	0	105	70	35	17.5
0	1	0	1	114	76	38	19
0	1	0	0	120	80	40	20
0	0	1	1	66.8	66.8	33.4	16.7
0	0	1	0	124	82.7	41.3	20.7
0	0	0	1	128.5	64.3	32.1	16.1
0	0	0	0	133.9	67	33.5	16.7

Block Diagram



Pin Configuration[1]



Note:

1. Internal 250-kΩ pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:2	35, 36, 39	O	***CPU Clock Outputs 0 through 2:*** CPU clock outputs. Their output voltage swing is controlled by voltage applied to VDDQ2.
SEL133/100#	25	I	***SEL133/100#:*** Frequency selection input pin as shown in *Table 1*.
PCI0/SEL2	7	I/O	***PCI Clock Output 0 and Selection Bit 2:*** As an output, this pin works in conjunction with PCI2:9. When an input, this pin functions as part of the frequency selection address (see *Table 1*).
PCI1/SEL1	8	I/O	***PCI Clock Output 1 and Selection Bit 1:*** As an output, this pin works in conjunction with PCI2:9. When an input, this pin functions as part of the frequency selection address (see *Table 1*).
PCI2:9	10, 11, 12, 13, 15, 16, 18, 19	O	***PCI Clock Outputs 2 through 9:*** Output voltage swing is controlled by voltage applied to VDDQ3.
3V66_0:2	21, 22, 23	O	***66-MHz Clock Outputs 0 through 2:*** Output voltage swing is controlled by voltage applied to VDDQ3.
CPUdiv2	42	O	***CPU-Divide-By-2 Output:*** This serves as a reference input signal for Direct Rambus Clock Generator (Cypress W134). The output voltage is determined by VDDQ2.
IOAPIC0:2	46, 45, 1	O	***I/O APIC Clock Output 0 through 2:*** Provide outputs synchronous to CPU clock. See *Table 1* and *Table 5* for their relation to other system clock outputs.
48MHZ/SEL0	27	I/O	***48-MHz Output and Selection Bit 0:*** Fixed clock output that defaults to 48-MHz following device power-up. When an input, this pin functions as part of the frequency selection address (see *Table 1*).
SIO/24_48#MHz	28	I/O	***Super I/O Reference Clock Output and SIO Clock Frequency Select:*** Fixed clock output that provides the reference input clock to a Super I/O device. The output frequency is determined by the input value on this pin during power up. If input is sampled HIGH, the output operates at 24 MHz, otherwise, the output operates at 48 MHz.
REF2X	2	O	***Fixed 14.318-MHz Output:*** With double strength driving capability.
PWRDWN#	31	I	***Power Down Control***
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
SDATA	34	I/O	***Serial Data Input:*** Data input for Serial Data Interface. Refer to Serial Data Interface section that follows.
SCLK	30	I	***Serial Clock Input:*** Clock input for Serial Data Interface. Refer to Serial Data Interface section that follows.
VDDQ2	37, 40, 43, 47	P	***Power Connection:*** Connected to 2.5V power supply.
VDDQ3	3, 9, 17, 24, 29, 33	P	***Power Connection:*** Connected to 3.3V supply.
GND	6, 14, 20, 26, 32, 38, 41, 44, 48	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Overview

The W167B, a motherboard clock synthesizer, provides 2.5V CPU clock outputs for advanced CPU and a CPU-divide-by-2 reference frequency for Direct Rambus Clock Generator (such as Cypress W134) interface. Fixed output frequencies are provided for other system functions.

I/O Pin Operation

Pins 7, 8, 27, and 28 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of these pins is latched and the pins then become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-kΩ "strapping" resistor is connected between each I/O pin and ground or V_{DD3}. Connection to ground sets a latch to "0", connection to V_{DD3} sets a latch to "1". *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connection.

Upon W167B power up, the first 2 ms of operation is used for input logic selection. During this period, these dual-purpose I/O pins are three-stated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic 0 or 1 condition of each I/O pin is then latched. Next, the output buffers are enabled, converting the I/O pins into operating clock outputs. The 2-ms timer starts when V_{DD} reaches 2.0V. The input bits can only be reset by turning V_{DD} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of the clock outputs is <40Ω (nominal) which is minimally affected by the 10-kΩ strap to ground or V_{DD}. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, target (normal) output frequency is delivered assuming that V_{DD} has stabilized. If V_{DD} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DD} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

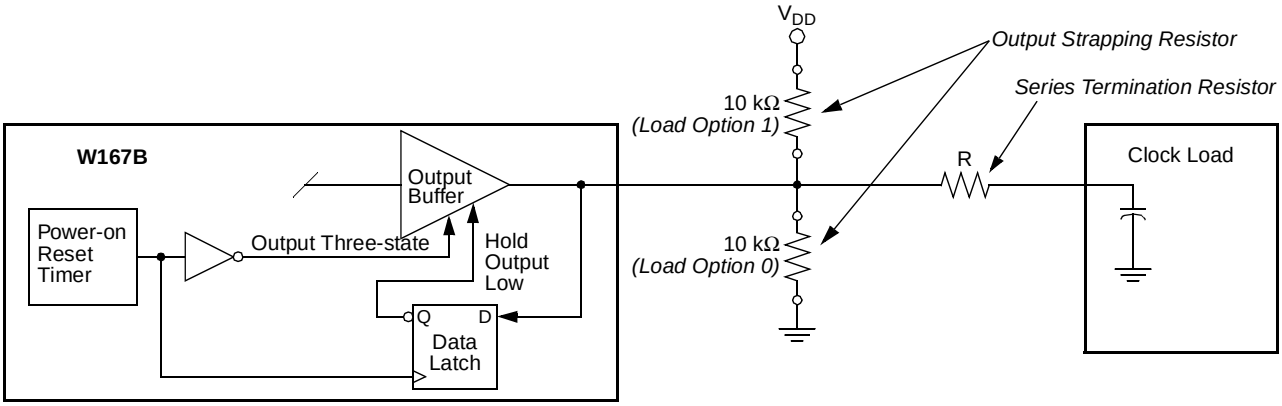


Figure 1. Input Logic Selection Through Resistor Load Option

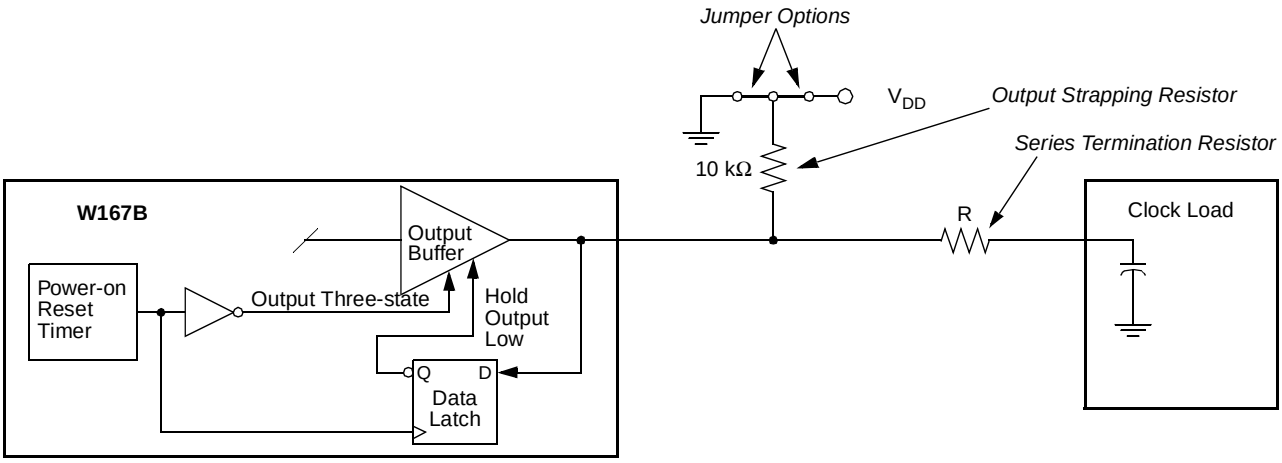


Figure 2. Input Logic Selection Through Jumper Option

CPU/PCI Frequency Selection

CPU frequency is selected with I/O pins 7, 8, 27, (SEL2/PCI0, SEL1/PCI1, 48MHz/SEL0, respectively) and input pin 25 (SEL133/100#). Refer to *Table 1* for CPU/PCI frequency programming information. Additional frequency selections are available through the serial data interface. Refer to *Table 5* on page 9.

Output Buffer Configuration

Clock Outputs

All clock outputs are designed to drive serial terminated clock lines. The W167B outputs are CMOS-type which provide rail-to-rail output swing.

Crystal Oscillator

The W167B requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W167B incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 18 pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 18 pF should be used. This will typically yield reference frequency accuracies within ±100 ppm.

Spread Spectrum Feature

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is –0.5% downspread. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

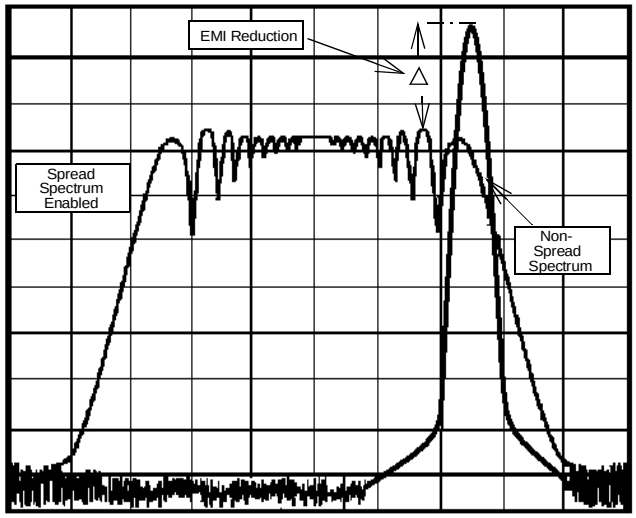


Figure 3. Typical Clock and SSFTG Comparison

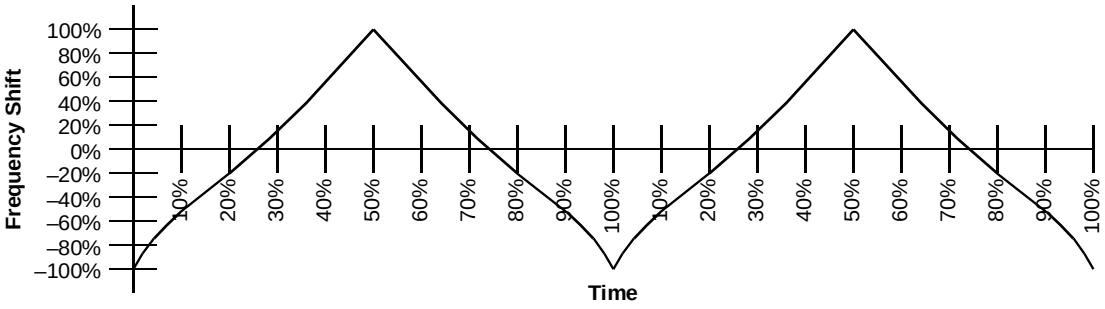


Figure 4. Typical Modulation Profile

Serial Data Interface

The W167B features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W167B initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high-impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to *Table 4*.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

Data is written to the W167B in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W167B to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W167B is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W167B, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W167B, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 4*	The data bits in these bytes set internal W167B registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 0–6. *Table 5* details additional frequency selections that are available through the serial data interface. *Table 6* details the select functions for Byte 0, bits 1 and 0.

Table 4. Data Bytes 0–6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	SEL133/100#	Refer to *Table 5*		0
6	--	--	SEL2	Refer to *Table 5*		0
5	--	--	SEL1	Refer to *Table 5*		0
4	--	--	SEL0	Refer to *Table 5*		0
3	--	--	Frequency Table Selection	Controlled by external pin (per *Table 1*)	Controlled by BYTE0 (per *Table 5*)	0
2	--	--	(Reserved)	--	--	0
1 - 0	--	--	Functional control	Refer to *Table 6*		00
Data Byte 1						
7	27	48MHz	Clock Output Disable	Low	Active	1
6	28	24/48MHz	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	42	CPUdiv2	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	39	CPU2	Clock Output Disable	Low	Active	1
1	36	CPU1	Clock Output Disable	Low	Active	1
0	35	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	16	PCI7	Clock Output Disable	Low	Active	1
6	15	PCI6	Clock Output Disable	Low	Active	1
5	13	PCI5	Clock Output Disable	Low	Active	1
4	12	PCI4	Clock Output Disable	Low	Active	1
3	11	PCI3	Clock Output Disable	Low	Active	1
2	10	PCI2	Clock Output Disable	Low	Active	1
1	8	PCI1	Clock Output Disable	Low	Active	1
0	7	PCI0	Clock Output Disable	Low	Active	1
Data Byte 3						
7	--	--	(Reserved)	--	--	0
6	23	3V66_2	Clock Output Disable	Low	Active	1
5	22	3V66_1	Clock Output Disable	Low	Active	1
4	21	3V66_0	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	19	PCI9	Clock Output Disable	Low	Active	1
0	18	PCI8	Clock Output Disable	Low	Active	1

Table 4. Data Bytes 0–6 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	1	IOAPIC2	Clock Output Disable	Low	Active	1
5	45	IOAPIC1	Clock Output Disable	Low	Active	1
4	46	IOAPIC0	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	2	REF2X	Clock Output Disable	Low	Active	1
Data Byte 5						
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
Data Byte 6						
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0
--	--	--	(Reserved)	--	--	0

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

SEL133/100#	SEL2	SEL1	SEL0	CPU MHz	3V66 MHz	PCI MHz	IOAPIC MHz
1	1	1	1	133.3	66.7	33.3	16.7
1	1	1	0	138	69	34.5	17.3
1	1	0	1	143	71.5	35.8	17.9
1	1	0	0	148	74	37	18.5
1	0	1	1	150	75	37.5	18.8
1	0	1	0	152.5	76.3	38.1	19.1
1	0	0	1	155	77.5	38.8	19.4
1	0	0	0	160	80	40	20
0	1	1	1	100.2	66.8	33.4	16.7
0	1	1	0	105	70	35	17.5
0	1	0	1	114	76	38	19
0	1	0	0	120	80	40	20
0	0	1	1	66.8	66.8	33.4	16.7
0	0	1	0	124	82.7	41.3	20.7
0	0	0	1	128.5	64.3	32.1	16.1
0	0	0	0	133.9	67	33.5	16.7

Table 6. Select Function for Data Byte 0, Bits 0:1

	Input Conditions		Output Conditions				
	Data Byte 0						
Function	Bit 1	Bit 0	CPU0:2,	PCI0:9	REF2X	IOAPIC0:2	48/24MHZ
Normal Operation	0	0	Note 2	Note 2	14.318 MHz	Note 2	48/24 MHz
Test Mode	0	1	TBD	TBD	TBD	TBD	TBD
Spread Spectrum	1	0	±0.25%	±0.25%	14.318 MHz	±0.25%	48/24 MHz
Three-state	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note:
2. CPU, IOAPIC, and PCI frequency selections are listed in *Table 1* and *Table 5*.

How To Use the Serial Data Interface

Electrical Requirements

Figure 5 illustrates electrical characteristics for the serial interface bus used with the W167B. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistors on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W167B is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

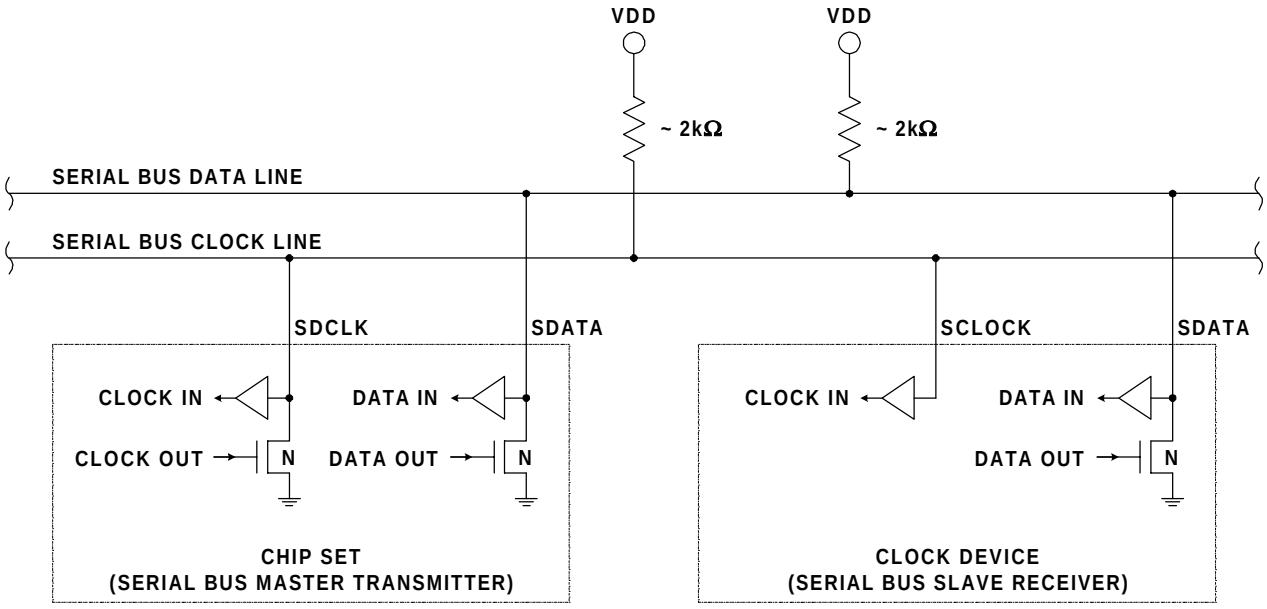


Figure 5. Serial Interface Bus Electrical Characteristics

Signaling Requirements

As shown in *Figure 6*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 7*. A “stop bit” signifies that a transmission has ended.

As stated previously, the W167B sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 8*.

Sending Data to the W167B

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).

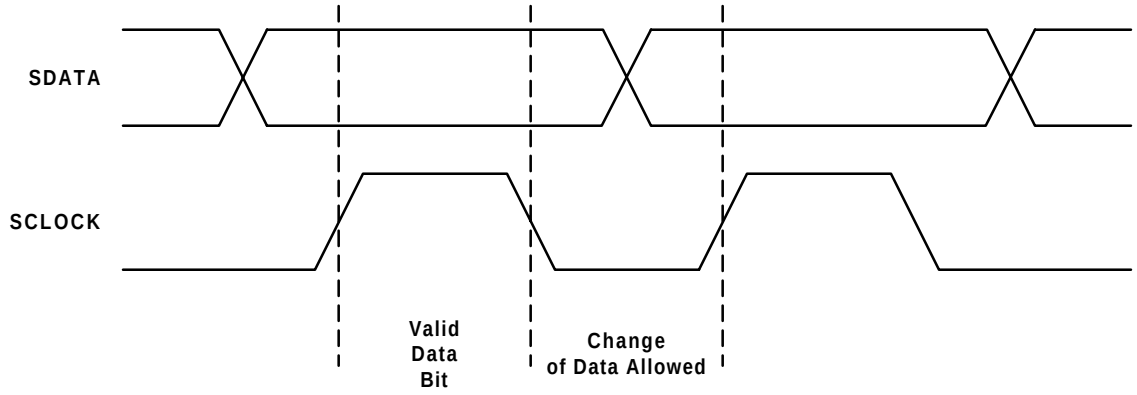


Figure 6. Serial Data Bus Valid Data Bit

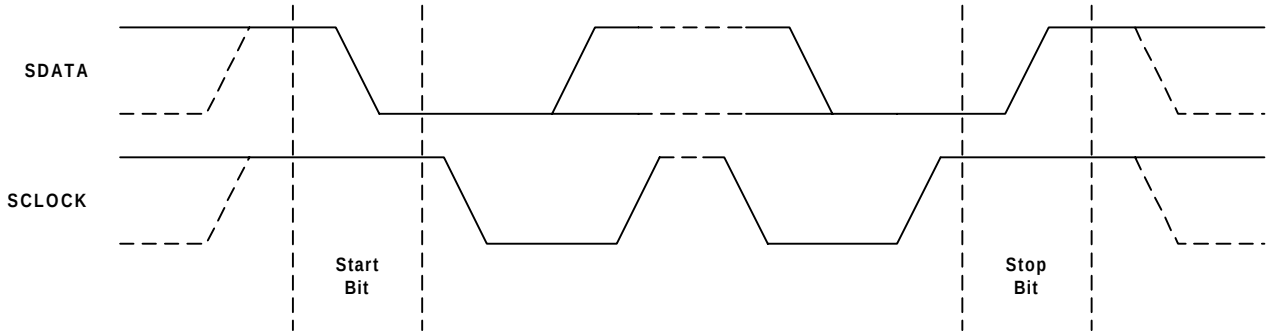


Figure 7. Serial Data Bus Start and Stop Bit

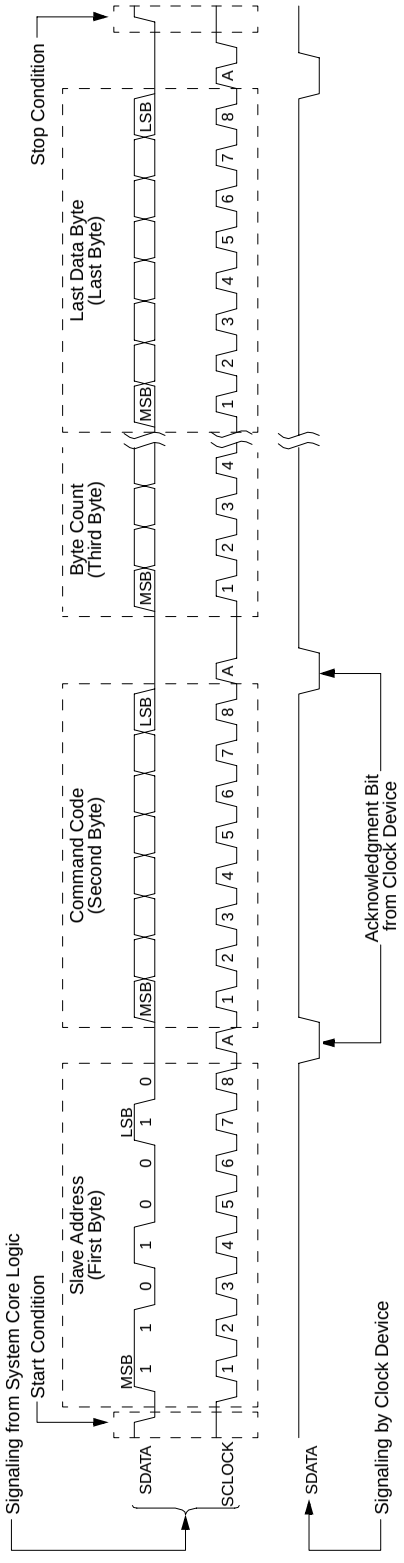


Figure 8. Serial Data Bus Write Sequence

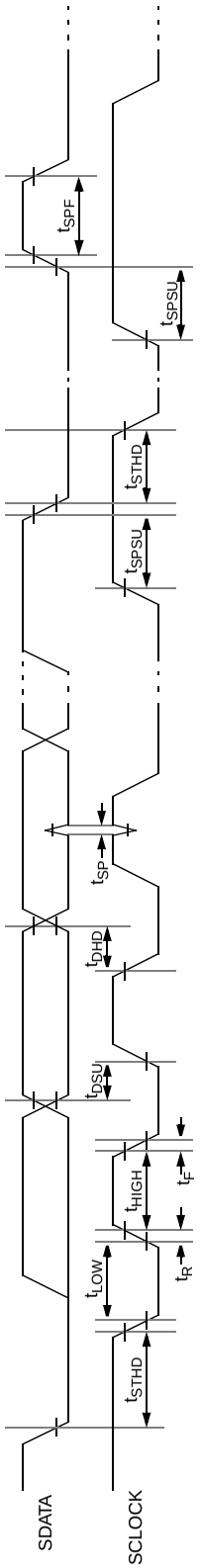


Figure 9. Serial Data Bus Timing Diagram

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Supply Current						
$I_{DD-3.3V}$	Combined 3.3V Supply Current	CPU0:3 =133 MHz[3]			160	mA
$I_{DD-2.5}$	Combined 2.5V Supply Current	CPU0:3 =133 MHz[3]			90	mA
Logic Inputs (All referenced to V_{DDQ3} = 3.3V)						
V_{IL}	Input Low Voltage		GND – 0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[4]				–25	µA
I_{IH}	Input High Current[4]				10	µA
I_{IL}	Input Low Current, SEL133/100#[4]				–5	µA
I_{IH}	Input High Current, SEL133/100#[4]				5	µA
Clock Outputs						
CPU, CPUdiv2, IOAPIC (Referenced to V_{DDQ2})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	V_{OL} = 1.25V	45	65	100	mA
I_{OH}	Output High Current	V_{OH} = 1.25V	45	65	100	mA
48MHz, REF (Referenced to V_{DDQ3})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	45	65	100	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	45	65	100	mA
PCI, 3V66 (Referenced to V_{DDQ3})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	70	100	145	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	65	95	135	mA

Notes:

3. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
4. W167B logic inputs have internal pull-up devices, except SEL133/100# (pull-ups not CMOS level).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[5]			1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[6]			18		pF
$C_{IN,X1}$	X1 Input Capacitance[7]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

3.3V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%,V_{DDQ2} = 2.5V± 5% f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[8]

3V66 Clock Outputs, 3V66_0:2 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency	Note 9		66.6		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

Notes:
5. X1 input threshold voltage (typical) is VDD/2.
6. The W167B contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
7. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
8. Period, jitter, offset, and skew measured on rising edge at 1.5V.
9. 3V66 is CPU/2 for CPU =133 MHz and (2 x CPU)/3 for CPU = 100 MHz.

PCI Clock Outputs, PCI0:9 (Lump Capacitance Test Load = 30 pF

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
t_P	Period	Measured on rising edge at 1.5V[10]	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	3V66 to PCI Clock Skew	Covers all 3V66/PCI outputs. Measured on rising edge at 1.5V. 3V66 leads PCI output.	1.5		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF Clock Outputs, REF0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

48-MHZ Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

Note:

10. PCI clock is CPU/4 for CPU = 133 MHz and CPU/3 for CPU = 100 MHz.

2.5V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2}= 2.5V±5%
f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[11]

CPU Clock Outputs, CPU0:2 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 133 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	7.5		7.65	10		10.2	ns
t_H	High Time	Duration of clock cycle above 2.0V	1.87			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	1.67			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

CPUdiv2 Clock Outputs, CPUdiv2 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 133 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.3	20		20.4	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.25			7.5			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.05			7.3			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

Note:
11. Period, Jitter, offset, and skew measured on rising edge at 1.25V.

IOAPIC Clock Output, IOAPIC (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min	Typ	Max	Unit
f	Frequency	Note 12		16.67		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

Note:

12. IOAPIC clock is CPU/8 for CPU = 133 MHz and CPU/6 for CPU = 100 MHz.

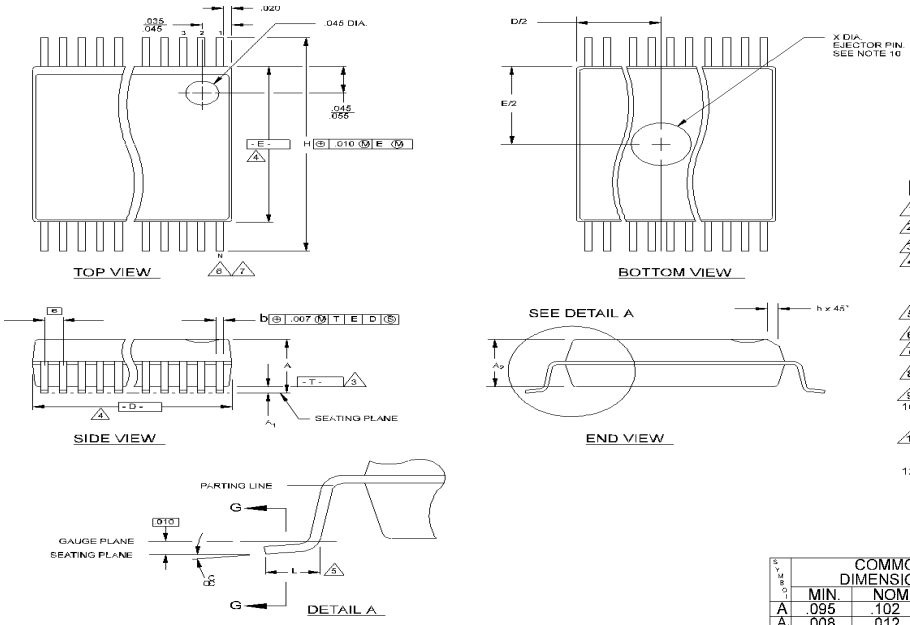
Ordering Information

Ordering Code	Package Name	Package Type
W167B	H	48-pin SSOP (300 mils)

Document #: 38-00816

Package Diagram

48-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			h_n / L	NOTE	4			6
	MIN.	NOM.	MAX.		VARI-ATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

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SYMBOL	COMMON DIMENSIONS			h_n / L	NOTE	4			6
	MIN.	NOM.	MAX.		VARI-ATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

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