VT82C42

KEYBOARD CONTROLLER

Preliminary Release
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VIA TECHNOLOGIES, INC.

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VT82C42 Keyboard Controller

Date : November 22, 1995

1. General Overview:

The VT82C42 is a compatible direct replacement for the Intel 80C42 BIOS version of the Keyboard Controller. The VT82C42 is fully implemented by hardware logic so that it has a very fast response capability for any command issued by the host. In addition to keyboard support, the VT82C42 also offers PS/2 mouse support. The VT82C42 also offers the Mouse Lock™ function (patent pending), a feature exclusively designed by VIA technologies, which locks the mouse when the keylock function is initiated.

2. Features:

- Fully hardware implemented, 0.8μm CMOS Technology.
- Very high speed response of A20 GATE & reset.
- Support PS2 style mouse.
- Compatible with all major BIOS, including AWARD, PHOENIX and AMI.
- 40 pin PDIP and 44 pin PLCC packages.

3. Function Description:

The internal timer counting is based on an 8Mhz clock input from X1, X2 (or X2, with X1 connected to ground). After the deassertion of RESET#, the VT82C42 will drive high at pin P23 and pin P27. After 6 μs (6 x 8 clocks) of driving, the VT82C42 will check on pins T1 & P10; if both pins are low, then the VT82C42 will switch to PS/2 mode. Otherwise, the VT82C42 will remain in AT mode.

If the VT82C42 is in AT mode after the self test, then it will drive P24 and P25 low with all other ports high. If the VT82C42 is in PS/2 mode, then it will drive P24, P25, P22, and P27 low with all other ports high. The VT82C42 will not change its driving value until it receives the command "AA" from the host. When receiving the command "AA" from the host, the VT82C42 will prepare a "55" in its output buffer and drive P24 (reflecting the internal OBF flag) high within 6 clocks. This response time is the typical active time for internal IBF flag. After this initialization procedure, the VT82C42 will drive P26 low (AT mode) or drive P26 and P23 low (PS/2 mode) in order for the keyboard and mouse interface to receive data from keyboard or mouse.

When the keyboard or mouse toggles the interface (KBCLK, KBDATA, MSCLK,MSDATA), the controller receives data from the serial interface and stores the received data into its internal output buffer. If the received data is from the keyboard, a scan code translation is executed before the data is sent to the output buffer. The VT82C42 also raises P24 or P25 to indicate a output buffer full. The host is signaled to issue a read command to the data port to read the received data out. When the VT82C42 receives data in the normal mode (pin 25 on DIP40 or pin 28 on PLCC44 parts connected to VCC) and the status of P17 is low, then the controller will not raise the P24, nor activate its internal OBF flag. It looks like the controller will consume the income data itself. And if the data is from the mouse, the controller will still raise P25 to indicate that data is coming from mouse. However, if the VT82C42 is in Mouse Lock™ mode (pin 25 on DIP40 or pin 28 on PLCC44 parts connected to GND), the data from either keyboard or mouse will be prohibited from sending to the host.

The host can program the output port (P20-P23 in AT mode, or P20-P21 in PS/2 mode) or in-out port (P10-P15 in AT mode, or P12-P15 in PS/2 mode) by issuing a command to the command register on the VT82C42. The controller will then quickly execute the specified command. Note that P16-P17 is implemented as an input port only. The host can also transmit data to the keyboard and mouse by issuing a command to the data register. The data coming to the data register (with A0 = 0, CS# = 0, RD# = 1, and WR# = 0) will be sent to the keyboard via the keyboard serial interfaces. The data sent to the mouse will be completed by 1) issuing a D4 command to the command register, 2) then writing the following data byte to the data register (to be sent to the mouse via mouse serial interface). In either case, the VT82C42 will wait for an acknowledgement from the keyboard or mouse to complete a transmission. At the same time as the completion of the transmission, the VT82C42 will raise P24 or P25 (when sending data to mouse) to signal the host of a completion of transmission. When the controller receives or transmits, the controller does a parity and time-out check. If any error occurs in the interface or inside the external devices (keyboard or mouse), the controller will reflect that error in the following status register.

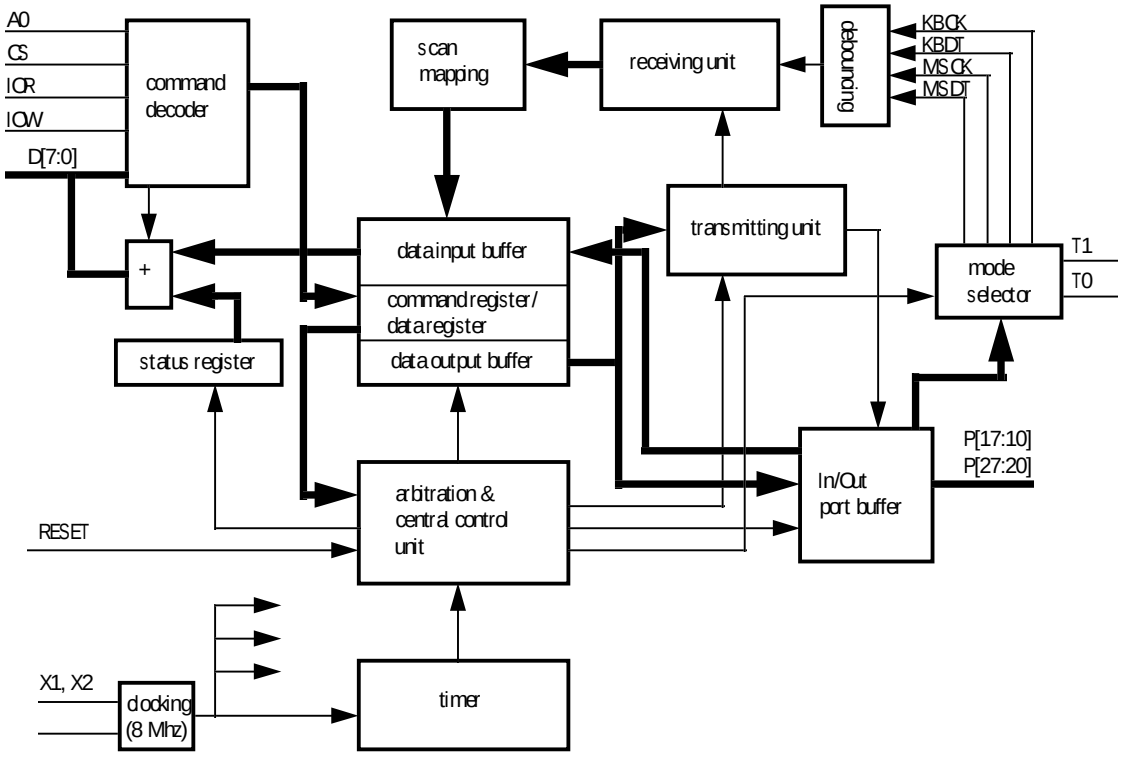


Fig 1. Block Diagram for VT82C42

4. Register

Table 1. Status register: read only (with A0 = 1, CS# = 0, RD# = 0, WR# = 1)

Bit0 : OBF	1 means output buffer is full, 0 means output buffer is empty.
Bit1 : IBF	1 means input buffer is full, 0 means input buffer is empty.
Bit2 : system flag	0 after power on
Bit3 : command/Data	1 means last write is command write. 0 means last write is data write.
Bit4 : keylock status	To represent the inhibition of keyboard. 0 means keyboard is inhibited. 1 means keyboard is not inhibited.
Bit5 : transmit time-out/mouse OBF	Act as transmit time-out on AT mode. 1 means error happens. Act as Mouse OBF on PS2 mode. 1 means mouse output buffer full.
Bit6 : receive time-out/general time-out	Act as receive time-out on AT mode. 1 means error happens. Act as general (receive/transmit) time-out on PS2 mode.
Bit7 : parity error	1 means even parity has occurred in the last transmit/receive.

Table 2. Command register: read/write (use command 20h/60h)

Bit0 : OBF enable	1 means controller will generate high (interrupt) on P24 when output buffer has been written.
Bit1 : mouse OBF enable	1 means controller will generate high (interrupt) on P25 when mouse data comes in output buffer.
Bit2 : system flag	Connect to the status register Bit2.
Bit3 : inhibit override	Write a '1' to this Bit will disable the keyboard inhibit function.
Bit4 : prohibit enabling of keyboard interface	Write a '1' to this Bit will disable keyboard interface
Bit5 : IBM PC keyboard type protocol/disable mouse interface	On AT mode, 0 means that the controller will do a IBM keyboard like checking on receiving. On PS2 mode, a '1' disable the mouse interface
Bit6 : PC compatible mode	Default is 1, means the scan code translation is on.
Bit7 : reserved.	

Table 3. Command List: (with A0 = 1, CS# = 0, RD# = 1, WR# = 0)

20h : read command byte register.	After command execution, OBF = 1 means data is ready on the output buffer.
60h : write command byte register.	Next byte write to Data port will be written to command byte register.
9xh : write low nibble to (Port13-Port10).	
A1h : controller's version number.	After command execution, OBF = 1 means data is ready on the output buffer.
A4h : check password command	Always return 'F1' on output buffer.
A7h : disable mouse interface	After the command execution, Command byte register bit5 = 1 and P23 = 1 on PS2 mode. No effect on AT mode.
A8h : enable mouse interface	After the command execution, Command byte register bit5 = 0 and P23 = 0 on PS2 mode. No effect on AT mode.
A9h : mouse interface test.	Return 00h if the interface is O.K..
AAh : controller's self test	Return 55h if the controller is O.K..
ABh : keyboard interface test.	Return 00h if the interface is O.K..
ADh : disable keyboard interface.	

AEh : enable keyboard interface.	
AFh : return version	

number.	
B0h : write 0 to P10.	
B1h : write 0 to P11.	
B2h : write 0 to P12.	
B3h : write 0 to P13.	
B4h : write 0 to P22.	
B5h : write 0 to P23.	
B6h : write 0 to P14.	
B7h : write 0 to P15.	
B8h : write 1 to P10.	
B9h : write 1 to P11.	
BAh : write 1 to P12.	
BBh : write 1 to P13.	
BCh : write 1 to P22.	
BDh : write 1 to P23.	
BEh : write 1 to P14.	
BFh : write 1 to P15.	
C0h : read controller's input ports P17-P10.	
C1h : poll input port low.	Read from P11,P12,P13 and write to status register bit5,bit6,bit7.
C2h : poll input port high.	Read from P15,P16,P17 and write to status register bit5,bit6,bit7.
C8h : enable D1 command be effective to P22 and P23.	
C9h : disable D1 command be effective to P22 and P23.	
CAh : return on bit0 the mode value.	1 for PS2 mode, 0 for AT mode.
D0h : return the controller's output port P20-P27.	
D1h : write output port.	The next byte written to data port will be put on output port.
D2h : write keyboard output buffer	The next byte written in to data port will be put on the output buffer and OBF = 1.
D3h : write mouse output buffer	The next byte written in to data port will be put on the output buffer and mouse OBF = 1.
D4h : write to mouse	The next byte written in to data port will be transmit to mouse.
E0h : read test inputs.	Return T0 & T1 values on bit0 & bit1 respectively.
Exh : active output ports	P23-P21 will change according to the status on bit3-bit1.
Fxh : pulse output ports	P23-P20 will be pulse low for 6us according to the status on bit3-bit0.

5. Design Example:

1. **To work with AT mode mother board.**

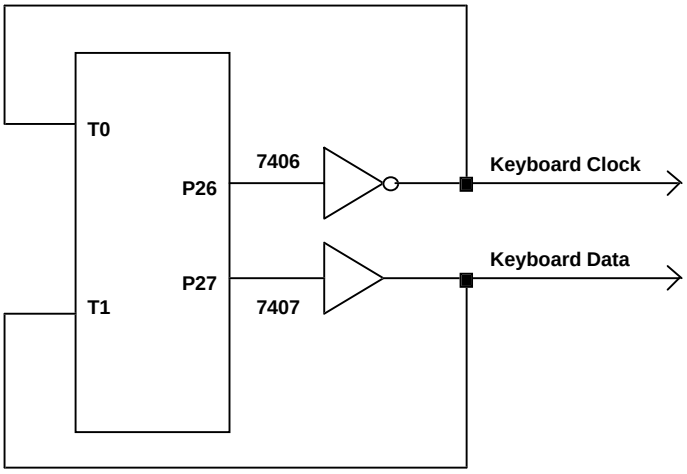


Fig 2.

2. To work with PS2 mode mother board.

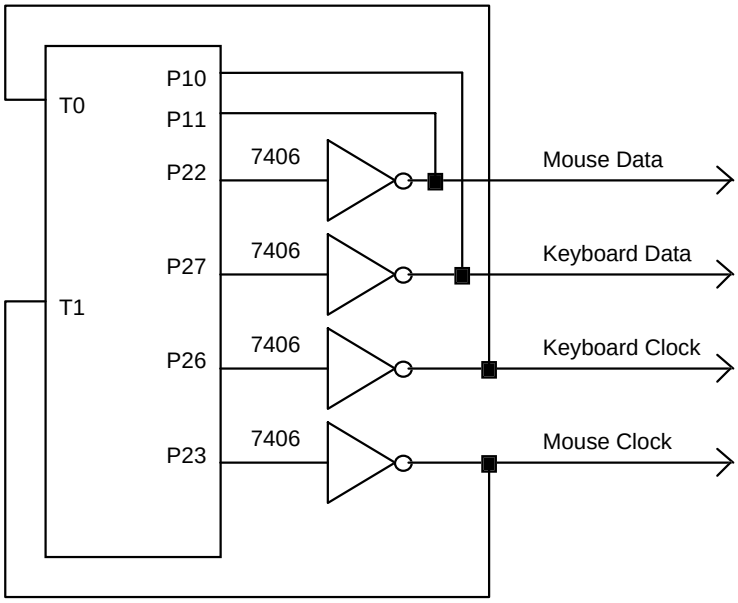


Fig 3.

6. VT82C42 Signal Description

Table 4. Signal Description for VT82C42

Symbol	40-Pin	44-Pin	Type	Name and Function
D_0-D_7 (BUS)	12-19	14-20	I/O	Act as data input or data output.
P_{10}-P_{13}	27-30	30-33	I/O	Pullup open drain port. Writing a '1' to these ports tri-states the ports. Act as input 'high' simultaneously if no outside 'low' connection. Writing a '0' to these ports results in generating a low on the port.
P_{20}-P_{27}	21-24 35-38	24-27 39-42	O	Output Port 20 - Output Port 23 Output Port 24 - Output Port 27
P_{14}-P_{15}	31, 32	35, 36	I/O	Pullup open drain port. Writing a '1' to these ports tri-states the ports. Act as input 'high' simultaneously if no outside 'low' connection. Writing a '0' to these ports results in generating a low on the port.
P_{16}-P_{17}	33, 34	37, 38	I	Input port 16, Input port 17
WR#	10	11	I	Act as a write signal.
RD#	8	9	I	Act as a read signal.
CS#	6	7	I	Chip select of this chip.
A_0	9	10	I	Command/Data select when RD# or WR# is active.
TEST 0, TEST 1	1 39	2 43	I	Act as Keyboard clock input in both AT mode & PS2 mode Act as Keyboard Data input in AT mode. Act as Mouse Clock input in PS2 mode.
XTAL 1, XTAL 2	2 3	3 4	I	Act as clock input to the chips. Can be connected to LC circuit or a single clock source (X2).
TH_SS TH_PROG TH_SSPP	5 25 26	6 28 29	I	Tie to VCC
TL_EA	7	8	I	Tie to ground.
SYNC	11	12	O	Internal state synchronous output.
NC		1, 13, 23, 34	I	No connection.
RESET#	4	5	I	A low in this pin reset the chip to a known state.
V_{CC}	40	44		Power supply of 4.5 to 5.5v.
GND	20	22		Ground.

1. Description for Table 4

RESET# is active low and is only an input pin. VT82C42 requires 10 clocks before RESET# goes to high to have the chip go to a known state.

Pins WR#, RD#, CS# and A_o are all input only pins and must activate for at least one clock cycle width to be recognised by the VT82C42.

D_0-d_7 are two-way pins, each having 4mA TTL compatible output driving. When D_0-D_7 is provided by the host, write cycle data should cover all the WR# CS# A_0 command width. When the D_0-D_7 is provided by the VT82C42, the D_0-D_7 is available as long as the RD#=0 CS#=0 command is asserted and is held one clock cycle after the command is deasserted.

TEST0,TEST1 are input only pins. TEST0 is expected to connect to KBCLK no matter what mode the VT82C42 is in. TEST1 is expected to connect to KBDATA when in AT-mode, and is expected to connect to MSCLK when in PS/2 mode. They have a 50K ohm pull up internally.

P16,P17 are input only pins. They have a 50K ohm pull up internally.

P20-P26 are all output only pins, each has 4mA TTL-compatible output. P27 is also output only pin, but with 16mA TTL-compatible output.

For two-way port pins, P_{10}-P_{15}, when floated (by written "1" to the port), the signals from these pins are all sustained tri-state output. That means when it is to be floated high, it will be driven high for one 8Mhz cycle before goes to float. The external connection is suggested to have a 4.7K pull-up resistor to maintain high after floating. The following logic diagram shows the corresponding functions. Note that the part surrounded by dash lines is a bi-directional TTL-compatible output with 4mA driving capabilities.

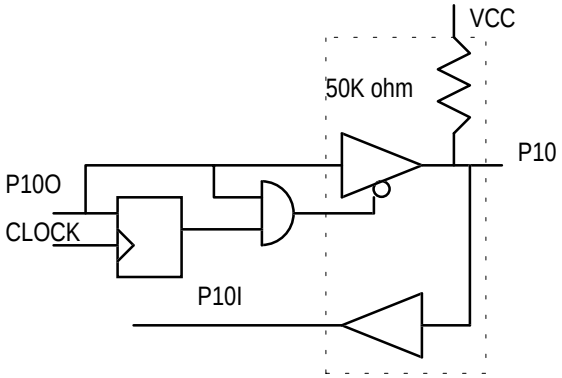


Fig 4.

TH_SS, TH_PROG and TH_SSPP are all input pins, and must be tied to high for normal operation. TL_EA is an input pin, and must be tied to low for normal operation.

SYNC is output pin, which drives some internal states out, this pin is only useful when in debugging stage. For normal operation, it should leave opened.

MSLKMD is the mouse lock enable pin. When this pin is tied low, the Mouse Lock mode is enabled, otherwise the Mouse Lock mode is disabled.

XTAL1, XTAL2 is the clocking source input of VT82C42, it can be implemented as in the figure 5. or figure 6. underneath:

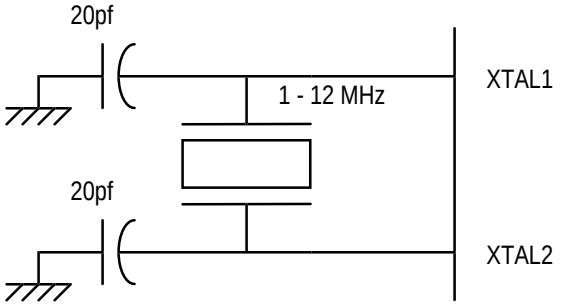


Figure 5. Crystal Connections for Clock source for VT82C42

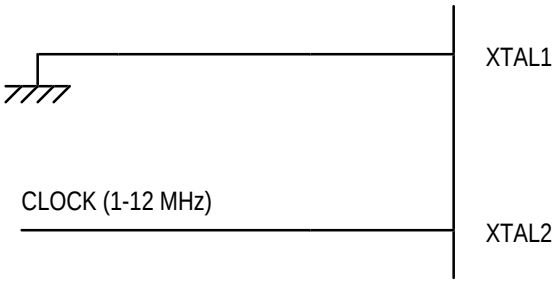


Figure 6. Clocking from other clock source for VT82C42

2. A transmission from Keyboard Controller to external device

* bitp means parity bit, bits means stop bit.
* CLOCK is driven by external device except the leading 250μs & ending 60μs low time.
* DATA is driven by KBC except the low time after the stop bit.
* If the maximum (a), (b), or (c) cannot be met, KBC will terminate the transmission with a timeout error.

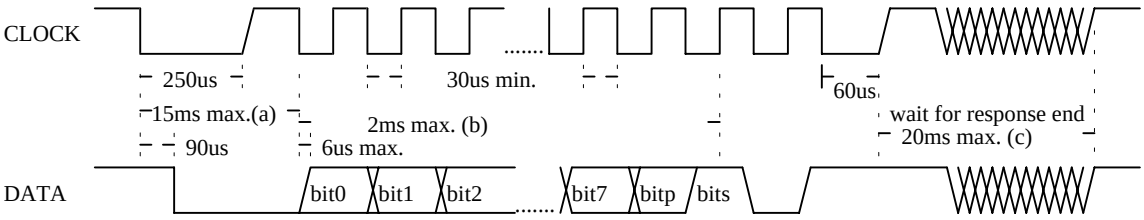


Fig 7.Timing from KBC to external device

3. A transmission from external device to Keyboard Controller

* CLOCK is driven by external device except the ending 60μs low time.
* DATA is driven by external devices.
* If the maximum (a) cannot be met, KBC will terminate the transmission with a timeout error.

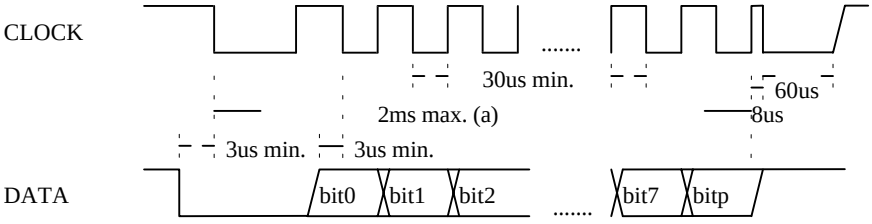


Fig 8.Timing from external device to KBC

4. Upon recieving commands which program the output ports from the host , the controller will put the corresponding data to the output port within 6 clocks. There is one exception, P_{20} is connected to system reset on a typical desktop application. For software compatibility the output of P_{20} is delayed for 4~8μs.

7. Pin Assignments

PLCC 44-Pin Configuration

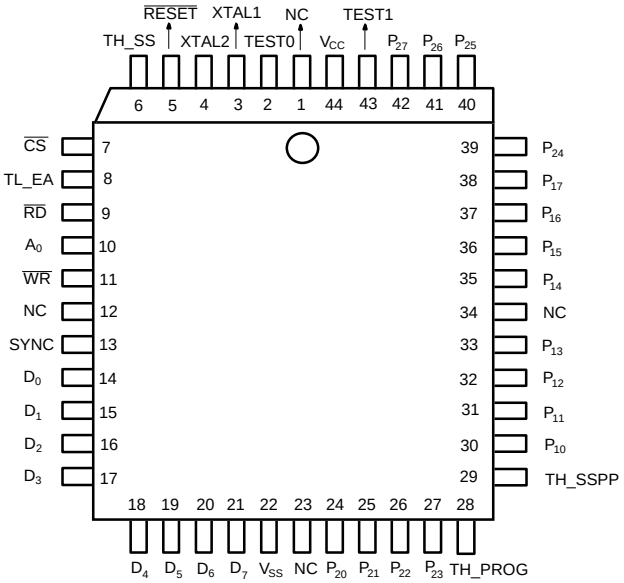


Fig 9.

DIP 40-Pin Configuration

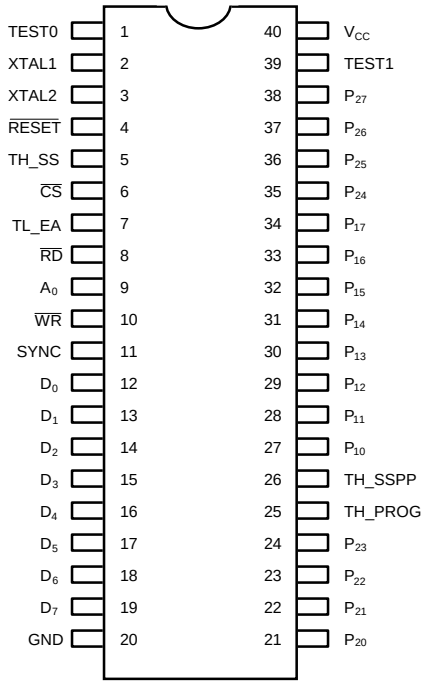


Fig 10.

8. Package Diagrams

44-Pin PLCC Dimension Diagram

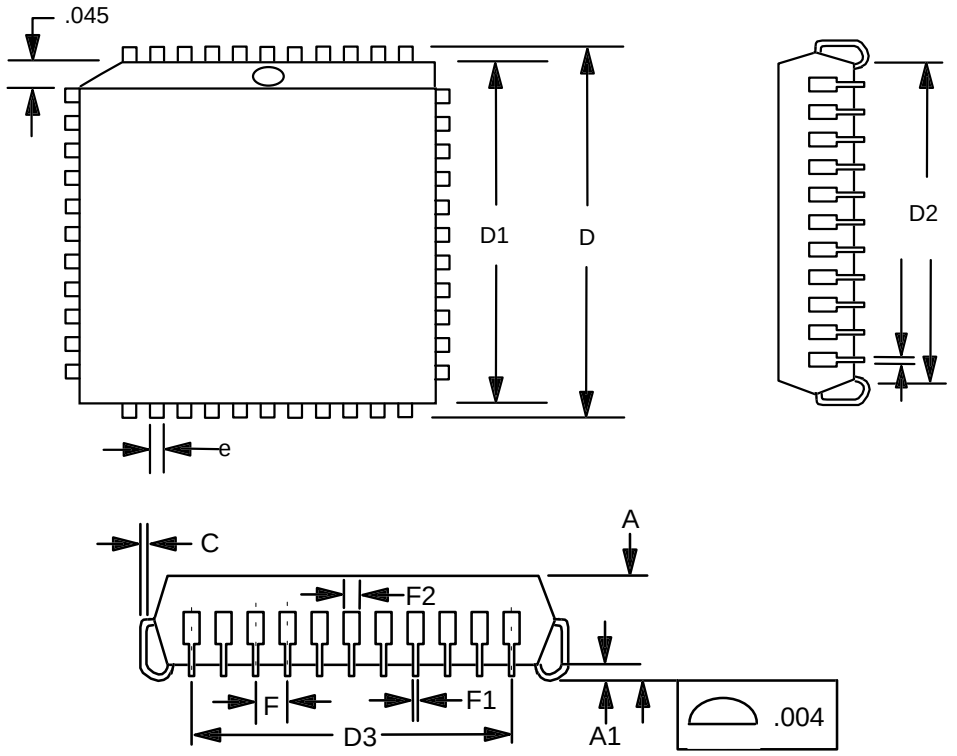


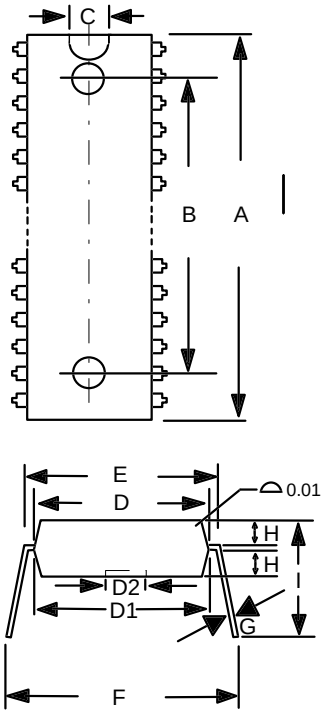
Fig 11.

44-Pin Quad PLCC (Q)

Talbe 5.

Dimension	Minimum	Typical	Maximum	Units
A	-	-	0.180	inches
A1	0.020	-	-	inches
C	-	0.010	-	inches
D	0.685	0.690	0.695	inches
D1	0.650	0.650	0.656	inches
D2	0.590	0.610	0.630	inches
D3	0.480	0.500	0.520	inches
F	-	0.050	-	inches
F1	0.013	-	0.021	inches
F2	0.026	-	0.032	inches
e	-	0.653	-	inches

40-Pin P-DIP Dimension Diagram



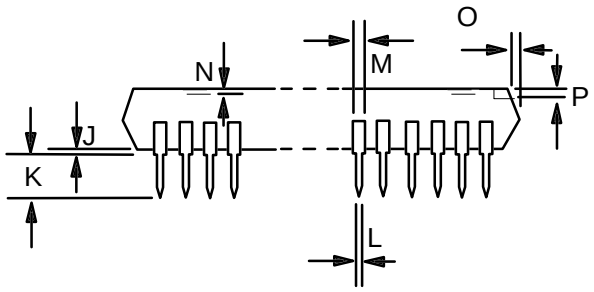


Fig 12.

40-Pin P-DIP

Table 6.

Dimension	Minimum	Typical	Maximum	Units
A	2.040	2.050	2.060	inches
B	1.530	1.540	1.550	inches
C	0.065	0.070	0.075	inches
D	0.546	0.550	0.554	inches
D1	0.550	0.554	0.558	inches
D2	0.130	0.150	0.170	inches
E	0.600	0.612	0.624	inches
F	0.630	0.650	0.670	inches
G	-	0.010	-	inches
H	0.066	0.070	0.074	inches
I	-	-	0.310	inches
J	0.015	-	-	inches
K	-	-	0.100	inches
L	0.016	0.018	0.02	inches
M	-	0.050	-	inches
N	-	0.015	-	inches
O	-	0.007	-	inches
P	0.030	0.035	0.040	inches