VT1622 and VT1622M

Digital TV Encoders

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VT1622 and VT1622M

Digital TV Encoders

PRODUCT FEATURES

- **Input Format**
  - Supports digital RGB (15/16 or 24-bit) or YCrCb (CCIR601 or CCIR656) 16 bit 4:2:2 input video data in both interlaced and non- interlaced formats
- **Output Format**
  - S-Video, Composite, YCbCr and SCART (RGB) with interlaced or non-interlaced scan output
  - YPbPr or RGB progressive scan output
  - NTSC (M and J) or PAL (B, D, G, H, I, M, N and Nc) TV output
  - SDTV output mode (525p or 625p) compliant with EIA770-1 and EIA770-2
- **High Quality 4x10-Bit Video DAC**
  - Simultaneous two S-Video or one S-Video with two composite outputs
  - Simultaneous RGB or YCbCr component output with one composite output
  - One progressive scan channel with YPbPr or RGB component output
- **Macrovision (VT1622M Only)**
  - Macrovision 7.1 anti-copy protection
  - Macrovision 1.0 AGC copy protection with 525p progressive scan output
- **Other Features**
  - Serial bus programming interface
  - Graphics resolution up to 1024x768
  - Second edition ProScale™ engine for support of any underscan or overscan size
  - Programmable power management
  - Master or slave video timing operation
  - P:P2 clocking mode for full TV screen
  - Adaptive deflicker filter to enhance TV image quality
  - Automatic detection of TV presence
  - 64-pin TQFP package

OVERVIEW

The VT1622 and VT1622M are digital television encoders that accept various RGB pixel data formats or YCrCb (compatible with CCIR656 or CCIR601) pixel data format from a VGA controller or MPEG decoder. These two TV encoder chips can support any input resolution from 320x200 up to 1024x768 and will or will not perform non-interlace to interlace conversion to generate high quality flicker-free composite video, S-video, component interlaced or progressive scan output signals.

Both VT1622 and VT1622M use the newest VIA ProScale® engine that provides the most advanced vertical and horizontal scaling technology. Using the programmable CRTC and the scaling factor, these two TV encoder chips can zoom an image in or out to any size. These two TV encoder chips uses an adaptive deflicker filter that checks the graphics on a pixel-by-pixel basis to maintain a flicker-free display.

The VT1622 and VT1622M can support various worldwide video standards, including NTSC-M (North America, Taiwan) NTSC-J (Japan), PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay) and PAL-Nc (Argentina). Because there are 4 DACs, these two TV encoder chips can simultaneously output composite video, S-video, component YCbCr, or RGB signals and output an analog progressive scan signal in YPbPr or RGB format.

The VT1622M can output video with the Macrovision 7.1 anticopy video signal or the Macrovision 1.0 AGC copy protection with 525p progressive scan output. The Macrovision anticopy process provides a means to deter the unauthorized copying of copy protected analog video signals onto a videocassette.

All features are software programmable through a serial bus interface that provides read/write access to all registers.

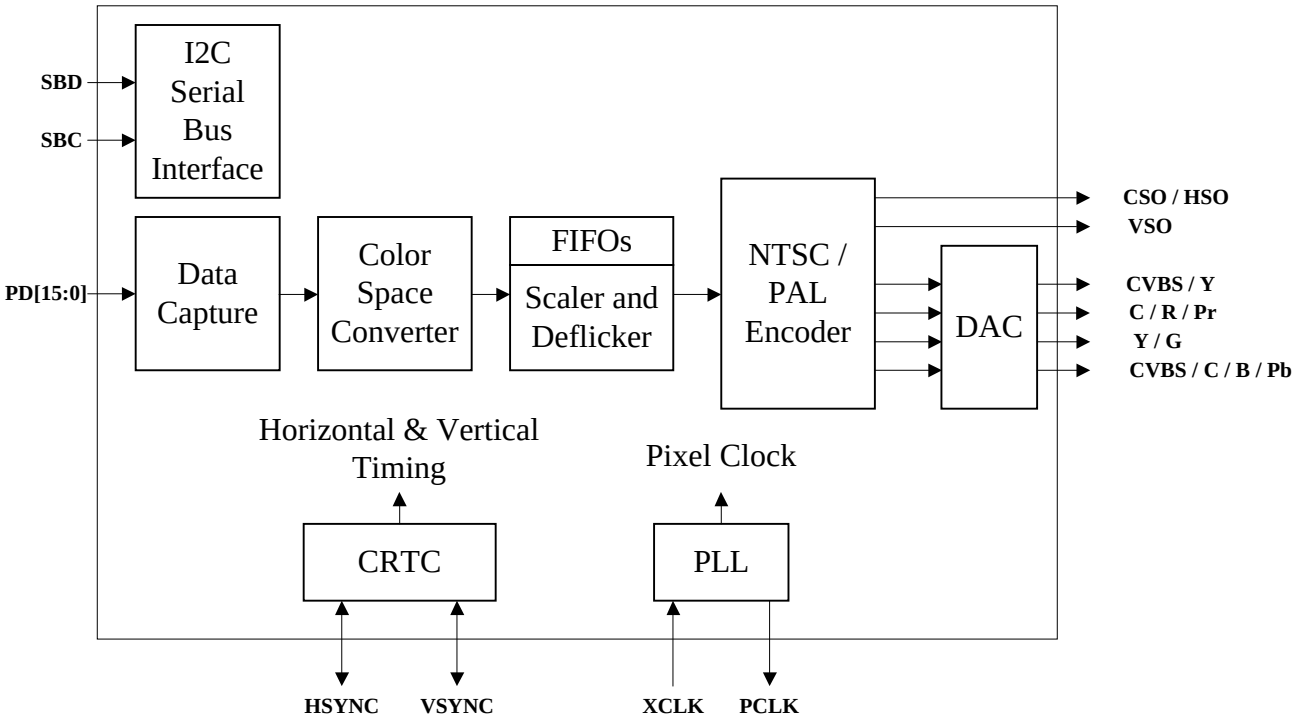


Figure 1. Functional Block Diagram

PINOUTS

Pin Diagram

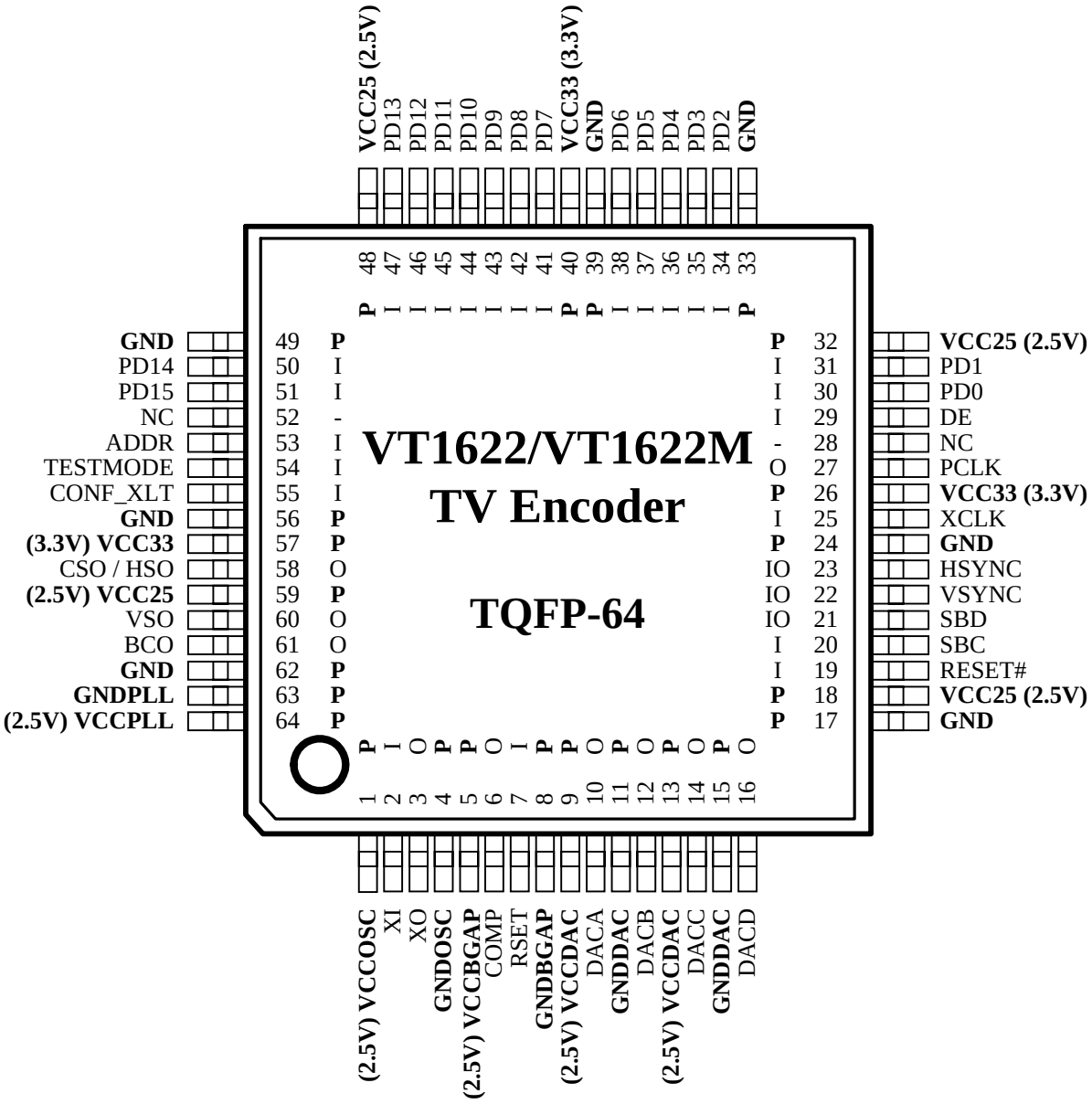


Figure 2. Pin Diagram (Top View)

Pin List

Table 1. Pin List (Alphabetical Order)

Pin	I/O	Pin Name	Pin	I/O	Pin Name
53	I	ADDR	38	I	PD6
61	O	BCO	41	I	PD7
6	O	COMP	42	I	PD8
55	I	CONF_XLT	43	I	PD9
58	O	CSO / HSO	44	I	PD10
10	O	DACA	45	I	PD11
12	O	DACB	46	I	PD12
14	O	DACC	47	I	PD13
16	O	DACD	50	I	PD14
29	I	DE	51	I	PD15
17	**P**	**GND**	19	I	RESET#
24	**P**	**GND**	7	I	RSET
33	**P**	**GND**	20	I	SBC
39	**P**	**GND**	21	IO	SBD
49	**P**	**GND**	54	I	TESTMODE
56	**P**	**GND**	**18**	**P**	**VCC25**
62	**P**	**GND**	**32**	**P**	**VCC25**
8	**P**	**GNDBGAP**	**48**	**P**	**VCC25**
11	**P**	**GNDDAC**	**59**	**P**	**VCC25**
15	**P**	**GNDDAC**	**26**	**P**	**VCC33**
4	**P**	**GNDOSC**	**40**	**P**	**VCC33**
63	**P**	**GNDPLL**	**57**	**P**	**VCC33**
23	IO	HSYNC	**5**	**P**	**VCCBGAP**
28	-	NC	**9**	**P**	**VCCDAC**
52	-	NC	**13**	**P**	**VCCDAC**
27	O	PCLK	**1**	**P**	**VCCOSC**
30	I	PD0	**64**	**P**	**VCCPLL**
31	I	PD1	60	O	VSO
34	I	PD2	22	IO	VSYNC
35	I	PD3	25	I	XCLK
36	I	PD4	2	I	XI
37	I	PD5	3	I	XO

Pin Descriptions

Table 2. Pin Descriptions

Pixel Data In			
Signal Name	**Pin #**	**Type**	**Description**
PD[15:0]	51, 50, 47, 46, 45, 44, 43, 42, 41, 38, 37, 36, 35, 34, 31, 30	I	**Pixel Data In.** These inputs can accept 8, 12, or 16 bit multiplexed or non-multiplexed RGB or YcbCr format.
DE	29	I	**Display Enable.** The rising edge of this signal identifies the first active pixel of data for each active line.
XCLK	25	I	**Input Clock.** Reference clock for Pixel Data inputs. It can operate on 1x, 2x or 3x pixel clock.
PCLK	27	O	**Pixel Clock Output.** This pin can provide and operate on a 1x, 2x or 3x pixel clock to a VGA.
HSYNC	23	IO	**Horizontal Sync.** When Rx1[2]=0, this pin can accept a horizontal sync input. When Rx1[2]=1, the device will output a horizontal sync pulse through this pin.
VSYNC	22	IO	**Vertical Sync.** When Rx1[3]=0, this pin can accept a vertical sync input. When Rx1[3]=1, the device will output a vertical sync pulse through this pin.

TV Output			
Signal Name	**Pin #**	**Type**	**Description**
VSO	60	O	**TV Vertical Sync.**
CSO / HSO	58	O	**TV Composite Sync / Horizontal Sync.**
DACA	10	O	**DAC A Analog Output.**
DACB	12	O	**DAC B Analog Output.**
DACC	14	O	**DAC C Analog Output.**
DACD	16	O	**DAC D Analog Output.**

Serial Bus Interface			
Signal Name	**Pin #**	**Type**	**Description**
SBD	21	IO	**Serial Bus Data.**
SBC	20	I	**Serial Bus Clock.**
ADDR	53	I	**Serial Bus Address Select.** Low = 40h, High = 42h.

Clock, Reset and Test			
Signal Name	**Pin #**	**Type**	**Description**
TESTMODE	54	I	**Test Mode Enable.** Pull down for regular operation.
CONF_XLT	55	I	**Internal / External Oscillator Select.** Selects internal or external oscillator. When pulled low, a crystal must be attached to pins 2 and 3. If pulled high, a stable 14.31818MHz external clock source must be supplied to pin 2, XI.
RESET#	19	I	**Reset.** When this pin is low, the device is held in the power-on reset condition.
BCO	61	O	**Bus Clock Out.** Output for providing a 14.31818 MHz clock to other devices.
XI	2	I	**Crystal In.** A 14.31818 MHz crystal is attached between XI and XO. An oscillator can also be connected to this pin.
XO	3	I	**Crystal Out.** A 14.31818 MHz crystal is attached between XI and XO. If an external oscillator is attached with XI, this pin should be connected to ground.
RSET	7	I	**External Resistor.** Used to set the full scale range of the DACs. Typical value is 4.64 KΩ (1%), attached between this pin and ground.
COMP	6	O	**Compensation.**
NC	28, 52	-	**Reserved For Future Use.** Do not connect.

Power and Ground			
Signal Name	**Pin #**	**Type**	**Description**
VCC33	**26, 40, 57**	**P**	**I/O Power.** 3.3V ±5%
VCC25	**18, 32, 48, 59**	**P**	**Core Power.** 2.5V ±5%
GND	**17, 24, 33, 39, 49, 56, 62**	**P**	**Digital Ground.** Connect to primary PCB ground plane.
VCCPLL	**64**	**P**	**PLL Power.** 2.5V ±5%
GNDPLL	**63**	**P**	**PLL Ground.** Connect to analog ground plane or connect to main digital ground plane through a ferrite bead to provide isolation from digital switching noise.
VCCDAC	**9, 13**	**P**	**DAC Power.** 2.5V ±5%
GNDDAC	**11, 15**	**P**	**DAC Ground.**
VCCBGAP	**5**	**P**	**Band Gap Power.** 2.5V ±5%
GNDBGAP	**8**	**P**	**Band Gap Ground.**
VCCOSC	**1**	**P**	**Oscillator Power.** 2.5V ±5%
GNDOSC	**4**	**P**	**Oscillator Ground.**

REGISTERS

Register Overview

The following tables summarize all on-chip registers. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 3. Register Summary

Offset	TV Encoder Registers	Default	Acc
00	Input Frame Format	00	RW
01	Input Sync Format	00	RW
02	Output Select	00	RW
03	Luma Filter	00	RW
04	Output Mode	00	RW
05	Control 1	00	RW
06	Control 2	00	RW
07	Start Active Video	00	RW
08	Start Horizontal Position	00	RW
09	Start Vertical Position	00	RW
0A	Cr Amplitude Factor	00	RW
0B	Black Level	00	RW
0C	Luma Amplitude Factor	00	RW
0D	Cb Amplitude Factor	00	RW
0E	Power Management	00	RW
0F	Status	00	**RO**
10	Special Effect 0	00	RW
11	Special Effect 1	00	RW
12	PLL P2 Value	00	RW
13	PLL D Value	00	RW
14	PLL N Value	00	RW
15	PLL Overflow	00	RW
16	Sub-carrier Value 0	00	RW
17	Sub-carrier Value 1	00	RW
18	Sub-carrier Value 2	00	RW
19	Sub-carrier Value 3	00	RW
1A	Reserved (Do Not Program)	00	RW
1B	Version ID	**03**	**RO**
1C	Overflow	00	RW
1D	Test 0	00	RW
1E	Test 1	00	RW
1F	- reserved -	00	–
20	TV Sync Step	00	RW
21	TV Burst Envelope Step	00	RW
22	TV Sub-carrier Phase Adjustment	00	RW
23	TV Blank Level	00	RW
24	TV Signal Overflow	00	RW
25-49	- reserved -	00	–

Offset	TV Encoder Registers	Default	Acc
4A	Input Aperture Threshold	00	RW
4B	Input Aperture Delta	00	RW
4C	Coring Function	00	RW
4D	Y Delay Control	00	RW
4E	UV Delay Control	00	RW
4F	Burst Maximum Amplitude	00	RW
50	Graphic Horizontal Total Pixels	00	RW
51	Graphic Horizontal Active Pixels	00	RW
52	Graphic Horizontal Overflow	00	RW
53	Graphic Vertical Total Lines	00	RW
54	Graphic Vertical Overflow	00	RW
55	TV Horizontal Total Pixels	00	RW
56	TV Horizontal Active Pixels	00	RW
57	TV Horizontal Sync Width	00	RW
58	TV Horizontal Overflow	00	RW
59	TV Burst Start	00	RW
5A	TV Burst End	00	RW
5B	TV Video Start	00	RW
5C	TV Video End	00	RW
5D	TV Video Overflow	00	RW
5E	Vertical Scale Factor	00	RW
5F	Horizontal Scale Factor	00	RW
60	Scaling Overflow	00	RW
61	Deflicker Threshold	00	RW
62	Deflicker Detection Length	00	RW
63	Scaling Horizontal Total Threshold	00	RW
64	Scaling Horizontal Total Pixel Overflow	00	RW
65	PY_G Amplitude Factor	00	RW
66	PB_B Amplitude Factor	00	RW
67	PR_R Amplitude Factor	00	RW
68	Auto Sub-carrier Value 0	00	**RO**
69	Auto Sub-carrier Value 1	00	**RO**
6A	Auto Sub-carrier Value 2	00	**RO**
6B	Auto Sub-carrier Value 3	00	**RO**
6C-FF	- reserved -	00	–

Register Descriptions

Offset 00 – Input Frame Format.....RW

7 Input Blurring.....INBLUR_E
- 0 Disable .....default
- 1 Enable

6 Interlace Input Mode.....ITL_IN
- 0 Disable .....default
- 1 Enable

5 Input Data Y Shift 16 .....YSH16
- 0 Disable .....default
- 1 Enable

4 Input Data Cr and Cb Shift 128 .....CSH128
- 0 Disable .....default
- 1 Enable

3-0 Input Data Format.....IDF
- 0000 16-bit non-multiplexed RGB (16-bit color) input .....default
- 0001 16-bit non-multiplexed YCrCb input
- 0010 16-bit multiplexed RGB (24-bit color) input
- 0011 15-bit non-multiplexed RGB (15-bit color) input
- 0100 12-bit multiplexed RGB (24-bit color) input (“C” multiplex scheme)
- 0101 12-bit multiplexed RGB (24-bit color) input (“I” multiplex scheme)
- 0110 8-bit multiplexed RGB (24-bit color) input
- 0111 8-bit multiplexed RGB (16-bit color) input
- 1000 8-bit multiplexed RGB (15-bit color) input
- 1001 8-bit multiplexed YCrCb input (Y, Cr and Cb multiplexed)
- 101x -reserved-
- 11xx -reserved-

Offset 01 – Input Sync Format ..... RW

7 Reserved ..... always reads 0

6 Field Signal Polarity..... FSP
- 0 Active Low ..... default
- 1 Active High

5 DS Input .....DSEN
- 0 Disable..... default
- 1 Enable - DS pin identifies the first active pixel of data for each active line

4 Detect Embedded Sync .....DES
- 0 Do not detect ..... default
- 1 Sync will be detected from the embedded codes on the pixel input stream

3 Vertical Sync Direction..... VSYO
- 0 Input ..... default
- 1 Output

2 Horizontal Sync Direction .....HSYO
- 0 Input ..... default
- 1 Output

1 Vertical Sync Polarity.....VSP
- 0 Active Low ..... default
- 1 Active High

0 Horizontal Sync Polarity .....HSP
- 0 Active Low ..... default
- 1 Active High

Offset 02 – Output Select ..... RW

7 CSO / HSO Pin I/O Select ..... CSO_EN
- 0 Output ..... default
- 1 Input

6 CSO / HSO Pin Polarity ..... CSO_HSOP
- 0 Active Low ..... default
- 1 Active High

5 CSO / HSO Output Pin Function ..... CSO_HSO
- 0 Output for HSO ..... default
- 1 Output for CSO

4 Sync on R or Pr ..... SYNC_R_PR
- 0 Disable ..... default
- 1 Enable

3 Sync on G ..... SYNC_G
- 0 Disable ..... default
- 1 Enable

2 Sync on B or Pb ..... SYNC_B_PB
- 0 Disable ..... default
- 1 Enable

1-0 DAC Select ..... DACSEL
- 00 DAC A/B/C/D = CVBS / C / Y / CVBS default
- 01 DAC A/B/C/D = Y / C / Y / C
- 10 DAC A/B/C/D = CVBS / R / G / B
- 11 DAC A/B/C/D = CVBS / Pr / Y / Pb

Offset 03 – Luma Filter Control ..... RW

7-5 Luma Filter Adjust ..... YBW
- 000 Lowpass (NTSC) 21 MHz TV Clock..... default
- 001 Lowpass (NTSC) 26 MHz TV Clock
- 010 Lowpass (NTSC) 33 MHz TV Clock
- 011 Notch (NTSC) 26 MHz TV Clock
- 100 Lowpass (PAL) 21 MHz TV Clock
- 101 Lowpass (PAL) 26 MHz TV Clock
- 110 Lowpass (PAL) 32 MHz TV Clock
- 111 Lowpass (All) 26 MHz TV Clock

(see "Luminance Filter" Table 5 on page 34).

4-2 Chroma Filter Adjust ..... CBW
- 000 Lowpass 21 MHz TV Clk, 3dB B/W=0.6MHz ..... default
- 001 Lowpass 26 MHz TV Clk, 3dB B/W=0.6MHz
- 010 Lowpass 33 MHz TV Clk, 3dB B/W=0.6MHz
- 011 -reserved-
- 100 -reserved-
- 101 -reserved-
- 110 -reserved-
- 111 Lowpass 26MHz TV Clk, 3dB B/W=4.43MHz

(see "Chrominance Filter" Table 6 on page 34).

1-0 Luma Channel Deflicker Adjust ..... FY
- 00 No Deflicker Filter ..... default
- 01 1:1:1 Deflicker Filter
- 10 1:2:1 Deflicker Filter
- 11 -reserved-

Offset 04 – Output Mode ..... RW

7 VSO Polarity ..... VSOP
- 0 Active Low ..... default
- 1 Active High

6 Filter Bypass ..... FIL_PASS
- 0 Disable ..... default
- 1 Enable

5 PAL_Nc Mode ..... PAL_NC
- 0 Disable ..... default
- 1 Enable (bits 1-0 must be 00b)

4 PAL_N Mode ..... PAL_N
- 0 Disable ..... default
- 1 Enable (bits 1-0 must be 00b)

3-2 Output Mode ..... OUT_MODE
- 00 Normal ..... default
- 01 Non-Interlaced
- 10 Progressive
- 11 -reserved-

1 Output Line Selection ..... LINE_SEL
- 0 625 ..... default
- 1 525

0 Output TV Standard ..... VOS
- 0 PAL ..... default
- 1 NTSC

Offset 05 – Control 1 ..... RW

7 Reserved ..... always reads 0

6 Master / Slave Clock Mode Select ..... **M_S**
- 0 Master Clock Mode ..... default
- 1 Slave Clock Mode

5 Reserved ..... always reads 0

4 FSCI Auto Adjust ..... **FCSI_ADJ_EN**
- 0 Disable (use FSCI value in Rx19-16) ..... default
- 1 Enable (use 14.31818 MHz to calculate FSCI [31:0] which may be read in Rx6B-68)

3 FSCI Auto Fine Tune ..... **FSCI_FINE_TUNE**
- 0 Disable ..... default
- 1 Enable

2 PCLK Clock Polarity ..... **PCLKP**
- 0 Normal ..... default
- 1 Inverted

1-0 PCLK Output Mode ..... **PCM**
- 00 1x ..... default
- 01 2x
- 10 3x
- 11 -reserved-

Offset 06 – Control 2 ..... RW

7 Color Bar ..... **CB_ENABLE**
- 0 Disable ..... default
- 1 Enable

6-5 XCLK Input Clock Mode ..... **XCM**
- 00 1x ..... default
- 01 2x
- 10 3x
- 11 -reserved-

4 Edge Used to Latch Input Data ..... **MCP**
- 0 Normal clock input ..... default
- 1 Inverted clock input

3-0 Input Clock Adjust ..... **DPA**
- 0000 Shortest input clock delay ..... default
- …
- 1111 Longest input clock delay

Each increment of this field is one AND gate delay

Offset 07 – Start Active Video ..... RW

7-0 Start Active Video Bits 7-0 ..... **SAV[7:0]**
(see Rx1C[3] for bit-8) ..... default = 00h
Sets the delay from the leading edge of horizontal sync to the start of active video.

Offset 08 –Start Horizontal Position ..... RW

7-0 Start Horizontal Position Bits 7-0 ..... **HP[7:0]**
(see Rx1C[2] for bit-8) ..... default = 00h
Used to shift the displayed TV image in a horizontal direction.

Offset 09 – Start Vertical Position ..... RW

7-0 Start Vertical Position Bits 7-0 ..... **VP[7:0]**
(see Rx1C[1] for bit-8) ..... default = 00h
Used to shift the displayed TV image in a vertical direction.

Offset 0A – Cr Amplitude Factor ..... RW

7-0 Cr Amplitude Factor ..... default = 00h

Offset 0B – Black Level ..... RW

7-0 Black Level ..... default = 00h

Offset 0C – Luma Amplitude Factor ..... RW

7-0 Luma Amplitude Factor ..... default = 00h

Offset 0D – Cb Amplitude Factor ..... RW

7-0 Cb Amplitude Factor ..... default = 00h

Offset 0E – Power Management ..... RW

7 Monitor Connection Status ..... SENSE_ENB
Set this bit from 0 to 1 then back to 0 to get the status of monitor connections ..... default = 0

6 Auto Sense ..... AUTOSENSE
0 Disable ..... default
1 Enable - the monitor connection status will be automatically sensed once per frame during the vertical blanking interval

5 Reserved ..... always reads 0

4 PLL Power Down ..... PWRPLL_ENB
0 Disable (PLL On) ..... default
1 Enable (PLL Off)

3 DAC A Power Down ..... PWRA_ENB
0 Disable (DAC A On) ..... default
1 Enable (DAC A Off)

2 DAC B Power Down ..... PWRB_ENB
0 Disable (DAC B On) ..... default
1 Enable (DAC B Off)

1 DAC C Power Down ..... PWRC_ENB
0 Disable (DAC C On) ..... default
1 Enable (DAC C Off)

0 DAC D Power Down ..... PWRD_ENB
0 Disable (DAC D On) ..... default
1 Enable (DAC D Off)

Offset 0F – Status ..... RO

7 Macrovision Copy Protection ..... MACRV (RO)
0 Disabled ..... default
1 Enabled

6-4 Reserved ..... always reads 0

3 DAC A Status ..... AST (RO)
0 Disabled ..... default
1 Enabled

2 DAC B Status ..... BST (RO)
0 Disabled ..... default
1 Enabled

1 DAC C Status ..... CST (RO)
0 Disabled ..... default
1 Enabled

0 DAC D Status ..... DST (RO)
0 Disabled ..... default
1 Enabled

Offset 10 – Special Effect 0 ..... RW

7-0 Hue Adjust Bits 7-0 ..... **HUE_ADJ[7:0]**
(see Rx11[7-5] for bits 10-8) ..... default = 00h

Offset 11 – Special Effect 1 ..... RW

7-4 Reserved (Do Not Program) ..... default = 0

3 Dot Crawl ..... **DOT_CRAWL**
0 Enable ..... default
1 Disable

2-0 Hue Adjust Bits 10-8 ..... **HUE_ADJ[10:8]**
(see Rx10 for bits 0-7) ..... default = 000b
Refer to Table 8, Master Clock Mode Clock Settings, for more information.

Offset 12 – PLL P2 Value ..... RW

7-5 Resister Selection Bits 2-0 ..... **R[2:0]**
Programmed in increments of 1.0 ..... default = 000b

4-0 Second Post Divider Control ..... **P2[4:0]**
Programmed in increments of 0.5 ..... def = 00000b

Offset 13 – PLL D Value ..... RW

7-6 Reserved ..... always reads 0

5-0 Pre-Divider Control ..... **D[5:0]**
Programmed in increments of 0.5 ..... def = 000000b

Offset 14 – PLL N Value ..... RW

7-0 VCO Output Division Factor Bits 7-0 ..... **N[7:0]**
(see Rx15[1:0] for bits 9-8) ..... default = 00h
N[9:8] defines the division factor applied to the VCO output. N is in increments of 1.0.

Offset 15 – PLL Overflow ..... RW

7 Reserved ..... always reads 0

6-2 First Post Divider Control ..... **P[4:0]**
Programmed in increments of 0.5 .... default = 00000b

1-0 VCO Output Division Factor [9:8] ..... **N[9:8]**
(see Rx14 for bits 0-7) ..... default = 00b
N[9:8] defines the division factor applied to the VCO output.

Offset 16 – Sub-Carrier Value 0 ..... RW

7-0 Sub-Carrier Value Bits 7:0 ..... default = 00h

Offset 17 – Sub-Carrier Value 1 ..... RW

7-0 Sub-Carrier Value Bits 15:8 ..... default = 00h

Offset 18 – Sub-Carrier Value 2 ..... RW

7-0 Sub-Carrier Value Bits 23:16 ..... default = 00h

Offset 19 – Sub-Carrier Value 3 ..... RW

7-0 Sub-Carrier Value Bits 31:24 ..... default = 00h

Offset 1B – Version ID (03h) ..... RO

7-0 Version ID ..... **always reads 03h**

Offset 1C – Overflow ..... RW

7-4 Reserved ..... always reads 0

3 Start Active Video Bit-8 ..... **SAV[8]**
(see Rx7 for bits 0-7) ..... default=0

2 Start Horizontal Position Bit-8 ..... **HP[8]**
(see Rx8 for bits 0-7) ..... default=0

1 Start Vertical Position Bit-8 ..... **VP[8]**
(see Rx9 for bits 0-7) ..... default=0

0 Frequency Conversion Parameter Bit-8 ..... **K0[8]**
(see Rx1A for bits 0-7) ..... default=0

Offset 20 – TV Sync Step ..... RW

7-0 TV Sync Step ..... [7:0]
(see TV Overflow Rx24[0] for bit-8)..... default = 00h
Step value to control the shape / slope of the sync.

Offset 21 – TV Burst Envelope Step ..... RW

7-0 TV Burst Envelope Step ..... [7:0]
(see TV Overflow Rx24[1] for bit-8)..... default = 00h
Step value to control the shape / slope of the burst.

Offset 22 – TV Sub-Carrier Phase Adjust ..... RW

7-0 TV Sub-Carrier Phase Adjust ..... [7:0]
(see Rx24[4-2] for bits 10-8) ..... default = 00h
Step value to control the shape / slope of the burst.

Offset 23 –TV Blank Level ..... RW

7-0 TV Blank Level ..... [7:0]
(see Rx24[5] for bit-8) ..... default = 00h
Step value to control the base level of the blank signal.

Offset 24 – TV Signal Overflow ..... RW

7-6 Reserved ..... always reads 0
5 Bit[8] of TV Blank Level (Rx23)..... default = 0
4-2 Bit[10:8] of Sub-Carrier Phase Adjust (Rx22)
..... default = 0
1 Bit[8] of TV Burst Envelope Step (Rx21) default = 0
0 Bit[8] of TV Sync Step (Rx20) ..... default = 0

Offset 4A – Input Aperture Threshold ..... RW

7-0 Input Data Threshold ..... IN_APR_TH
Threshold for input data..... default = 00h

Offset 4B - Input Aperture Delta ..... RW

7-0 Input Data Adjustment Value..... IN_APR_DLT
Adjustment value for input data..... default = 00h

Offset 4C – Coring Function ..... RW

7 Coring Function ..... COR_EN
0 Disable..... default
1 Enable
6-0 Coring Function Threshold ..... COR_TH
..... default = 00h

Offset 4D – Y Delay Control ..... RW

7-3 Reserved..... always reads 0
2-0 Y Delay Depth..... default = 0

Offset 4E – UV Delay Control ..... RW

7 Burst Max Amplitude Bit-8 ..... **BURST_AMP[8]**
(see Rx4F for bits 7:0)..... default = 0
6-4 U Delay Depth..... **U_DELAY**
000 Shortest input clock delay..... default
… …
111 Longest input clock delay
Each increment of this field is one clock cycle
3 Y, Cb, Cr Underflow Check ..... **UF_CHK**
0 Disable..... default
1 Enable
2-0 V Delay Depth..... **V_DELAY**
000 Shortest input clock delay..... default
… …
111 Longest input clock delay
Each increment of this field is one clock cycle

Offset 4F – Burst Maximum Amplitude ..... RW

7-0 Burst Maximum Value..... **BURST_AMP[7:0]**
(see Rx4E[7] for bit-8) ..... default = 00h

Offset 50 – Graphic Horizontal Total Pixels.....RW

7-0 Graphic Horiz Total Pixels .....GH_TOTAL[7:0]
(see Rx52[2-0] for bits 10:8) .....default = 00h

Offset 51 – Graphic Horizontal Active Pixels.....RW

7-0 Graphic Horiz Active Pixels..... GH_ACTIVE[7:0]
(see Rx52[5-4] for bits 9:8) .....default = 00h

Offset 52 – Graphic Horizontal Overflow.....RW

7-6 Reserved ..... always reads 0
5-4 Gr H Active Pixels Overflow..... GH_ACTIVE[9:8]
(see Rx51 for bits 7:0) ..... default = 00b
3 Reserved ..... always reads 0
2-0 Gr H Total Pixels Overflow .....GH_TOTAL[10:8]
(see Rx50 for bits 7:0) ..... default = 000b

Offset 53 – Graphic Vertical Total Lines.....RW

7-0 Graphic Vert Total Pixels .....GV_TOTAL[7:0]
(see Rx54[2-0] for bits 10:8) .....default = 00h

Offset 54 – Graphic Vertical Overflow .....RW

7-3 Reserved ..... always reads 0
2-0 Gr V Total Pixels Overflow.....GV_TOTAL[10:8]
(see Rx53 for bits 7:0) ..... default = 000b

Offset 55 – TV Horizontal Total Pixels .....RW

7-0 TV Horiz Total Pixels..... TH_TOTAL[7:0]
(see Rx58[2-0] for bits 10:8) .....default = 00h

Offset 56 – TV Horizontal Active Pixels.....RW

7-0 TV Horiz Active Pixels .....TH_ACTIVE[7:0]
(see Rx58[5-4] for bits 9:8) .....default = 00h

Offset 57 – TV Horizontal Sync Width .....RW

7-0 TV Horiz Sync Width..... THSYNC_WIDTH [7:0]
.....default = 00h

Offset 58 – TV Horizontal Overflow .....RW

7-6 Reserved ..... always reads 0
5-4 TV H Active Pixels Overflow.....TH_ACTIVE[9:8]
(see Rx56 for bits 7:0) ..... default = 00b
3 Reserved ..... always reads 0
2-0 TV H Total Pixels Overflow..... TH_TOTAL[10:8]
(see Rx55 for bits 7:0) ..... default = 000b

Offset 59 – TV Burst Start..... RW

7-0 TV Burst Start..... TBURST_START[7:0]
(see Rx58[2-0] for bits 10:8).....default = 00h
(start point relative to analog HSYNC falling edge)

Offset 5A – TV Burst End..... RW

7-0 TV Burst End..... TBURST_END[7:0]
(see Rx5D[6] for bit 8)..... default = 00h
(end point relative to analog HSYNC falling edge)

Offset 5B – TV Video Start Point..... RW

7-0 TV Video Start.....TVIDEO_START[7:0]
(see Rx5D[4] for bit 8)..... default = 00h
(number of pixels between leading edge of analog HSYNC and active video)

Offset 5C – TV Video End Point ..... RW

7-0 TV Video End ..... TVIDEO_END[7:0]
(see Rx5D[3-0] for bits 11:8)..... default = 00h
(number of pixels between leading edge of analog HSYNC and video end)

Offset 5D – TV Video Overflow ..... RW

7 Reserved..... always reads 0
6 TV Burst End Overflow..... TBURST_END[8]
(see Rx5A for bits 7:0)..... default = 0
5 Reserved..... always reads 0
4 TV Video Start Overflow..... TVIDEO_START[8]
(see Rx5B for bits 7:0) ..... default = 0
3-0 TV Video End Overflow ..... TVIDEO_END[11:8]
(see Rx5C for bits 7:0) ..... default = 0000b

Offset 5E – Vertical Scale Factor ..... RW

7-0 Vertical Scale Factor..... VSCALE_FAC[7:0]
(see Rx60[3-0] for bits 11:8)..... default = 00h

Offset 5F – Horizontal Scale Factor..... RW

7-0 Horizontal Scale Factor ..... HSCALE_FAC[7:0]
(see Rx60[6-4] for bits 10:8)..... default = 00h

Offset 60 – Scaling Overflow ..... RW

7 Reserved..... always reads 0
6-4 H Scale Factor Overflow ..... HSCALEFAC[10:8]
(see Rx5F for bits 7:0)..... default = 000b
3-0 V Scale Factor Overflow..... VSCALE_FAC[11:8]
(see Rx5E for bits 7:0) ..... default = 0000b

Offset 61 – Deflicker Threshold ..... RW

7-0 Deflicker Threshold ..... DFK_THD[7:0]
..... default = 00h

Offset 62 – Deflicker Detection Length ..... RW

7-2 Reserved ..... always reads 0
1-0 Deflicker Det Length ..... DFKDT_LENGTH[1:0]
00 No detection ..... default
01 7 pixels
10 9 pixels
11 11 pixels

Offset 63 – Scaling Horizontal Total Pixels ..... RW

7-0 Scaling H Total Pixels ..... SH_TOTAL[7:0]
(see Rx64[3-0] for bits 11:8) ..... default = 00h

Offset 64 – Scaling Horizontal Total Pixels Overflow ... RW

7-4 Reserved ..... always reads 0
3-0 Scaling H Tot Pixels Overflow ... SH_TOTAL[11:8]
(see Rx63 for bits 7:0) ..... default = 0000b

Offset 65 – PY_G Amplitude Factor ..... RW

7-0 PY or G Amplitude Factor ..... PYGAF[7:0]
..... default = 00h

Offset 66 – PB_B Amplitude Factor ..... RW

7-0 PB or B Amplitude Factor ..... PBBAF[7:0]
..... default = 00h

Offset 67 – PR_R Amplitude Factor ..... RW

7-0 PR or R Amplitude Factor ..... PRRAF[7:0]
..... default = 00h

Offset 68 – Auto Sub-Carrier Value 0 ..... RO

7-0 Auto Adjust FSCI Value Byte 0 ..... A_FSCI[7:0]
(1 byte of a 32-bit value in Rx68-6B) .. default = 00h†

Offset 69 – Auto Sub-Carrier Value 1 ..... RO

7-0 Auto Adjust FSCI Value Byte 1 ..... A_FSCI[15:8]
(1 byte of a 32-bit value in Rx68-6B) .. default = 00h†

Offset 6A – Auto Sub-Carrier Value 2 ..... RO

7-0 Auto Adjust FSCI Value Byte 2 ..... A_FSCI[23:16]
(1 byte of a 32-bit value in Rx68-6B) .. default = 00h†

Offset 6B – Auto Sub-Carrier Value 3..... RO

7-0 Auto Adjust FSCI Value Byte 3 ..... A_FSCI[31:24]
(1 byte of a 32-bit value in Rx68-6B) .. default = 00h†

†After reset, the above registers all read 00h, FSCI is disabled, and the FSCI value in Rx19-16 is used. If Rx5[3] is set to one to enable "FSCI Auto Adjust", FSCI is generated by on-chip circuitry and the FSCI value may be read from registers Rx6B-68 above (in this case, the value in Rx19-16 is ignored).

FUNCTIONAL DESCRIPTION

Architecture Description

Refer to Figure 3 below for the following module descriptions.

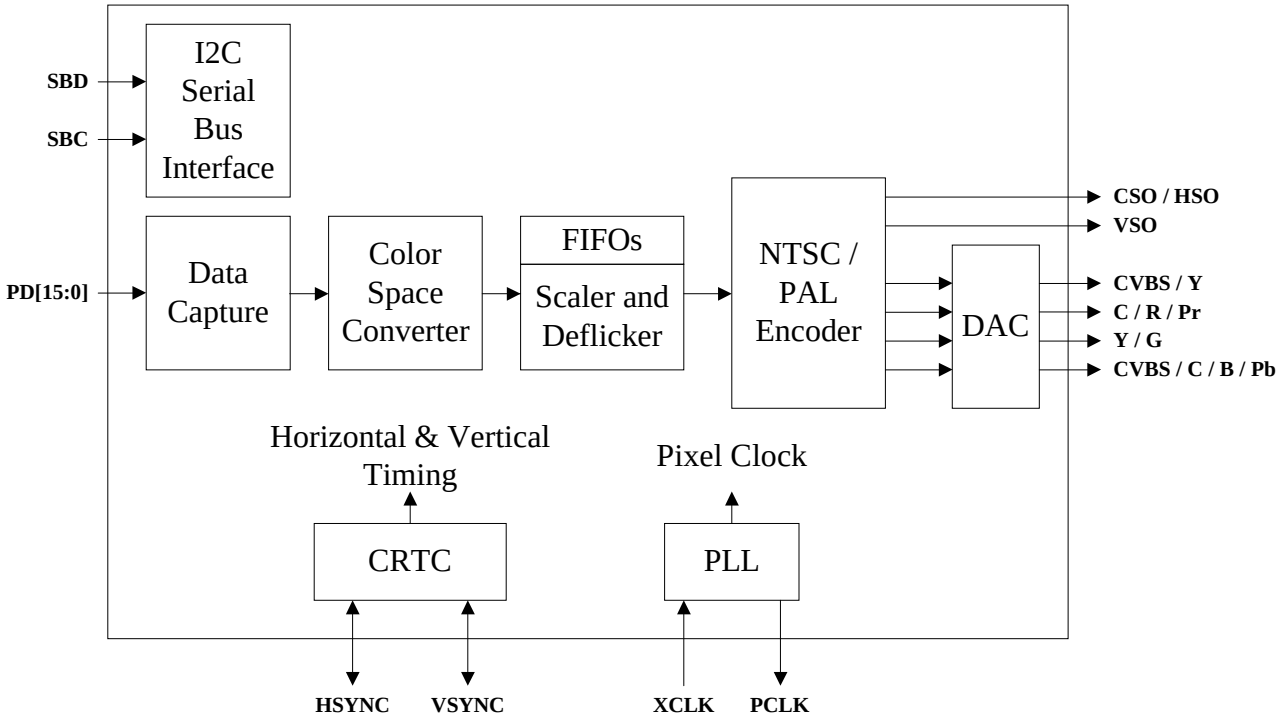


Figure 3. Architectural Description Block Diagram

Data Capture

8-bit, 12-bit, 16-bit multiplexed or 16-bit non-multiplexed input data is captured by this module and transferred to 24-bit data for one pixel.

Color Space Converter

The data from the Data Capture module is RGB or YCrCb format. This module converts both formats to YUV 422 format.

Scaler and Deflicker

This module converts the lines of input pixel data to the appropriate number of output lines for producing a full-screen image on the television receiver. The image can be scaled to 100% within the viewable area of the screen. The device can perform vertical filtering to reduce the effects of picture flicker due to the interlacing of the output image. Because this process trades off vertical resolution in order to reduce flicker, the amount of flicker filtering is programmable and allows the process to be optimized for the specific image. This module generates YUV444 pixel data from the interlaced image to the encoder module.

Encoder

This module accepts the YUV444 pixel data and converts it to a standard baseband television signal that is compatible with worldwide standards including PAL (B, D, G, H, I, N, Nc, M) and NTSC (M, J). The Y data can be manipulated for contrast control and a setup level can be added for brightness control. The U, V data can be scaled to achieve color saturation control. Also, the U, V signals are modulated by the appropriate sub-carrier sine/cosine waveforms and a phase offset may be added onto the color sub-carrier during active video to allow hue adjustment. The resulting U and V signals are added together to make up the chrominance signal. The luma (Y) and chroma signals are added together to make up the composite video signal. Separated luma and chroma signals make up the S-video signal.

DAC

The VT1622 and VT1622M contain four 10-bit DACs. Each DAC is used to convert digital composite, luma, chroma, RGB, YCbCr, or YPbPr data to analog signals and can be individually powered off if not required. In addition, the DAC module has an auto-detection circuit, which provides a way to sense the connection of a TV.

Serial Bus Interface

The VT1622 and VT1622M contain a standard serial bus control port through which the control registers can be written and read. The serial bus address is 40h or 42h depending on the strapping of the ADDR pin.

CRTC

The VGA controller normally supplies the horizontal and vertical sync signals, however, they can also be selected to be generated by the VT1622 or the VT1622M. This module generates the horizontal and vertical sync signals. In CCIR656 input mode, the embedded sync may also be used.

PLL

Both of the VT1622 and VT1622M contain a high accuracy, low-jitter phase-locked-loop to create outstanding quality video. Normal operation requires the encoding clock to be generated by the PLL. In master clock mode, the reference clock of the PLL is provided by OSC and the frequency is 14.31818 MHz. In slave clock mode, the reference clock is input via the XCLK pin.

Master/Slave Clock Mode

Both of the VT1622 and VT1622M can be configured for either master or slave clock mode. In master clock mode, they provide the pixel clock signal to the video source and expect incoming data to be available when required. In slave clock mode, the two TV encoder chips accept the external pixel clock from the video source.

Master Mode

In master clock mode, the VT1622 and VT1622M work as a master and the video source device works as a slave. They provide a clock signal through the PCLK pin to the video source device and the video source device will use this clock as a frequency reference. Then the video source will generate a clock signal into the XCLK pin. The two TV encoders chips will use this clock signal to latch incoming data. The PCLK clock signal can also be used as the input clock signal connected directly to the XCLK pin. The HSYNC and VSYNC signals can be programmed to be either input or output to the two TV encoder chips. The master clock mode can be configured as mode 1 and mode 2 illustrated in Figure 4 and Figure 5.

Slave Mode

In slave clock mode, the VT1622 and VT1622M work as a slave and the video source device works as a master. The video source device will generate a clock signal input to the XCLK pin. Through the XCLK pin, they receive a clock from the video source device and use this clock to latch incoming data. Moreover, this clock will be a reference clock of the two TV encoder chips for generating a pixel clock. The HSYNC and VSYNC signals can be programmed to be either input or output to the two TV encoder chips. In slave clock mode, both of the VT1622 and VT1622M can be configured as illustrated in Figure 6.

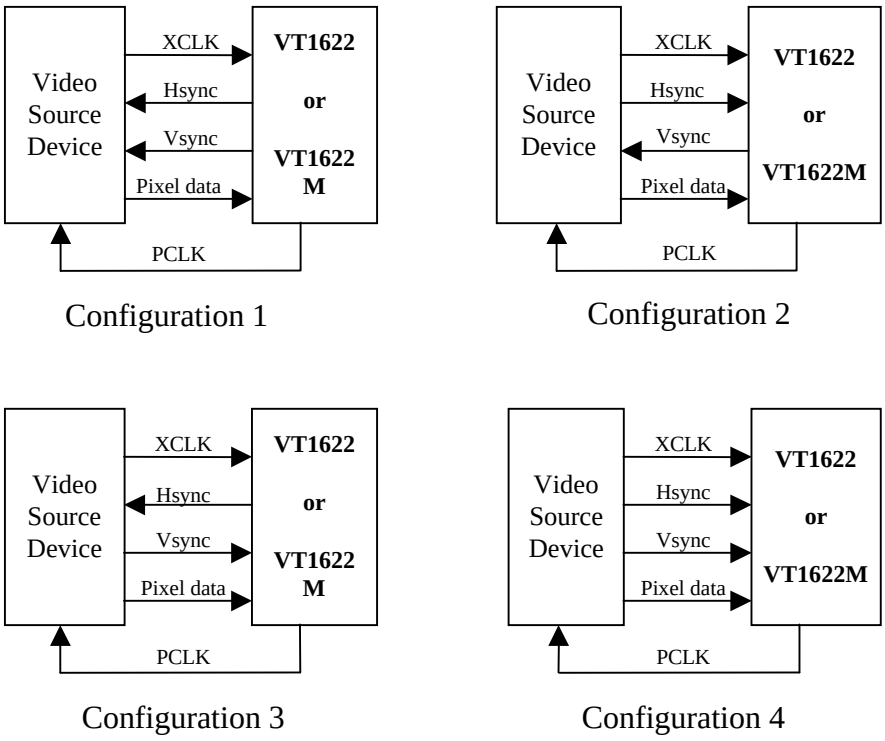
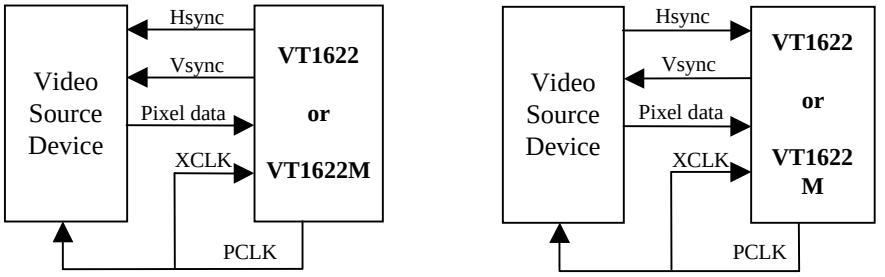
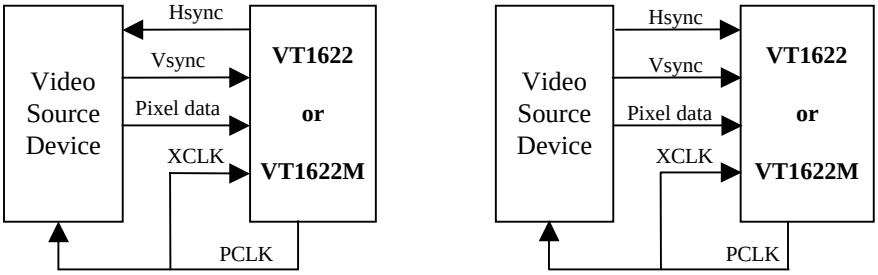


Figure 4. Master Clock Mode 1

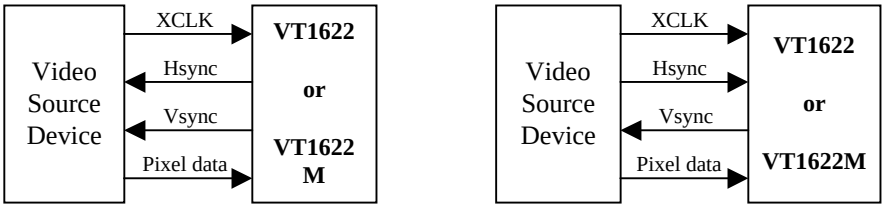


Configuration 5 Configuration 6

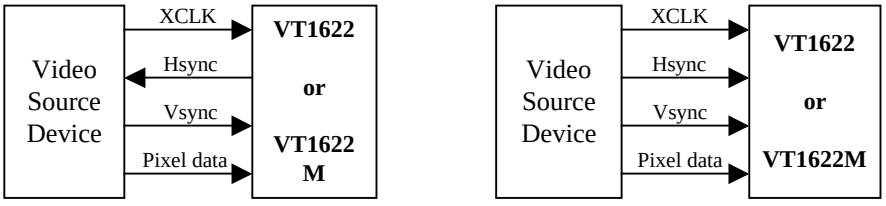


Configuration 7 Configuration 8

Figure 5. Master Clock Mode 2



Configuration 1 Configuration 2



Configuration 3 Configuration 4

Figure 6. Slave Clock Mode

Digital Video Interface

The VT1622 and VT1622M can be configured with an 8-bit, 12-bit, or 16-bit input data bus. They accept RGB 16-bit, RGB 15-bit, RGB 24-bit or YCrCb 16-bit (CCIR 656) data format.

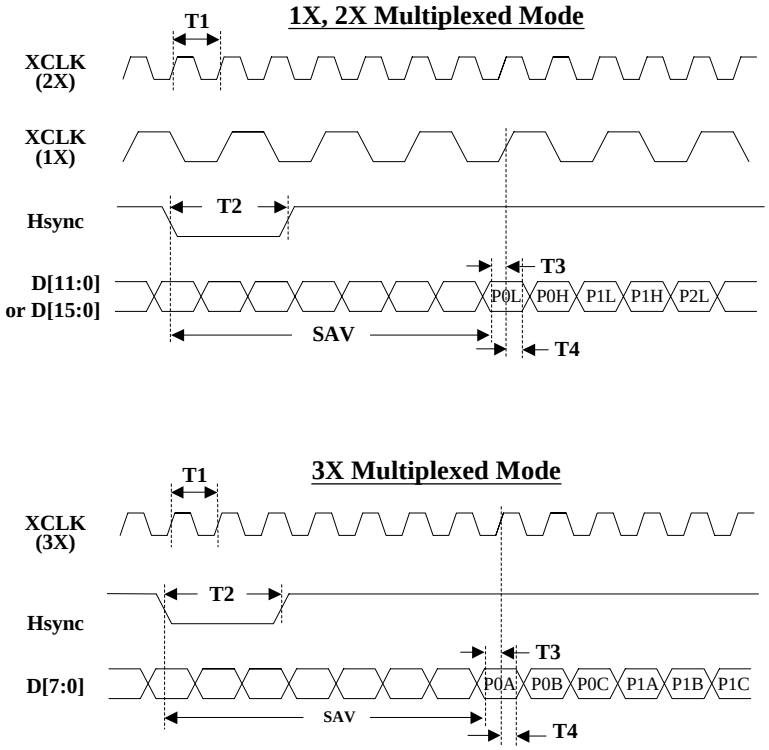
- **8-bit Multiplexed Mode**
  - RGB 15-bit: 5-5-5 over two bytes
  - RGB 16-bit: 5-6-5 over two bytes
  - RGB 24-bit: 8-8-8 over three bytes
  - YCrCb 16-bit: Cb, Y0, Cr, Y1, …(CCIR656 style)
- **12-bit Multiplexed Mode**
  - RGB 24-bit: 8-8-8 over two words
- **16-bit Multiplexed Mode**
  - RGB 24-bit: 8-8, 8x over two words
- **16-bit Non-multiplexed Mode**
  - RGB 15-bit: 5-5-5 each word
  - RGB 16-bit: 5-6-5 each word
  - YCrCb 16-bi : CbY0, CrY1, …(CCIR656 style)

Table 4. Input Data Format

IDF	0 16-bit RGB	1 16-bit YCrCb	2 24-bit RGB		3 15-bit RGB	4 24-bit RGB		5 24-bit RGB		6 24-bit RGB			7 16-bit RGB		8 15-bit RGB		9 16-bit YCrCb	
Pixel / Pin	P#	P#	P#A	P#B	P#	P#A	P#B	P#A	P#B	P#A	P#B	P#C	P#A	P#B	P#A	P#B	P#A	P#B
PD15	R4	Y7	G7	X	X													
PD14	R3	Y	G6	X	R4													
PD13	R2	Y5	G5	X	R3													
PD12	R1	Y4	G4	X	R2													
PD11	R0	Y3	G3	X	R1	G3	R7	G4	R7									
PD10	G5	Y2	G2	X	R0	G2	R6	G3	R6									
PD9	G4	Y1	G1	X	G4	G1	R5	G2	R5									
PD8	G3	Y0	G0	X	G3	G0	R4	B7	R4									
PD7	G2	Cr/Cb7	B0	R7	G2	B7	R3	B6	R3	B7	G7	R7	G2	R4	G2	x	Cr/Cb7	Y7
PD6	G1	Cr/Cb6	B6	R6	G1	B6	R2	B5	G7	B6	G6	R6	G1	R3	G1	R4	Cr/Cb6	Y6
PD5	G0	Cr/Cb5	B5	R5	G0	B5	R1	B4	G6	B5	G5	R5	G0	R2	G0	R3	Cr/Cb5	Y5
PD4	B5	Cr/Cb4	B4	R4	B4	B4	R0	B3	G5	B4	G4	R4	B4	R1	B4	R2	Cr/Cb4	Y4
PD3	B4	Cr/Cb3	B3	R3	B3	B3	G7	G0	R2	B3	G3	R3	B3	R0	B3	R1	Cr/Cb3	Y3
PD2	B3	Cr/Cb2	B2	R2	B2	B2	G6	B2	R1	B2	G2	R2	B2	G5	B2	R0	Cr/Cb2	Y2
PD1	B1	Cr/Cb1	B1	R1	B1	B1	G5	B1	R0	B1	G1	R1	B1	G4	B1	G4	Cr/Cb1	Y1
PD0	B0	Cr/Cb0	B0	R0	B0	B0	G4	B0	G1	B0	G0	R0	B0	G3	B0	G3	Cr/Cb0	Y0

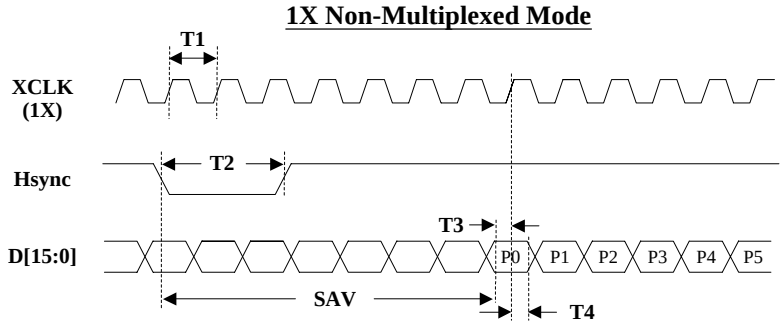
# denotes the pixel number

Each rising edge (or each rising and falling edge) of the XCLK signal will latch data from the video source device. The non-multiplexed and multiplexed input data formats are shown in Figure 7. The Pixel Data bus represents an 8, 12, or 16-bit multiplexed or 16-bit non-multiplexed data stream, which contains either RGB or YCrCb formatted data. In IDF settings of 0, 1 and 3, the input data rate is 1x the pixel clock frequency, and each 15/16-bit P# value will contain a complete pixel encoded in either RGB 5-6-5, 5-5-5 or YCrCb format. In IDF settings 2, 4, 5, 7, 8 and 9, the input data rate is 2x the pixel clock frequency, and each pair of P# values (for example, P#A and P#B) will contain a complete pixel, encoded as shown in
Table 4 above. When IDF = 6, the input data rate is 3x the pixel clock frequency, and each triplet of P# values (for example, P#A, P#B and P#C) will contain a complete pixel, encoded as shown in
Table 4 above. When the input data is YCrCb format, the color-difference data will be transmitted at half the data rate of the luminance data and the transmission sequence will be Cb, Y, Cr, Y. When IDF = 1, H and V sync signals can be embedded into the data stream and the embedded sync will be similar to CCIR656 convention. When IDF = 9, H and V sync signals can be embedded into the data stream. In this mode, the embedded sync will follow CCIR656 convention, and the first byte of the "video timing reference code" will be assumed to occur when a Cb sample occurs if the video stream is continuous.



SAV = Start of Active Video (see Rx7 and Rx1C[3])

Figure 7. Multiplexed Input Interface Protocol



SAV = Start of Active Video (see Rx7 and Rx1C[3])

Figure 8. Non-Multiplexed Input Interface Protocol

Video Standards

The VT1622 and VT1622M can be configured in 3 kinds of output modes (interlaced, non-interlaced and progressive), which are selected by the OUT_MODE[1:0] register bits (Rx4[3:2]). In addition, the both TV encoders can generate output video signals as S-Video, composite, YCbCr, SCART (RGB), and VGA-style RGB for the interlaced and non-interlaced output modes, and YPbPr or RGB for progressive output mode.

While in interlaced or non-interlaced output mode, there are several bits (VOS, LINE_SEL, PAL_N, PAL_Nc) that control the generation of various video standards. They allow the generation of all NTSC and PAL video standards and control the specific encoding process parameters. Other registers may also need to be modified to meet all the video parameters of the particular video standard. The difference between interlaced and non-interlaced output mode is that non-interlaced output mode always outputs the odd field. For NTSC, that is 262 lines per frame and 60 frames per second, and for PAL, it is 312 lines per frame and 50 frames per second. Interlaced and non-interlaced video timing diagrams are illustrated from Figure 9 to Figure 17, which summarize all the common video standards. Composite and S-video outputs are supported in either NTSC or PAL format. Figure 18 through Figure 23 illustrate composite and S-video output waveforms for different color bars.

While in progressive output mode, the LINE_SEL register bit controls whether the output lines are 525 lines or 625 lines per frame and whether the frame rate is 60 Hz or 50 Hz. The progressive analog component signal is comprised of three signals, analog RGB or YPbPr, which are compliant with EIA770-1 and EIA770-2. Progressive video timing diagrams are illustrated from Figure 24 to Figure 25.

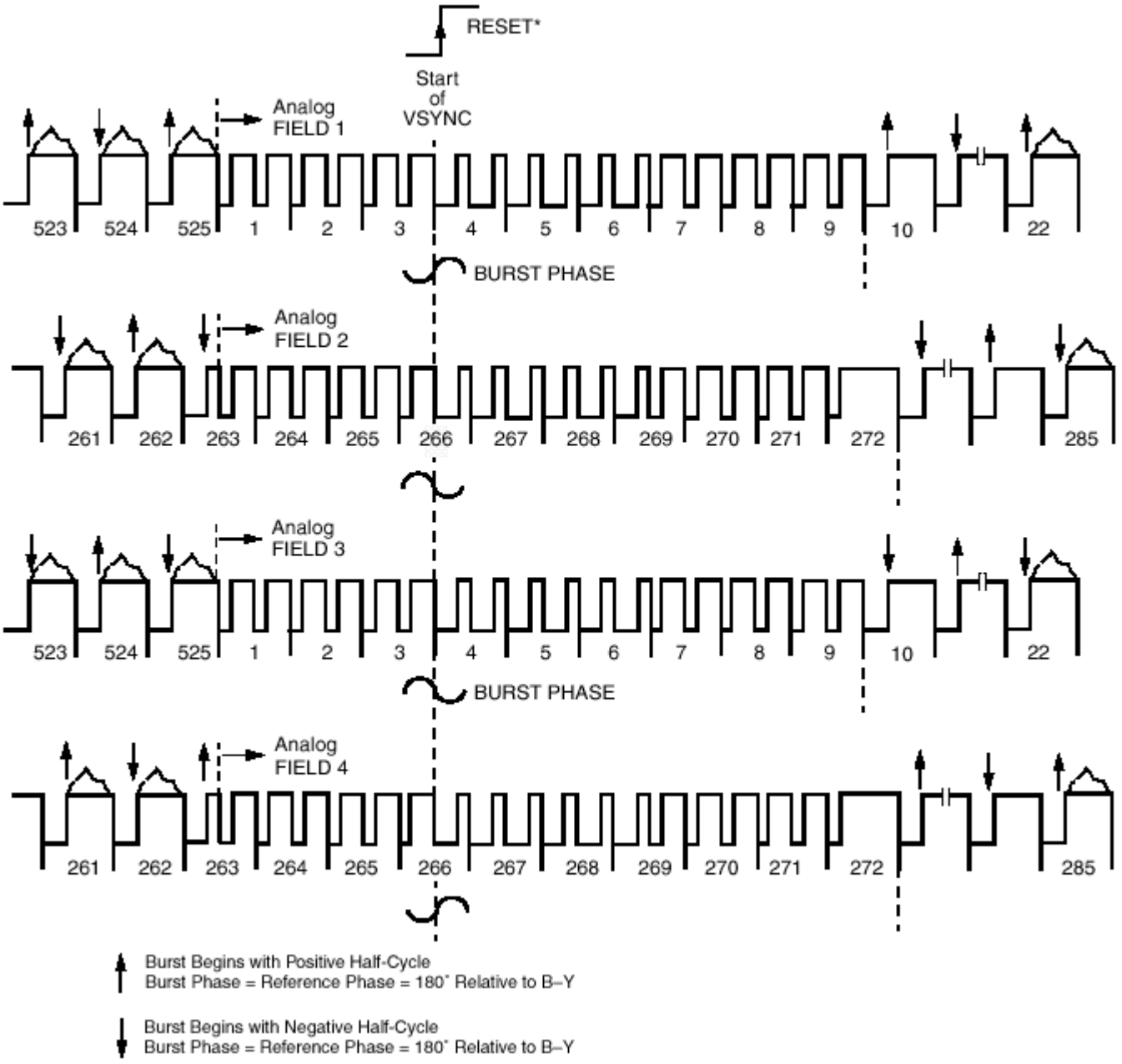


Figure 9. Interlaced 525-Line (NTSC) Video Timing

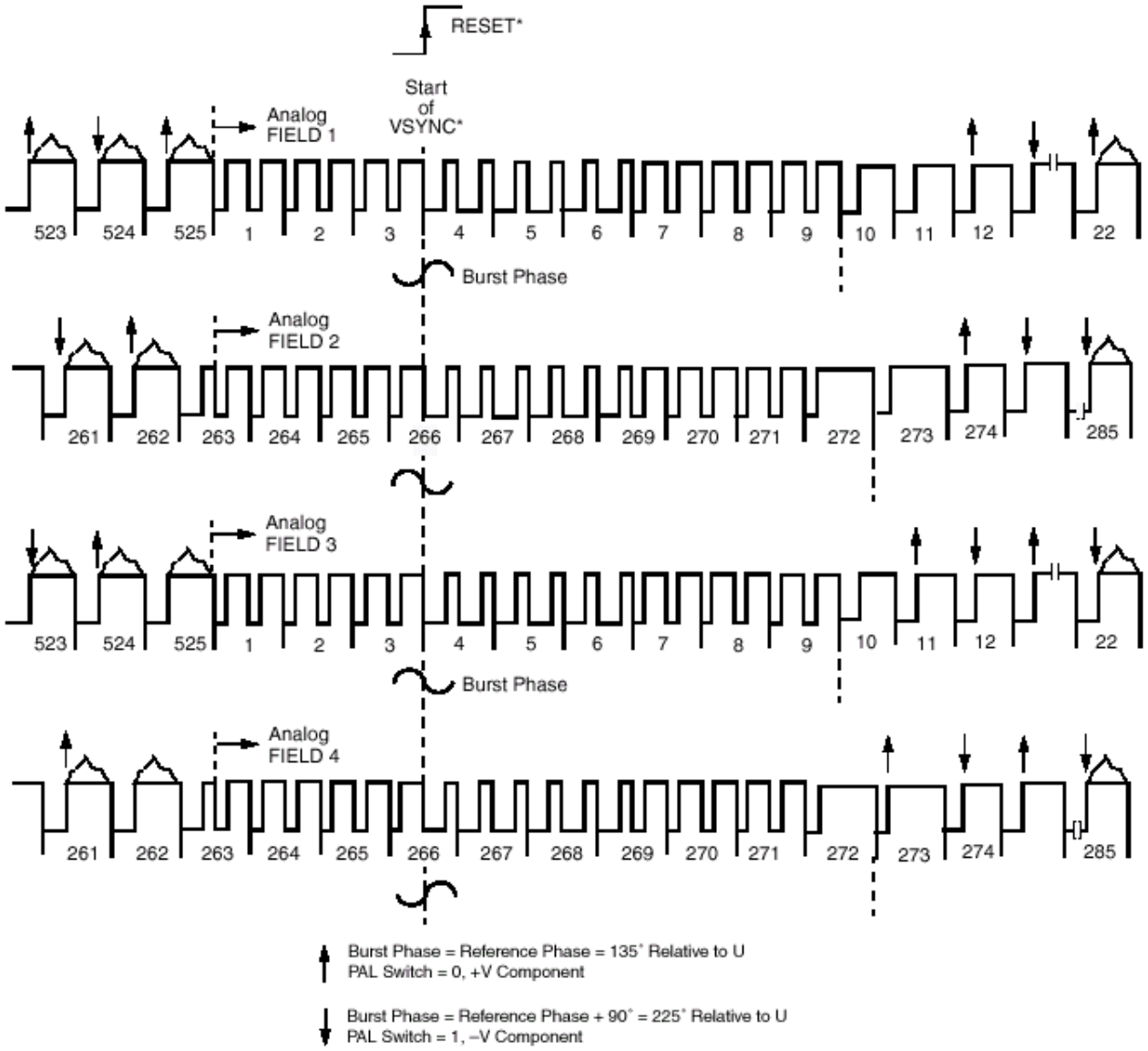


Figure 10. Interlaced 525-Line (PAL-M) Video Timing

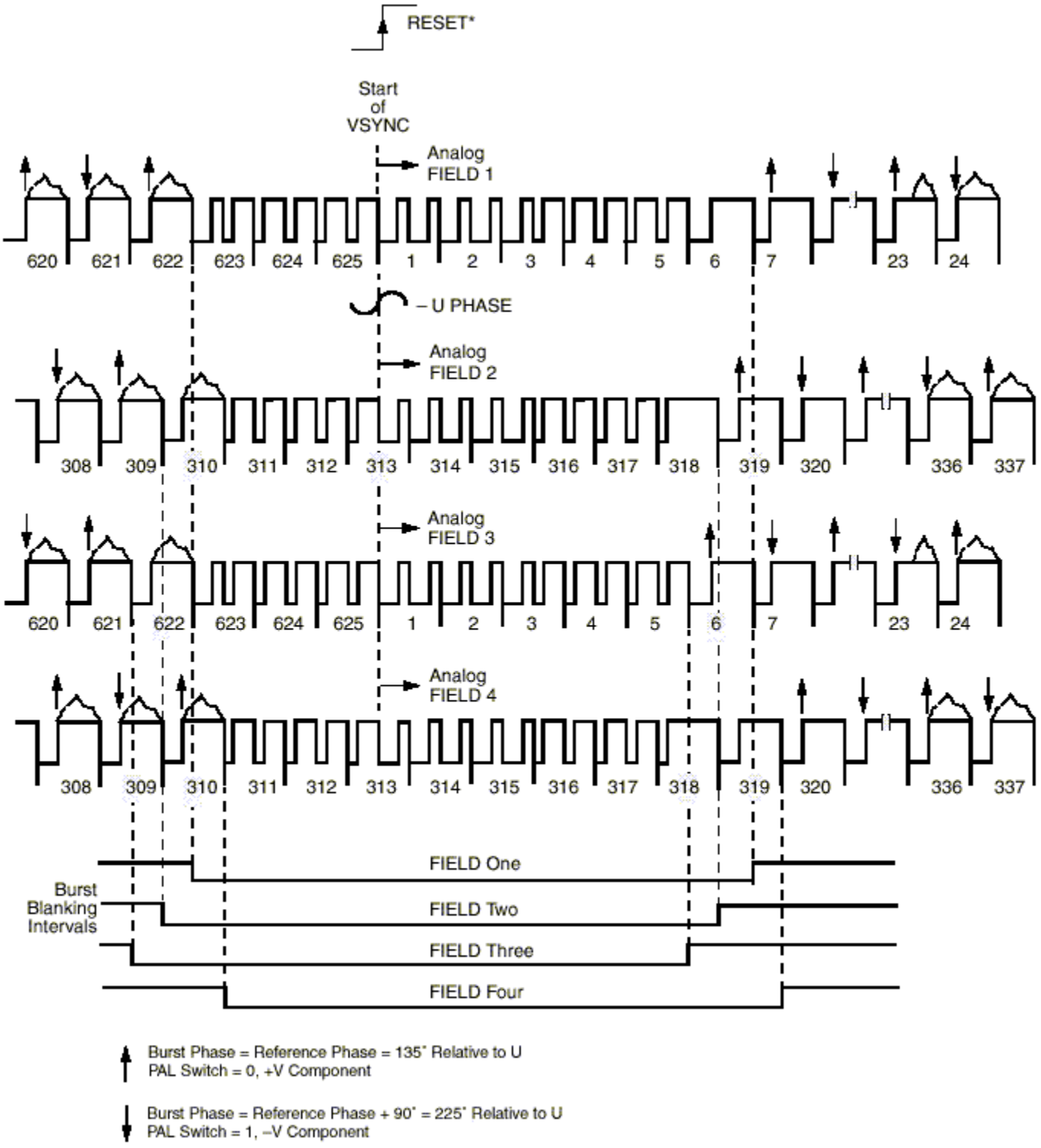


Figure 11. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 1-4)

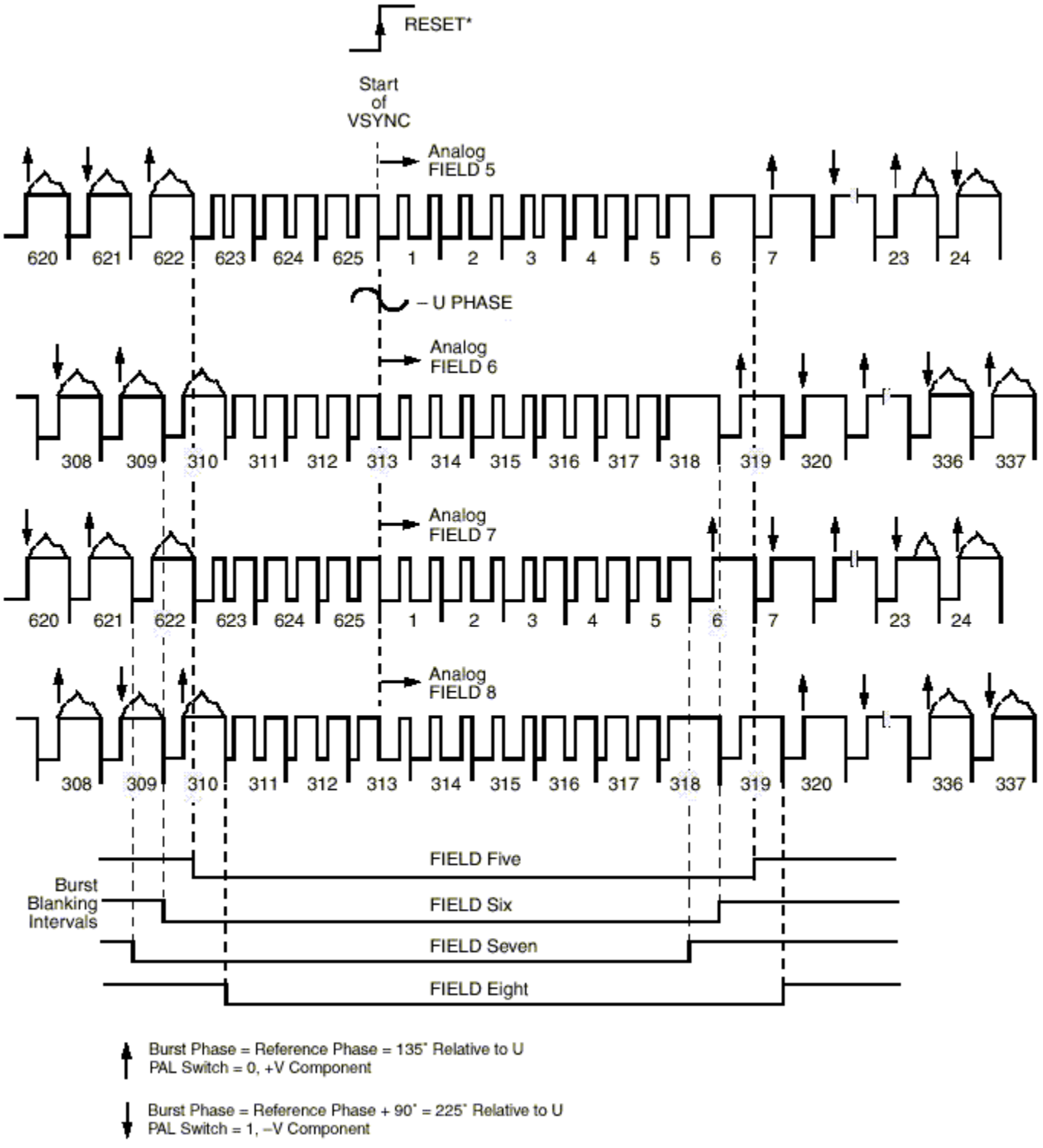


Figure 12. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 5-8)

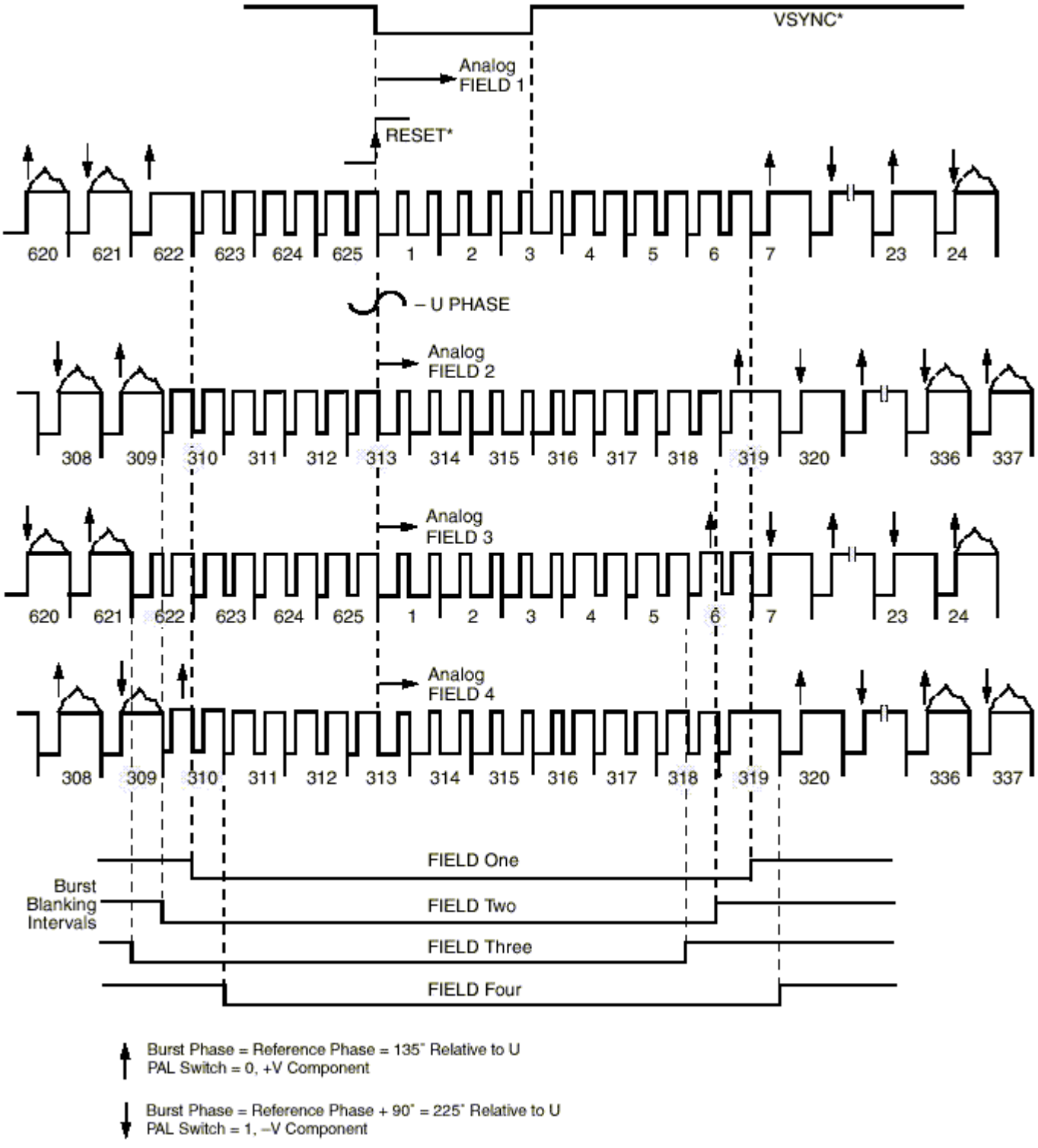


Figure 13. Interlaced 625-Line (PAL-N) Video Timing (Fields 1-4)

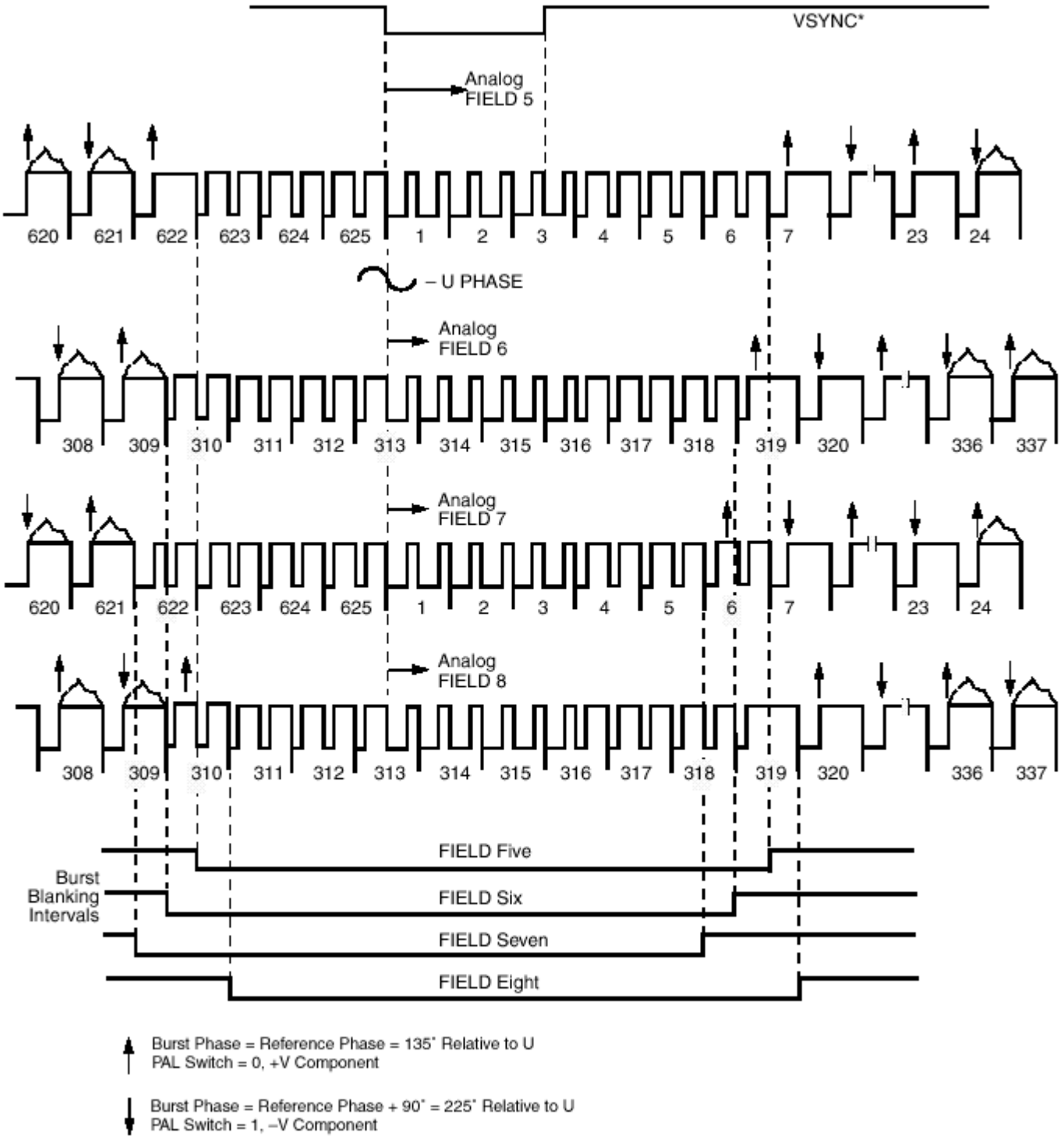


Figure 14. Interlaced 625-Line (PAL-N) Video Timing (Fields 5-8)

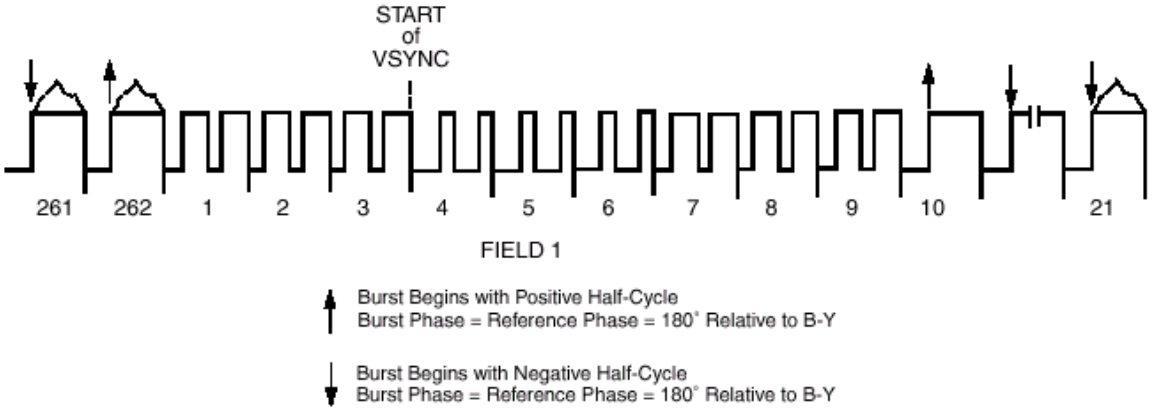


Figure 15. Non-interlaced 262-Line (NTSC) Video Timing

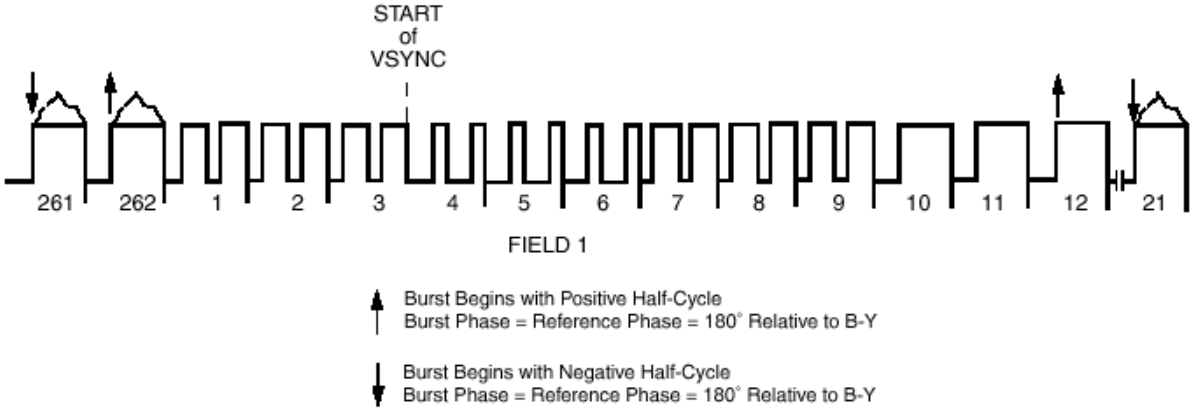


Figure 16. Non-interlaced 262-Line (PAL-M) Video Timing

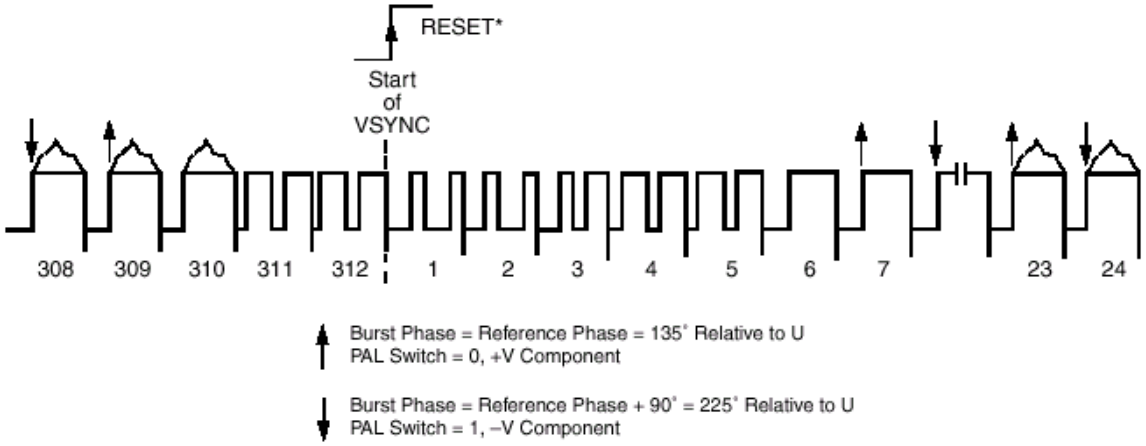


Figure 17. Non-interlaced 312-Line (PAL-B, D, G, H, I, N, Nc) Video Timing

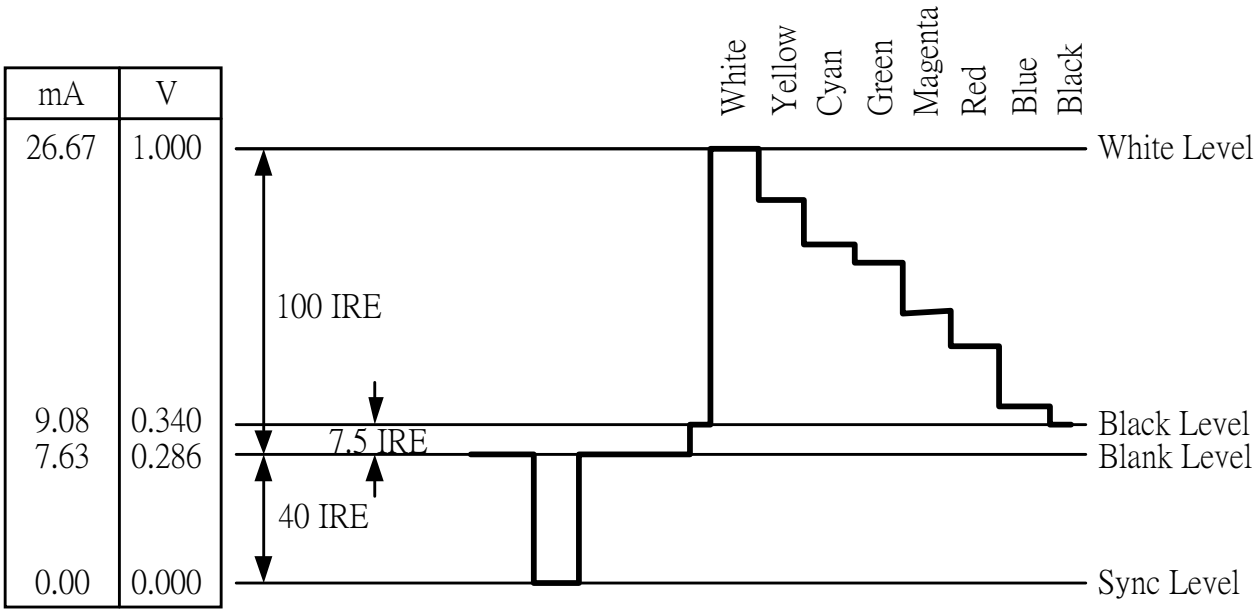


Figure 18. 525-Line (NTSC/PAL-M) Y (Luma) Video Test Pattern Waveform

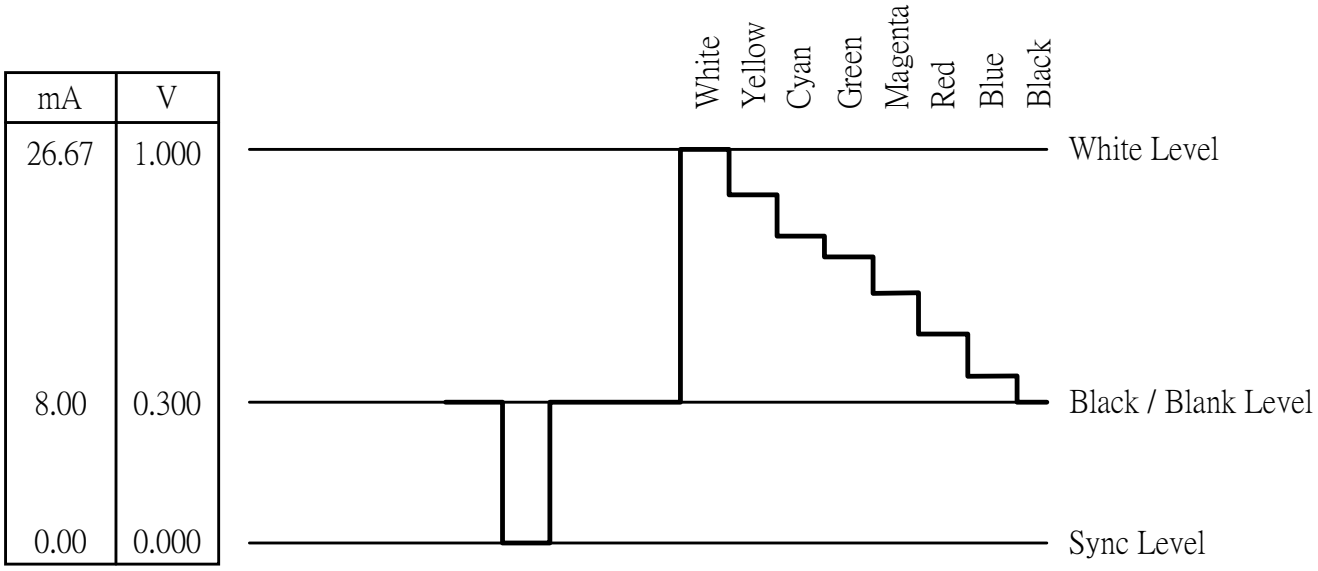


Figure 19. 625-Line (PAL-B, D, G, H, I, N, Nc) Y (Luma) Test Pattern Waveform

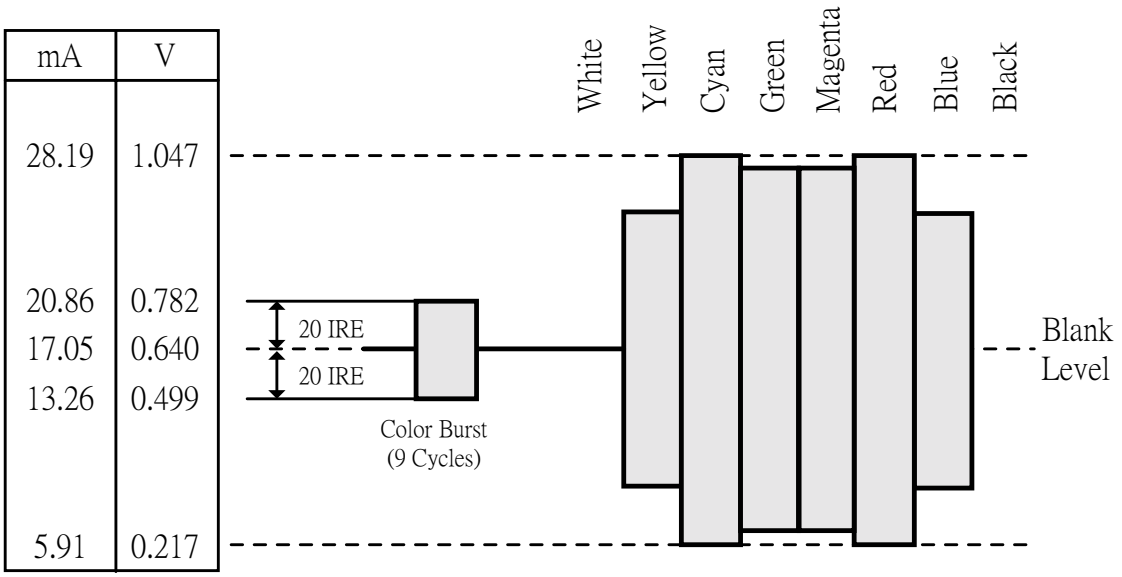


Figure 20. 525-Line (NTSC/PAL-M) C (Chroma) Video Test Pattern Waveform

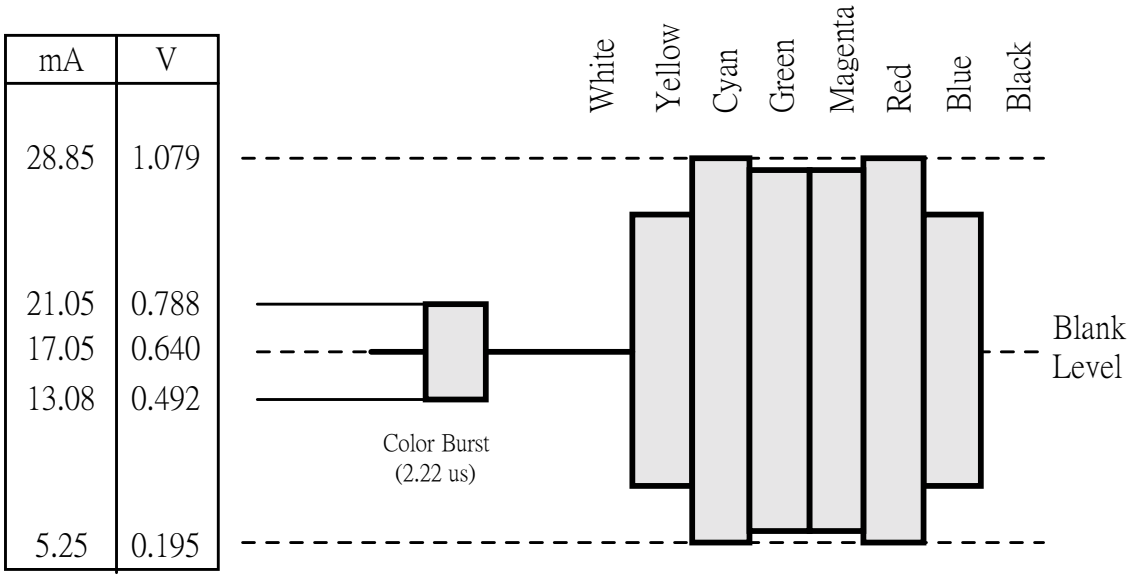


Figure 21. 625-Line (PAL-B, D, G, H, I, N, Nc) C (Chroma) Video Test Pattern Waveform

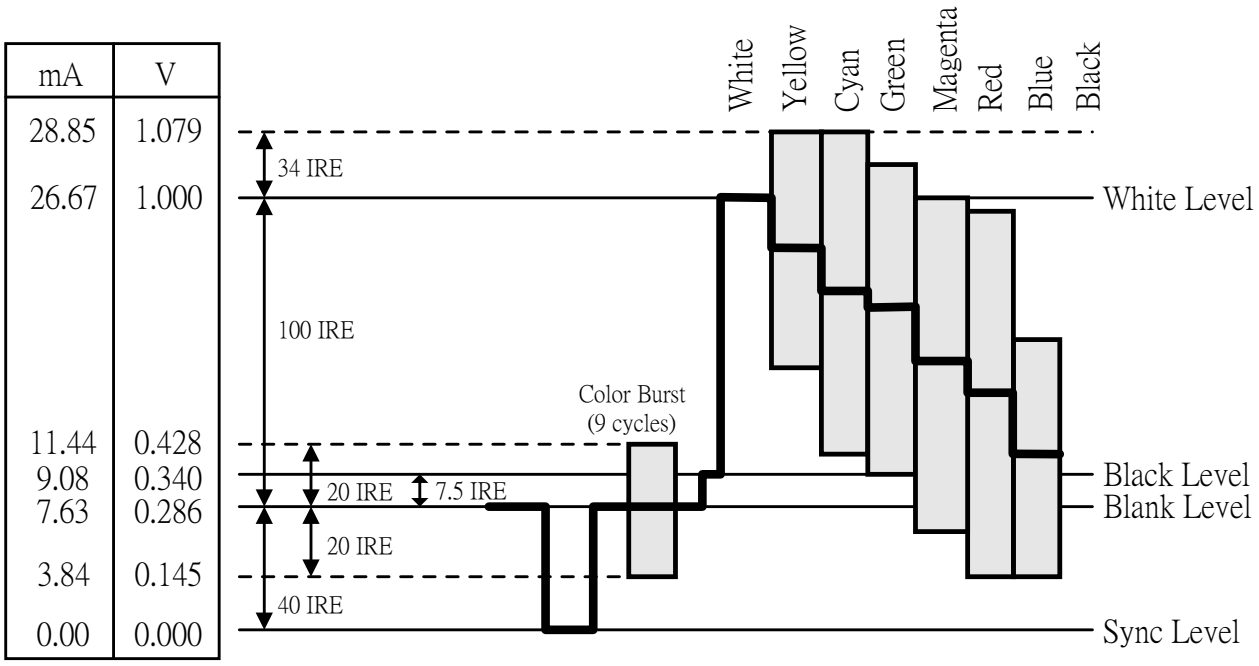


Figure 22. Composite 525-Line (NTSC/PAL-M) Video Test Pattern Waveform

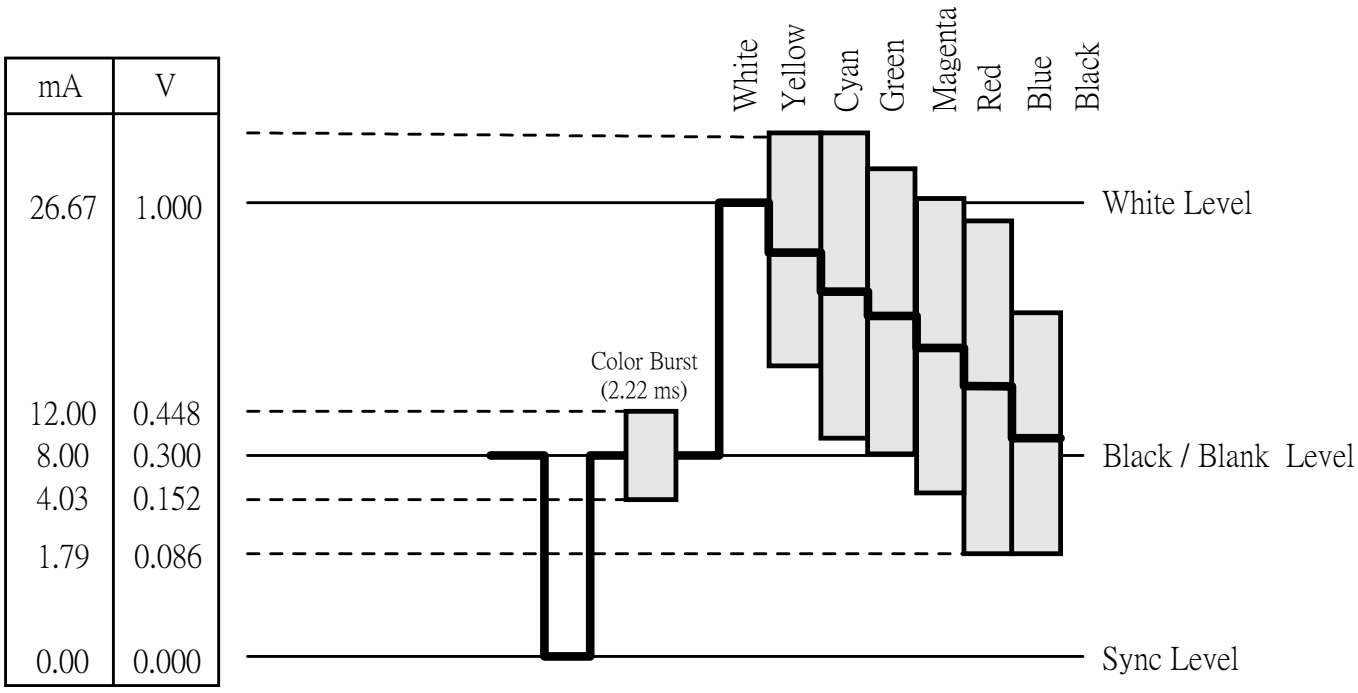


Figure 23. Composite 625-Line (PAL-B, D, G, H, I, N, Nc) Video Test Pattern Waveform

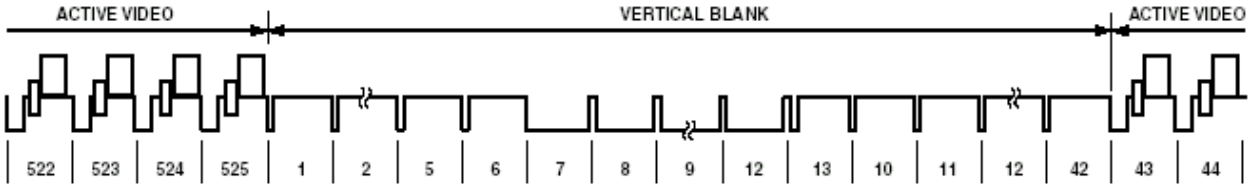


Figure 24. 525-Line Progressive Video Timing

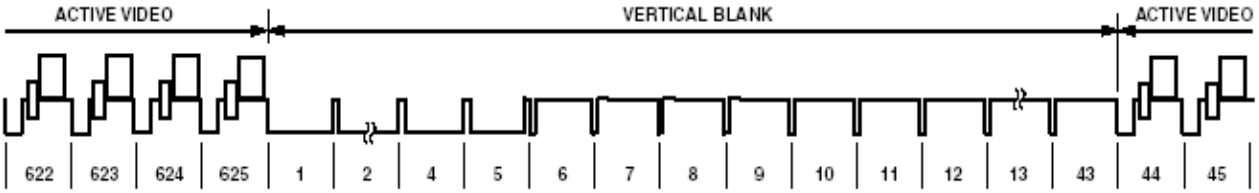


Figure 25. 625-Line Progressive Video Timing

Luminance and Chrominance Filter Option

The VT1622 and VT1622M contain a set of luminance and chrominance filters to provide a controllable bandwidth output on both composite and S-video outputs. The coefficients of the filter are selected via the YBW[2:0] and CBW[2:0] register bits. The filter selection principle is illustrated in Table 5 and Table 6 and the filter frequency response is illustrated in Figure 26 through Figure 31.

Table 5. Luminance Filter

Filter	Rx03[7:5] YBW[2:0]	TVCLK (MHz)	3dB Bandwidth (MHz)
Lowpass (NTSC)	000	21	2.28
Lowpass (NTSC)	001	26	2.28
Lowpass (NTSC)	010	33	2.28
Notch (NTSC)	011	26	2.28/3.58/4.88
Lowpass (PAL)	100	21	3.13
Lowpass (PAL)	101	26	3.13
Lowpass (PAL)	110	32	3.13
Lowpass (ALL)	111	26	4.43

Table 6. Chrominance Filter

Filter	Rx03[4:2] CBW[2:0]	TVCLK (MHz)	3dB Bandwidth (MHz)
Lowpass	000	21	0.6
Lowpass	001	26	0.6
Lowpass	010	33	0.6
Lowpass	111	26	4.43

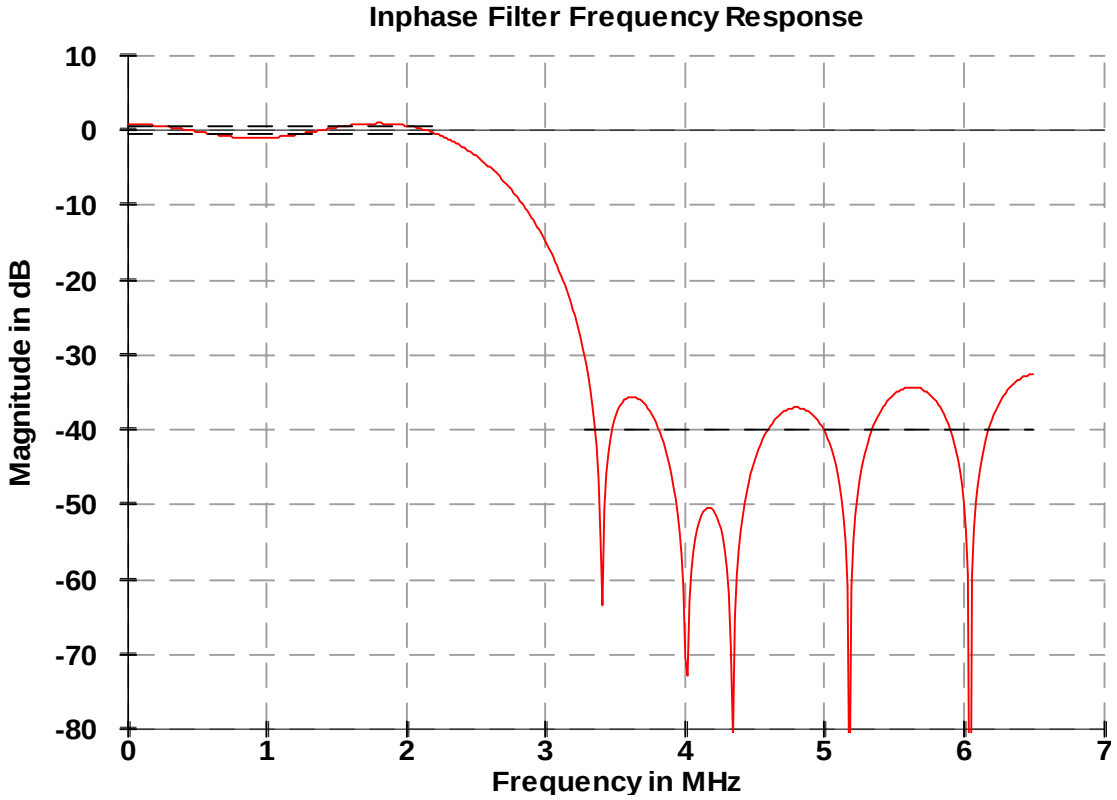


Figure 26. Low-Pass Luma Filter NTSC

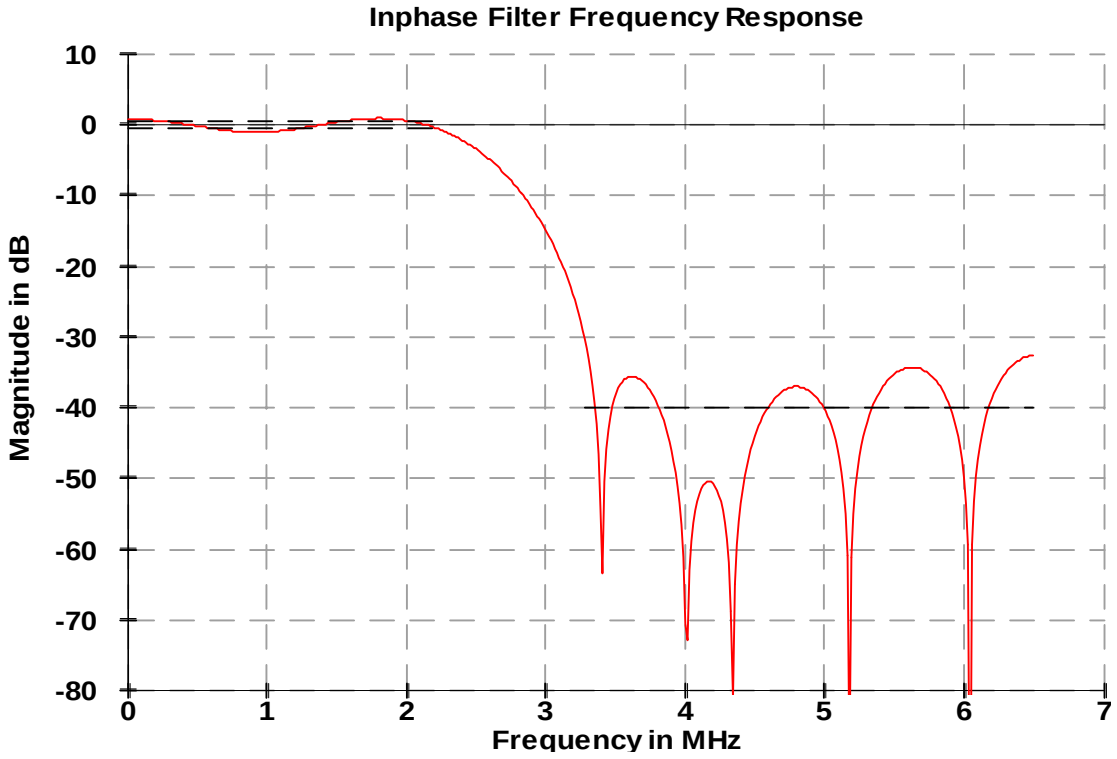


Figure 27. Low-Pass Luma Filter PAL

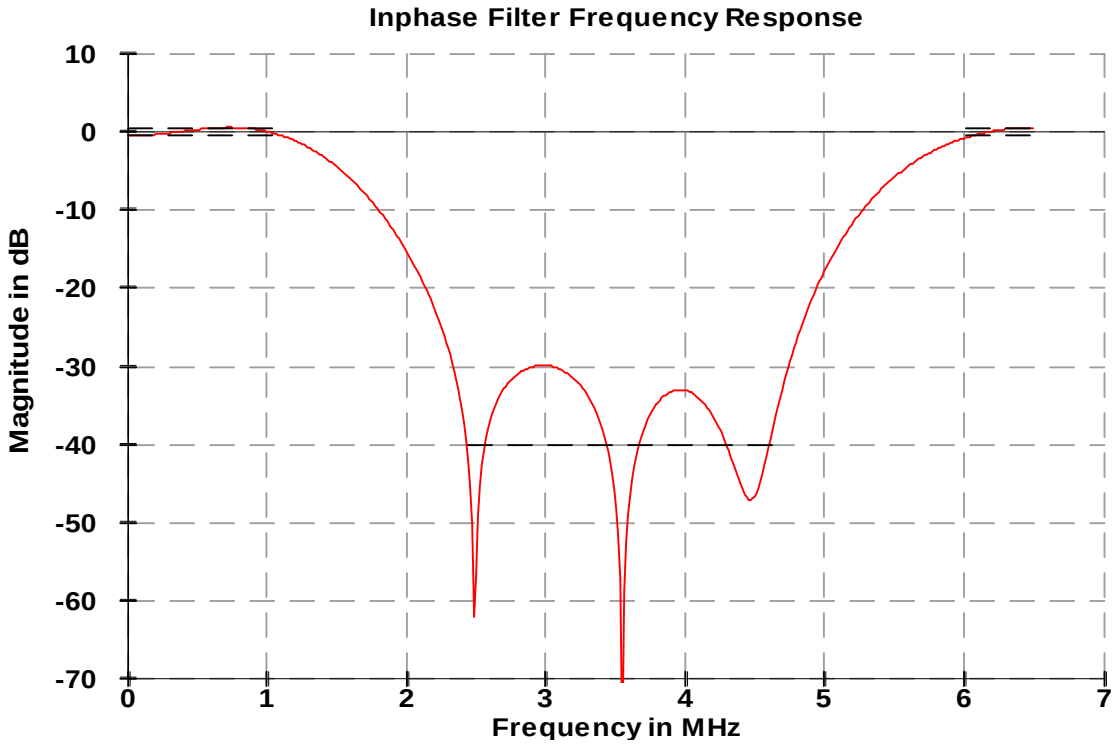


Figure 28. Notch Luma Filter NTSC

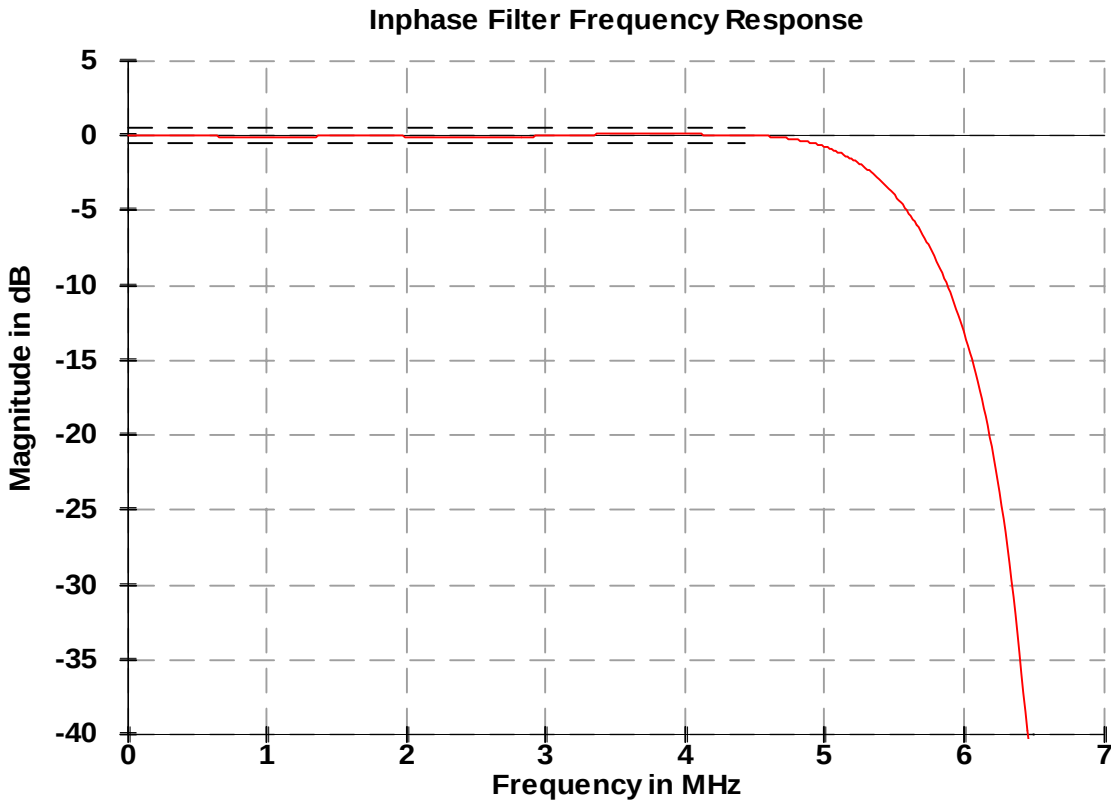


Figure 29. Wide Bandwidth Luma Filter

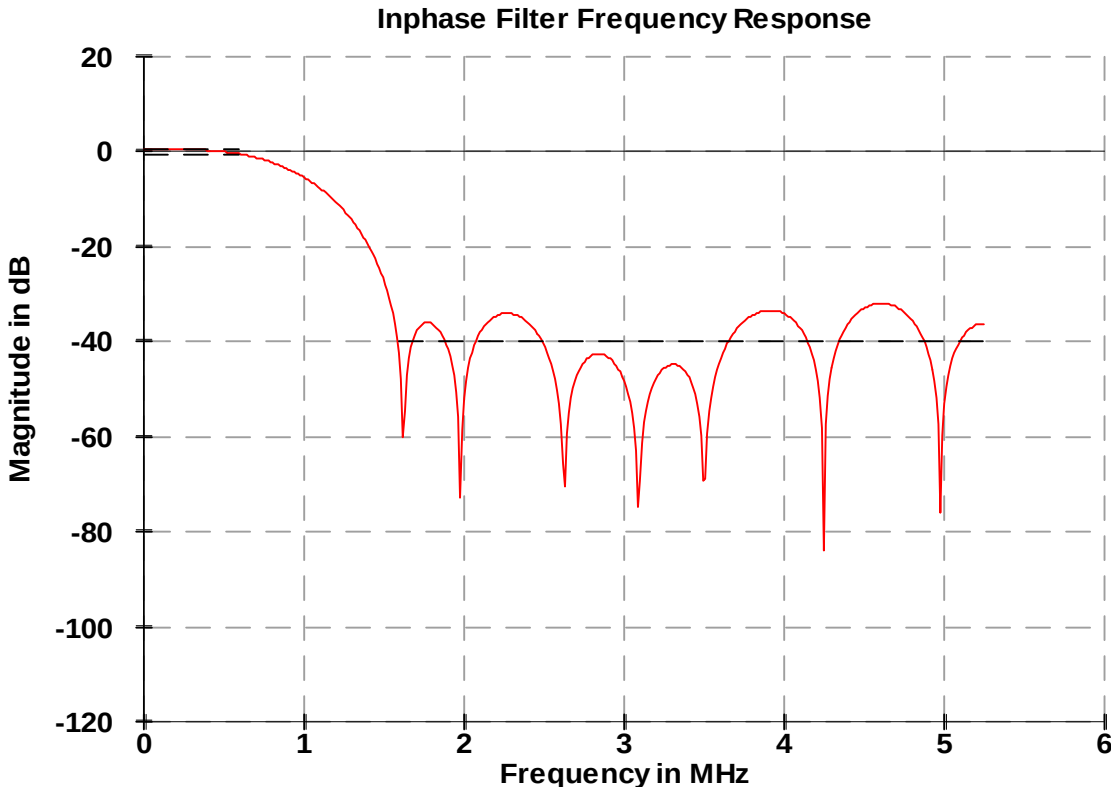


Figure 30. Lowpass Chroma Filter

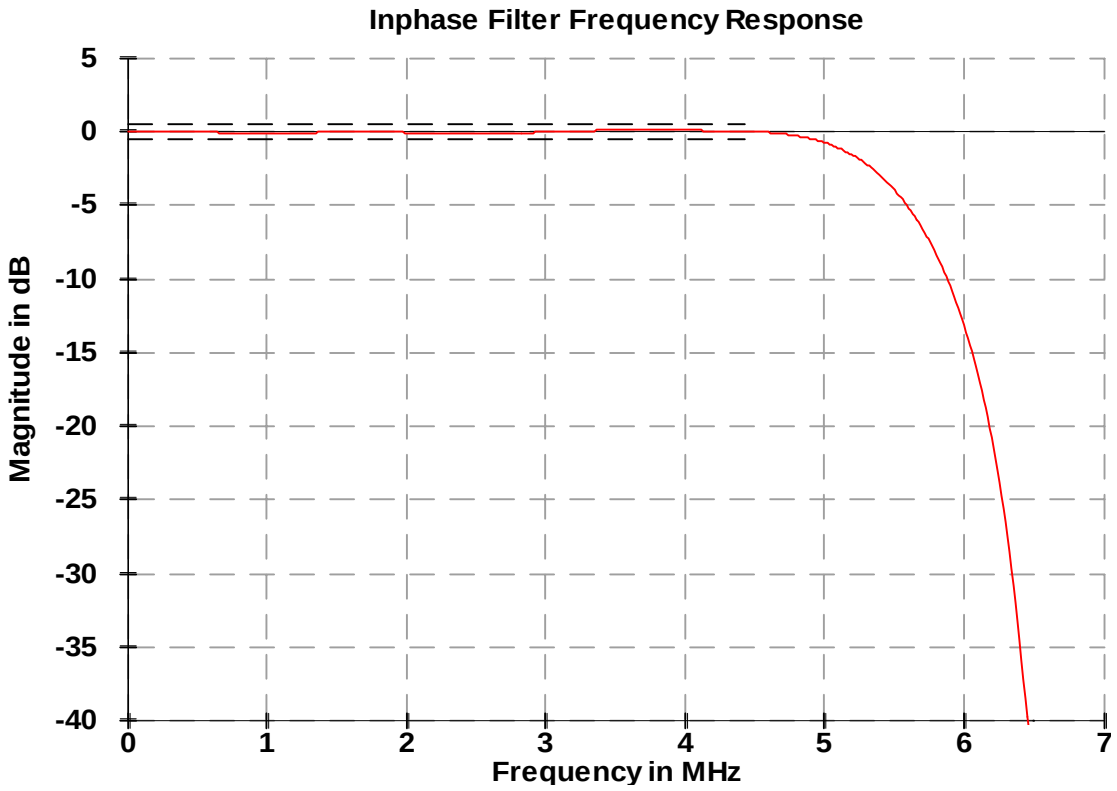


Figure 31. Wide Bandwidth Chroma Filter

Color Bar Test Pattern Generator

The VT1622 and VT1622M have a built-in color bar generator that generates the 75% amplitude and 100% saturation EIA colors for the NTSC and PAL standards. While in color bar mode, input pixel data is ignored.

Subcarrier Generation

The VT1622 and VT1622M use a 32-bit-word to synthesize the subcarrier. The value of the sub-carrier increment required to generate the desired subcarrier frequency is found with the following equations:

NTSC: $FSCI[31:0] = 2^{32} * [455 / (2 * H\_Total)]$
-or- $FSCI[31:0] = (int) (2^{32} * 3.579545 / F_{clk})$

PAL: $FSCI[31:0] = 2^{32} * [(1135/4 + 1/625) / (H\_Total)]$
-or- $FSCI[31:0] = (int) (2^{32} * 4.43361875 / F_{clk})$

where H_Total is the number of output pixels per line and F_{clk} is the encoder clock frequency if FSCI_ADJ_EN = 0 and F_{clk} = 14.31818 MHz if FSCI_ADJ_EN = 1. This allows the generation of any desired subcarrier for any desired video standard. The 32-bit subcarrier increment FSCI[31:0] must be loaded by the serial interface before the subcarrier can be enabled. In order to prevent any residual errors from accumulating and maintain the correct SCH phase, the subcarrier is reset every two lines for the NTSC standard and every field for the PAL standard.

Burst Generation

Subcarrier burst generation is a function of the video standard (e.g. NTSC or PAL), the subcarrier frequency increment (FSCI), and the burst horizontal begin (TBURST_START) and end (TBURST_END) register settings. The burst will automatically be blanked during horizontal sync to prevent invalid sync pulses from being generated. Burst blanking is automatically controlled by the selected video format and the burst amplitude can be programmed by the BURST_AMP setting.

Power Down Mode

The VT1622 and VT1622M can be powered down by programming their registers and each of the DACs can be powered down independently if the DAC is not used. All register contents are maintained when the VT1622 and VT1622M are in power down mode.

Macrovision Anti-Copy Protection

The VT1622M implements the Macrovision 7.1 anti-copy protection process and Macrovision 1.0 AGC copy protection with 525p progressive scan output. This process changes the encoded output of the NTSC/PAL signals to inhibit recording on VCR devices while not affecting viewing on a TV. All parameters that control the anti-copy protection process are fully programmable but are not documented in this data sheet per legal requirements of Macrovision Corporation.

Display Modes

The VT1622 and VT1622M are designed to accept any input resolution from 320x200 up to 1024x768 by setting the TV CRTC registers, the scaling registers and the TV timing registers. The TV CRTC registers include the GH_TOTAL, GV_TOTAL, GH_ACTIVE, SH_TOTAL, TH_TOTAL, and TH_ACTIVE register bits. These registers decide the horizontal active and total pixels, total lines for the input data, and the output horizontal active and total pixels for the TV display after scaling. The two TV encoder chips can scale down or up the input images in any size from 1.5 to 0.5 factors in the vertical and horizontal directions by setting the VSCAL_FAC and HSCAL_FAC register bits. The two TV encoder chips do not contain a frame memory. Therefore, their output frame rate must be synchronous to the input frame rate. To accomplish this, the input total, output total, scaling ratio, and the pixel frequency must be set to proper values for a corresponding relationship.

Because the pixel frequency varies from every input resolution, and further, the TV timing is fixed, we must program different values in the TV timing registers for every input resolution. The TV timing registers include the THSYNC_WIDTH, TBURST_START, TBURST_END, TVIDEO_START, and TVIDEO_END register bits. Table 7 lists the display modes for the NTSC and PAL TV standards.

Table 7. Display Modes

Mode	Output Standard	Input Active Video	Input Total	Scaling Ratio	V % Overscan	Pixel Clock
0	NTSC	1024x768	1144x1050	1/2	-20	72.000000
1	NTSC	1024x768	1176x975	7/13	-14	68.727272
2	NTSC	1024x768	1160x945	5/9	-11	65.706293
3	NTSC	1024x768	1232x900	7/12	-7	66.461538
4	NTSC	1024x768	1200x840	5/8	0	60.419580
5	NTSC	1024x768	1200x805	15/23	4	57.902097
6	PAL	1024x768	1160x1125	5/9	-26	65.250000
7	PAL	1024x768	1200x1075	25/43	-22	64.500000
8	PAL	1024x768	1400x1000	5/8	-17	70.000000
9	PAL	1024x768	1200x925	25/37	-10	55.500000
10	PAL	1024x768	1400x875	5/7	-5	61.250000
11	PAL	1024x768	1200x825	25/33	1	49.500000
12	NTSC	800x600	1040x840	5/8	-22	52.363637
13	NTSC	800x600	1080x805	15/23	-18	52.111888
14	NTSC	800x600	1064x750	7/10	-13	47.832169
15	NTSC	800x600	960x700	3/4	-6	40.279720
16	NTSC	800x600	1080x665	15/19	-1	43.048951
17	NTSC	800x600	920x630	5/6	4	34.741258
18	PAL	800x600	960x875	5/7	-25	42.000000
19	PAL	800x600	1000x800	25/32	-18	40.000000
20	PAL	800x600	920x750	5/6	-13	34.500000
21	PAL	800x600	1000x700	25/28	-7	35.000000
22	PAL	800x600	1000x650	25/26	0	32.500000
23	PAL	800x600	896x625	1/1	4	28.000000
24	NTSC	640x480	728x675	7/9	-22	29.454545
25	NTSC	640x480	800x630	5/6	-17	30.209790
26	NTSC	640x480	784x600	7/8	-13	28.195805
27	NTSC	640x480	720x560	15/16	-6	24.167832
28	NTSC	640x480	712x525	1/1	0	22.405594
29	NTSC	640x480	840x500	21/20	5	25.174825
30	PAL	640x480	720x750	5/6	-30	27.000000
31	PAL	640x480	800x700	25/28	-25	28.000000
32	PAL	640x480	800x650	25/26	-20	26.000000
33	PAL	640x480	840x625	1/1	-17	26.250000
34	PAL	640x480	800x600	25/24	-13	24.000000
35	PAL	640x480	840x500	5/4	4	21.000000
36	NTSC	640x400	840x600	7/8	-27	30.209790
37	NTSC	640x400	840x525	1/1	-17	26.433566
38	NTSC	640x400	840x420	5/4	4	21.146853
39	PAL	640x400	1008x625	1/1	-30	31.500000
40	PAL	640x400	1000x500	5/4	-13	25.000000
41	NTSC	720x400	936x525	1/1	-16	29.454545
42	NTSC	720x400	945x420	5/4	4	23.790210
43	PAL	720x400	1116x625	1/1	-30	34.875000
44	PAL	720x400	1080x500	5/4	-13	27.000000
45	NTSC	512x384	784x525	1/1	-20	24.671329
46	NTSC	512x384	800x420	5/4	0	20.139860
47	PAL	512x384	840x625	1/1	-33	26.250000
48	PAL	512x384	840x500	5/4	-17	21.000000

Clock Frequency

A crystal must be present between the XI and XO pins for generating a 14.31818 MHz reference clock for the PLL (Phase Lock Loop). In master clock mode, the PLL uses this clock as a reference. In slave clock mode, the PLL uses the clock from the XCLK pin as a reference clock. The PLL generates 2 clocks: One is the pixel clock output on the PCLK pin (for master mode use only) and the other is the pixel clock used by the Encoder engine. The frequency is calculated using the following formula:

$$F_{CLK} = F_{REFCLK} * N / (D*P)$$

The settings of the PLL control registers are listed in Table 8 (D, P, and P2 are programmed in increments of 0.5; N and R are programmed in increments of 1.0).

Table 8. Master Clock Mode Clock Settings

Mode	Pixel (MHz)	D	N	P	R	P2	Rx12 (Bits 7:5=R, 4:0=P2)	Rx13 (D)	Rx14 (N)	Rx15 (Bits 6:2=P, 1:0=N[9:8])
0x1	72.000000	3.5	88	2.5	3	5.5	6B	07	58	14
1x1	68.727272	2	48	2.5	1	5	2A	04	30	14
2x1	65.706293	18	413	2.5	7	5	EA	24	9D	15
3x1	66.461538	13.5	376	3	7	6	EC	1B	78	19
4x1	60.419580	25.5	538	2.5				33	1A	16
5x1	57.902097	26.5	643	3				35	83	1A
6x1	65.250000	14	319	2.5	7	5	EA	1C	3F	15
7x1	64.500000	17.5	473	3	7	6	EC	23	D9	19
8x1	70.000000	4.5	110	2.5	5	5	AA	09	6E	14
9x1	55.500000	15	407	3.5	7	6	EC	1E	97	1D
10x1	61.250000	4.5	77	2	3	3.5	67	09	4D	10
11x1	49.500000	17.5	242	2	6	3	C6	23	F2	10
12x1	52.363637	2.5	64	3.5	2	7	4E	05	40	1C
13x1	52.111888	21.5	313	2	7	4	E8	2B	39	11
14x1	47.832169	6.5	152	3.5				0D	98	1C
15x1	40.279720	6.5	128	3.5				0D	80	1C
16x1	43.048951	30	451	2.5	7	4	E8	3C	C3	15
17x1	34.741258	21.5	313	3	7	4	E8	2B	39	19
18x1	42.000000	7.5	110	2.5	3	4	68	0F	6E	14
19x1	40.000000	4.5	88	3.5	3	5	6A	09	58	1C
20x1	34.500000	17.5	253	3	7	4	E8	23	FD	18
21x1	35.000000	1.5	33	4.5	0	6	0C	03	21	24
22x1	32.500000	10.5	286	6	7	7.5	EF	15	1E	31
23x1	28.000000	22.5	572	6.5	5	7	AE	2D	3C	36
24x1	29.454545	17.5	216	3	0	4	08	23	D8	18
25x1	30.209790	13	192	3.5	7	5	EA	1A	C0	1C
26x1	28.195805	5	128	6.5	6	8	D0	0A	80	34
27x1	24.167832	30	557	5.5	7	6	EC	3C	2D	2E
28x1	22.405594	9.5	223	7.5	7	7.5	EF	13	DF	3C
29x1	25.174825	6.5	160	7	3	8	70	0D	A0	38
30x1	27.000000	2.5	66	7	0	9	12	05	42	38
31x1	28.000000	12.5	220	4.5	5	6	AC	19	DC	24
32x1	26.000000	22.5	286	3.5				2D	1E	1D
33x1	26.250000	6	110	5	1	6	2C	0C	6E	28
34x1	24.000000	7.5	176	7	3	8	70	0F	B0	38
35x1	21.000000	2.5	44	6	1	6	2C	05	2C	30
36x1	30.209790	6.5	96	3.5	4	3.5	87	0D	60	1C
37x1	26.433566	6.5	96	4	4	4	88	0D	60	20
38x1	21.146853	2.5	48	6.5	1	6.5	2D	05	30	34
39x1	31.500000	2	44	5	1	5	2A	04	2C	28
40x1	25.000000	3.5	55	4.5	2	4.5	49	07	37	24
41x1	29.454545	2.5	36	3.5	0	3.5	07	05	24	1C
42x1	23.790210	2.5	54	6.5	2	6.5	4D	05	36	34
43x1	34.875000	14	341	5	7	5	EA	1C	55	29
44x1	27.000000	7	132	5				0E	84	28
45x1	24.671329	2.5	56	6.5	2	6.5	4D	05	38	34
46x1	20.139860	3.5	64	6.5	2	6.5	4D	07	40	34
47x1	26.250000	2	44	6	1	6	2C	04	2C	30
48x1	21.000000	2.5	44	6	1	6	2C	05	2C	30

DESIGN GUIDELINES

PC Board Layout Considerations

This section focuses on PCB design considerations for the VIA VT1622 and VT1622M TV Encoder. By using these chips, PC images can be easily displayed on a TV set. A typical TV out connection between the VT1622/VT1622M and a VIA VT8605 UMA North Bridge chip is shown in Figure 32.

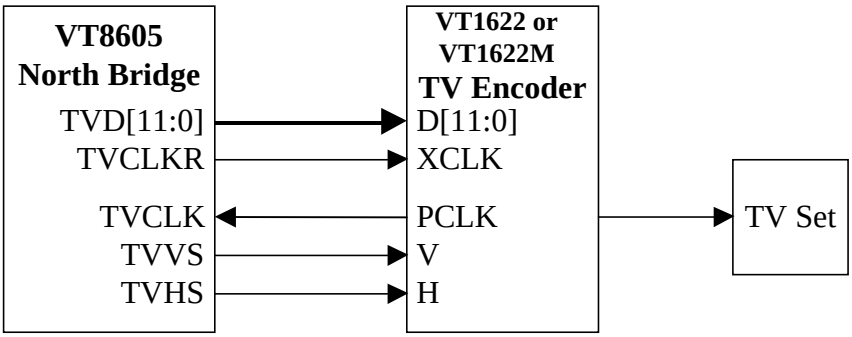


Figure 32. Interconnect with PM133 Chipset VT8605 North Bridge

Component Placement

Components associated with the VT1622 and VT1622M TV encoder should be placed as close as possible to their respective pins. The following discussion will describe guidelines on how to connect critical pins as well as the guidelines for the placement and layout of components associated with these pins.

Power Supply Decoupling

Optimum power supply decoupling is accomplished by placing a 0.1uF ceramic capacitor next to each of the power supply pins as shown in Figure 33. These capacitors should connect as close as possible to their respective power and ground pins using short, wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the VT1622 and VT1622M ground pins, in addition to ground vias. See Figure 33 for details.

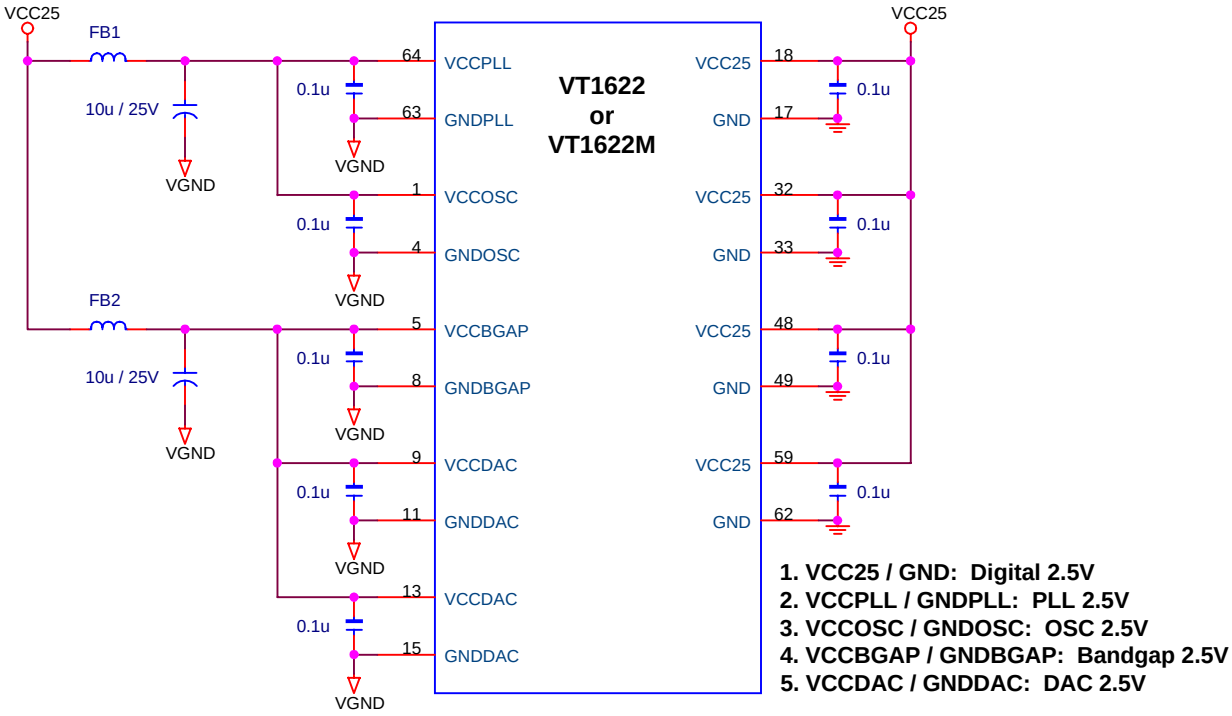


Figure 33. Decoupling Capacitors Arrangement

Ground Pins

The analog and digital grounds of the VT1622 and VT1622M should connect to different ground planes to provide low impedance return paths with the supply currents. Whenever possible, each of the VT1622 and VT1622M ground pins should connect directly to their respective decoupling capacitor ground lead, then connect to the ground plane through a ground via. Short and wide traces should be used to minimize lead inductance. See Figure 33 for details.

Power Pins

Separate digital, analog, and DAC power planes are recommended. See Figure 33 for power supply pin assignments.

General Controls and Inputs

RSET Pin

RSET (pin 7) acts as the current reference source for the TV DAC Output. A 4.64 KOhm resister with 1% precision should be connected to this pin through AGND. The resister should be placed as close as possible to chip and the routing trace should be on the component side with no via connection. Due to TV Out quality issues, wide trace widths are also recommended.

DAC Outputs

There are four DAC output pins: DACA (pin 10), DACB (pin 12), DACC (pin 14), and DACD (pin 16). The components associated with these pins should be placed as close as possible to the VT1622 or VT1622M. The 75Ω output termination, output filter network, and output connectors should be located as close as possible to the VT1622 to minimize noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

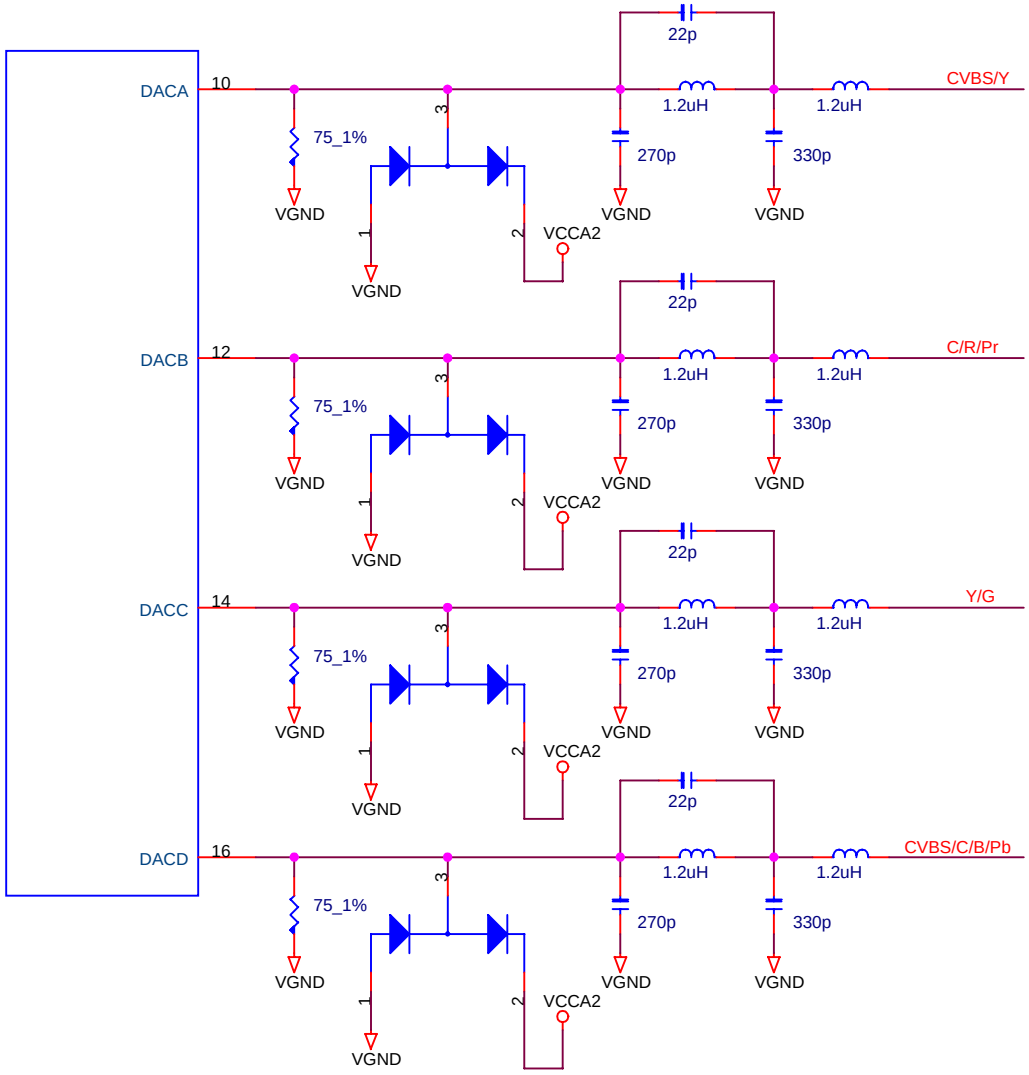


Figure 34. DAC Output Configuration

Crystal Inputs

The 14.31818 MHz (±50ppm for NTSC systems, ±25ppm for PAL systems) crystal must be placed as close as possible to the XI and XO pins (pins 2 and 3), with traces connected from point to point, overlaying the ground plane. Since the crystal generates the timing reference for the VT1622 and VT1622M encoder, it is very important that noise should not couple into these pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected as close as to the pin 4 ground in the VT1622 or VT1622M (see Figure 34).

Reference Crystal Oscillator

Both of the VT1622 and VT1622M also include an oscillator circuit, which allows an inexpensive 14.31818 MHz crystal to be connected directly. Alternatively, an externally generated 14.31818 MHz clock source may be supplied to the VT1622 and VT1622M. If an external clock source is used, it should have CMOS level specifications. The clock should connect to the XI pin, the XO pin should tied to ground, and with the pull up resister 10 KOhm of CONF_XLT (pin 55). The external source must exhibit ±50ppm or better frequency tolerance, and have low jitter characteristics.

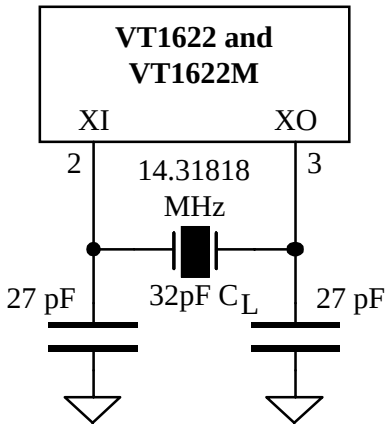


Figure 35. Crystal Configuration

If a crystal is used, the designer should ensure that the following conditions are met:

- The crystal is specified as 14.31818 MHz, ±50ppm, fundamental type, parallel resonant (NOT series resonant)
- The crystal is operated with a load capacitance equal to its specified value (C_L)
- External load capacitors have their ground connection very close to the VT1622 or VT1622M.
- To allow tunability, a variable cap may be used from XI to ground

BCO Output

The VT1622 and VT1622M BCO output (pin 61) reflect the 14.31818 MHz generated by the crystal inputs through the PLL. For operation to work normally, a capacitor of 10pF connected to ground is recommended.

External Clock Input

The external clock input, XCLK (pin 25), receives a pixel clock from the chipset north bridge chip.

Pixel Data Inputs

The VT1622 and VT1622M support up to 16 bits of data input for support of various input data formats. The host interface supported by the VT8605 north bridge chip is 12 bits. In this case, the interconnect should be started from the least significant bits, i.e. connect TVD[11:0] of the VT8605 to D[11:0] of the VT1622 or VT1622M. Un-connected pins D[15:12] should be connected to ground to prevent unexpected operation.

PC Board Layout Example

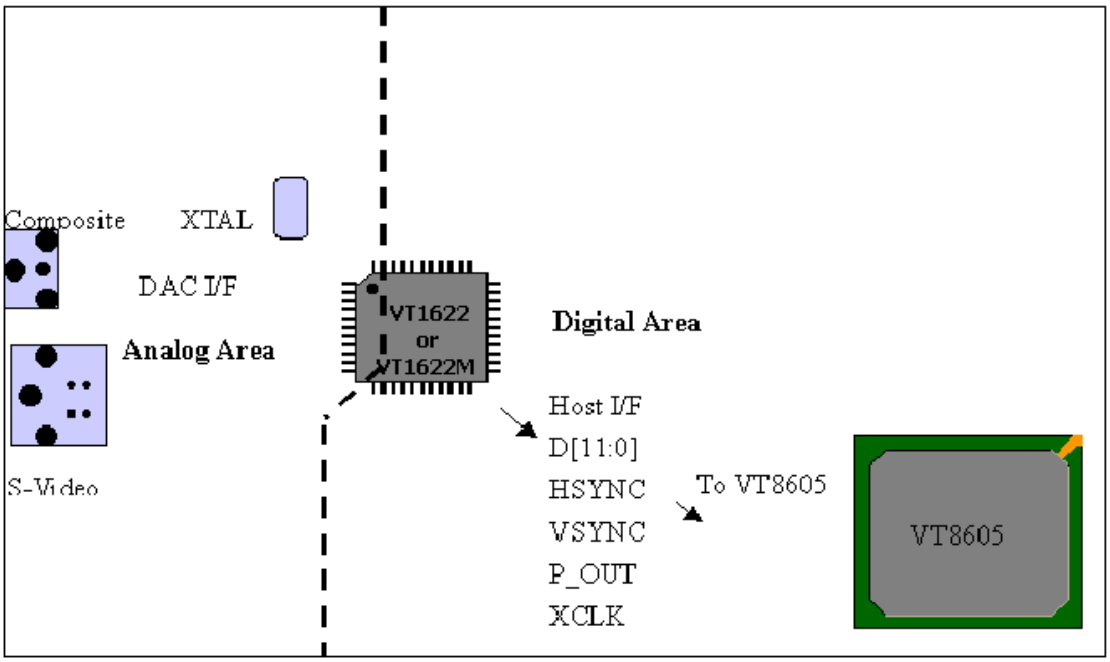


Figure 36. PCB Layout Example

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
T_{STG}	Storage Temperature	–65		150	ºC
T_C	Junction Operating Temperature			125	ºC
T_{AMB}	Ambient Operating Temperature	0		45 (desktop) 70 (notebook)	ºC
T_C	Case Operating Temperature	0		55	ºC
T_{SC}	Analog Output Short Circuit Duration		indefinite		Seconds
V_I	Input Voltage (all digital pins)	GND – 0.25		VCC+0.25	V
V_{ESD}	Electrostatic Discharge (Human Body)			2	KV
T_{VPS}	Vapor Phase Soldering (1 min.)			220	ºC

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33	I/O Voltage	3.15	3.3	3.45	V
VCC25	Digital Power Supply Voltage	2.25	2.5	2.75	V
VCCPLL	PLL Power	2.25	2.5	2.75	V
VCCDAC	DAC Power	2.25	2.5	2.75	V
VCCOSC	Oscillator Power	2.25	2.5	2.75	V
VCCBGAP	Band Gap Power	2.25	2.5	2.75	V
R_L	Output load to DAC outputs		37.5		Ω

Power Supply Current and Total Power Consumption Specifications

Symbol	Description	Min	Typ	Max	Unit
I_{D33}	VCC33 (3.3V)		8.9		mA
I_{D25}	VCC25 (2.5V)		66		mA
I_{PLL}	VCCPLL (2.5V)		7.6		mA
I_{OSC}	VCCOSC (2.5V)		2.8		mA
I_{BGON}	VCCBGAP (2.5V) – All 4 DAC Outputs Powered On		1.6		mA
I_{BGOFF}	VCCBGAP (2.5V) – All 4 DAC Outputs Powered Off		1.0		**uA**
I_{DACON}	VCCDAC (2.5V) – All 4 DAC Outputs Powered On		154		mA
I_{DACOFF}	VCCDAC (2.5V) – All 4 DAC Outputs Powered Off		640		**uA**
P_{TOTAL}	Total Power Consumption	276		610	mW

Operating Conditions: VCC25 = VCCA = VCCPLL = VCCDAC = VCCOSC = VCCBGAP = 2.5V, VCC33 = 3.3V, T_A = 25ºC, RSET = 4.64 KΩ

DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VCC33	I/O voltage	3.0		3.6	V	Normal op.
V_{IL}	Input low voltage	–0.5		0.3 VCC	V	non 5V tolerant
V_{IH}	Input high voltage	0.7 VCC		1.05 VCC	V	non 5V tolerant
V_{IH5T}	Input high voltage	0.7 VCC		5.5 V	V	5V tolerant
V_{OL}	Output low voltage	-		0.1 VCC	V	I_{OL}= 3.2mA
V_{OH}	Output high voltage	0.7 VCC		-	V	I_{OH}= -200mA
I_{OZ}	Input leakage	–10		10	mA	$0 < V_{IN} < VCC$
C_{IN}	Input capacitance	-		10	pF	
C_{OUT}	Output capacitance	-		10	pF	

DAC DC Characteristics

Parameter	Min	Typ	Max	Unit
Full Scale Current		34.00		mA
Lsb		33.20		uA
Operating Temperature	0	60	120	ºC
Operating Voltage	2.25	2.50	2.75	V
Output Voltage		1.28		V
Output Voltage Compliance	0		1.4	V
SENSE Reference Voltage		1.235		V
Band-Gap Reference Voltage		1.235		V
RSET Resistor		4.64 K		Ω
Output Load Resistor		37.5		Ω
Output Loading		10		pF
DAC Resolution		10		Bits
INL		± 1.0		Lsb
DNL		± 1.0		Lsb
DAC to DAC Matching		5		%
Gain Error		8		%

DAC AC Characteristics

Parameter	Min	Typ	Max	Units
Frequency			135	MHz
Output Rise Time		2		ns
Output Fall Time		2		ns
Output Full Scale Settling Time (1 %)		21.5		ns

Note: VCCDAC = 2.5V; RL = 37.5Ω; RSET = 4.64 KΩ; Temp = 60°C, unless otherwise noted

Display Signal Characteristics

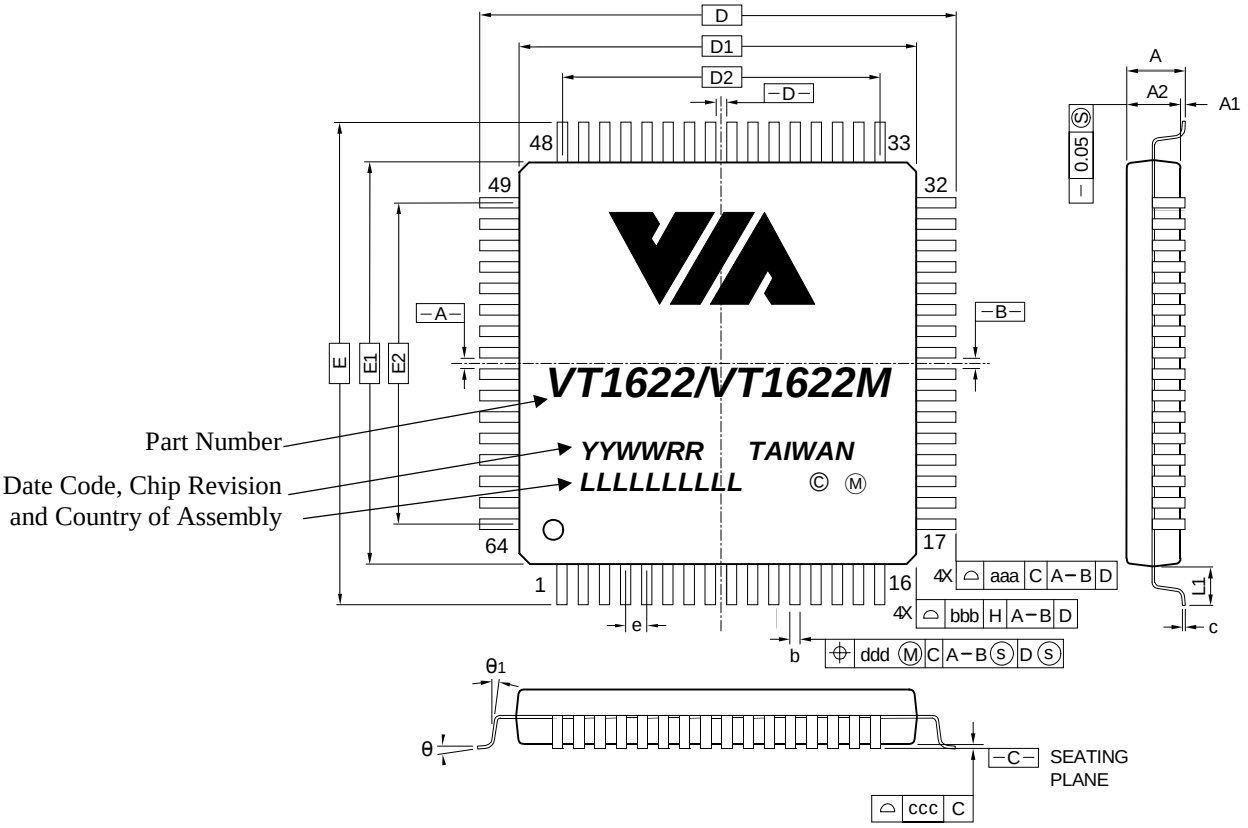
Symbol	Parameters	Min	Typ	Max	Unit
T_1	Pixel Clock Width	6.25		25	ns
T_2	Horizontal Sync Width	1			tp
T_3	Setup time from Pixel Data to Pixel Clock	2.5		17	ns
T_4	Hold time from Pixel Clock to Pixel Data	1.5			ns

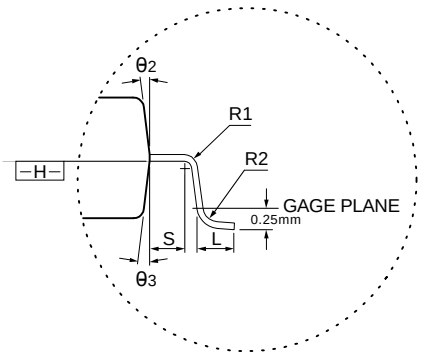
PLL Characteristics

Operating Conditions	Min	Typ	Max	Unit
Power Supply	2.25		2.75	V
Clock Output Duty Cycle	45		55	%

Note: Crystal Spec: 14.31818MHz (± 50 ppm)

PACKAGE MECHANICAL SPECIFICATIONS





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	12.00 BASIC			0.472 BASIC		
E	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.393 BASIC		
E1	10.00 BASIC			0.393 BASIC		
D2	7.50 BASIC			0.295 BASIC		
E2	7.50 BASIC			0.295 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 37. Mechanical Specification – 64-Pin TQFP Thin Quad Flat Pack