NOV 1 1992

VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

# VL82C3216

## BUS EXPANDING CONTROLLER (BANC) CACHE WITH WRITE BUFFER

### FEATURES

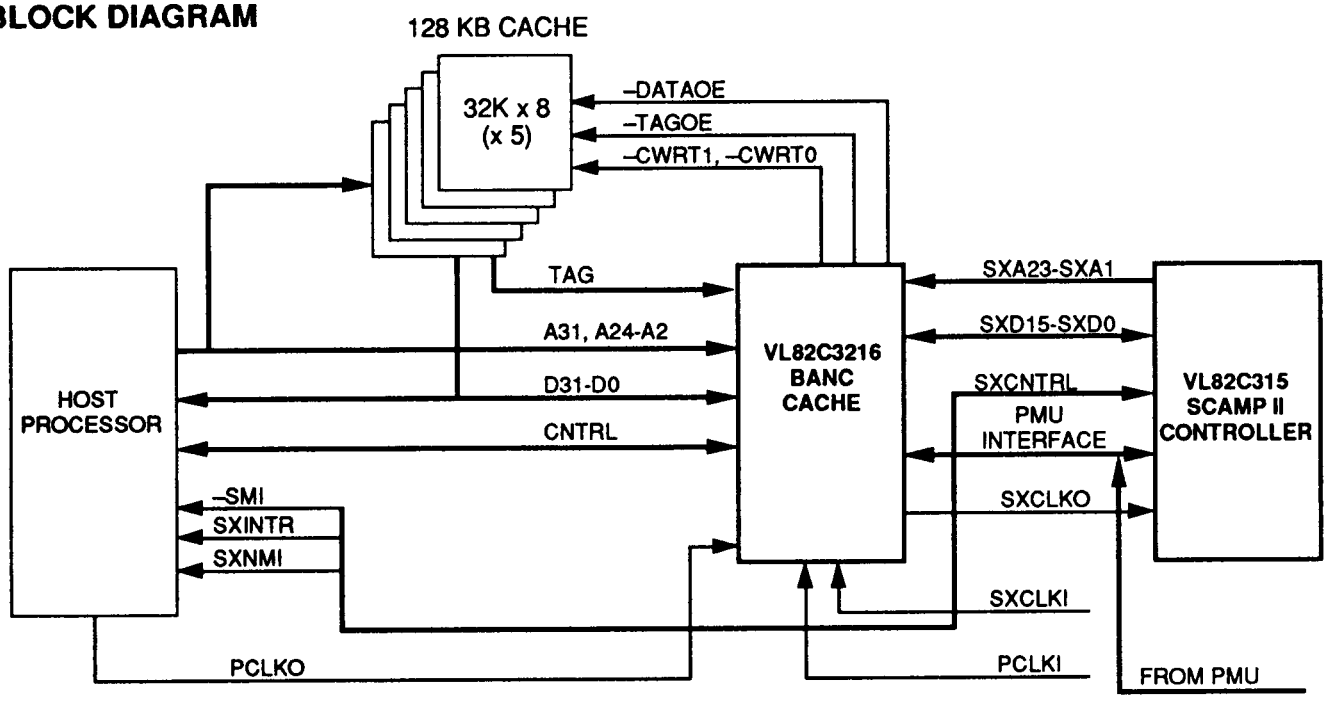
- High-performance 386DX, 486SX or 486DX interface
- Write Buffer - 64 byte (16 DWord)
- External second-level cache - 128 KB
- i486™ internal cache control
- BIOS control of second-level cache
- 386SX local bus emulation
- 386SX local bus address pipelining with four word FIFO
- 32-16 bit cycle type translation
- Auto peek cycle operations for both first and second-level cache
- i486 BIOS initialize
- 40 MHz max CPU freq @ 5.0 V, 33 MHz max SX freq @ 5.0 V, 25 MHz max CPU and SX freq @ 3.3 V
- Power management plus support for AMD's System Management Mode (SMM)
- 0.8-micron CMOS technology
- 160-lead metric quad flat pack (MQFP)

### DESCRIPTION

The VL82C3216 Bus Expanding Controller (BANC) Cache with Write Buffer is specifically designed to provide a high-performance, low-cost solution for interfacing 386SX PC/AT-compatible chip sets to 386DX, Am386™DXL, Am386DXLV, 486DX, 486SX, or compatible processors. The designs may be entirely new systems or upgrades to existing ones. Power management features also make this device ideal for laptop computers or other battery operated systems. The performance is achieved through the use of a write buffer structure, an external second level cache, prediction algorithms, and maximizing the internal first level cache of the i486, if used.

The high level of integration is centered on the VL82C3216. It controls all functions between the host processor bus and the 386SX local bus. In addition to the write buffer and second- and first-level cache controls, the VL82C3216 contains prediction and burst mode algorithms that take full advantage of the page mode design of existing 386SX system architecture. Through the use of pipelined page mode accesses to system memory, the VL82C3216 bursts data to and from memory at rates up to 25 MB per second. This provides 32-bit memory performance at 16-bit memory costs.

### BLOCK DIAGRAM



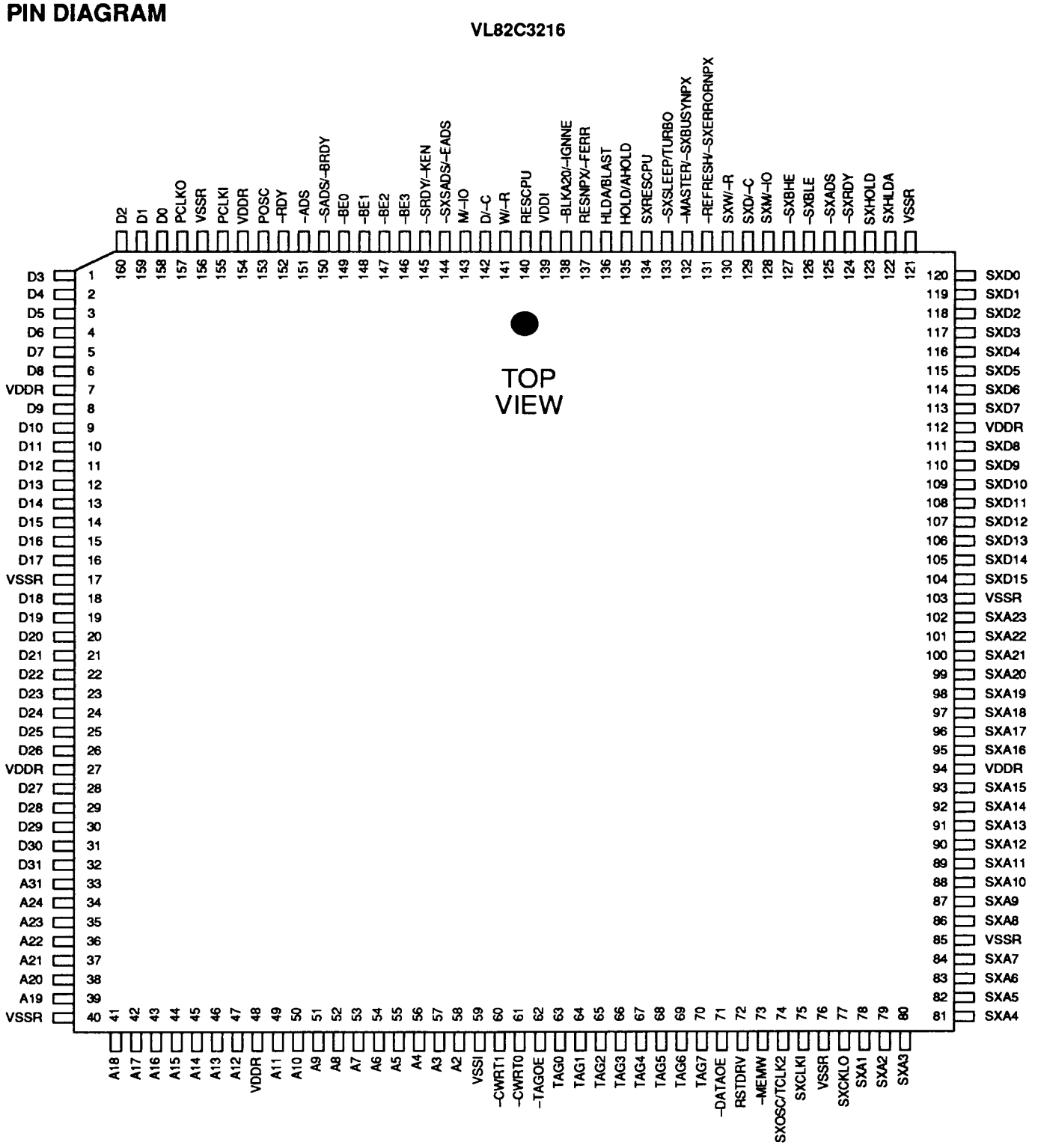

### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL82C3216-FC | Metric Quad Flat Pack |

**Note:** Operating temperature range is 0°C to + 70°C.

Am386 is a trademark of AMD Corp.
i486 is a trademark of Intel Corp.

## PIN DIAGRAM


VL82C3216
TOP VIEW
1 D3
2 D4
3 D5
4 D6
5 D7
6 D8
7 VDDR
8 D9
9 D10
10 D11
11 D12
12 D13
13 D14
14 D15
15 D16
16 D17
17 VSSR
18 D18
19 D19
20 D20
21 D21
22 D22
23 D23
24 D24
25 D25
26 D26
27 VDDR
28 D27
29 D28
30 D29
31 D30
32 D31
33 A31
34 A24
35 A23
36 A22
37 A21
38 A20
39 A19
40 VSSR
41 A18
42 A17
43 A16
44 A15
45 A14
46 A13
47 A12
48 VDDR
49 A11
50 A10
51 A9
52 A8
53 A7
54 A6
55 A5
56 A4
57 A3
58 A2
59 VSSI
60 -CWRT1
61 -CWRT0
62 -TAGOE
63 TAG0
64 TAG1
65 TAG2
66 TAG3
67 TAG4
68 TAG5
69 TAG6
70 TAG7
71 -DATAOE
72 RSTDRV
73 -MEMW
74 SXOSC/TCLK2
75 SXCLKI
76 VSSR
77 SXCKLO
78 SXA1
79 SXA2
80 SXA3
81 SXA4
82 SXA5
83 SXA6
84 SXA7
85 VSSR
86 SXA8
87 SXA9
88 SXA10
89 SXA11
90 SXA12
91 SXA13
92 SXA14
93 SXA15
94 VDDR
95 SXA16
96 SXA17
97 SXA18
98 SXA19
99 SXA20
100 SXA21
101 SXA22
102 SXA23
103 VSSR
104 SXD15
105 SXD14
106 SXD13
107 SXD12
108 SXD11
109 SXD10
110 SXD9
111 SXD8
112 VDDR
113 SXD7
114 SXD6
115 SXD5
116 SXD4
117 SXD3
118 SXD2
119 SXD1
120 SXD0
121 VSSR
122 SXHLDA
123 SXHOLD
124 -SXRDY
125 -SXADS
126 -SXBLE
127 -SXBHE
128 SXM/-IO
129 SXD/-C
130 SXW/-R
131 -REFRESH/-SXERRORNPX
132 -MASTER/-SXBUSYNPX
133 -SXSLEEP/TURBO
134 SXRESCPU
135 HOLD/AHOLD
136 HLDA/BLAST
137 RESNPX/-FERR
138 -BLKA20/-IGNNE
139 VDDI
140 RESCPU
141 W/-R
142 D/-C
143 M/-IO
144 -SXSADS/-EADS
145 -SRDY/-KEN
146 -BE3
147 -BE2
148 -BE1
149 -BE0
150 -SADS/-BRDY
151 -ADS
152 -RDY
153 POSC
154 VDDR
155 PCLKI
156 VSSR
157 PCLKO
158 D0
159 D1
160 D2

## PIN TYPE BY OPERATIONAL STATE

| Pin # | Pin Name | Pin Type | Input Type | Drive (mA) | Pin # | Pin Name | Pin Type | Input Type | Drive (mA) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | D3 | IO | TTL | 4 | 33 | A31 | IO | TTL | 4 |
| 2 | D4 | IO | TTL | 4 | 34 | A24 | IO | TTL | 4 |
| 3 | D5 | IO | TTL | 4 | 35 | A23 | IO | TTL | 4 |
| 4 | D6 | IO | TTL | 4 | 36 | A22 | IO | TTL | 4 |
| 5 | D7 | IO | TTL | 4 | 37 | A21 | IO | TTL | 4 |
| 6 | D8 | IO | TTL | 4 | 38 | A20 | IO | TTL | 4 |
| 7 | VDDR | PWR | | | 39 | A19 | IO | TTL | 4 |
| 8 | D9 | IO | TTL | 4 | 40 | VSSR | GND | | |
| 9 | D10 | IO | TTL | 4 | 41 | A18 | IO | TTL | 4 |
| 10 | D11 | IO | TTL | 4 | 42 | A17 | IO | TTL | 4 |
| 11 | D12 | IO | TTL | 4 | 43 | A16 | IO | TTL | 4 |
| 12 | D13 | IO | TTL | 4 | 44 | A15 | IO | TTL | 4 |
| 13 | D14 | IO | TTL | 4 | 45 | A14 | IO | TTL | 4 |
| 14 | D15 | IO | TTL | 4 | 46 | A13 | IO | TTL | 4 |
| 15 | D16 | IO | TTL | 4 | 47 | A12 | IO | TTL | 4 |
| 16 | D17 | IO | TTL | 4 | 48 | VDDR | PWR | | |
| 17 | VSSR | GND | | | 49 | A11 | IO | TTL | 4 |
| 18 | D18 | IO | TTL | 4 | 50 | A10 | IO | TTL | 4 |
| 19 | D19 | IO | TTL | 4 | 51 | A9 | IO | TTL | 4 |
| 20 | D20 | IO | TTL | 4 | 52 | A8 | IO | TTL | 4 |
| 21 | D21 | IO | TTL | 4 | 53 | A7 | IO | TTL | 4 |
| 22 | D22 | IO | TTL | 4 | 54 | A6 | IO | TTL | 4 |
| 23 | D23 | IO | TTL | 4 | 55 | A5 | IO | TTL | 4 |
| 24 | D24 | IO | TTL | 4 | 56 | A4 | IO | TTL | 4 |
| 25 | D25 | IO | TTL | 4 | 57 | A3 | IO | TTL | 4 |
| 26 | D26 | IO | TTL | 4 | 58 | A2 | IO | TTL | 4 |
| 27 | VDDR | PWR | | | 59 | VSSI | GND | | |
| 28 | D27 | IO | TTL | 4 | 60 | –CWRT1 | O-TS | | 8 |
| 29 | D28 | IO | TTL | 4 | 61 | –CWRT0 | O-TS | | 8 |
| 30 | D29 | IO | TTL | 4 | 62 | –TAGOE | O-TS | | 8 |
| 31 | D30 | IO | TTL | 4 | 63 | TAG0 | IO | TTL | 4 |
| 32 | D31 | IO | TTL | 4 | 64 | TAG1 | IO | TTL | 4 |

## PIN TYPE BY OPERATIONAL STATE (Cont.)

| Pin # | Pin Name | Pin Type | Input Type | Drive (mA) | Pin # | Pin Name | Pin Type | Input Type | Drive (mA) |
|---|---|---|---|---|---|---|---|---|---|
| 65 | TAG2 | IO | TTL | 4 | 97 | SXA18 | IO | TTL | 4 |
| 66 | TAG3 | IO | TTL | 4 | 98 | SXA19 | IO | TTL | 4 |
| 67 | TAG4 | IO | TTL | 4 | 99 | SXA20 | IO | TTL | 4 |
| 68 | TAG5 | IO | TTL | 4 | 100 | SXA21 | IO | TTL | 4 |
| 69 | TAG6 | IO | TTL | 4 | 101 | SXA22 | IO | TTL | 4 |
| 70 | TAG7 | IO | TTL | 4 | 102 | SXA23 | IO | TTL | 4 |
| 71 | –DATAOE | O-TS | | 8 | 103 | VSSR | GND | | |
| 72 | RSTDRV | I | TTL | | 104 | SXD15 | IO | TTL | 4 |
| 73 | –MEMW | I | TTL | | 105 | SXD14 | IO | TTL | 4 |
| 74 | SXOSC/TCLK2 | IO | CMOS | 8 | 106 | SXD13 | IO | TTL | 4 |
| 75 | SXCLKI | I | CMOS | | 107 | SXD12 | IO | TTL | 4 |
| 76 | VSSR | GND | | | 108 | SXD11 | IO | TTL | 4 |
| 77 | SXCLKO | O-TS | | 12 | 109 | SXD10 | IO | TTL | 4 |
| 78 | SXA1 | O-TS | TTL | 4 | 110 | SXD9 | IO | TTL | 4 |
| 79 | SXA2 | IO | TTL | 4 | 111 | SXD8 | IO | TTL | 4 |
| 80 | SXA3 | IO | TTL | 4 | 112 | VDDR | PWR | | |
| 81 | SXA4 | IO | TTL | 4 | 113 | SXD7 | IO | TTL | 4 |
| 82 | SXA5 | IO | TTL | 4 | 114 | SXD6 | IO | TTL | 4 |
| 83 | SXA6 | IO | TTL | 4 | 115 | SXD5 | IO | TTL | 4 |
| 84 | SXA7 | IO | TTL | 4 | 116 | SXD4 | IO | TTL | 4 |
| 85 | VSSR | GND | | | 117 | SXD3 | IO | TTL | 4 |
| 86 | SXA8 | IO | TTL | 4 | 118 | SXD2 | IO | TTL | 4 |
| 87 | SXA9 | IO | TTL | 4 | 119 | SXD1 | IO | TTL | 4 |
| 88 | SXA10 | IO | TTL | 4 | 120 | SXD0 | IO | TTL | 4 |
| 89 | SXA11 | IO | TTL | 4 | 121 | VSSR | GND | | |
| 90 | SXA12 | IO | TTL | 4 | 122 | SXHLDA | IO | TTL | 4 |
| 91 | SXA13 | IO | TTL | 4 | 123 | SXHOLD | I | TTL | |
| 92 | SXA14 | IO | TTL | 4 | 124 | –SXRDY | I | TTL | |
| 93 | SXA15 | IO | TTL | 4 | 125 | –SXADS | O-TS | | 4 |
| 94 | VDDR | PWR | | | 126 | –SXBLE | O-TS | | 4 |
| 95 | SXA16 | IO | TTL | 4 | 127 | –SXBHE | O-TS | | 4 |
| 96 | SXA17 | IO | TTL | 4 | 128 | SXM/–IO | O-TS | | 4 |

## PIN TYPE BY OPERATIONAL STATE (Cont.)

| Pin # | Pin Name | Pin Type | Input Type | Drive (mA) | Pin # | Pin Name | Pin Type | Input Type | Drive (mA) |
|---|---|---|---|---|---|---|---|---|---|
| 129 | SXD/–C | O-TS | | 4 | 145 | –SRDY/–KEN | IO | TTL | 4 |
| 130 | SXW/–R | O-TS | | 4 | 146 | –BE3 | I | TTL | |
| 131 | –REFRESH/–SXERRORNPX | IO | TTL | 4 | 147 | –BE2 | I | TTL | |
| 132 | –MASTER/–SXBUSYNPX | IO | TTL | 4 | 148 | –BE1 | I | TTL | |
| 133 | –SXSLEEP/TURBO | I-PU | TTL | | 149 | –BE0 | I | TTL | |
| 134 | SXRESCPU | I | TTL | | 150 | –SADS/–BRDY | IO-PU | TTL | 4 |
| 135 | HOLD/AHOLD | IO | TTL | 4 | 151 | –ADS | I-PU | TTL | |
| 136 | HLDA/–BLAST | I | TTL | | 152 | –RDY | IO | TTL | 4 |
| 137 | RESNPX/–FERR | IO-PU | TTL | 8 | 153 | POSC | I | CMOS | |
| 138 | –BLKA20/–IGNNE | IO-PU | TTL | 4 | 154 | VDDR | PWR | | |
| 139 | VDDI | PWR | | | 155 | PCLKI | I | CMOS | |
| 140 | RESCPU | O-TS | | 8 | 156 | VSSR | GND | | |
| 141 | W/–R | I-PU | TTL | | 157 | PCLKO | O | | 12 |
| 142 | D/–C | I-PU | TTL | | 158 | D0 | IO | TTL | 4 |
| 143 | M/–IO | I-PU | TTL | | 159 | D1 | IO | TTL | 4 |
| 144 | –SXSADS/–EADS | O | TTL | 4 | 160 | D2 | IO | TTL | 4 |

**Legend:**

| | |
|---|---|
| CMOS | CMOS-compatible input |
| GND | Ground pin |
| I | Input-only pin |
| IO | Bidirectional pin |
| O | Output-only pin |
| PWR | Power supply pin |
| TTL | TTL-compatible input |
| -PU | Indicates a high-impedance with approximately 10 KΩ minimum resistance to VDD (internal pull-up resistor on pin). |
| -TS | Three-state |

## SIGNAL DESCRIPTIONS

In order to reduce the number of pins required for this device, some functions which are processor specific share the same pin. "For 386DX" and "For 486" appear in parentheses in the Signal Description column to specify pin functionality with a description for each mode following.

| Signal Name | Pin Number | Signal Description |
|---|---|---|
| **CACHE INTERFACE SIGNALS** | | |
| –CWRT0 | 61 | Cache Write Enable Low - Used for enabling data bytes 1 and 0. |
| –CWRT1 | 60 | Cache Write Enable High - Used for enabling data bytes 3 and 2. |
| –TAGOE | 62 | Tag Output Enable - Used to enable the tag field of the second-level cache. |
| –DATAOE | 71 | Data Output Enable - Used to enable the data in the second-level cache. |
| TAG7-TAG0 | 70-63 | Tag Field bus bits 7 through 0 - Bits TAG6-TAG0 contain the A23-A17 of the tag entry. TAG7 contains the valid bit. |
| **CLOCK INTERFACE SIGNALS** | | |
| SXOSC/TCLK2 | 74 | SX Oscillator input or TCLK2 output - When the VL82C3216 is in the Asynchronous Mode, this signal is the external oscillator input which provides the fundamental timing for the SX Interface. When in the Synchronous Mode this signal is the TCKL2 clock output and provides the VL82C315 SCAMP II Controller with the TCLK2IN clock. |
| SXCLKI | 75 | SX Clock Input - The VL82C3216 reference clock input is normally connected to SXCLKO. |
| SXCLKO | 77 | SX Processor Clock - This signal output provides the fundamental timing for the system. |
| POSC | 153 | 2X Processor Clock - An input that provides the fundamental timing for the CPU Interface of the VL82C3216. It is buffered and driven out on PCLKO. |
| PCLKI | 155 | Processor Clock In - This is the reference clock input to the VL82C3216. It is normally tied to PCLKO. |
| PCLKO | 157 | Processor Clock - An output that provides the appropriate fundamental timing for the host processor, depending on whether it is a 386DX, 486DX or 486SX. Note: In 386DX systems PCLKO = POSC. In 486 systems PCLKO = POSC/2. |
| **CPU & SX INTERFACE SIGNALS** | | |
| A31, A24-A2 | 33-39, 41-47, 49-58 | Address Bus bits 31 and 24 through 2 - These bits accept and output the physical memory or port I/O addresses for the CPU Interface of the VL82C3216. |
| SXA23-SXA1 | 102-95, 93-86, 84-78 | SX Address bus bits 23 through 1 - This is the address bus for the SX Interface. |
| D31-D0 | 32-28, 26-18, 16-8, 6-1, 160-158 | Data Bus bits 31 through 0 - This bus inputs data from the host processor on write cycles and outputs data to the host processor on read cycles. |
| SXD15-SXD0 | 104-111, 113-120 | SX Data Bus - This bus inputs the data from the SX Interface during a host processor read cycle and outputs the data to the SX Interface during a host processor write cycle. |
| RSTDRV | 72 | Reset Drive - This is a system reset which occurs during the power-on sequence. |
| –SXBLE | 126 | SX Low Byte Enable. |
| –SXBHE | 127 | SX High Byte Enable. |
| SXRESCPU | 134 | SX Reset CPU - This signal will reset only the CPU and has no affect on the VL82C3216 or available coprocessor. |
| HLDA/–BLAST | 136 | (For 386DX) Hold Acknowledge - The response given to an active Hold signal.<br>(For 486) Burst Last - Indicates that the next time –BRDY is returned, the burst cycle is complete. |
| RESCPU | 140 | Reset CPU - This signal forces the host processor to reset to a known state. It is the SXRESCPU signal resynchronized to PCLK. |

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Description |
|---|---|---|
| –ADS | 151 | Address Status - This pin indicates that a valid bus cycle definition and address are available on the CPU bus. |
| –MEMW | 73 | Memory Write - An input signal that is generated when a write is occurring on the AT bus of the system. The VL82C3216 expects the 386SX Bus Emulation Unit to contain a valid address which it will capture. Both the internal 486 cache and the second-level cache will snoop the bus. |
| SXHLDA | 122 | SX Bus Hold Acknowledge - Indicates that the VL82C3216 has surrendered control of the system bus to another Bus Master.<br><br>The state of this pin is sampled on the falling edge of RSTDRV in order to determine asynchronous or synchronous clock mode operation. If high, the operation is in the Synchronous Mode. If low, the operation is in the Asynchronous Mode. |
| SXD/–C | 129 | SX Data or Control - A bus cycle definition pin that identifies whether the cycle is data (i.e., memory or I/O) or control (i.e., interrupt acknowledge, halt and code fetch) on the SX Interface. |
| D/–C | 142 | Data/Control - A bus cycle definition pin that identifies whether the cycle is data (i.e., memory or I/O) or control (i.e., interrupt acknowledge, halt and code fetch) on the CPU Interface. |
| HOLD/AHOLD | 135 | (For 386DX) Bus Hold Request - A signal that indicates that the VL82C3216 is requesting control of the local bus.<br><br>(For 486) Address Hold - This signal is generated when the VL82C3216 is taking control of the address bus for a cache to invalidate cycle.<br><br>On the falling edge of RSTDRV, this pin is sampled to determine whether to operate in 486 Mode or 386DX Mode. Low = 386DX Mode. High = 486 Mode. |
| SXW/–R | 130 | SX Write/Read - A bus cycle definition pin that identifies whether a read or write cycle is on the SX Interface. |
| SXHOLD | 123 | SX Bus Hold Request - An input that allows another Bus Master to request control of the system bus. |
| –SXRDY | 124 | SX Bus Ready - Indicates that the bus cycle on the system bus successfully terminated. |
| –SXADS | 125 | SX Address Status - This signal indicates that a valid bus definition and address are available on the system bus. |
| SXM/–IO | 128 | SX Memory or I/O - A bus cycle definition pin that identifies whether the cycle is a memory cycle or an input/output cycle on the SX Interface. |
| W/–R | 141 | Write/Read - A bus cycle definition pin that identifies whether it is a read cycle or a write cycle on the CPU Interface. |
| M/–IO | 143 | Memory I/O - A bus cycle definition pin that identifies whether the cycle is a memory cycle or an input/output cycle on the CPU Interface. |
| –BE3 - –BE0 | 146-149 | Byte Enables - These bits indicate which data bytes of the data bus take part in a bus cycle on the CPU Interface. |
| –RDY | 152 | Bus Ready (non-burst) - This output indicates that the current bus cycle has been successfully completed on the CPU Interface.<br><br>On the falling edge of RSTDRV, this pin is sampled to determine the SXCLKO frequency if synchronous operating mode is active. When low, SXCLKO = POSC/2. When high, SXCLKO = POSC. If SXHLDA is sampled high on the falling edge of RSTDRV, the state of –RDY is ignored. |

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| **COPROCESSOR INTERFACE SIGNALS** | | | |
| –REFRESH/ –SXERRORNPX | 131 | | (For 386DX) Refresh - This pin is configured as the –REFRESH input. It is connected to the –REFRESH signal from the VL82C315 SCAMP II Controller.<br><br>(For 486) Numeric Coprocessor Error - An output to the system bus to indicate that a floating point error has occurred in the 486. |
| –MASTER/ –SXBUSYNPX | 132 | | (For 386DX) Master - This pin is configured as the –MASTER input and is connected to the ISA bus –MASTER signal from the VL82C315 SCAMP II Controller.<br><br>(For 486) SX Busy Coprocessor - Driven by the coprocessor, this signal indicates to the SX Interface that the coprocessor is currently executing an instruction. |
| –SXSLEEP/ TURBO | 133 | | SX Sleep Mode or Turbo - When the internal power management hardware is enabled via a logic high on the –SRDY/–KEN pin on the falling edge of RSTDRV, this pin is configured as –SXSLEEP. When –SXSLEEP is pulled low, the internal Sleep Mode clock dividers are activated.<br><br>**Note:** When interfacing to the VL82C315 SCAMP II Controller, the VL82C315's –SLEEP and –WAKEUP signals must be externally ANDed. The output of this AND is then connected to the –SXSLEEP input of the VL82C3216.<br><br>When –SRDY/–KEN is sampled low on the falling edge of RSTDRV, this pin becomes a TURBO input. In this mode, a logic low on TURBO activates the programmable Turbo Mode clock divider and invokes the Non-Turbo Mode. In order to run the system full speed (Turbo Mode), the TURBO pin must be high and each internal software means of Turbo Mode control must be inactive. |
| RESNPX/ –FERR | 137 | | (For 386DX) Reset Numeric Processor - This output causes the 387 math coprocessor to cease all present activity and enter an idle state.<br><br>(For 486) Numeric Floating Point Error - An input which indicates that a floating point error has occurred in the 486. |
| –BLKA20/ –IGNNE | 138 | | (For 386DX) Block A20 - When this input is low, A20 is held low for accesses to the cache and then driven out to the SX Interface. When high, A20 follows CPU A20. (When the VL82C3216 is in the 486 Mode, the VL82C315's –BLKA20 signal is connected directly to the 486 which handles the A20 gating function.)<br><br>(For 486) Ignore Numeric Error - This output causes a 486 to ignore a numeric error and continue executing non-control floating point instructions. –IGNNE is asynchronous. |
| **SMI INTERFACE PINS** | | | |
| –SXSADS/ –EADS | 144 | | (For Am386DXLV) SMI SX Address Status - An output that is utilized by the SX Interface during power management.<br><br>(For 486) External Address Status - An output signal which indicates to the 486 that a valid external address has been driven onto its address pins. |
| –SRDY/–KEN | 145 | | (For Am386DXLV) SMI Ready - The Ready output pin utilized by the Am386DXLV during power management.<br><br>(For 486) Cache Enable - This output is sent to the 486 to indicate that the current cycle is cacheable.<br><br>This signal is sampled on the falling edge of RSTDRV to determine whether the internal power management functions are enabled or disabled. If low, they are disabled. If high, they are enabled. |
| –SADS/–BRDY | 150 | | (For Am386DXLV) SMI Address Strobe - An input that indicates a valid SMI bus cycle definition and address are available on the system bus.<br><br>(For 486) Burst Ready - An output which indicates that the current burst cycle is complete. |

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| **POWER AND GROUND PINS** | | | |
| VDDR | 7, 27, 48, 94, 112, 154 | | Ring Power +5.0 V or 3.3 V |
| VDDI | 139 | | Core Logic Power - Must be tied to VDDR. |
| VSSR | 17, 40, 76, 85, 103, 121, 156 | | Ring Ground - 0.0 V. |
| VSSI | 59 | | Internal Core Logic Ground - 0.0 V. |

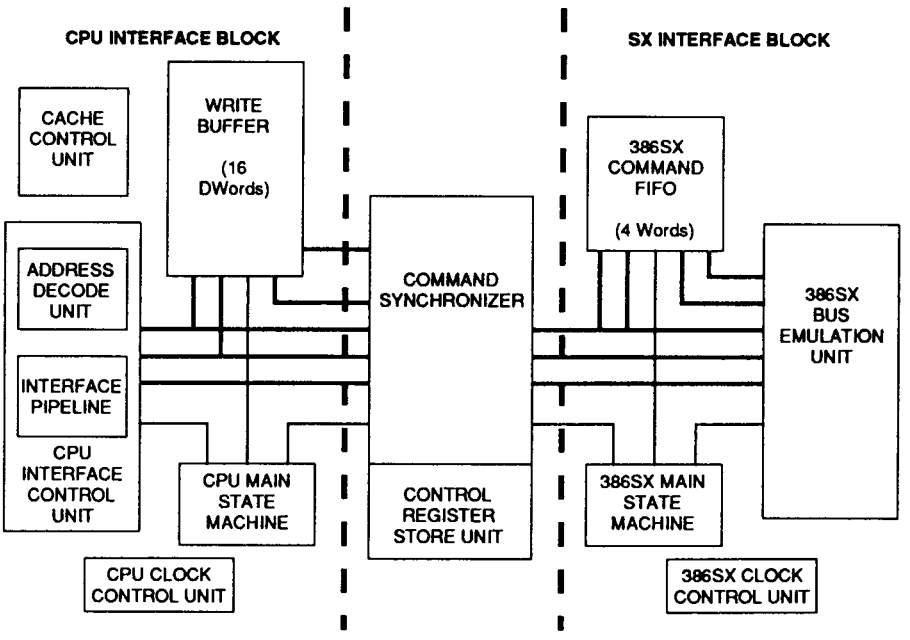
## FUNCTIONAL DESCRIPTION

The VL82C3216 Cache Controller and Interface Unit can be divided into two main functional blocks:

- SX (system) Interface Block - Contains the 386SX Main State Machine, the 386SX Bus Emulation Unit, the 386SX Command FIFO and the 386SX Clock Control Unit.
- CPU Interface Block - Includes the CPU Interface Control Unit, the Cache Control Unit, the Write Buffer, the CPU Main State Machine and the CPU Clock Control Unit.

The additional interface units are the Command Synchronizer (which interfaces the commands between the CPU Interface and SX Interface) and the Control Registers. The functional blocks and the configuration and control selections that affect them will be discussed in the following sections. An internal block diagram of the VL82C3216 is shown in Figure 1.

**FIGURE 1. VL82C3216 INTERNAL BLOCK DIAGRAM**




### CPU INTERFACE BLOCK

The VL82C3216 is responsible for decoding the processor (486SX/DX or 386DX) commands, initiating the requested action and/or forwarding the command to the SX Interface and responding in a manner required by the processor bus protocol.

The VL82C3216 responds to all processor bus cycles.

Based on the cycle type from the processor, the VL82C3216 may do one or more of the following: forward the command to the SX Interface, generate cache read(s) or write(s), post a data write to the Write Buffer, perform a local I/O read or write, perform a 387 coprocessor ready handshake, or convert and forward a 486 special cycle to a 386SX special cycle.

The CPU Clock Control Unit will perform system requested clock rate changes for power management or non-turbo requests.

The VL82C3216 is responsible for performing cache line invalidate cycles to the 486 cache and to its own cache.

**CPU Interface Control Unit**

The CPU Interface Control Unit contains the processor Interface Pipeline, the Address Decode Unit and the processor Hold logic.

This unit couples tightly to the Cache Control Unit, the Write Buffer and the Command Synchronizer. It is controlled by the CPU Main State Machine.

**Processor Interface Pipeline**

The processor Interface Pipeline interfaces the processor signals and executes the command handshake with the processor. It latches the processor commands and then starts the CPU Main State Machine. Upon command completion, it returns the appropriate Ready, SMI Ready (–SRDY) or Burst Ready (–BRDY) signal to the processor.

This interface also supports the SMI Address Strobe (–SADS) for the Am386DXLV processor and synchronization for reset to the processor.

**386DX Vs 486SX/DX Processor Mode**

The VL82C3216 can be configured to operate with either a 386DX or a 486SX/DX processor through the processor type configuration pin. A jumper on pin 135 (HOLD/AHOLD) is used to select either mode at the falling edge of RSTDRV according to the following definition:

**HOLD/AHOLD**

| State | Processor Mode |
|---|---|
| Logic 0 | 386DX Mode - The VL82C3216 will provide the oscillator frequency (double clock) output to the processor and will operate with a 386DX style command handshake. Any pins that have dual functionality based on the processor type will operate in the 386DX support mode. |
| Logic 1 | 486 Mode - The VL82C3216 will provide one-half the oscillator frequency (fundamental clock) out to the processor and will operate with a 486 style command handshake. Any pins that have dual functionality based on the processor type will operate in the 486 support mode. |

**Address Decode Unit**
The Address Decode Unit is used to determine cacheable memory address ranges, 387 floating point unit memory address range, internal Configuration Register I/O address ranges and emulated AT system I/O address ranges for Turbo/Non-Turbo Mode. The functions driven by these decoded addresses will be discussed in their own section of the specification.

**Hold Logic**
This function controls the propagation and processing of the SXHOLD requests and –MEMW driven cache invalidate requests to the 386DX and 486 processors.

**386DX Hold Processing**
In 386 Mode, when the SXHOLD request signal is received, it is synchronized to the processor clock and immediately passed to the processor as a HOLD request. After the HLDA signal is returned from the processor, the Write Buffer is held and the 386SX Command FIFO is allowed to empty. When the 386SX Command FIFO is idle, SXHLDA is asserted.

When the SXHOLD request is deasserted, it is again synchronized and the HOLD request is deasserted. SXHLDA is removed, at the same time as HOLD is removed.

Normal AT bus refresh cycles are detected by monitoring the signals –REFRESH and –MASTER. If a non-master driven refresh is recognized, the HOLD request to the processor will be released early to allow the processor to operate out of the cache.

**486 Hold Processing**
In 486 Mode, when the SXHOLD request signal is received, it is synchronized to the processor clock and as soon as the CPU Main State Machine enters the idle state, it is passed to the processor as an AHOLD (address hold) request. As soon as the 386SX Command FIFO completes the current SX command, SXHLDA is asserted.

When the SXHOLD request is deasserted, it is again synchronized and the AHOLD request is deasserted. SXHLDA is removed at the same time as AHOLD is removed.

**CPU Main State Machine**
The CPU Main State Machine is the VL82C3216's primary control center. Its function is to dispatch commands to the SX Interface and Cache Control Unit. It is also responsible for dumping the Write Buffer contents to the SX Interface when required. It issues –RDY to the processor immediately after either the Cache Controller, Write Buffer, 386SX Bus Emulation Unit or local I/O and coprocessor completes the command.

The CPU Main State Machine operates at the same rate as the processor's fundamental cycle and sits at idle until it receives a command from the processor. It returns to idle after completing every processor command.

A processor reset initializes the CPU Main State Machine to an idle state.

**CACHE CONTROL UNIT**
The VL82C3216 contains a write-through cache controller for use with 386DX or 486 processors as well as providing the interface to the internal 486 primary cache. It provides the overall cache enable/disable features for 486 cache and internal cache. It supports four programmable non-cacheable regions that can be mapped to any region (on 4 KB boundaries) in the 16 MB cacheable address space.

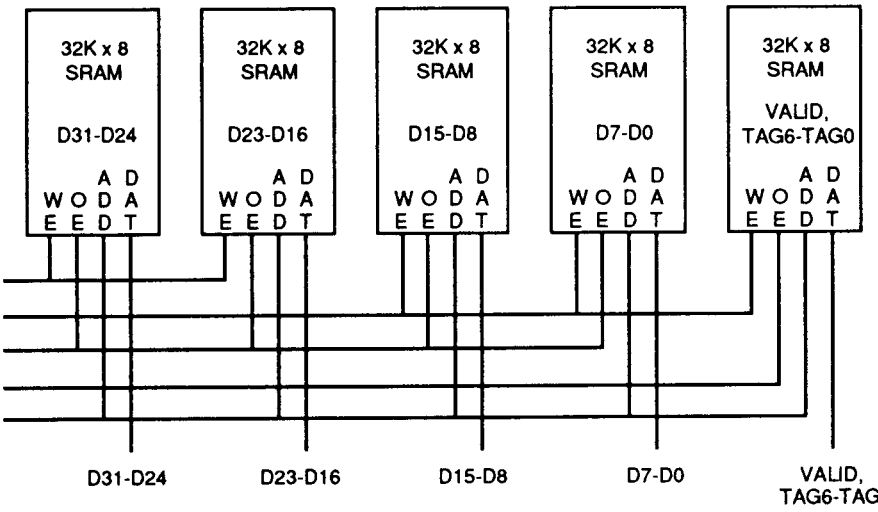
The Primary cache is enabled by the KEN enable (ENKEN), bit 7 in the Control Register MCONFIG (40h).

The secondary cache is enabled by the second level cache enable bit (ENCCH), bit 6 in the Control Register MCONFIG (40h).

**Write-Through Cache Controller**
The write-through cache controller in the VL82C3216 supports a direct mapped 128 KB cache. The cache Tag and data RAMs are external. For a 386DX processor, asynchronous data RAMs are supported and for a 486 processor, asynchronous or synchronous data RAMs are supported. The external cache RAM is organized as one bank of five 32K x 8 SRAMs. The cache line consists of two Words of data and one byte of Tag. The Tag consists of one valid bit and a 7-bit Tag address. Figure 2 shows the cache Tag RAM and SRAM connections to the VL82C3216.

**Write-Through Cache Performance**
For 386DX processors, cache reads are completed in zero wait states and cache write cycles require one wait state. For the 486 processors, cache reads complete in zero wait states and cache burst reads complete in 2,2,2,2 clocks. Cache writes are zero wait

**FIGURE 2. CACHE TAG RAM & SRAM CONNECTION TO VL82C3216**




*TAG6-TAG0 is generated from ADDR23-ADDR17.

states using synchronous data RAMs and one wait state using asynchronous RAMs. See Table 1 for SRAM speed requirements.

**Byte/Word Update Capability**
The VL82C3216 provides two cache write signals to support a number of cache write options.

A VL82C3216-based design can be configured to update the cache on processor byte writes with the addition of a single LS08 device externally. Figure 3 shows the external logic required to perform cache byte write operations for improved performance with byte-intensive applications and benchmarks. This maximizes the cache performance by ensuring that all writes to previously cached locations remain in the cache. Alternately, the cache write signals can be enabled as –CWRT0 and –CWRT1 and the external TTL device eliminated. This will allow all DWord and aligned Word writes to update the cache, but byte writes and unaligned Word writes would update only the main memory and mark the cached entry invalid.

For synchronous data RAMs with a 486, the cache write lines are defined as Cache Data Write and Cache Tag Write with adjusted timing on the Cache Data Write.

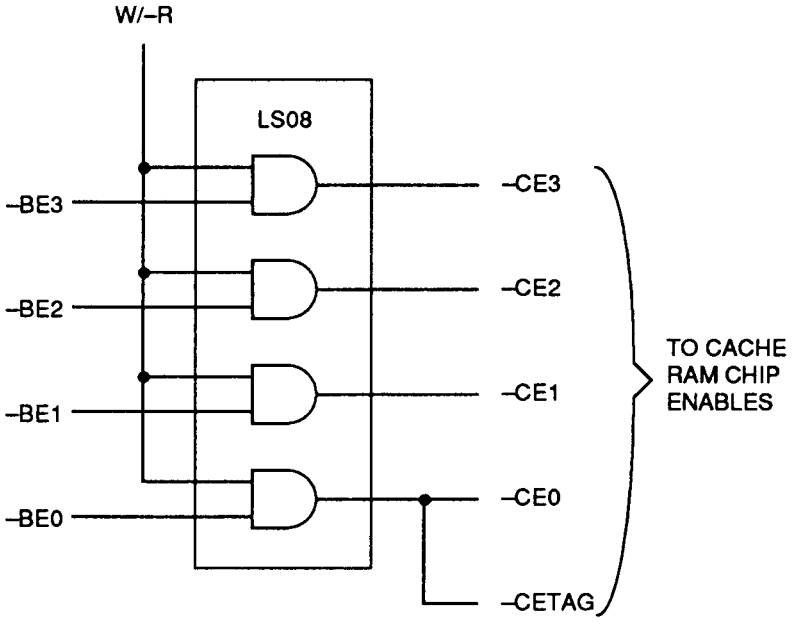
Byte write updates to the external cache are enabled by the byte write valid enable bit (BVALEN), bit 1 in the Control Register MCONFIG (40h).

**Cache Read-Miss Cycle**
On any memory read cycle from a cacheable address range, a full DWord is read from main memory and entered into the cache at the same time it is returned to the processor. On burst memory reads from a 486, all four DWords of burst data are entered into the cache. Cache validity is maintained on DWord quantities. Refer to Figure 4 for functional timing of a cache read-miss.

## TABLE 1. CACHE RAM SPEED REQUIREMENTS

| Processor | 386DX | | 486 | | | |
|---|---|---|---|---|---|---|
| CPU Frequency | Tag | Data | Tag | Async Data | Sync Data | Unit |
| 33 MHz | 17 | 17 | 17 | 17 | 25 | ns |
| 25 MHz | 25 | 25 | 25 | 25 | 35 | ns |
| 20 MHz | NA | NA | 30 | 30 | 40 | ns |

**FIGURE 3. EXTERNAL LOGIC FOR CACHE BYTE WRITES**



**Cache Write Cycle**
Cache data writes can be done on aligned Word or DWord transfers, or on any write data transfer, depending on the status of the BVALEN bit. (See "Byte/Word Update Capability."). Due to the timing of cacheable range detection, Tag comparison, data validity, and address hold, the write pulse must occur in the first half of the second T2 state. This gives one wait state for cacheable write cycles with a 386DX and with a 486 using asynchronous SRAMs. With a 486 using synchronous SRAMs, the write request is sampled by the SRAMs at the end of the first T2 and the cycle can be completed in zero wait states. Refer to Figure 5 for the functional timing of a cache write.

If BVALEN is inactive, then byte writes to cached locations invalidate the line in the cache and are written only to main memory.

**Cache Read-Hit**
Cache reads occur in zero wait states. Valid range and Tag are checked for every memory read cycle. If a valid range and entry are in the cache, then –RDY is returned to the processor in the first T2. Refer to Figure 6.

**Secondary Cache Initialization**
After a processor reset, the secondary cache must be initialized before use. This can be done by a routine in the BIOS that maps a 128 KB range of memory as cacheable, enabling the cache and reading the memory. This will initialize all locations of the secondary cache. This should also be done if the cacheable ranges are ever modified.

**Cache Peek Cycles**
Peek cycles for a 386DX are initiated by activity on the –MEMW line during a HLDA cycle. The VL82C3216 will detect this case, latch the SX bus address, pass this address to the processor bus and generate a write to that line of the cache with the Tag bit set invalid.

Peek cycles for a 486 are similar with the addition that the processor internal cache must also be invalidated. This is done by asserting –EADS to the 486 with the peek address presented on the processor bus. Figure 7 shows the functional timing of a cache peek cycle for both the 386DX and 486.

**Non-Cacheable Ranges**
The VL82C3216's cacheable address range is from 0 to 16 MB. The VL82C3216 supports one fixed and four selectable non-cacheable regions of memory. The fixed region is defined as that where A31 and A24 are non-zero (area above 16 MB). Each non-cacheable region is defined by a base and limit upper address written in the Control Registers 41h through 4Ch. The base and limit address values are made up of the upper 12 bits of 386SX address (A23-A12). This allows the non-cacheable area to be set in minimum increments of 4 KB on 4K boundaries anywhere in the 386SX 16 MB address space. The four programmable regions are controlled by the registers defined below.

For any non-cacheable range, if the processor address is greater or equal to the base address and less than the limit address then the cycle will not be cached. To turn off any of the programmable non-cacheable ranges, set the limit address to be the same as (or less than) the base address.

**FIGURE 4. CACHE READ-MISS CYCLE**

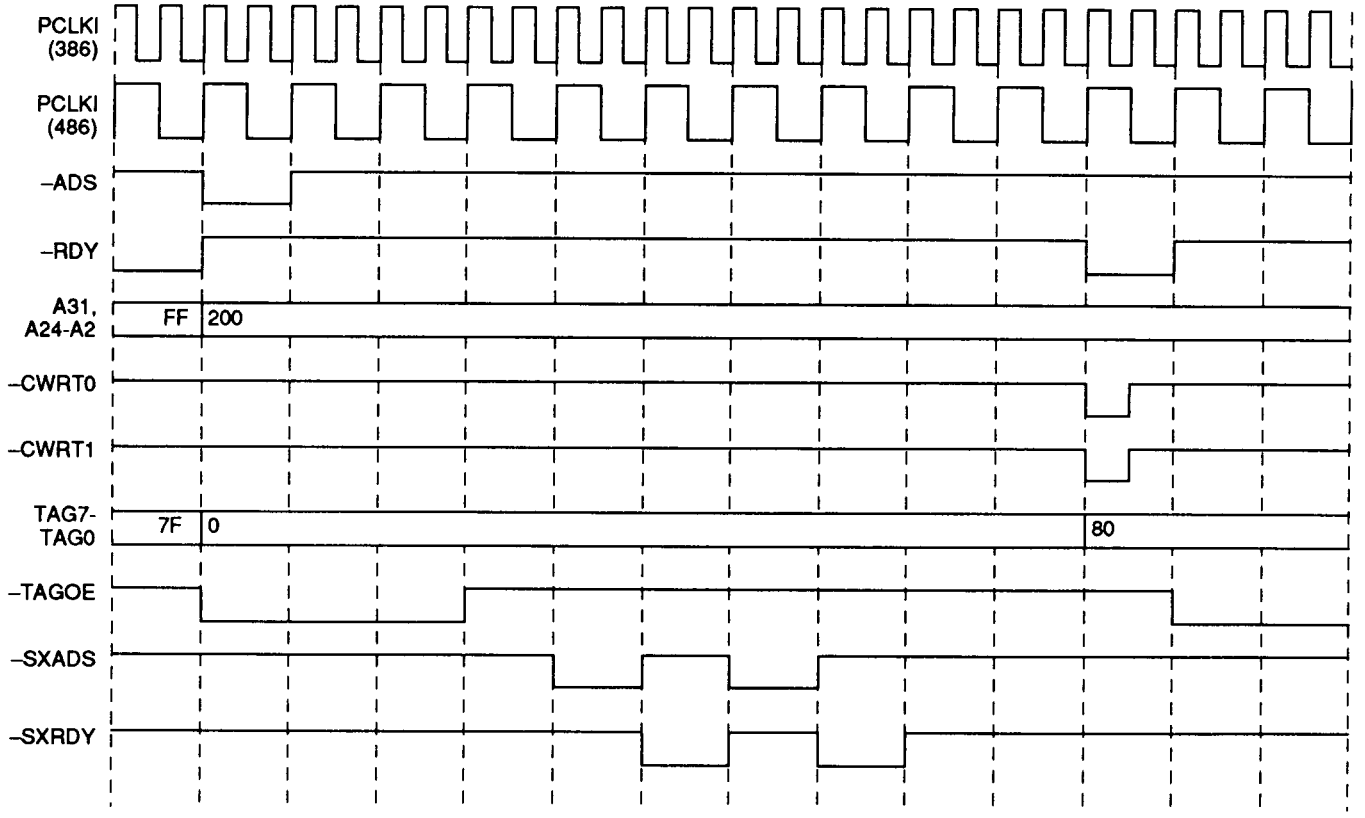



**FIGURE 5. CACHE WRITE CYCLE**

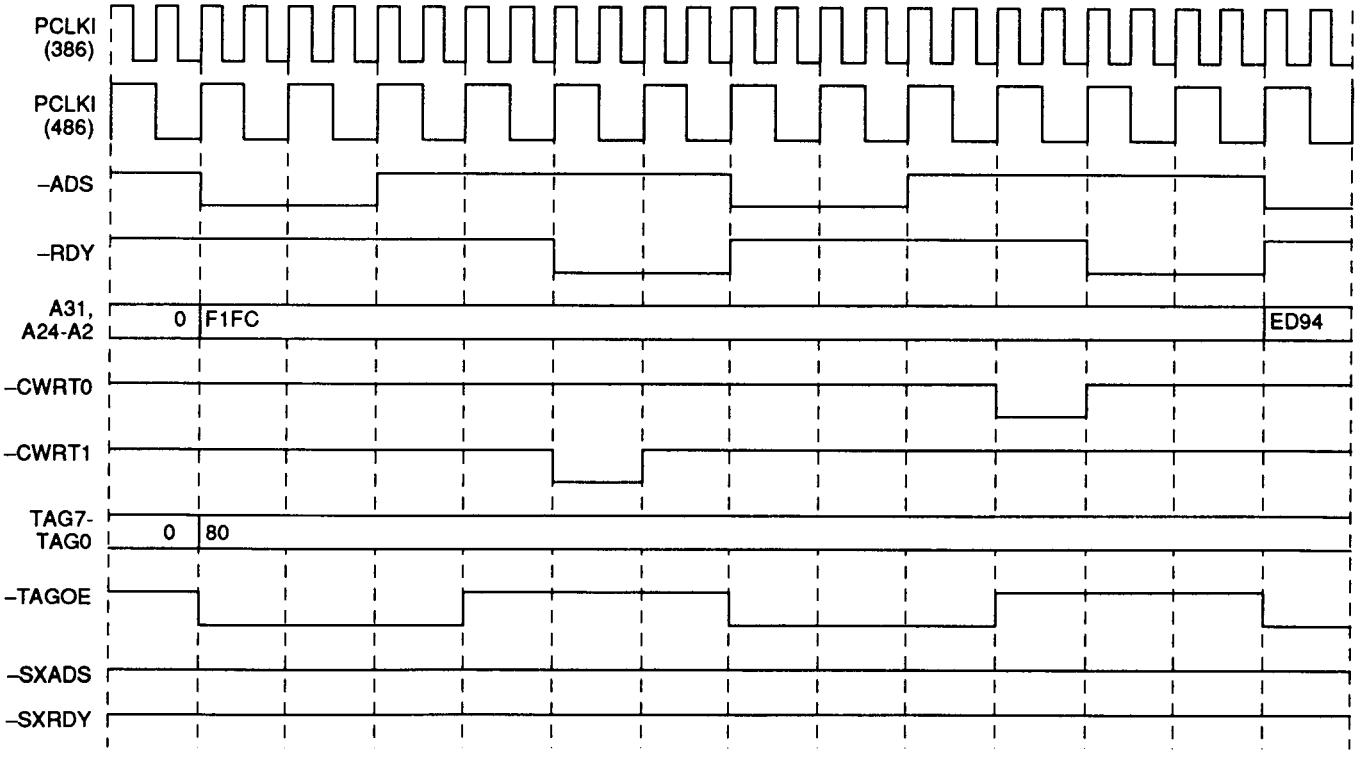


**FIGURE 6. CACHE READ-HIT CYCLE**

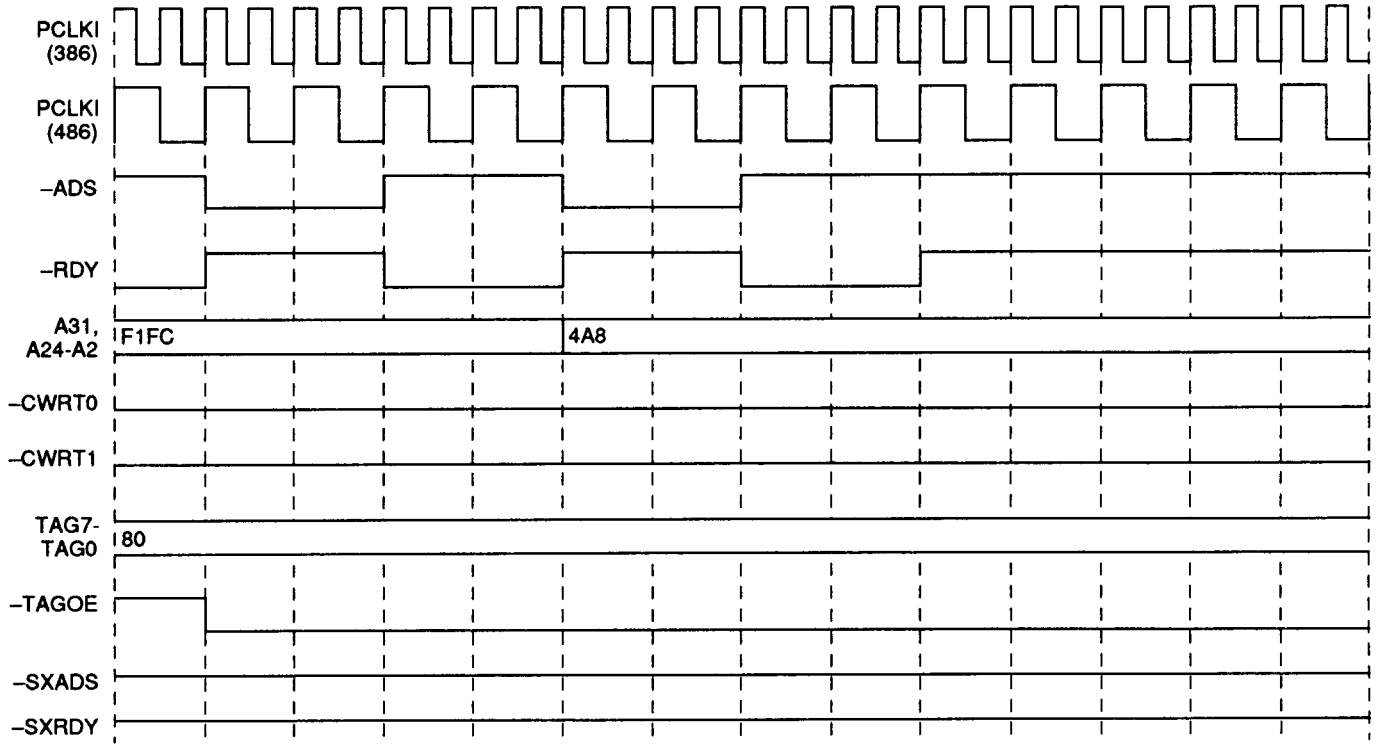
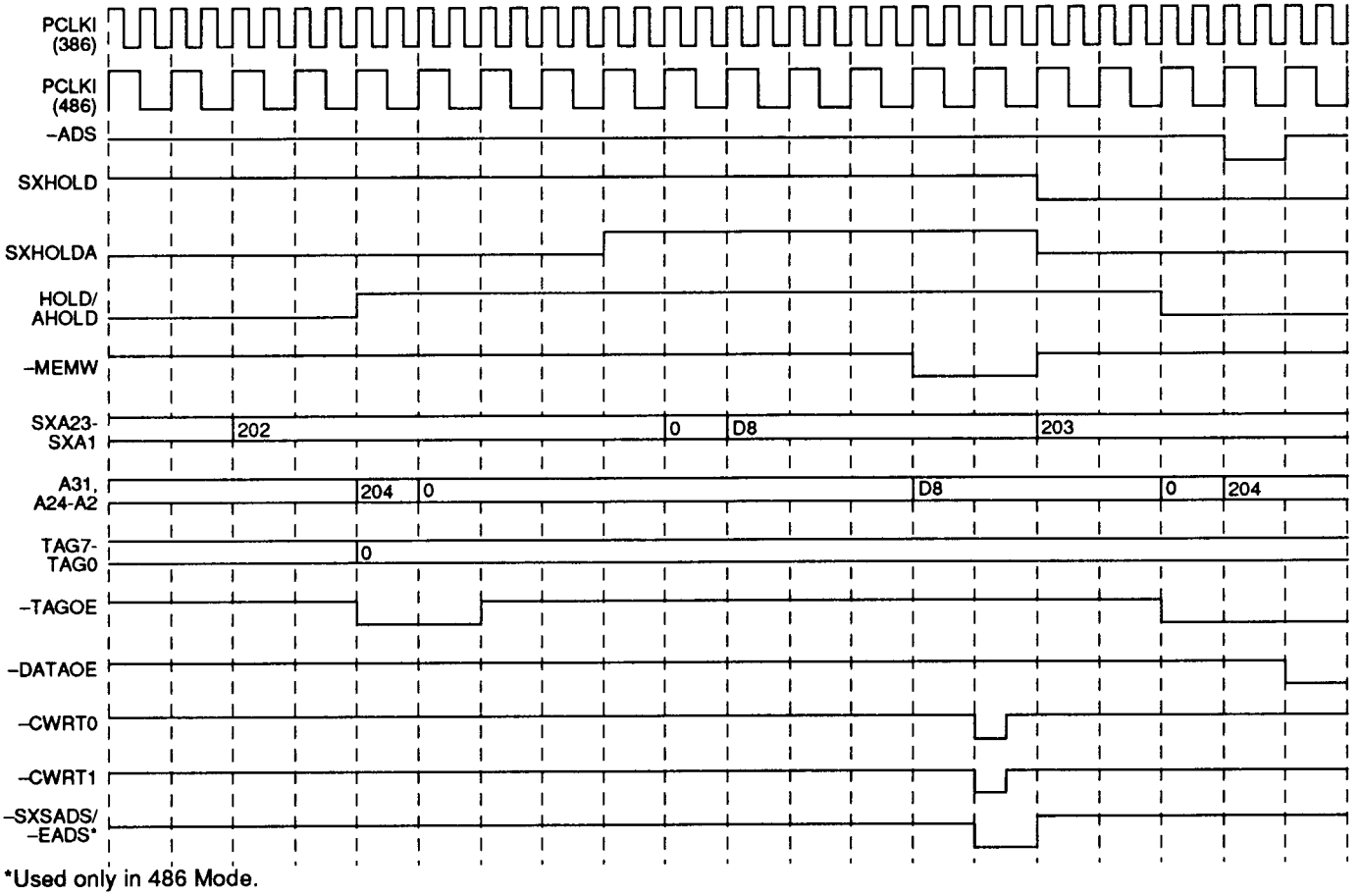



**FIGURE 7. CACHE PEEK CYCLE**




*Used only in 486 Mode.

**NON-CACHEABLE REGION CONFIGURATION REGISTERS (READ/WRITE)**

| Data Port (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| NCxBASEH (41h, 44h, 47h, 4Ah) | BA23 | BA22 | BA21 | BA20 | BA19 | BA18 | BA17 | BA16 |
| POR Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Name | Function |
|---|---|---|
| 7-0 | NCxBASEH | Non-Cache Region Base Address High Order Bits: The upper 8 of 12 high order address bits are programmed into this register and used to determine the base address of a non-cacheable region. The CPU address, A23-A16, are written to this register. The lower four address bits required to define the base of this non-cacheable region are programmed into NCxLMTBASL(3)-NCxLMTBASL(0). |

| Data Port (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| NCxLIMITH (42h, 45h, 48h, 4Bh) | LA23 | LA22 | LA21 | LA20 | LA19 | LA18 | LA17 | LA16 |
| POR Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Name | Function |
|---|---|---|
| 7-0 | NCxLIMITH | Non-Cache Region Limit High Order Bits: The upper 8 of 12 high order address bits are programmed into this register and used to determine the limit of a non-cacheable region. The CPU address, A23-A16, are written to this register. The lower four address bits required to define the limit of this non-cacheable region are programmed into NCxLMTBASL(7)-NCxLMTBASL(4) Note that to disable any of the four non-cacheable areas, it is necessary to set the base address and the limit address to the same value (or program the limit address below the base address). This is done automatically on reset since the default value of these registers is all 0s. |

| Data Port (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| NCxLMTBASL (43h, 46h, 49h, 4Ch) | LA15 | LA14 | LA13 | LA12 | BA15 | BA14 | BA13 | BA12 |
| POR Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Name | Function |
|---|---|---|
| 7-4 | NCxLIMITL | Non-Cache Region Limit Low Order Bits: These four bits are the lower limit address bits of a 12-bit non-cacheable base address (NCxLIMITH + NCxLIMITL) that can be set on 4K boundaries across the entire address range of the 386SX CPU's 16 MB memory space. |
| 3-0 | NCxBASEL | Non-Cache Region Base Address Low Order Bits: These four bits are the lower base address bits of a 12-bit non-cacheable base address (NCxBASEH + NCxBASEL) that can be set on 4K boundaries across the entire address range of the 386SX CPU's 16 MB memory space. In order to form a valid non-chacheable region NCxLIMITH + NCxHLIMITL > NCxBASEH + NCxBASEL. |

**486 Cache**
The 486 cache is enabled by the –KEN signal which is enabled/disabled by the enable internal cache bit (ENKEN) in MCONFIG Control Register (40h). When the 486's cache is enabled, then the VL82C3216's non-cacheable ranges also are in effect for the 486.

**WRITE BUFFER**
The Write Buffer consists of a 16 deep FIFO buffer that captures the address, byte enables (four) and data (Dword) for memory write cycles from the processor. The Write Buffer passes each write command in order through the Command Synchronizer to the 386SX Command FIFO as the pending 386SX commands are executed. If the Write Buffer completely fills up, further writes from the processor wait to complete until a space in the Write Buffer is available.

**Write Buffer Performance**
Writes to the Write Buffer with the cache off, or for cache misses return –RDY to the processor in zero wait states. Writes that hit in the cache have their timing determined by the cache write timing. All writes that are in the Write Buffer will complete to memory as quickly as the SX Interface and memory controller can process them. This allows the 386DX and 486 to operate most of the time at the maximum rate, even though the memory subsystem is an SX-based 16-bit interface. Only when a non-cache cycle occurs, or the Write Buffer fills up, does the processor have to wait for the SX Interface.

Only memory writes occupy the Write Buffer. All other cycles including I/O writes are not buffered, they will complete the cycle before issuing –RDY to the processor.

Any CPU cycle other than cache reads and memory writes waits until the Write Buffer is emptied to complete.

The Write Buffer is enabled by the write buffer enable bit (ENWBF) in the Control Register MCONFIG (40h).

A processor reset resets the Write Buffer and its control logic.

**SX INTERFACE BLOCK**
The SX Interface Block interfaces command requests passed from the processor through the CPU Interface and the Command Synchronizer to the 386SX Bus Emulation Unit. Its command handshake emulates a 386SX processor and is compatible with 386SX system components. It is responsible for completing the command to the SX Bus and returning –SXRDY (and data if required) to the CPU Interface. It is also responsible for passing SXHOLD requests through to the CPU Interface.

**386SX Main State Machine**
The 386SX Main State Machine is the control center for the SX Interface. It acts as a slave to the CPU Main State Machine. It is used to process 386SX commands that are passed to it through the 386SX Command FIFO.

When the 386SX Main State Machine is idle, it waits for a valid command to be present in the 386SX Command FIFO. It determines the command type, memory read or write, I/O read or write, memory burst read, INTA, halt, shutdown or other special cycle and causes the SX Interface to generate the appropriate 386SX signals and sequences. When all of the 386SX cycles required to complete the command have been finished, the 386SX Main State Machine returns to idle to process the next command. A processor reset clears the 386SX Main State Machine and returns it to idle.

**386SX Command FIFO**
The 386SX Command FIFO is the stage that feeds the 386SX Bus Emulation Unit. It receives the synchronized commands from the Command Synchronizer and holds them until completely processed by the 386SX Bus Emulation Unit. To minimize the impact of clock synchronization on command throughput, the 386SX Command FIFO has two stages so the Command Synchronizer can transfer its next command to the empty stage without waiting for the current 386SX command handshake to complete. This acts as a buffer for synchronization purposes and minimizes or eliminates the impact of clock synchronization cycles required on back to back writes, or reads following writes to the SX Interface. The clock synchronization is done when the commands are added to the 386SX Command FIFO. All commands in the 386SX Command FIFO can proceed with no 386SX idle cycles between them.

This is the stage that feeds the 386SX Bus Emulation Unit. On a system or processor reset, it is cleared.

**386SX Bus Emulation Unit**
The 386SX Bus Emulation Unit takes the processor commands that are passed to it from the 386SX Command FIFO and generates the appropriate 386SX control signals, address, and data on the SX Bus to complete the commands. When –SXRDY is returned from the SX Bus, the 386SX Bus Emulation Unit indicates to the 386SX State Machine and the Command Synchronizer that the command is done. The 386SX Bus Emulation Unit is under control of the 386SX Main State Machine.

This 386SX Bus Emulation Unit is tuned to give high performance with Page Mode memory controllers by supporting the 386SX pipelined address mode.

**386SX Bus Emulation Unit Performance**
The 386SX Bus Emulation Unit is capable of zero wait state operation with no latency between cycles for translated DWord to Double Word reads and for 486 burst reads to eight Word reads. It is also capable of zero wait state operation with no latency for write buffer generated sequential write cycles (for as long as the write buffer is occupied). This results in efficient use of the 386SX Bus Emulation Unit and the Page Mode memory controllers generating a much higher percentage of page-hits than with a 386SX processor driving the bus.

Pipeline address generation is supported and gives even higher system performance when used with a memory controller that is compatible.

Pipelined addressing is enabled by the enable next address bit (ENNA), bit 4 in the Control Register MCONFIG (40h).

**OTHER BLOCKS**
In addition to the CPU Interface Block and the SX Interface Block, the Command Synchronizer and Control Register Store Unit complete the VL82C3216 device.

**Command Synchronizer**
The Command Synchronizer provides a synchronization stage for the commands from the CPU Interface to the SX Interface and the following –SXRDY

completion and data from the SX Interface back to the CPU Interface.

The commands from the processor are registered and then clocked synchronously with the 386SX Clock into the 386SX Command FIFO.

**Burst Cycle Synchronization**
For burst read commands, the four Dword read commands that are required are requested by the CPU Main State Machine and passed through the Command Synchronizer. Each Dword read is executed as two Word reads on the 386SX Bus Emulation Unit and the data is passed back and assembled in the Command Synchronizer's data register. For each DWord, the synchronous –BRDY is generated to the processor and the remaining –SXRDY and data transfers are processed.

**Write Cycle Synchronization**
When the Write Buffer contains valid write commands, it unloads those commands through the Command Synchronizer to the 386SX Command FIFO. When a location in the 386SX Command FIFO is empty, the Command Synchronizer transfers the first write command from the Write Buffer to it. Since –RDY has already been given to the processor, there is no return handshake on memory writes. As the next location of the 386SX Command FIFO frees up, the next write is transferred.

**Other Cycle Synchronization**
All other cycles that pass through to the SX Interface simply wait until the Write Buffer is empty and a location in the 386SX Command FIFO is available, then they are synchronized to the 386SX Command FIFO. Upon completion of the 386SX cycle, –SXRDY and data are synchronized back to the processor.

**Control Register Store Unit**
The Control Register Store Unit consists of 17 single byte registers that configure and enable features of the VL82C3216 device. These registers are individually described in detail where applicable throughout this document. They are all summarized in Table 4. The registers are accessed through an Index Register and Data Register combination located in I/O address space.

A system reset (RSTDRV) initializes the VL82C3216 Control Registers and Index Register.

The Main Configuration Register of the VL82C3216 is the MCONFIG Register. It is used to enable or disable most of the key features of the chip.

**MCONFIG REGISTER DESCRIPTION (READ/WRITE)**

| Data Port (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| MCONFIG (40h) | ENKEN | ENCCH | ENWBF | ENNA | WRWS | EN486SYNC | BVALEN | R |
| POR Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bit | Name | Function |
|---|---|---|
| 7 | ENKEN | Enable –KEN: Cache Enable to the 486 when set to 1. In 386DX Mode this bit has no effect. |
| 6 | ENCCH | Enable Second Level Cache when set to 1. |
| 5 | ENWBF | Enable Write Buffer when set to 1. |
| 4 | ENNA | Enable Next Address Mode: Used to control the Pipeline Mode of the 386SX Interface both in 386DX and 486 Modes. When 1, the SX Interface Side is run in Pipeline Mode, whenever possible, on memory cycle. When 0, the SX Interface Side is always run in Non-Pipelined Mode. I/O cycles are always in Non-Pipelined Mode. |
| 3 | WRWS | Write Cycle Wait States: When set to 1, one wait state write cycles are run to the cache. Zero wait state cycles are run for 486 Mode only, if the bit is changed to 0 and synchronous SRAMs are selected. Read cycles and non-cached writes are in zero wait state cycles. |
| 2 | EN486SYNC | Enable 486 Synchronous SRAM: Used to indicate that synchronous data SRAMs are used for the 486 secondary cache. This redefines the cache write signals from –CWRT1 and –CWRT0 to –TAGOE and –DATAOE. |
| 1 | BVALEN | Enable Byte Write Validates to Second Level Cache: Due to pin limitations, only two cache write signals are supported. This means that without an external TTL package, a byte access must cause an invalidate cycle for the entire DWord which contains that byte in the external cache. However, it is possible to support byte writes to cache via external logic. If that is done, the byte write validation is enabled by setting this bit to 1. |
| 0 | R | Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always maintain its previous value during a write operation. |

## VL82C3216 CLOCK CONTROL

As controller, arbiter, and overall system monitor, the VL82C3216 controls clock generation for both the processor and system interface. It can stop the clocks on the CPU Interface, SX Interface or both based on internal system activity monitors. Programming of the nominal clock frequencies is done by the BIOS power management software.

### Clock Modes

1. Synchronous Clock Mode: Figure 8 shows the clock routing for this mode. A single oscillator is used. The VL82C3216 sources the clocks to the CPU and its own internal logic after applying the programmed internal dividers for each interface. The VL82C3216 also sources a clock for the TCLK2 signal out of the VL82C3216.
2. Asynchronous Clock Mode: Figure 9 shows the clock connections for the Asynchronous Mode. Separate external oscillators are used for the CPU and system clocks. The VL82C3216 sources the clocks to the CPU and its own internal logic after applying the programmed internal dividers for each interface. The 386SX chip set's TCLK2IN signal is taken directly from SXOSC.

### Clock Divider Options

The VL82C3216 controls the clocks to both the CPU Interface and the 386SX Interface. Several dividers are required in order to:

1. maintain the system clock at or below CPU clock frequencies,
2. provide optimum power management, and
3. support older software requiring Non-Turbo Mode.

When programmed in the proper combinations, a wide range of possibilities is provided from stop clock to CPU maximum frequency for 386DX-, 486DX-, and 486SX-based systems in the 20 to 40 MHz range.

### Selection of Synchronous Vs Asynchronous System Clocks

The VL82C3216 can operate in either the Synchronous or Asynchronous Clock Mode. A jumper on pin 122 (SXHLDA) is used to select either mode at the falling edge of RSTDRV according to the following definition:

| SXHLDA State | Clock Mode |
|---|---|
| Logic 0 | Synchronous Clock Mode - System clocks are derived from the CPU clock frequency. |
| Logic 1 | Asynchronous Clock Mode - System clocks are derived from an external oscillator. |

### System Clock Divider (Synchronous Clock Option)

If the VL82C3216 is configured into the Synchronous Clock Mode, an external jumper on pin 152 (–RDY) is used to select a +1 or +2 system clock input frequency which is driven out on SXCLKO. The +2 option is used when POSC is greater than 50 MHz. The +1 option is used when POSC is equal to or less than 50 MHz. These are the only two possible values for the system clock (SXCLKO) frequency in this mode.

| –RDY State | Synchronous Clock Mode |
|---|---|
| Divider | |
| Logic 0 | System clock frequency is +1 of the CPU clock frequency. |
| Logic 1 | System clock input frequency is a +2 of the CPU clock frequency. |

### Laptop/Desktop Features

The state of pin 145 (–SRDY/–KEN) is latched on the falling edge of RSTDRV. When low, Desktop Mode is active. When high, Laptop Mode is active. In Desktop Mode, programming the Sleep Mode clock dividers and stop clock bits in the CPUCLKCTK and SXCLKCTL Registers has no effect. The –SXSLEEP/TURBO pin (pin 133) is configured as a TURBO input. Therefore, an external source for controlling the Turbo Mode is added to the internal sources.

**FIGURE 8. VL82C3216 SYNCHRONOUS CLOCK CONNECTIONS**

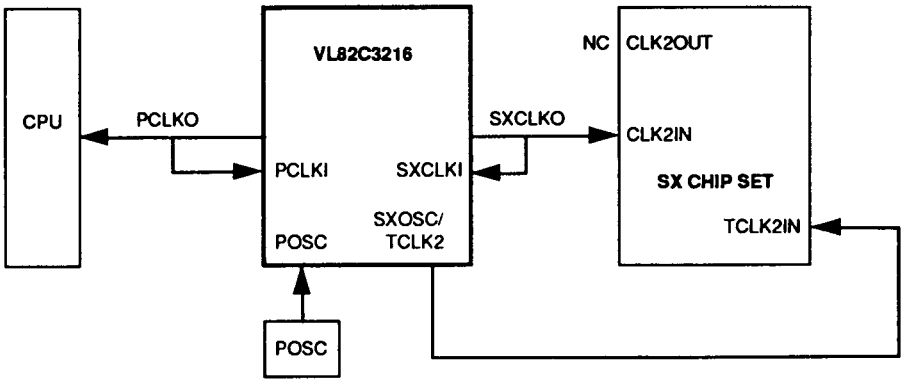
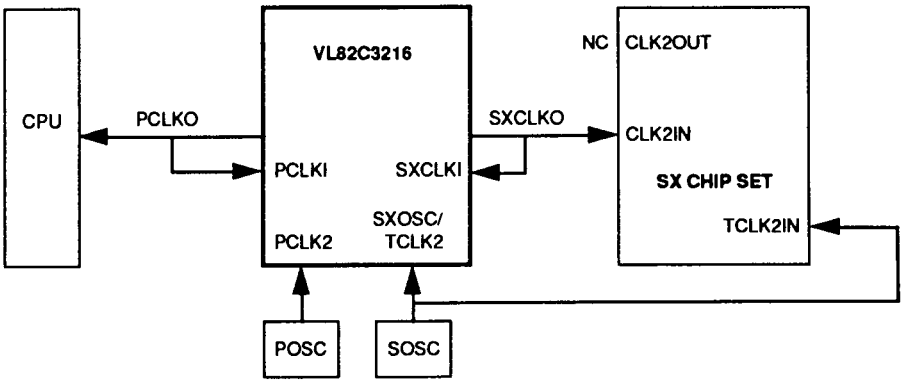



**FIGURE 9. VL82C3216 ASYNCHRONOUS CLOCK CONNECTIONS**



**Non-Turbo Clock Dividers (386DX Mode Only)**
Two non-turbo dividers are used to divide the clock frequency for speed sensitive software applications. Dividers are included on both the CPU Interface and SX Interface to accomplish this task. For desktop systems, a TURBO pin is required in order to accommodate an external turbo switch The VL82C3216 also emulates the keyboard Turbo command (write to port 64h).

**Divider Options:**
+1, +3, +4, +5 CPU Clock
+1, +3, +4, +5 System Clock

**Non-Turbo Mode for Current 486-Based Systems**
CPU clock switching is not used as a non-turbo option in the 486 Mode. Operation at minimum 486 CPU frequency still provides excessive performance for non-turbo operation. Therefore, when this mode is activated by any of the enabled methods, the VL82C3216 generates continuous invalidates (via –EADS). The SX Interface's non-turbo divider is still active in Non-Turbo Mode. The CPU non-turbo divider is used to determine the duty cycle of the –EADS modulation required to approximate the performance of a 386DX system whose clock is divided by the programmed amount.

**Sleep Mode Clock Dividers**
Two Sleep Mode clock dividers are used to divide the clock frequency for low-power operation. Clock dividers are included on both the CPU Interface and SX Interface to maintain the CPU frequency at or above the system clock frequency in all cases. (The only exception is if the CPU clock is stopped.) Driving the –SLEEP pin is required in order to simultaneously invoke the dividers.

**Divider Options:**
+1, +2, +3, +4, +5, +8, +16, +32 CPU Clock
+1, +2, +3, +4, +5, +8, +16, +32 System Clock

**CPU CLOCK CONTROL REGISTER (READ/WRITE)**

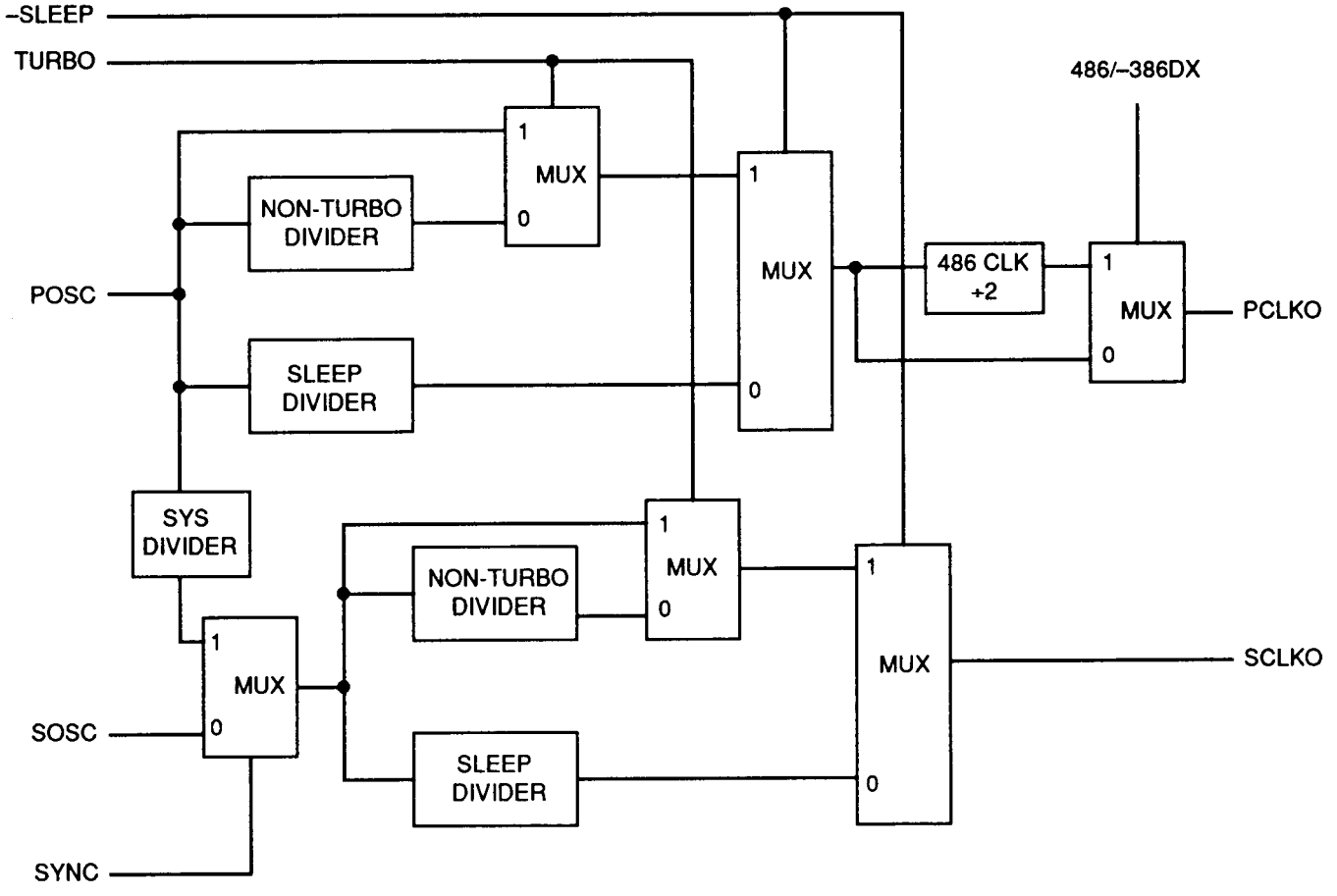
| Data Port (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| CPUCLKCTL (4Dh) | CPUSTP | CCLKDV | R | NTDIV1 | NTDIV0 | SLPDIV2 | SLPDIV1 | SLPDIV0 |
| POR Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Name | Function |
|---|---|---|
| 7 | CPUSTP | Clock Stop: If set to 1, the CPU clock stops regardless of the divider, even if in the Sleep Mode. If 0, the CPU clock is running at the Sleep divider setting. This bit only has effect in the Sleep Mode. |
| 6 | CCLKDV | Clock Divider : This bit is the CPU Sleep Mode clock divider for 486 operations. Normally, there is a fixed +2 in the CPU clock path for 486 systems. This bit, once set, allows this stage to be bypassed during the Sleep Mode so that the CPU frequency can be 8 MHz for lowest power operation (e.g., 20 MHz 486 CPU). When 0, the CPU clock is +2 for 486 systems. When set 1, the CPU clock is +1 for 486 systems (Sleep Mode). |
| 5 | R | Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always maintain its previous value during a write operation. |
| 4, 3 | NTDIV1, NTDIV0 | Non-Turbo Mode Divider: Defined as follows - **Bit 4 / Bit 3 / Meaning**: 0 0 +1; 0 1 +3; 1 0 +4; 1 1 +5 |
| 2-0 | SLPDIV2-SLPDIV0 | Sleep Mode Divider: Defined as follows - **Bit 2 / Bit 1 / Bit 0 / Meaning**: 0 0 0 +1; 0 0 1 +2; 0 1 1 +3; 0 1 1 +4; 1 0 0 +5; 1 0 1 +8; 1 1 0 +16; 1 1 1 +32 |

Separate control bits allow the selection of the Static Clock Mode no matter how the divider is programmed when in the Sleep Mode.

**VL82C3216 Stop Clock Operation**
By setting bit 7 (CPUSTP) of the CPUCLKCTL Register (4Dh) and bit 7 (SXSTP) of the SXCLKCTL Register (4Eh), it is possible to stop the clocks for both the CPU and SX interface for reduced power consumption (Static Clock Mode). If the –SLEEP pin is driven low after programming these bits to logic one, the VL82C3216 waits for a hold request from the chip set (to service a DRAM refresh, for example). A hold acknowledge is granted to the chip set before stopping the SX clock. If programmed, the CPU clock is stopped following the SX clock (the CPU clock speed must always be equal to or greater than the SX clock speed). A low-to-high transition on the –SXSLEEP input would immediately trigger the VL82C3216 to restart both clocks. During peek cycles (e.g. DMA) in the Stop Clock Mode, the SX addresses and write strobe are passed through asynchronously to the CPU Interface Block for cache invalidation.

**FIGURE 10. CLOCK CONTROL BLOCK DIAGRAM**



**SYSTEM CLOCK CONTROL REGISTER (READ/WRITE)**

| Data Port (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| SXCLKCTL (4Eh) | SXSTP | SCLKDV | R | NTDIV1 | NTDIV0 | SLPDIV2 | SLPDIV1 | SLPDIV0 |
| POR Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Name | Function |
|---|---|---|
| 7 | SXSTP | System Clock Stop: If set to 1, the system clock stops regardless of the divider, even if in the Sleep Mode. If 0, the system clock is running at the Sleep divider setting when in the Sleep Mode. |
| 6 | SCLKDV | Synchronous Clock Mode Divider : When 0, the system clock (SXCLKO) is +1. When set 1, the system clock is +2. This bit has no effect in the Asynchronous Mode. |
| 5 | R | Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always maintain its previous value during a write operation. |
| 4, 3 | NTDIV1, NTDIV0 | Non-Turbo Mode Divider: Defined as follows - **Bit 4 / Bit 3 / Meaning**: 0 0 +1; 0 1 +3; 1 0 +4; 1 1 +5 |
| 2-0 | SLPDIV2-SLPDIV0 | Sleep Mode Divider: Defined as follows - **Bit 2 / Bit 1 / Bit 0 / Meaning**: 0 0 0 +1; 0 0 1 +2; 0 1 1 +3; 0 1 1 +4; 1 0 0 +5; 1 0 1 +8; 1 1 0 +16; 1 1 1 +32 |

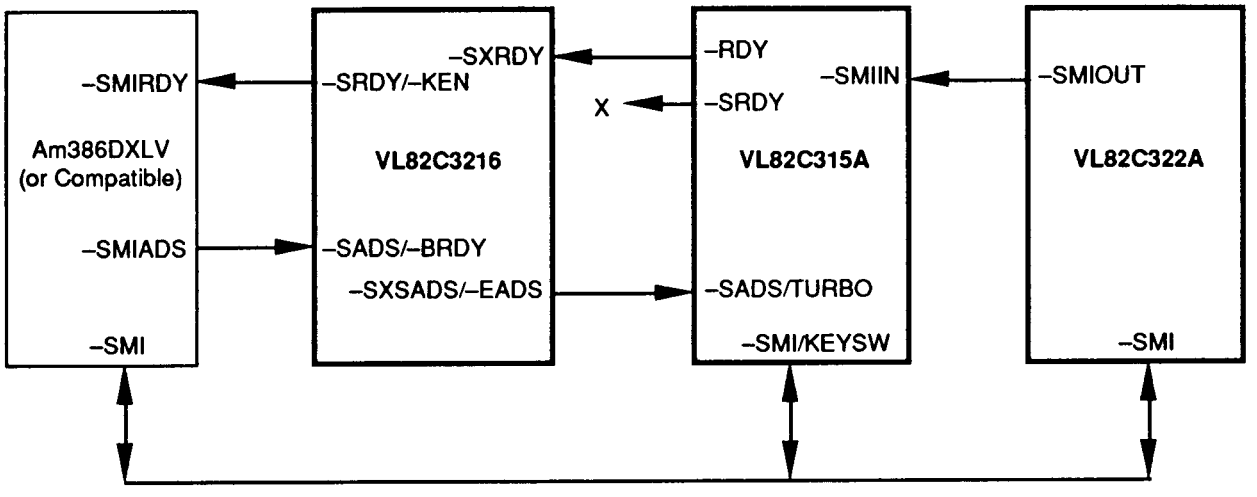
**SYSTEM MANAGEMENT MODE (SMM)**

The VL82C3216 supports the Am386DXLV or compatible processors in conjunction with 386SX chip sets that support the System Management Mode (SMM) features such as the VL82C315 SCAMP II Controller. When the VL82C3216 sees a cycle that starts via the –SADS signal rather than via the –ADS signal, a non-cache cycle results. The cycle is passed to the SX Interface and –SXSADS is driven rather than –SXADS. When the –SXRDY input is activated by the SX Interface for a –SXSADS initiated cycle, the VL82C3216 drives the –SRDY output to the 386DX rather than the normal –RDY output.

The VL82C3216 does not monitor or drive the –SMI (System Management Interrupt) signal. –SMI connects directly from the CPU to the SX Interface.

Figure 11 shows how to connect an Am386DXLV or compatible processor, the VL82C3216 Cache Controller and Interface Unit, the VL82C315 SCAMP II Controller, and the VL82C322 Power Management Unit for SMM support. Refer to the VL82C315 data manual for detailed capabilities of the SMI features.

**FIGURE 11. CONNECTION OF SMI INTERFACE SIGNALS**



**VLSI SPECIAL FEATURES (VSF) REGISTERS**
**MISCSET (WRITE-ONLY) (Monitoring for VSF Access)**

| Data Port EDh | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET (14h) | –VSF | X | X | X | X | X | X | X |
| POR Value | 0 | X | X | X | X | X | X | X |

Reads and writes to the MISCSET Register are always passed through to the SX Interface. However, on writes to the MISCSET Register, the state of bit 7 is latched in the VL82C3216 for the purpose of allowing the VSF features at I/O port registers EDh, F4h, F5h, to be enabled and disabled. The VL82C3216 will not drive the D bus on a read of this register. The default value of 0 enables the internal VSF features.

**VERIDSTAT (READ-ONLY)**

| Data Port EDh | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| VERIDSTAT (4Fh) | REV1 | REV0 | ID3 | ID2 | ID1 | ID0 | R | TURBO |
| POR Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

D7 and D6 contain the version number of this chip. D5-D3 contains a read-only code which indicates that this part is a VLSI Technology, Inc. device. By using this byte, a customized BIOS can compensate for "feature" differences based on the version number.

D0 reflects the current state of the TURBO pin.

## CONTROL REGISTER SUMMARY

The registers and features described next are a fully compatible superset of the VLSI Special Features (VSF). All port decodes used between E8h and FFh are shown in Table 2.

## TABLE 2. DEDICATED CONTROL REGISTERS

| Port Address | Function |
|---|---|
| ECh | Configuration Index Register |
| EDh | Configuration Data Port |
| F4h* | Slow CPU |
| F5h* | Fast CPU |
| F9h* | Configuration Disable |
| FBh* | Configuration Enable |

*Can be disabled in case of a conflict by setting bit 7 (–VSF) of the MISCSET Register to a 1.

### CONFIGURATION INDEX PORT REGISTER (READ/WRITE)

| ECh | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Config. Index | X | X | X | X | X | X | X | X |

The Index Register is a byte wide read/write register that determines which of the Control/Configuration Registers in the system is currently accessed through the Data Port Register at I/O address EDh.

I/O writes to the Index Register update the contents of the VL82C3216 Index Register and are also passed through the SX Interface. I/O writes to the Index Register and I/O reads or writes to the Data Port Register are completed by the VL82C3216 if a VL82C3216 register is currently indexed by the Index Register, otherwise the I/O command will be passed to the system through the SX Interface.

### CONFIGURATION DATA PORT REGISTER (READ/WRITE)

| EDh | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Config. Data | X | X | X | X | X | X | X | X |

The registers accessible through I/O address EDh are summarized in Table 4. They are accessed by writing their addresses to the Index Register at I/O address ECh, then by accessing the Data Port Register at I/O address EDh.

### CPU SPEED CONTROL REGISTERS (WRITE-ONLY)

| F4h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Non-Turbo Clock | X | X | X | X | X | X | X | X |

| F5h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Turbo Clock | X | X | X | X | X | X | X | X |

A write to port F5h causes the CPU to run at normal "fast" speed. A write to port F4h invokes the non-turbo clock divider circuits. These dividers are set by writing the appropriate code to the NTDIV bits in the SXCLKCTL and CCLKCTL Registers. Default on reset is "fast" speed.

The CPU Speed Control Registers are controlled by bit 7 (–VSF) in the MISCSET Register. –VSF should be 0 to enable these registers. However, if –VSF is disabled, it is still possible to control the CPU speed with the keyboard controller if allowed by the BIOS. Also, when the Desktop Mode is enabled, the Non-Turbo Mode can be invoked by externally pulling the TURBO pin low.

An I/O write to either F4h or F5h is also passed through to the SX Interface. An I/O read operation on these two I/O port addresses is also passed through to the SX Interface. The SX Interface must respond to the read. The VL82C3216 does not drive the data bus.

### CONFIGURATION ENABLE/DISABLE REGISTERS (WRITE-ONLY)

| FBh | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Config. Enable | X | X | X | X | X | X | X | X |

| F9h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Config. Disable | X | X | X | X | X | X | X | X |

When enabled and used as described below, the Configuration Registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to FBh enables the Configuration Registers. A write to F9h disables the Configuration Registers (as per Table 3).

An I/O write to either FBh or F9h is also passed through to the SX Interface Side. An I/O read operation on these two I/O port addresses is also passed through to the SX Interface. The SX Interface must respond to the read. The VL82C3216 does not drive the data bus.

## TABLE 3. REGISTERS AFFECTED BY CONFIGURATION DISABLE COMMAND

| Port Address | Function | VSF Enabled | VSF Disabled |
|---|---|---|---|
| ECh | Configuration Index Register | Read/Write | Read/Write |
| EDh | Configuration Data Port | Read/Write | Read-Only |
| F4h | Slow CPU | Write-Only | Inaccessible |
| F5h | Fast CPU | Write-Only | Inaccessible |
| F9h | Configuration Disable | Write-Only | Write-Only |
| FBh | Configuration Enable | Write-Only | Write-Only |

**Note:** If an F9h disable command is followed by a write of "1" to bit 7 (–VSF) of the MISCSET Register, the configuration disable feature triggered by the write to F9h is overridden. When VSF features are disabled, accesses to F4h, F5h, F9h, and FBh have no affect and ECh/EDh accesses are read/write.

## TABLE 4. INDEXED CONFIGURATION REGISTER MAP

| Index Port | | (ECh) | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Data Port | | (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MISCSET | (W-O) | (14h) | -VSF | R | R | R | R | R | R | R |
| MCONFIG | (R/W) | (40h) | ENKEN | ENCCH | ENWBF | ENNA | WRWS | EN486SYNC | BVALEN | R |
| NC1BASEH | (R/W) | (41h) | BA23 | BA22 | BA21 | BA20 | BA19 | BA18 | BA17 | BA16 |
| NC1LIMITH | (R/W) | (42h) | RA23 | RA22 | RA21 | RA20 | RA19 | RA18 | RA17 | RA16 |
| NC1LMTBASL | (R/W) | (43h) | RA15 | RA14 | RA13 | RA12 | BA15 | BA14 | BA13 | BA12 |
| NC2BASEH | (R/W) | (44h) | BA23 | BA22 | BA21 | BA20 | BA19 | BA18 | BA17 | BA16 |
| NC2LIMITH | (R/W) | (45h) | RA23 | RA22 | RA21 | RA20 | RA19 | RA18 | RA17 | RA16 |
| NC2LMTBASL | (R/W) | (46h) | RA15 | RA14 | RA13 | RA12 | BA15 | BA14 | BA13 | BA12 |
| NC3BASEH | (R/W) | (47h) | BA23 | BA22 | BA21 | BA20 | BA19 | BA18 | BA17 | BA16 |
| NC3LIMITH | (R/W) | (48h) | RA23 | RA22 | RA21 | RA20 | RA19 | RA18 | RA17 | RA16 |
| NC3LMTBASL | (R/W) | (49h) | RA15 | RA14 | RA13 | RA12 | BA15 | BA14 | BA13 | BA12 |
| NC4BASEH | (R/W) | (4Ah) | BA23 | BA22 | BA21 | BA20 | BA19 | BA18 | BA17 | BA16 |
| NC4LIMITH | (R/W) | (4Bh) | RA23 | RA22 | RA21 | RA20 | RA19 | RA18 | RA17 | RA16 |
| NC4LMTBASL | (R/W) | (4Ch) | RA15 | RA14 | RA13 | RA12 | BA15 | BA14 | BA13 | BA12 |
| CPUCLKCTL | (R/W) | (4Dh) | CPUSTP | CCLKDV | R | NTDIV1, NTDIV0 | | SLPDIV2-SLPDIV0 | | |
| SXCLKCTL | (R/W) | (4Eh) | SXSTP | SCLKDV | R | NTDIV1, NTDIV0 | | SLPDIV2-SLPDIV0 | | |
| VERIDSTAT | (R-O) | (4Fh) | REVISION | | ID | | | | R | TURBO |

**Note:** Bits denoted as "R" are reserved. No guarantee is made as to their value on a read. For compatibility, these bits should always be written back to the same state they were in prior to the write.

MISCSET is write-only and is used to monitor bit 7 for determination of Special Features enable/disable.

Index Register values 50h through 5Fh are reserved and are decoded by the VL82C3216 as a valid access. Data returned on reads to this space is not defined.

## TABLE 5. INDEXED CONFIGURATION REGISTER RESET VALUES

| Index Port | | (ECh) | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Data Port | | (EDh) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MISCSET | (W-O) | (14h) | 0 | R | R | R | R | 0 | R | R |
| MCONFIG | (R/W) | (40h) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | R |
| NC1BASEH | (R/W) | (41h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC1LIMITH | (R/W) | (42h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC1LMTBASL | (R/W) | (43h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC2BASEH | (R/W) | (44h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC2LIMITH | (R/W) | (45h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC2LMTBASL | (R/W) | (46h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC3BASEH | (R/W) | (47h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC3LIMITH | (R/W) | (48h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC3LMTBASL | (R/W) | (49h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC4BASEH | (R/W) | (4Ah) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC4LIMITH | (R/W) | (4Bh) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC4LMTBASL | (R/W) | (4Ch) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CPUCLKCTL | (R/W) | (4Dh) | 0 | 0 | R | 0 | 0 | 0 | 0 | 0 |
| SXCLKCTL | (R/W) | (4Eh) | 0 | 0 | R | 0 | 0 | 0 | 0 | 0 |
| VERIDSTAT | (R-O) | (4Fh) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note:** Bits denoted as "R" are reserved. No guarantee is made as to their value on a read. For compatibility, these bits should always be written back to the same state they were in prior to the write.

MISCSET is write-only and is used to monitor bit 7 for determination of VLSI Special Features enable/disable.

## AC CHARACTERISTICS:

3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V
5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V

| Symbol | Parameter | 25 MHz | | 33 MHz | | 40 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| **386DX Interface - Clock Timing, See Figure 12** | | | | | | | | | |
| t1 | POSC Period | 20.0 | | 15.0 | | 12.5 | | ns | |
| t2a | POSC High | 7.0 | | 6.0 | | 5.0 | | ns | VIL=VIH=VDD/2 |
| t2b | POSC Low | 7.0 | | 6.0 | | 5.0 | | ns | VIL=VIH=VDD/2 |
| t3a | POSC Rise Time | 5.0 | | 4.0 | | 4.0 | | ns | 30% to 70%*VDD |
| t3b | POSC Fall Time | 5.0 | | 4.0 | | 4.0 | | ns | 70% to 30%*VDD |
| t4a | PCLKI High | 7.0 | | 6.0 | | 5.0 | | ns | VIL=VIH=VDD/2 |
| t4b | PCLKI Low | 7.0 | | 6.0 | | 5.0 | | ns | VIL=VIH=VDD/2 |
| t5a | PCLKO Fall Time | | 5.0 | | 4.0 | | 4.0 | ns | CL=50 pF<br>70% to 30%*VDD |
| t5b | PCLKO Rise Time | | 5.0 | | 4.0 | | 4.0 | ns | CL=50 pF<br>30% to 70%*VDD |
| t6 | POSC to PCLKO | 3.0 | 35.0 | 3.0 | 30.0 | 3.0 | 25.0 | ns | CL=50 pF |
| **386DX Interface - Bus Interface Timing, See Figures 13, 14, 15, & 16** | | | | | | | | | |
| tSU10a | A31, A24-A2 Setup Time to PCLKI | 19.0 | | 15.0 | | 12.0 | | ns | |
| tH10b | A31, A24-A2 Hold Time from PCLKI | 4.0 | | 4.0 | | 4.0 | | ns | |
| tSU11a | –BE3 - –BE0 Setup Time to PCLKI | 16.0 | | 15.0 | | 12.0 | | ns | |
| tH11b | –BE3 - –BE0 Hold Time from PCLKI | 4.0 | | 4.0 | | 4.0 | | ns | |
| tSU12a | W/–R, M/–IO, D/–C Setup Time to PCLKI | 19.0 | | 15.0 | | 12.0 | | ns | |
| tH12b | W/–R, M/–IO, D/–C Hold Time from PCLKI | 4.0 | | 4.0 | | 4.0 | | ns | |
| tSU13a | –ADS Setup Time to PCLKI | 19.0 | | 15.0 | | 12.0 | | ns | |
| tH13b | –ADS Hold Time from PCLKI | 4.0 | | 4.0 | | 4.0 | | ns | |

## AC CHARACTERISTICS:

**3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V**
**5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V**

| Symbol | Parameter | 25 MHz | | 33 MHz | | 40 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| **386DX Interface - Bus Interface Timing, See Figures 13, 14, 15, & 16 (Cont.)** | | | | | | | | | |
| tSU14a | D31-D0 Setup Time to PCLKI | 13.0 | | 6.0 | | 6.0 | | ns | |
| tH14b | D31-D0 Hold Time from PCLKI | 2.0 | | 2.0 | | 2.0 | | ns | |
| tSU15a | HLDA Setup Time to PCLKI | 18.0 | | 10.0 | | 8.0 | | ns | |
| tH15b | HLDA Hold Time from PCLKI | 4.0 | | 4.0 | | 4.0 | | ns | |
| tSU16a | –SADS Setup Time to PCLKI | 15.0 | | 15.0 | | 12.0 | | ns | |
| tH16b | –SADS Hold Time from PCLKI | 4.0 | | 4.0 | | 4.0 | | ns | |
| tD20 | –RDY Valid Delay from PCLKI | 4.0 | 31.0 | 4.0 | 23.0 | 4.0 | 18.0 | ns | CL=50 pF |
| tD21 | –SRDY Valid Delay from PCLKI | 4.0 | 31.0 | 4.0 | 23.0 | 4.0 | 18.0 | ns | CL=50 pF |
| tD22a | D31-D0 Read Valid Delay from PCLKI | 5.0 | 33.0 | 4.0 | 25.0 | 4.0 | 21.0 | ns | CL=50 pF |
| tD22b | D31-D0 Float Delay from PCLKI | 4.0 | 25.0 | 4.0 | 20.0 | 4.0 | 20.0 | ns | CL=50 pF |
| tD23 | HOLD Valid Delay from PCLKI | 3.0 | 25.0 | 3.0 | 19.0 | 3.0 | 17.0 | ns | CL=50 pF |
| tD24 | RESCPU Valid Delay from PCLKI | 3.0 | 10.0 | 3.0 | 10.0 | 3.0 | 8.5 | ns | CL=30 pF |
| tD25 | RESNPX Valid Delay from PCLKI | 3.0 | 10.0 | 3.0 | 10.0 | 3.0 | 8.5 | ns | CL=30 pF |

## AC CHARACTERISTICS:

**3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V**
**5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V**

| Symbol | Parameter | 25 MHz | | 33 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **486SX/DX Interface - Clock Timings See Figure 12** | | | | | | | |
| t1 | POSC Period | 40.0 | | 30.0 | | ns | |
| t2a | POSC High | 14.0 | | 11.0 | | ns | VIL=VIH=VDD/2 |
| t2b | POSC Low | 14.0 | | 11.0 | | ns | VIL=VIH=VDD/2 |
| t3a | POSC Rise Time | 4.0 | | 3.0 | | ns | 30% to 70%*VDD |
| t3b | POSC Fall Time | 4.0 | | 3.0 | | ns | 70% to 30%*VDD |
| t4a | PCLKI High | 14.0 | | 11.0 | | ns | VIL=VIH=VDD/2 |
| t4b | PCLKI Low | 14.0 | | 11.0 | | ns | VIL=VIH=VDD/2 |
| t5a | PCLKO Fall Time | | 4.0 | | 3.0 | ns | CL=50 pF. 70% to 30%*VDD |
| t5b | PCLKO Rise Time | | 4.0 | | 3.0 | ns | CL=50 pF. 30% to 70%*VDD |
| t6 | POSC to PCLKO | 3.0 | 35.0 | 3.0 | 30.0 | ns | CL=50 pF |
| **486SX/DX Interface - Bus Interface Timing, See Figures 13, 14, 15, 16, & 17** | | | | | | | |
| tSU10a | A31, A24-A2 Setup Time to PCLKI | 18.0 | | 14.0 | | ns | |
| tH10b | A31, A24-A2 Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tSU11a | –BE3 - –BE0 Setup Time to PCLKI | 18.0 | | 14.0 | | ns | |
| tH11b | –BE3 - –BE0 Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tSU12a | W/–R, M/–IO, D/–C Setup Time to PCLKI | 18.0 | | 14.0 | | ns | |
| tH12b | W/–R, M/–IO, D/–C Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tSU13a | –ADS Setup Time to PCLKI | 18.0 | | 14.0 | | ns | |
| tH13b | –ADS Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tSU14a | D31-D0 Setup Time to PCLKI | 18.0 | | 12.0 | | ns | |
| tH14b | D31-D0 Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |

## AC CHARACTERISTICS:

**3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V**
**5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V**

| Symbol | Parameter | 25 MHz | | 33 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **486SX/DX Interface - Bus Interface Timing, See Figures 13, 14, 15, 16, & 17 (Cont.)** | | | | | | | |
| tSU15a | HLDA Setup Time to PCLKI | 18.0 | | 14.0 | | ns | |
| tH15b | HLDA Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tSU17a | –BLAST Setup Time to PCLKI | 13.0 | | 10.0 | | ns | |
| tH17b | –BLAST Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tSU18a | –FERR Setup Time to PCLKI | 18.0 | | 14.0 | | ns | |
| tH18b | –FERR Hold Time from PCLKI | 3.0 | | 3.0 | | ns | |
| tD20 | –RDY, –BRDY Valid Delay from PCLKI | 3.0 | 32.0 | 3.0 | 25.0 | ns | CL=50 pF |
| tD22a | D31-D0 Read Valid Delay from PCLKI | 3.0 | 35.0 | 3.0 | 25.0 | ns | CL=50 pF |
| tD22b | D31-D0 Float Delay from PCLKI | | 30.0 | | 20.0 | ns | CL=50 pF |
| tD23 | HOLD, AHOLD Valid Delay from PCLKI | 3.0 | 30.0 | 3.0 | 24.0 | ns | CL=50 pF |
| tD24 | RESCPU Valid Delay from PCLKI | 3.0 | 30.0 | 3.0 | 25.0 | ns | CL=30 pF |
| tD26 | –EADS Valid Delay from PCLKI | 3.0 | 32.0 | 3.0 | 25.0 | ns | CL=50 pF |
| tD27 | –KEN Valid Delay from PCLKI | 3.0 | 32.0 | 3.0 | 25.0 | ns | CL=50 pF |
| tD28 | –IGNNE Valid Delay from PCLKI | 3.0 | 30.0 | 3.0 | 25.0 | ns | CL=50 pF |

## AC CHARACTERISTICS:

3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V
5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V

| Symbol | Parameter | 25 MHz | | 33 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **Local Bus Interface - Clock Timing, See Figure 18** | | | | | | | |
| t31 | SXOSC Period | 20.0 | | 15.0 | | ns | |
| t32a | SXOSC High | 7.0 | | 6.0 | | ns | VIL=VIH=VDD/2 |
| t32b | SXOSC Low | 7.0 | | 6.0 | | ns | VIL=VIH=VDD/2 |
| t33a | SXOSC Rise Time | 5.0 | | 4.0 | | ns | 30% to 70%*VDD |
| t33b | SXOSC Fall Time | 5.0 | | 4.0 | | ns | 70% to 30%*VDD |
| t34a | SXCLKI High | 7.0 | | 6.0 | | ns | VIL=VIH=VDD/2 |
| t34b | SXCLKI Low | 7.0 | | 6.0 | | ns | VIL=VIH=VDD/2 |
| t35a | SXCLKO Fall Time | | 5.0 | | 4.0 | ns | CL=50 pF. 70% to 30%*VDD |
| t35b | SXCLKO Rise Time | | 5.0 | | 4.0 | ns | CL=50 pF. 30% to 70%*VDD |
| t36 | SXOSC to SXCLKO | 3.0 | 35.0 | 3.0 | 30.0 | ns | CL=50 pF |
| **Local Bus Interface - Bus Interface Timing, See Figures 19, 20, 21, & 22** | | | | | | | |
| tSU40a | –SXREADY Setup Time to SXCLKI | 9.0 | | 7.0 | | ns | |
| tH40b | –SXREADY Hold Time from SXCLKI | 4.0 | | 4.0 | | ns | |
| tSU41a | SXD15-SXD0 Read Data Setup Time to SXCLKI | 7.0 | | 5.0 | | ns | |
| tH41b | SXD15-SXD0 Read Data Hold Time from SXCLKI | 5.0 | | 3.0 | | ns | |
| tSU42a | SXHOLD Setup Time to SXCLKI | 15.0 | | 9.0 | | ns | |
| tH42b | SXHOLD Hold Time from SXCLKI | 3.0 | | 2.0 | | ns | |
| tSU43a | SXRESCPU Setup Time to SXCLKI | 10.0 | | 10.0 | | ns | |
| tH43b | SXRESCPU Hold Time from SXCLKI | 3.0 | | 2.0 | | ns | |
| tD44a | SXA23-SXA1 Valid Delay from SXCLKI | 4.0 | 21.0 | 4.0 | 15.0 | ns | CL=50 pF |
| tD44b | SXA23-SXA1 Float Delay from SXCLKI | 4.0 | 30.0 | 4.0 | 20.0 | ns | CL=50 pF |

## AC CHARACTERISTICS:

**3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V**
**5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V**

| Symbol | Parameter | 25 MHz | | 33 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **Local Bus Interface - Bus Interface Timing, See Figures 19, 20, 21, & 22 (Cont.)** | | | | | | | |
| tD45a | –SXBHE, –SXBLE Valid Delay from SXCLKI | 4.0 | 21.0 | 4.0 | 15.0 | ns | CL=50 pF |
| tD45b | –SXBHE, –SXBLE Float Delay from SXCLKI | 4.0 | 30.0 | 4.0 | 20.0 | ns | CL=50 pF |
| tD46a | SXM/–IO, SXD/–C, SXW/–R Valid Delay from SXCLKI | 4.0 | 21.0 | 4.0 | 15.0 | ns | CL=50 pF |
| tD46b | SXM/–IO, SXD/–C, SXW/–R Float Delay from SXCLKI | 4.0 | 30.0 | 4.0 | 20.0 | ns | CL=50 pF |
| tD47a | –SXADS Valid Delay | 4.0 | 21.0 | 4.0 | 15.0 | ns | CL=50 pF |
| tD47b | –SXADS Float Delay | 4.0 | 30.0 | 4.0 | 20.0 | ns | CL=50 pF |
| tD48a | –SXSADS Valid Delay | 4.0 | 25.0 | 4.0 | 15.0 | ns | CL=50 pF |
| tD48b | –SXSADS Float Delay | 4.0 | 30.0 | 4.0 | 20.0 | ns | CL=50 pF |
| tD49a | SXD15-SXD0 Write Data Valid Delay from SXCLKI | 4.0 | 27.0 | 4.0 | 23.0 | ns | CL=50 pF |
| tD49b | SXD15-SXD0 Write Data Hold from SXCLKI | 2.0 | | 2.0 | | ns | CL=50 pF |
| tD49c | SXD15-SXD0 Write Data Float Delay from SXCLKI | 4.0 | 22.0 | 4.0 | 17.0 | ns | CL=50 pF |
| tD50 | SXHLDA Valid Delay from SXCLKI | 4.0 | 22.0 | 4.0 | 20.0 | ns | CL=50 pF |

## AC CHARACTERISTICS:

**3.3 V: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V**
**5.0 V: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V**

| Symbol | Parameter | 25 MHz | | 33 MHz | | 40 MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| **Cache Interface - CPU Access Timing, See Figures 23 & 24** | | | | | | | | | |
| tD60 | –DATAOE Valid Delay from PCLKI | 4.0 | 15.0 | 4.0 | 12.0 | 4.0 | 12.0 | ns | CL=50 pF |
| tD61 | –TAGOE Valid Delay from PCLKI | 4.0 | 15.0 | 4.0 | 12.0 | 4.0 | 12.0 | ns | CL=30 pF |
| tD62 | –CWRT1, –CWRT0 Valid Delay from PCLKI | 4.0 | 15.0 | 4.0 | 12.0 | 4.0 | 12.0 | ns | CL=30 pF |
| tPW63 | –CWRT1, –CWRT0 Minimum Pulse Width | 16.0 | 24.0 | 11.0 | 19.0 | 11.0 | 14.0 | ns | CL=30 pF |
| tD64a | TAG7-TAG0 Valid Delay from PCLKI | 4.0 | 15.0 | 4.0 | 12.0 | 4.0 | 12.0 | ns | CL=30 pF |
| tSU64b | TAG7-TAG0 Setup Time to PCLKI | 15.0 | | 10.0 | | 10.0 | | | |
| **Cache Interface - Peek Cycle Timing, See Figure 25** | | | | | | | | | |
| tD65 | SXA23-SXA1 to A23-A1 Valid Delay | 4.0 | 35.0 | 4.0 | 30.0 | 4.0 | 25.0 | ns | CL=50 pF (Snoop Cycles) |
| tD66 | –MEMW to –CWRT1, –CWRT0 Delay | 4.0 | 35.0 | 4.0 | 30.0 | 4.0 | 25.0 | ns | CL=30 pF (Snoop Cycles) |
| **Miscellaneous Timing, See Figure 26** | | | | | | | | | |
| tSU74a | –BLKA20 Setup Time to PCLKI | | 15.0 | | 10.0 | | 7.0 | ns | Note 2 |
| tH74b | –BLKA20 Hold Time to PCLKI | | 3.0 | | 3.0 | | 3.0 | ns | Note 2 |
| tD75 | –SXBUSYNPX Delay from PCLKI | 3.0 | 25.0 | 3.0 | 20.0 | 3 | 17.0 | ns | CL=50 pF |
| tD76 | –SXERRORNPX Delay from PCLKI | 3.0 | 25.0 | 3.0 | 20.0 | 3 | 17.0 | ns | CL=50 pF |

**Notes:** 1. Specification is characterized and guaranteed, not 100% tested.

2. Asynchronous input, for test purposed only to assure recognition at a particular clock edge.

3. Measurement point is when the pin is no longer driving.

**FIGURE 12. CPU CLOCK TIMING**

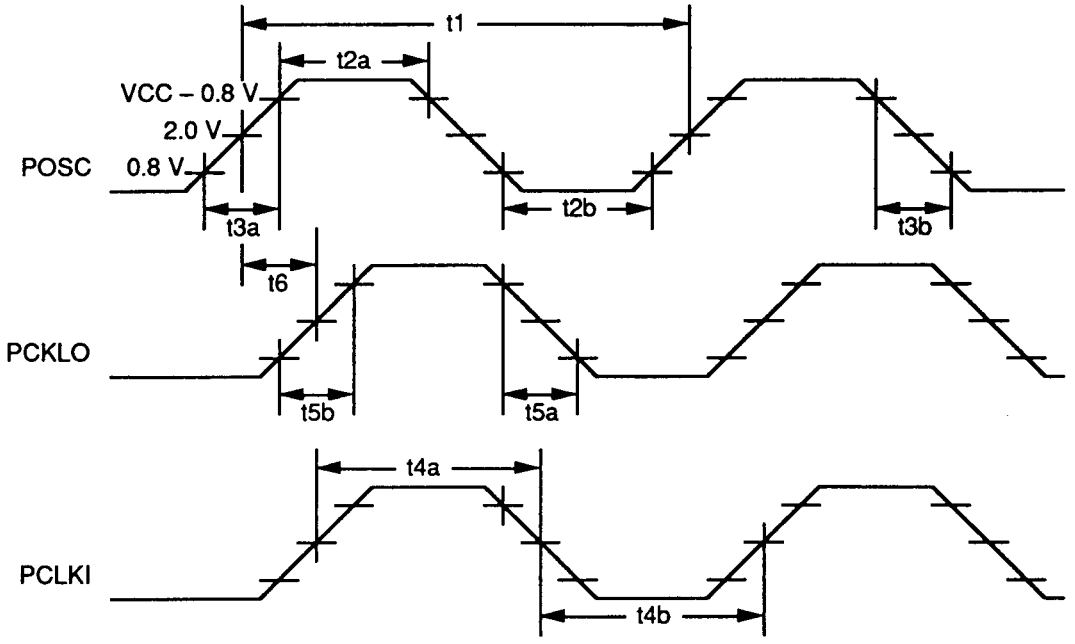



**FIGURE 13. CPU INTERFACE SETUP AND HOLD TIMING**

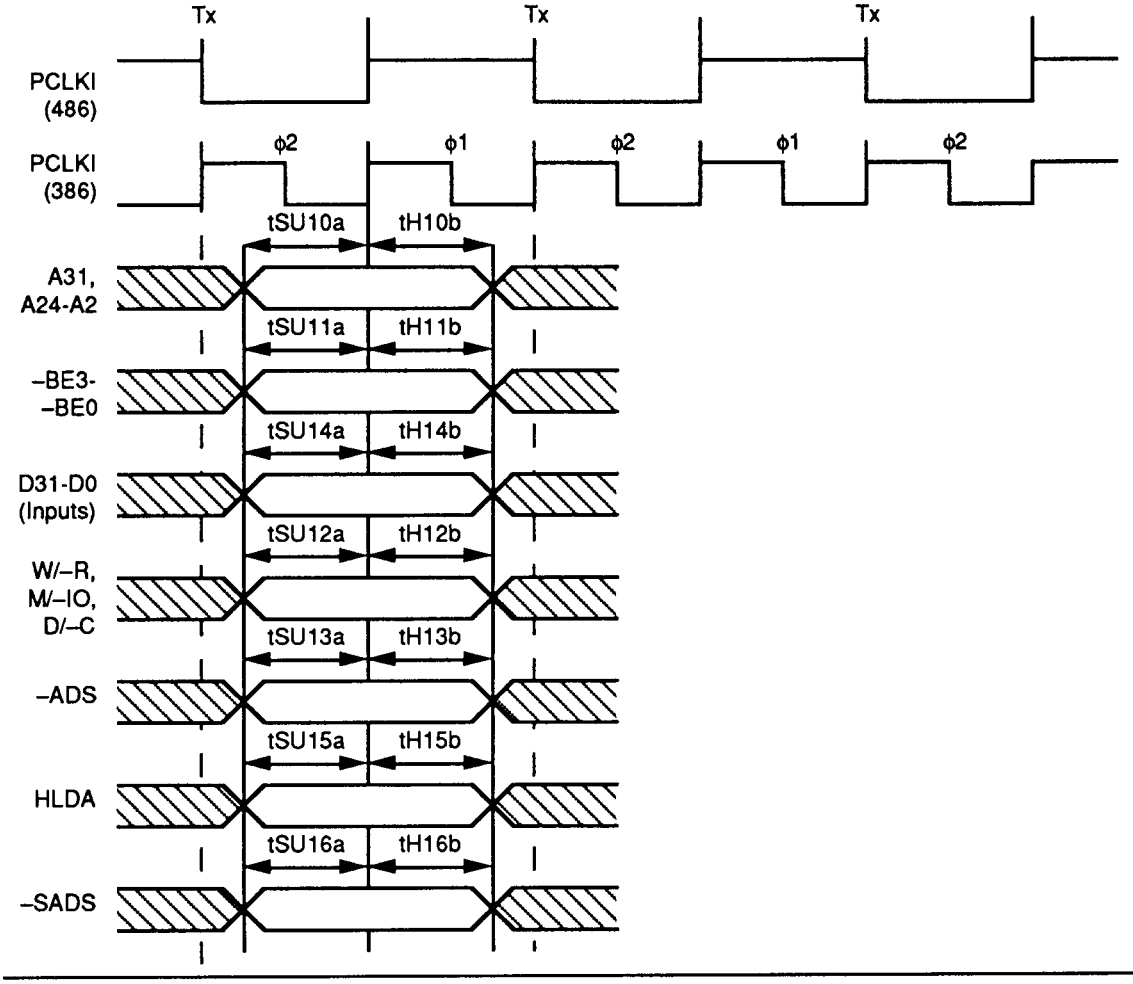


**FIGURE 14. CPU DELAY TIMING**

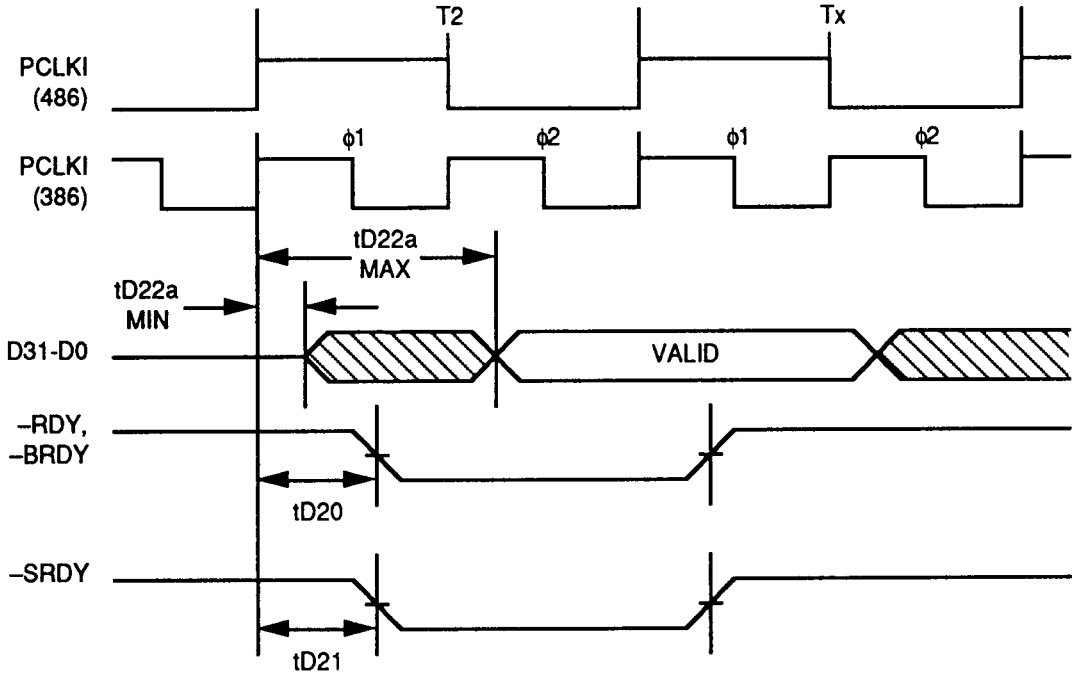



**FIGURE 15. CPU OUTPUT FLOAT DELAY & HOLD VALID DELAY TIMING**

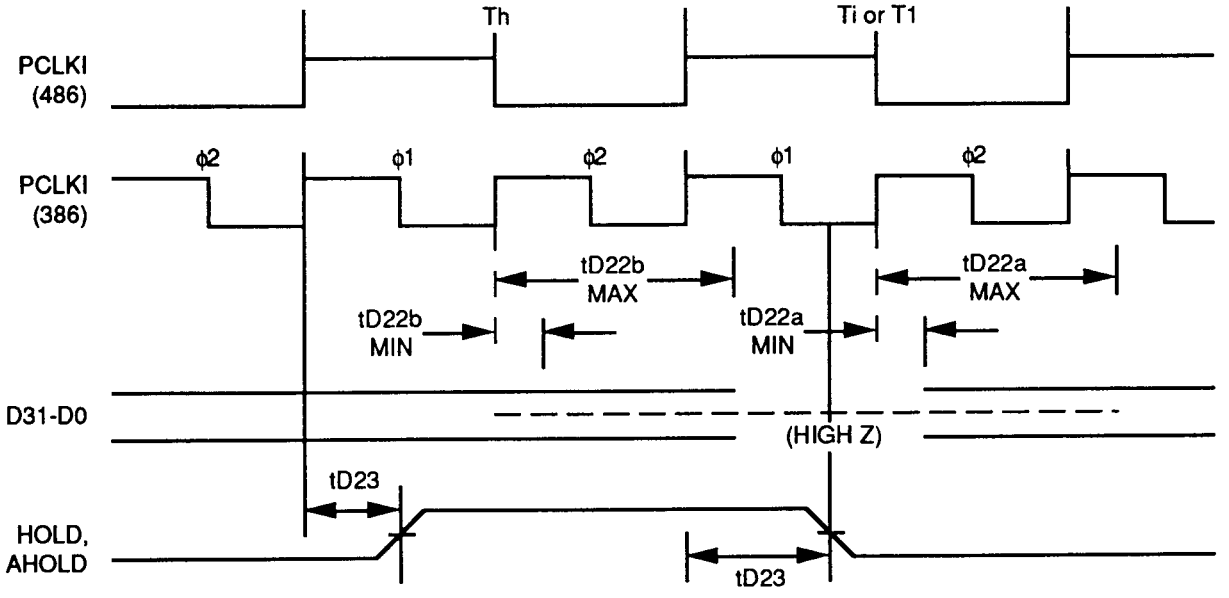


**FIGURE 16. RESET TIMING**

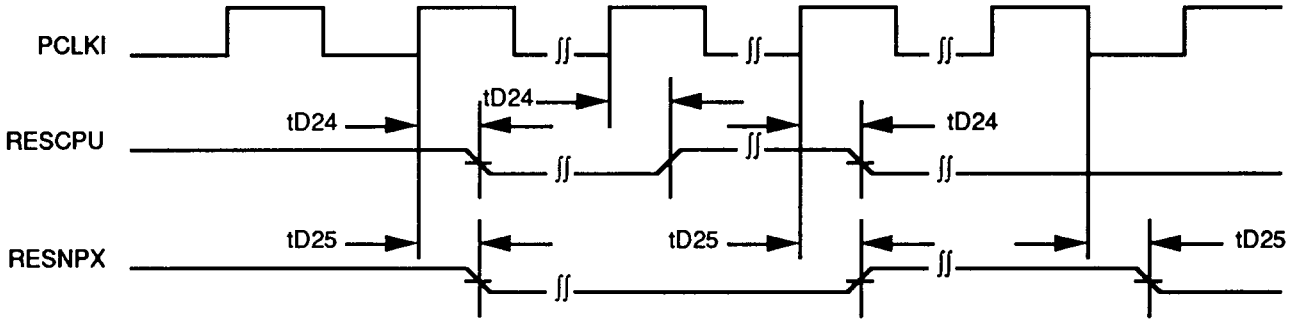



**FIGURE 17. 486 CPU INTERFACE**

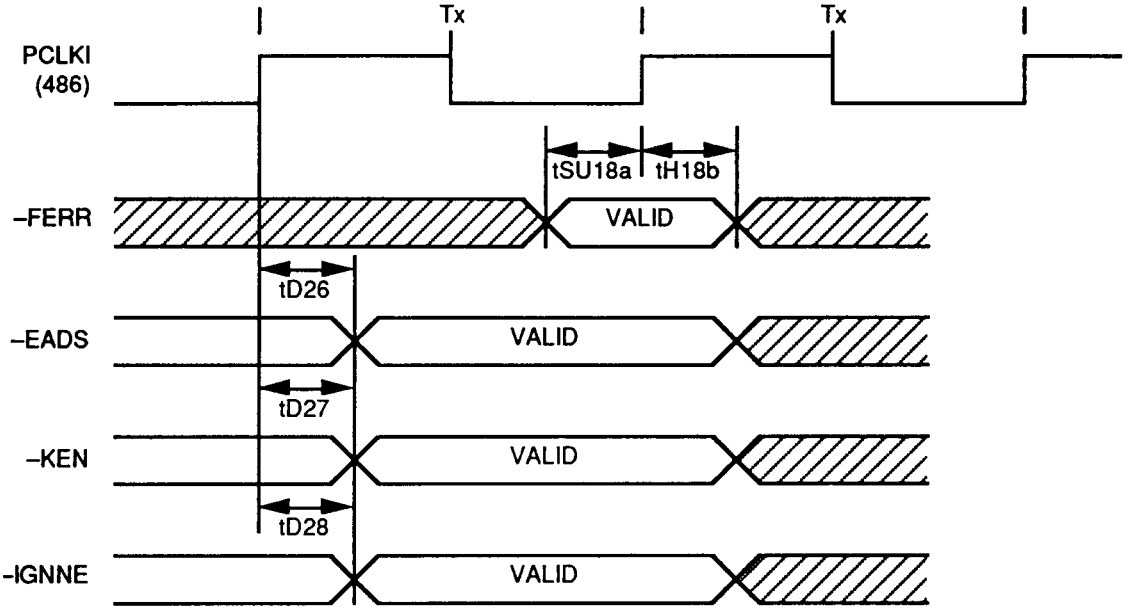


**FIGURE 18. SX CLOCK TIMING**

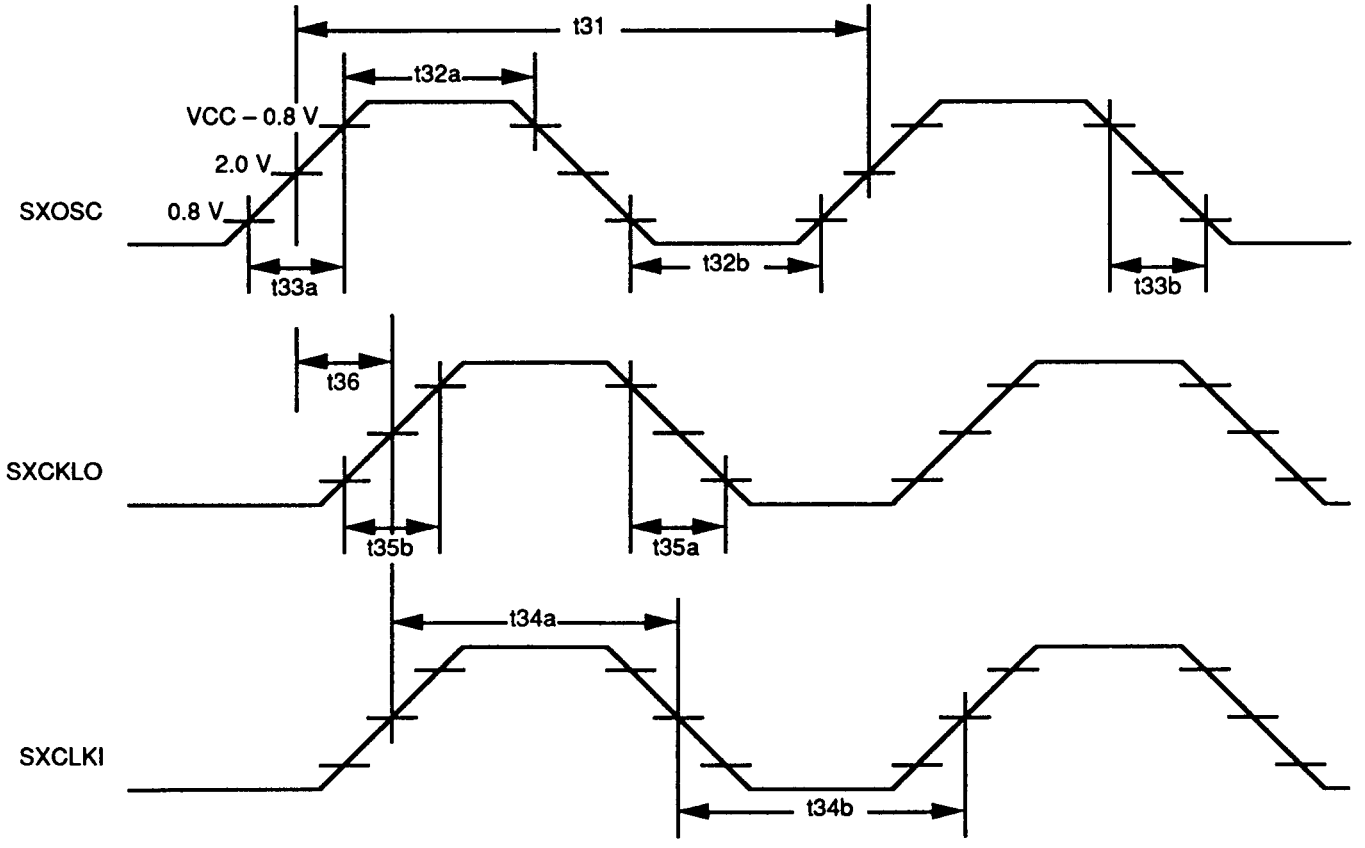



**FIGURE 19. SX INTERFACE SETUP AND HOLD**

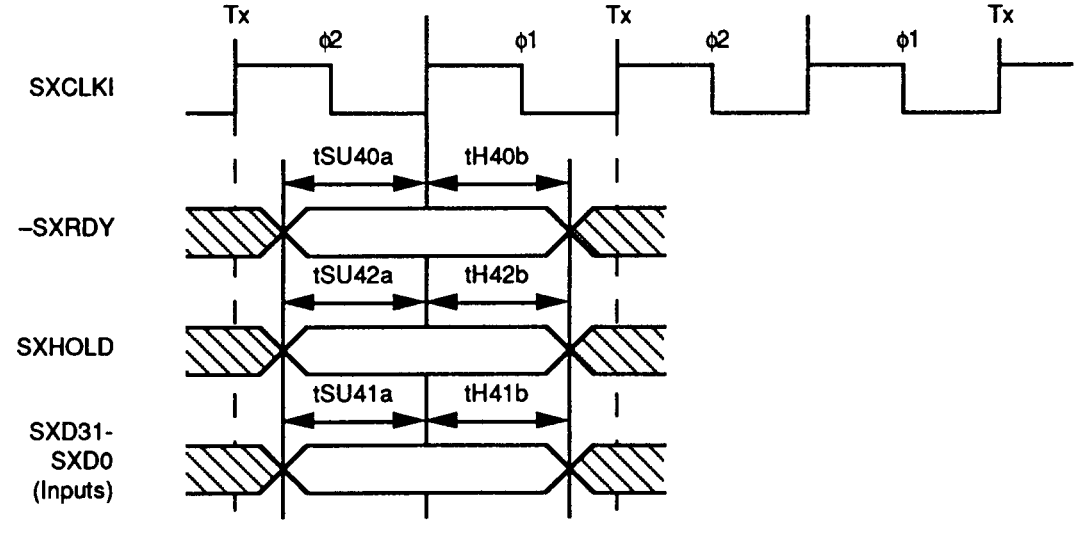


**FIGURE 20. SX OUTPUT FLOAT DELAY AND HOLD VALID DELAY TIMING**

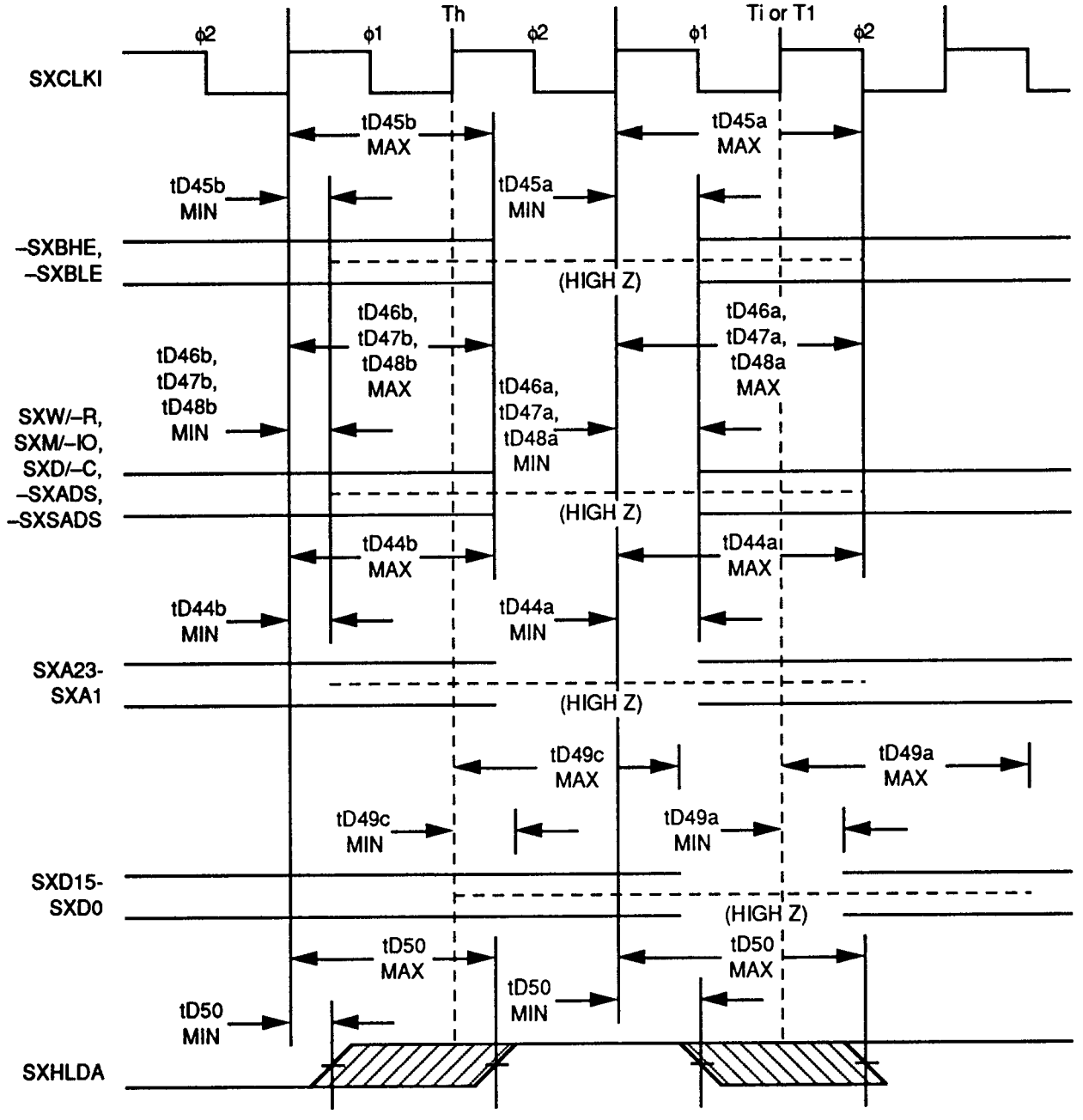


**FIGURE 21. SX RESET TIMING**

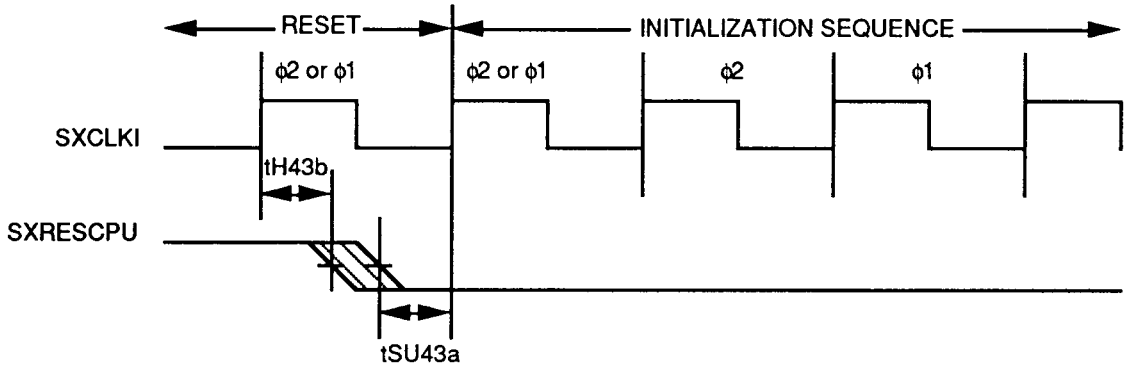



**FIGURE 22. WRITE DATA HOLD TIMING**

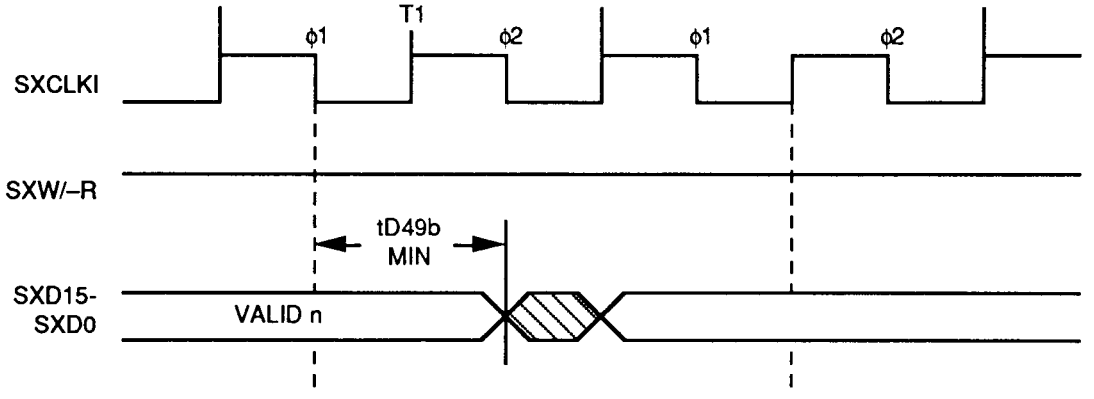


**FIGURE 23. CACHE INTERFACE TIMING - CACHE READ**

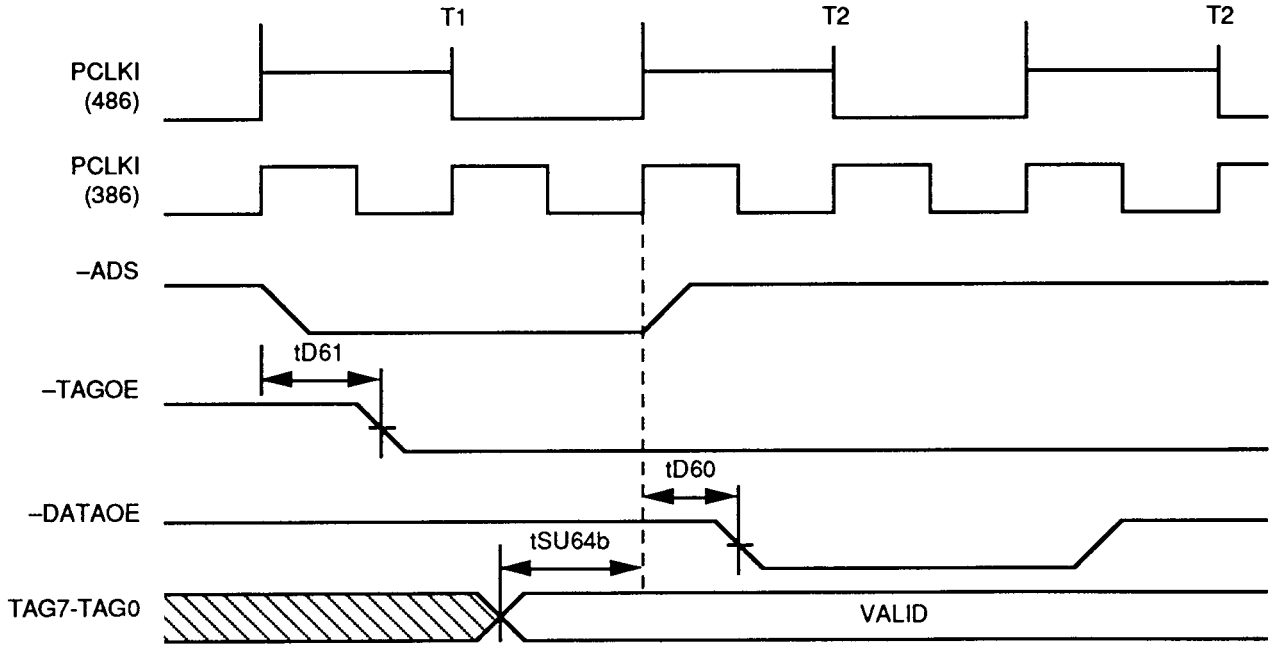



**FIGURE 24. CACHE INTERFACE TIMING - CACHE WRITE**

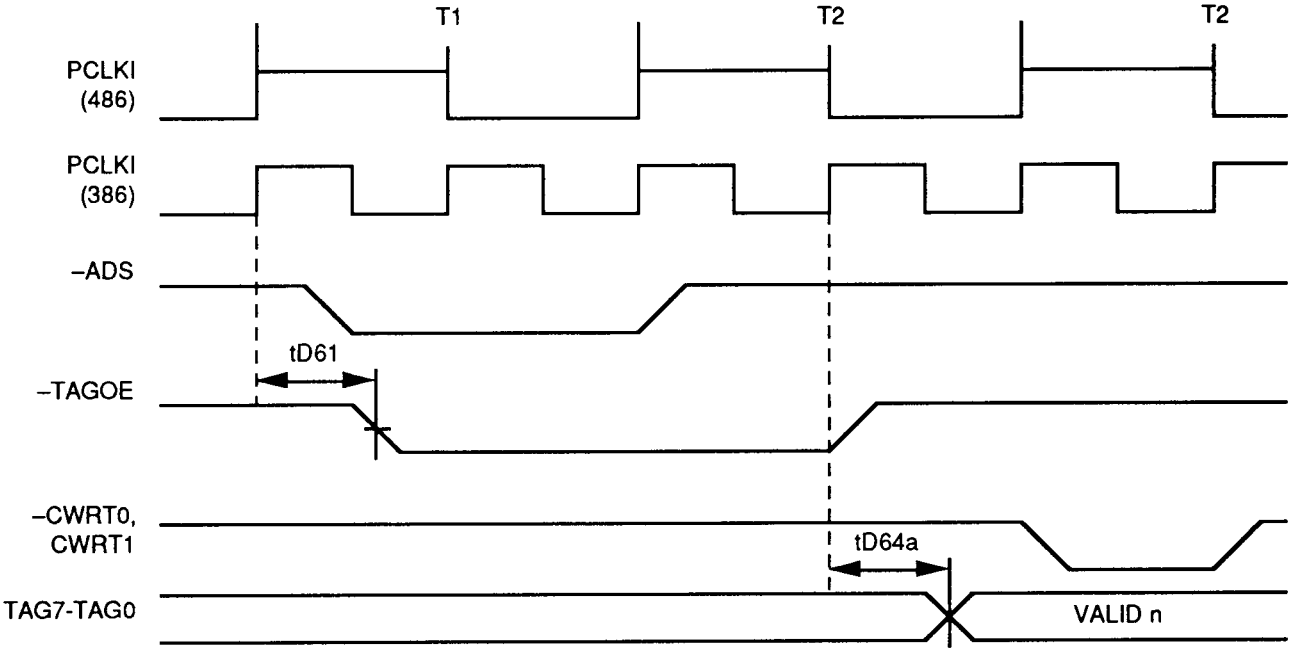


**FIGURE 25. PEEK CYCLE TIMING (386 STOP CLOCK)**

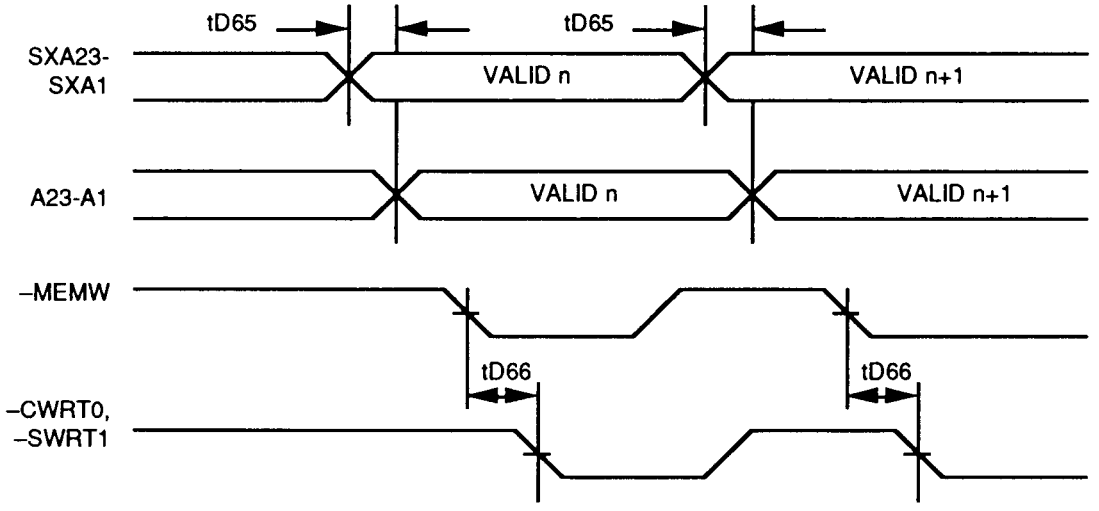
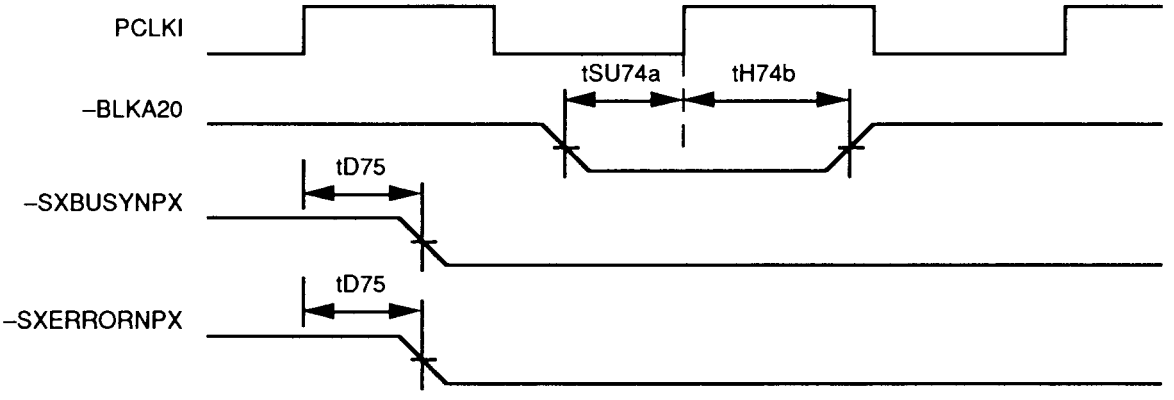



**FIGURE 26. MISCELLANEOUS TIMING**



## ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground Potential –0.5 V to 7.0 V

Applied Output Voltage –0.5 V to VDD + 0.5 V

Applied Input Voltage –0.5 V to 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS - 5.0 VOLT OPERATION: TA = 0°C to +70°C, VDD = 5 V ±10, VSS = 0 V

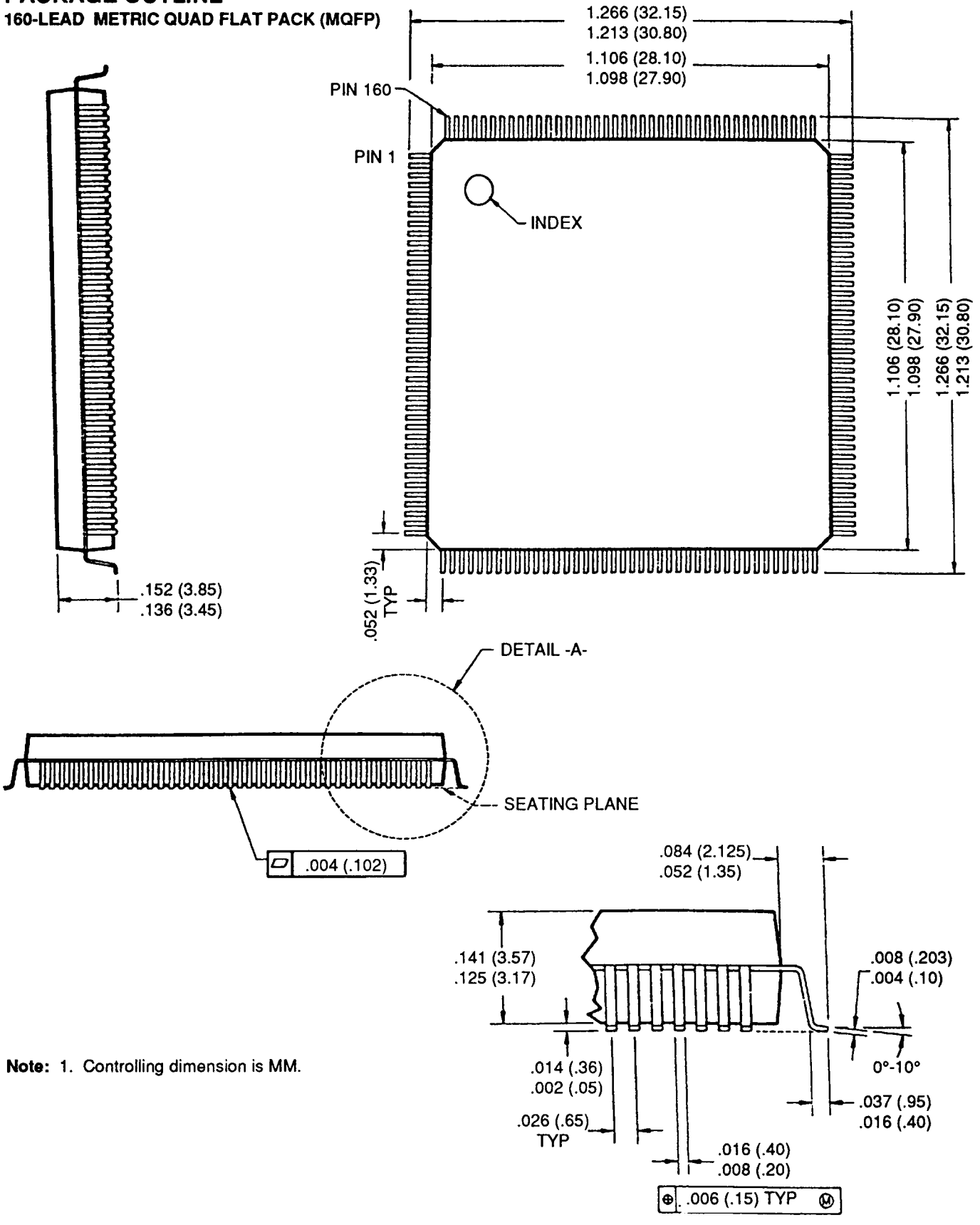
| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VIL | Input Low Voltage | –0.3 | 0.8 | V | TTL-Compatible Inputs |
| VIH | Input High Voltage | 2.0 | VDD + 0.3 | V | TTL-Compatible Inputs |
| VIL | Input Low Voltage | –0.3 | VDD x 0.2 | V | CMOS-Compatible Inputs (PCLKI, POSC, SXCLKI, SXOSC) |
| VIH | Input High Voltage | VDD x 0.7 | VDD + 0.3 | V | CMOS-Compatible Inputs (PCLKI, POSC, SXCLKI, SXOSC) |
| VOL1 | Output Low Voltage | | 0.4 | V | IOL = 4 mA |
| | | | 0.2 | V | IOL = 100 µA |
| VOL2 | Output Low Voltage (PCLKO, SXCLKO) | | 0.4 | V | IOL = 8 mA |
| | | | 0.2 | V | IOL = 100 µA |
| VOH1 | Output High Voltage | 2.4 | | V | IOH = –2 mA |
| | | VDD – 0.2 | | V | IOH = –100 µA |
| VOH2 | Output High Voltage (PCLKO, SXCLKO) | 2.4 | | V | IOH = –4 mA |
| | | VDD – 0.2 | | V | IOH = –100 µA |
| ILI | Input Leakage Current | | ±3 | µA | 0.1 V ≤ VIN ≤ VDD – 0.1 V |
| ILO | Output Three-State Leakage Current | | ±5 | µA | 0.1 V ≤ VOUT ≤ VDD – 0.1 V |
| LIPU | Input Current - Internal Pull-up | –30 | –500 | µA | VIN = 0.1 V |
| IDDSB | Static Power Supply Current | | 225 | µA | No DC Loads. VIL = 0.1 V, VIH = VDD – 0.1 V |
| IDDOP | Dynamic Power Supply Current | | 3.5 | mA/MHz | No DC Loads - Outputs Open. VIL = 0.1 V, VIH = VDD – 0.1 V |
| CIN | Input or I/O Capacitance | | 10 | pF | FC = 1 MHz |
| | | | 15 | pF | PCLKI, SXCLKI |
| COUT | Output Capacitance | | 10 | pF | FC = 1 MHz |

## DC CHARACTERISTICS - 3.3 VOLT OPERATION: TA = 0°C to +70°C, VDD = 3.3 V ±10%, VSS = 0 V

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VIL | Input Low Voltage | –0.3 | 0.8 | V | TTL-Compatible Inputs |
| VIH | Input High Voltage | 2.0 | VDD + 0.3 | V | TTL-Compatible Inputs |
| VIL | Input Low Voltage | –0.3 | VDD x 0.2 | V | CMOS-Compatible Inputs (PCLKI, POSC, SXCLKI, SXOSC) |
| VIH | Input High Voltage | VDD x 0.7 | VDD + 0.3 | V | CMOS-Compatible Inputs (PCLKI, POSC, SXCLKI, SXOSC) |
| VOL1 | Output Low Voltage | | 0.4 | V | IOL = 2 mA |
| | | | 0.2 | V | IOL = 100 µA |
| VOL2 | Output Low Voltage (PCLKO, SXCLKO) | | 0.4 | V | IOL = 4 mA |
| | | | 0.2 | V | IOL = 100 µA |
| VOH1 | Output High Voltage | 2.4 | | V | IOH = –1 mA |
| | | VDD – 0.2 | | V | IOH = –100 µA |
| VOH2 | Output High Voltage (PCLKO, SXCLKO) | 2.4 | | V | IOH = –2 mA |
| | | VDD – 0.2 | | V | IOH = –100 µA |
| ILI | Input Leakage Current | | ±3 | µA | 0.1 V ≤ VIN ≤ VDD – 0.1 V |
| ILO | Output Three-State Leakage Current | | ±5 | µA | 0.1 V ≤ VOUT ≤ VDD – 0.1 V |
| LIPU | Input Current - Internal Pull-up | –10 | –300 | µA | VIN = 0.1 V |
| IDDSB | Static Power Supply Current | | 225 | µA | No DC Loads |
| IDDOP | Dynamic Power Supply Current | | 2.0 | mA/MHz | No DC Loads - Outputs Open |
| CIN | Input or I/O Capacitance | | 10 | pF | FC = 1 MHz |
| | | | 15 | pF | PCLKI, SXCLKI |
| COUT | Output Capacitance | | 10 | pF | FC = 1 MHz |

## PACKAGE OUTLINE

**160-LEAD METRIC QUAD FLAT PACK (MQFP)**




**Note:** 1. Controlling dimension is MM.

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195321-002 2.5M 10/92