VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

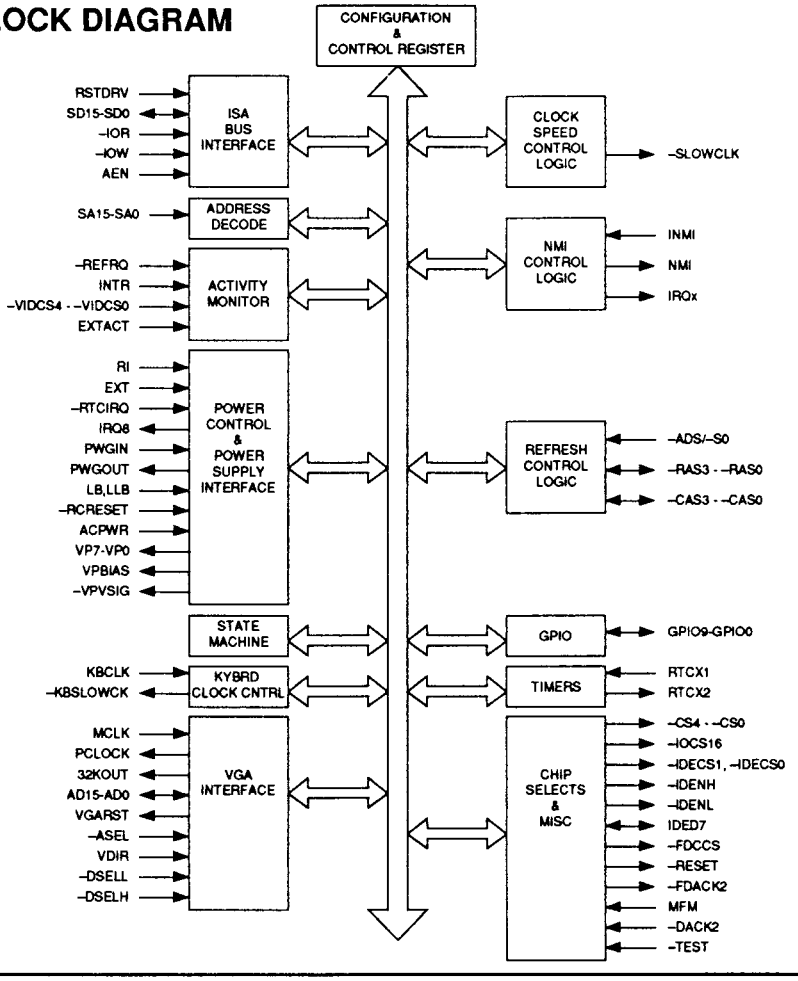
VL82C312

SCAMP™ POWER MANAGEMENT UNIT

FEATURES

- Provides system activity monitoring, peripheral control, power supply control, mode timers, and general purpose I/O for laptop/notebook power management
- Five operation modes:
  - On Mode
  - Doze Mode
  - Sleep Mode
  - Suspend Mode
  - Off Mode
- Independent programmable timers for power saving modes
- Independent programmable timers for LCD and backlight control
- Ten individual power control outputs
  - Three for LCD power
  - Seven general purpose for peripherals
- Four "low battery" warning monitors: two standard and two optional
- Multiple power-on sources from Suspend/Off Mode:
  - Pushbutton
  - RTC alarm
  - Modem ring
- AC power monitoring to disable PMU function
- Refresh support in Suspend Mode
- Leakage control of outputs during Suspend Mode
- Wide range of LCD panel power-up/down sequencing
- Ten general purpose I/O ports; eight with additional I/O features:
  - One programmable blinking I/O
  - Two optional low battery inputs
  - Three inputs AND/OR selectable I/O with one common GPIO output
- Watchdog timer to turn off system power if low battery NMI is not serviced
- Programmable NMI generation on:
  - PMU power mode
  - Low battery warning
  - External input
  - LCD panel timer
  - Reschedule Suspend Mode NMI by BIOS
- Controls SCAMP's SLEEP pin
- RTC alarm IRQ output pin for SCAMP
- Additional logic included to minimize system board component count
- Provides chip selects for:
  - IDE interface
  - Floppy disk controller
  - VL16C452 serial/parallel I/O chip
- Provides multiplexed address/data bus for VGA controller
- Chip ID and revision register
- 144-pin MQFP low-power CMOS IC

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C312-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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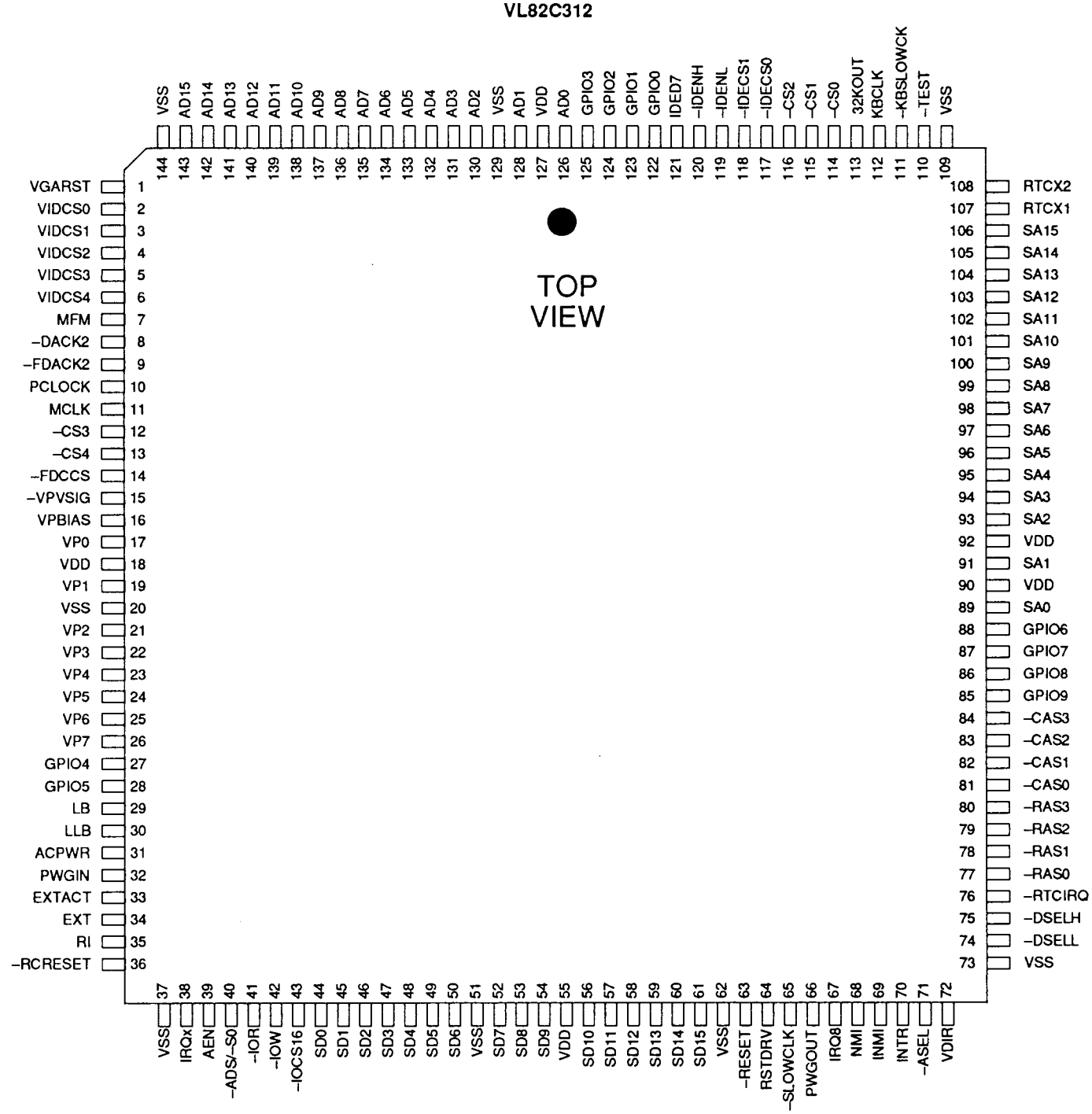
PIN DIAGRAM


VL82C312
TOP VIEW
1 VGARST
2 VIDCS0
3 VIDCS1
4 VIDCS2
5 VIDCS3
6 VIDCS4
7 MFM
8 -DACK2
9 -FDACK2
10 PCLOCK
11 MCLK
12 -CS3
13 -CS4
14 -FDCCS
15 -VPVSIG
16 VPBIAS
17 VP0
18 VDD
19 VP1
20 VSS
21 VP2
22 VP3
23 VP4
24 VP5
25 VP6
26 VP7
27 GPIO4
28 GPIO5
29 LB
30 LLB
31 ACPWR
32 PWGIN
33 EXTACT
34 EXT
35 RI
36 -RCRESET
37 VSS
38 IRQx
39 AEN
40 -ADS/-S0
41 -IOR
42 -IOW
43 -IOCS16
44 SD0
45 SD1
46 SD2
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48 SD4
49 SD5
50 SD6
51 VSS
52 SD7
53 SD8
54 SD9
55 VDD
56 SD10
57 SD11
58 SD12
59 SD13
60 SD14
61 SD15
62 VSS
63 -RESET
64 RSTDRV
65 -SLOWCLK
66 PWGOUT
67 IRQ8
68 NMI
69 INMI
70 INTR
71 -ASEL
72 VDIR
73 VSS
74 -DSELL
75 -DSELH
76 -RTCIRQ
77 -RAS0
78 -RAS1
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81 -CAS0
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91 SA1
92 VDD
93 SA2
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97 SA6
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108 RTCX2
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128 AD1
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136 AD8
137 AD9
138 AD10
139 AD11
140 AD12
141 AD13
142 AD14
143 AD15
144 VSS

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
VGARST	1	O-TTL (4 mA)	VGA controller reset signal.
–VIDCS4 - –VIDCS0	2-6	IO-TTL (4 mA)	VGA controller write enable signals.
MFM, –DACK2	7, 8	IO-TTL (4 mA)	Inputs to condition floppy disk controller –DACK signal for certain controllers.
–FDACK2	9	O-TTL (4 mA)	–DACK signal to floppy disk controller to be used for certain controllers instead of normal –DACK2 signal.
PCLOCK	10	O-TTL (4 mA)	RAMDAC pixel clock output.
MCLK	11	IO-TTL (4 mA)	Clock input from VGA controller.
–CS4, –CS3	13, 12	O-TTL (8 mA)	Floppy disk controller's chip select signals.
–FDCCS	14	IO-TTL (24 mA)	Floppy disk controller's chip select. This pin may be pulled high or low at reset to determine its address decoding range.
–VPVSIG	15	O-TTL (8 mA)	Enable signal for LCD clock and data buffer. Active low, open drain.
VPBIAS	16	O-TTL (8 mA)	Power control signal for controlling LCD display's bias power. The polarity is the same as VP0.
VP7-VP2	26-21	O-TTL (8 mA)	Power control signal for controlling user selected power. The polarity is determined by the Polarity Register.
VP1	19	O-TTL (8 mA)	Power control signal for controlling LCD backlight power. The polarity is determined by the Polarity Register.
VP0	17	O-TTL (8 mA)	Power control signal for controlling LCD panel power. The polarity is determined by the Polarity Register.
GPIO9-GPIO6	85-88	IO-TTL (4 mA)	General purpose I/O with optional AND/OR output.
GPIO5-GPIO4	28-27	IO-TTL (4 mA)	General purpose I/O with low battery NMI warning option.
GPIO3	125	IO-TTL (4 mA)	General purpose I/O with blinking option.
GPIO2-GPIO0	124-122	IO-TTL (4 mA)	General purpose I/O.
LB	29	I-TTL (4 mA)	Low battery warning indicator from power supply, active high.
LLB	30	I-TTL (4 mA)	Low low battery warning indicator from power supply, active high.
ACPWR	31	I-TTL (4 mA)	AC power indicator signal from power supply. When this signal is high, the Doze Timer is disabled, thus hardware power management functions are disabled.
PWGIN	32	I-TTL	Power good input signal from power supply.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
EXTACT	33	IO-TTL (4 mA)	External activity input signal. On the rising edge, the PMU exits from the Doze or Sleep Mode or generates an NMI. It has no effect in the On Mode.
EXT	34	I-TTL (4 mA)	External wake-up signal, active high. Usually, this signal is derived from a switch, and is debounced by the PMU. A rising edge puts the PMU in the On Mode if it was in Off or Suspend Mode, and can generate an NMI if the PMU is not in Off or Suspend Mode.
RI	35	I-TTL	Ring Indicator input, active high. The PMU puts the system into the On Mode when it detects a pre-programmed number of transitions while in the Suspend or Off Mode.
–RCRESET	36	I-TTL	External RC reset signal to reset the PMU itself when its power is first applied.
–ADS/–S0	40	IO-TTL (4 mA)	Connect to –ADS input if the CPU is 386. Connect to –S0 input if the CPU is 286.
IRQx	38	O-TTL (4 mA)	Alternate interrupt request output.
AEN	39	IO-TTL (4 mA)	System bus address enable from system bus.
–IOR	41	IO-TTL (4 mA)	I/O read command from VL82C310 SCAMP-LT Controller.
–IOW	42	IO-TTL (4 mA)	I/O write command from VL82C310 SCAMP-LT Controller.
–IOCS16	43	O-TTL (24 mA)	I/O bus size 16 bits from system bus.
SD15-SD0	61-56, 54-52, 50-44	I/O2 (24 mA)	System data bus from system bus.
–RESET	63	O-TTL (4 mA)	Inverted RSTDRV signal for use with IDE and other peripherals.
RSTDRV	64	IO-TTL (4 mA)	System reset input from system bus.
–SLOWCLK	65	O-TTL (4 mA)	CPU clock speed control signal to VL82C310 SCAMP-LT Controller. When –SLOWCLK is low, the VL82C310 reduces the CPU clock speed to the minimum CPU clock speed.
PWGOUT	66	O-TTL (4 mA)	Power good output signal to the VL82C310 SCAMP-LT Controller.
IRQ8	67	O-TTL (4 mA)	RTC interrupt request signal generated for real-time clock. Connect to VL82C310 SCAMP-LT Controller.
NMI	68	O-TTL (4 mA)	NMI output to the CPU.
INMI	69	IO-TTL (4 mA)	NMI input from VL82C310 SCAMP-LT Controller.
INTR	70	IO-TTL (4 mA)	INTR pin from VL82C310 SCAMP-LT Controller, active high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ASEL	71	IO-TTL (4 mA)	Address select for the multiplex data and address bus to the VGA controller.
VDIR	72	IO-TTL (4 mA)	Video data bus direction control input signal. High is read. Low is write.
–DSELL	74	IO-TTL (4 mA)	Low data byte select input from the VGA controller.
–DSELH	75	IO-TTL (4 mA)	High data byte select input from the VGA controller.
–RTCIRQ	76	IO-TTL (4 mA)	RTC IRQ input from VL82C107 SCAMP Combination I/O chip. The PMU puts the system into the On Mode when it detects any transition on this pin while in the Suspend or Off Mode.
–RAS3 - –RAS0	80-77	IO-TTL (12 mA)	DRAM RAS signals. Wired OR with RAS lines from the VL82C310 SCAMP-LT Controller. These signals are driven low by the PMU only in the Suspend Mode and three-state when they are not in the Suspend Mode. The VL82C310 three-states these signals in the Suspend Mode. Unused –RAS pins must be pulled up.
–CAS3 - –CAS0	84-81	IO-TTL (12 mA)	DRAM CAS signals. Wired OR with CAS lines from the VL82C310 SCAMP-LT Controller. These signals are driven low by the PMU only in the Suspend Mode and three-state when not in the Suspend Mode. The VL82C310 three-states these signals in the Suspend Mode. Unused –CAS pins must be pulled up.
SA15-SA0	106-93, 91, 89	IO-TTL (4 mA)	System address lines from the VL82C310 SCAMP-LT Controller.
–TEST	110	I-TPU	Reserved for testing the chip.
RTCX1	107	I-CMOS	32 kHz clock in from crystal.
RTCX2	108	O	32 kHz clock feedback.
32KOUT	113	O-TTL (8 mA)	Refresh clock for VGA controller in the Suspend Mode.
–KBSLOWCK	111	O-TTL (4 mA)	Keyboard clock control pin. When low, the VL82C107 SCAMP Combination I/O chip stops the keyboard clock. When high, the VL82C107 starts the keyboard clock.
KBCLK	112	IO-TTL (4 mA)	Keyboard clock input from keyboard. When a transition is detected on this signal the PMU drives –KBSLOWCK high to enable the clock to the keyboard controller.
–CS0	114	O-TTL (8 mA)	Chip select for the COM1.
–CS1	115	O-TTL (8 mA)	Chip select for the COM2.
–CS2	116	O-TTL (8 mA)	Chip select for the LPT port.
–IDECS1, –IDECS0	118, 117	O-TTL (8 mA)	IDE chip selects.
–IDENL	119	O-TTL (8 mA)	IDE low data byte enable.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–IDENH	120	O-TTL (8 mA)	IDE high data byte enable.
IDED7	121	IO-TTL (24 mA)	IDE data bit 7.
AD15-AD0	143-130, 128, 126	IO-TTL (8 mA)	Multiplexed address/data bus to/from the VGA controller.
VDD	18, 55, 90, 92, 127	PWR	Power Connections, nominally +5 volts.
VSS	20, 37, 51, 62, 73, 109, 129, 144	GND	Ground Connections, 0 volts.

SIGNAL LEGEND

Signal Code	Signal Type
I-CMOS	CMOS level input
I-TTL	TTL level input
I-TPU	TTL level input with 30k ohm pull-up resistor
I-TST	TTL level Schmitt-trigger input
IO-TTL	TTL level input/output
IO-TOD	TTL level input/output open drain
IO-TODNP	TTL level input/output open drain with 3k ohm NMOS pull-up
IO-TODPU	TTL level input/output open drain with 30k ohm pull-up resistor
IO-TODS	TTL level with open drain output/Schmitt-trigger input
IO-TPU	TTL level input/output with 30k ohm pull-up resistor
O	CMOS and TTL level compatible output
GND	Ground
PWR	Power

FUNCTIONAL DESCRIPTION

Intended to be used in conjunction with VLSI's VL82C310 SCAMP-LT Single Chip PC/AT® SCAMP Controller and VL82C107 SCAMP Combination I/O chip; the VL82C312 SCAMP Power Management Unit (PMU) dramatically reduces overall system power consumption and provides special features for laptop/notebook PC/AT-compatible computers. The power reduction is accomplished via an activity monitor which detects inactivity in the system, and reduces the CPU clock frequency and/or removes power from peripheral devices.

The PMU has five operation modes:

- On Mode
- Doze Mode
- Sleep Mode
- Suspend Mode
- Off Mode

By monitoring the system activity, the PMU switches between modes to achieve power savings without impacting system performance. The PMU also provides an auto power-on feature to turn on system power via a pushbutton switch, modem ring indicator, or real-time clock time of day alarm.

The PMU also supports a suspend/resume function in conjunction with BIOS to allow the user to turn the system power off and save the system information from the current application. When system power is turned back on, the user is able to resume the application from the point where it was suspended.

Additionally, the PMU integrates many of the ordinary glue logic ICs normally found in laptop and notebook systems, such as providing the external logic many floppy disk controllers require, a multiplexed address/data bus that most video controllers require, and the necessary chip selects for two serial ports, a parallel printer port, and an IDE hard disk interface.

PC/AT BUS INTERFACE

The VL82C312 resides on the ISA bus. Four control signals, –IOR, –IOW, AEN, and –IOCS16, are used to interface to the VL82C310 SCAMP Controller. The VL82C310 will present the address and data on the SA and SD buses, and ISA bus control signals for all I/O cycles. The PMU is tied to SA15-SA0 and SD15-SD0 buses. The PMU monitors SA15-SA0 constantly. If an access of the PMU internal registers occurs, the PMU places the data on SD15-SD0 while –IOR is asserted for an I/O read operation, or it latches the data at the rising edge of the –IOW for an I/O write operation. The PMU does not drive –IOCHRDY so the VL82C310 uses its programmed number of I/O wait states to terminate the bus cycle. The PMU fully decodes SA15-SA0.

PC/AT is a registered trademark of IBM Corporation.

VL82C310 SCAMP CONTROLLER AND VL82C107 SCAMP COMBINATION I/O CHIP INTERFACE

Clock Switching

The VL82C312 SCAMP PMU controls the CPU clock speed via the –SLOWCLK pin of the VL82C310 SCAMP Controller if the VL82C310 has its sleep function enabled. When the PMU is in the Doze or Sleep Mode, it drives the –SLOWCLK signal low. The VL82C310 slows down the clock when it detects a transition from high-to-low on its –SLOWCLK input pin, and it speeds up to the maximum programmed CPU clock speed when it detects a transition from low-to-high. The –SLOWCLK signal is a glitch free signal and provides a 250 ns minimum pulse width. The frequency of the slow clock depends on the minimum speed of the CPU. It can be set by the BIOS during the system initialization in the configuration registers of VL82C310. Please refer to the VL82C310 SCAMP Controller data sheet for detailed information. Normally, the slow clock frequency is set to the minimum clock speed that the CPU supports.

The PMU drives the –SLOWCLK pin high without exiting the Doze or Sleep Mode for an INTR. It pushes each interrupt occurrence on an internal stack register and an "end of interrupt" (EOI) instruction pops each interrupt occurrence from the stack to prevent multiple nested interrupts from slowing the CPU clock until the last EOI. The depth of the stack is 15 deep. When the last EOI is received, the PMU waits for 15 to 30 µs before it drives the –SLOWCLK pin low, forcing the VL82C310 back into slow CPU clock operation. The VL82C312 flushes the stack if the AUTOFLUSH bit in the MISC Register is set or when the FLUSH bit in the MISC Register is set. If the FLUSH bit is set, the stack operation is disabled and the VL82C312 drives the –SLOWCLK pin low 15 to 30 µs after any EOI. The VL82C310 switchs to maximum CPU clock speed for DMA or refresh operations automatically. If the –SLOWCLK pin is switched from high-to-low during DMA operation, the VL82C310 waits for the completion of the DMA cycle and then slows down the CPU clock.

If the MSK_VIDM bit in the ACTMASK Register is set, any –VIDCS4 - –VIDCS0 low transition is not treated as an activity detection. The VL82C312 temporarily brings the –SLOWCLK pin high for 8 ms without exiting from the Doze or Sleep Mode. If the MSK_VIDM bit is reset, any –VIDCS4 - –VIDCS0 low transition causes an activity detection. Please refer to the section titled "System Activity Monitor" for further information.

At the end of any NMI service routine, the BIOS writes any data to the NMICAUSE-I Register. The VL82C312 then waits for 15 to 30 µs and drives the –SLOWCLK pin low, restoring slow CPU clock speed. If the BIOS fails to do so, eventually an EOI occurs in response to a Doze Timer interrupt and the VL82C312 brings the –SLOWCLK pin low at that time.

If the HI_CLK bit in the MISC Register is set, the –SLOWCLK and –KBSLOWCK pins stay high but the VL82C312 still enters the Doze and Sleep Mode, thus the CPU clock remains at high speed but some unused peripheral devices can still be turned off. This is for the calculation intensive application programs.

If the ACPWR signal is high, the Doze Timer is disabled and thus the power management function via the internal hardware timer scheme is disabled. However, the Doze or Sleep Mode is still available by a command to the Status Register.

PMU Registers

The VL82C312 internal registers are accessed via an indexed address and data register scheme which is compatible with the VL82C310 SCAMP Controller. The index value is first written to the Index Register (ECh) and the data is read or written from the Data Register (EDh). The Index Register is a read/write register. When reading the Index Register, the VL82C310 returns the value to the CPU. The Index Register is a write-only register in the VL82C312.

The PMU's register range is from C0h to DFh. Write access to the data registers is locked out when entering the Suspend or Off Mode, or when power is first applied to the PMU. Bit 0 in the Supply Register is set to indicate that write access is not allowed. To unlock the write access, the CPU must first read the Supply Register. Once the write access is unlocked, the VL82C312 stays unlocked until it enters the Suspend or Off Mode, or until –RCRESET is asserted. See the section "Register Descriptions" for detailed information.

RTC IRQ8 Interrupt Handling

The VL82C312 can be placed into the On Mode by the RTC's time of day interrupt. The –RTCIRQ pin is an edge sensitive input from VL82C107 SCAMP Combination I/O chip. In the Suspend Mode, the system power is off and the RTC logic in the VL82C107 and the VL82C312 remain powered. In order to prevent the leakage through the unpowered VL82C310 SCAMP Controller, the –RTCIRQ signal from the VL82C107 is connected to the VL82C312. The VL82C312 will regenerate the IRQ8 signal to VL82C310 from the VL82C107 in normal operation. An external pull-up resistor is required on the –RTCIRQ input pin of the VL82C312 because the VL82C107 uses an open drain output buffer for –RTCIRQ.

Keyboard Clock Control

To further reduce power consumption, the VL82C312 controls the keyboard clock in the VL82C107 SCAMP Combination I/O chip via two control signals: –KBSLOWCK and KBCLK. When the PMU is in the Doze or Sleep Mode, the VL82C312 drives the –KBSLOWCK signal low and the VL82C107 stops the clock to the keyboard controller. Only when the VL82C312 detects a high-to-low transition on the KBCLK signal from the keyboard or an access to ports 60h or 64h occurs, does it drive –KBSLOWCK to high for 0.5 to 1.0 seconds, activating the keyboard controller. Activity other than keyboard accesses do not cause the –KBSLOWCK signal to go high unless the VL82C312 goes back to the On Mode. The –KBSLOWCK signal is a glitch free signal and provides a 142 ns minimum width pulse.

POWER SUPPLY INTERFACE

The VL82C312 controls the power to individual system devices to achieve maximum power savings. It is designed to interface to an intelligent power supply. To take full advantage of the VL82C312 PMU features, the power supply should have the following features.

Power Control Signals

The LB and LLB input signals are used to report low battery condition. The VL82C312 has ten power control output signals VP7-VP0, VPBIAS, and –VPVSIG. VP7-VP2 are general purpose power control outputs. VP1 is used to control the LCD backlight power. VP0 is used to control the LCD panel power. VPBIAS is used to control the LCD bias power and –VPVSIG is used to control the LCD clock and data buffer. PWGIN is an input signal from the power supply indicating the power is good. PWGOUT is an output signal to the VL82C310 SCAMP Controller. ACPWR is an input signal from the power supply to indicate the system is running on AC power. Figure 1 shows the power supply interface.

LCD Panel Power-Up/Down Sequencing

Most LCD panels have a +5 V power supply and a bias power supply. These power sources, along with the clock and data lines to the LCD panel, are required to be sequenced correctly to prevent damage to the LCD panel. In addition, isolation must be provided between the LCD controller and the LCD panel to prevent destructive CMOS latch-up when power is applied. Therefore, VP0, VPBIAS, and –VPVSIG are provided to serve this purpose.

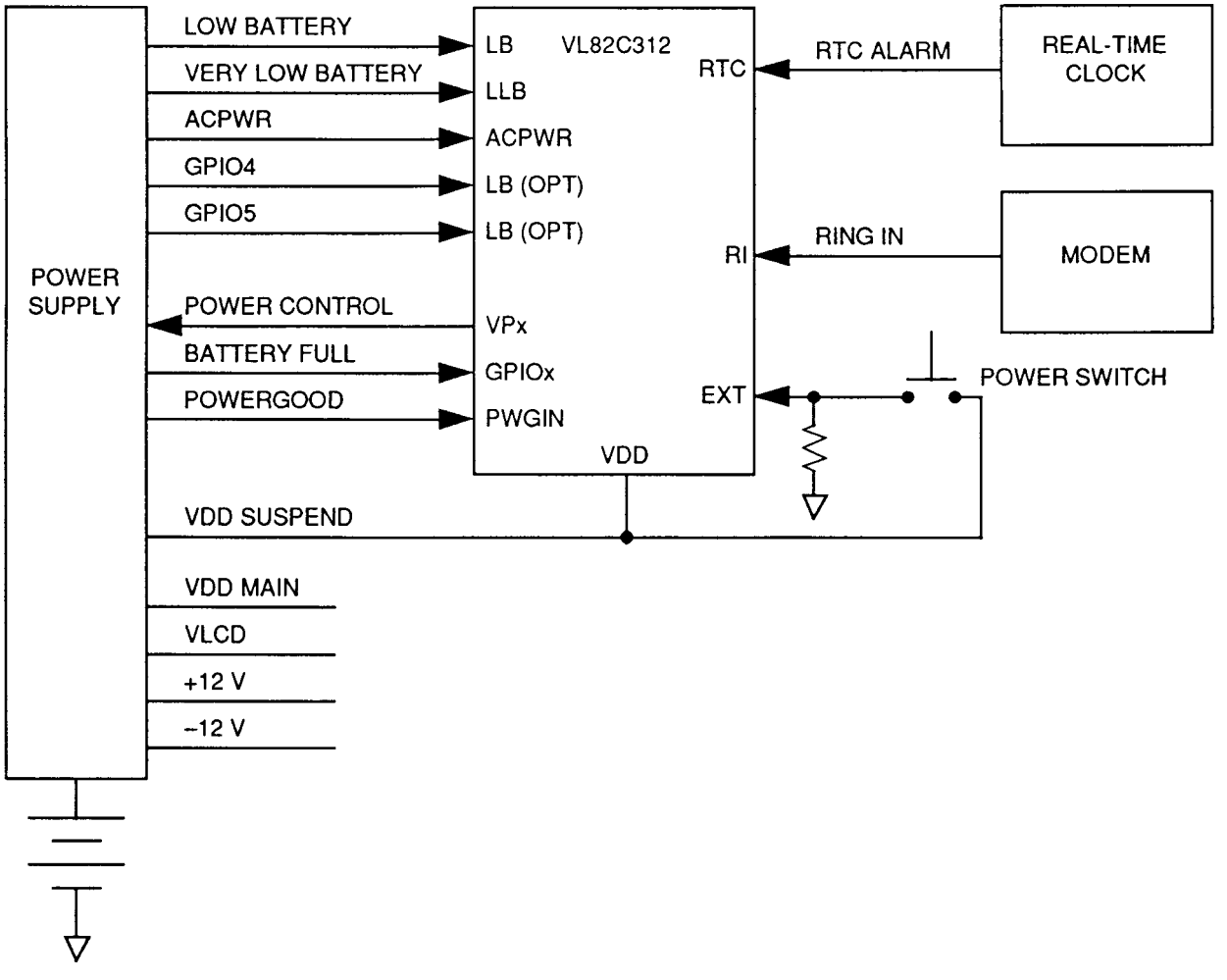
*** Warning: Improper LCD Power Sequencing May Cause LCD Panel Damage.***

The polarity of VPBIAS and VP0 are controlled by bit 0 in the Polarity Register. The polarity of –VPVSIG is defined to be active low for power-on, and is not programmable.

VP0 is active when bit 0 is set in the PWR Register for the currently active mode, and (in most cases) when the LCD Timer has not timed out.

When power is first applied to the PMU, –RCRESET clears bits EN_LCDSEQ, LCDTMG1, and LCDTMG0 in the MISC Register, and sets MSK_LCD in the

FIGURE 1. POWER SUPPLY INTERFACE



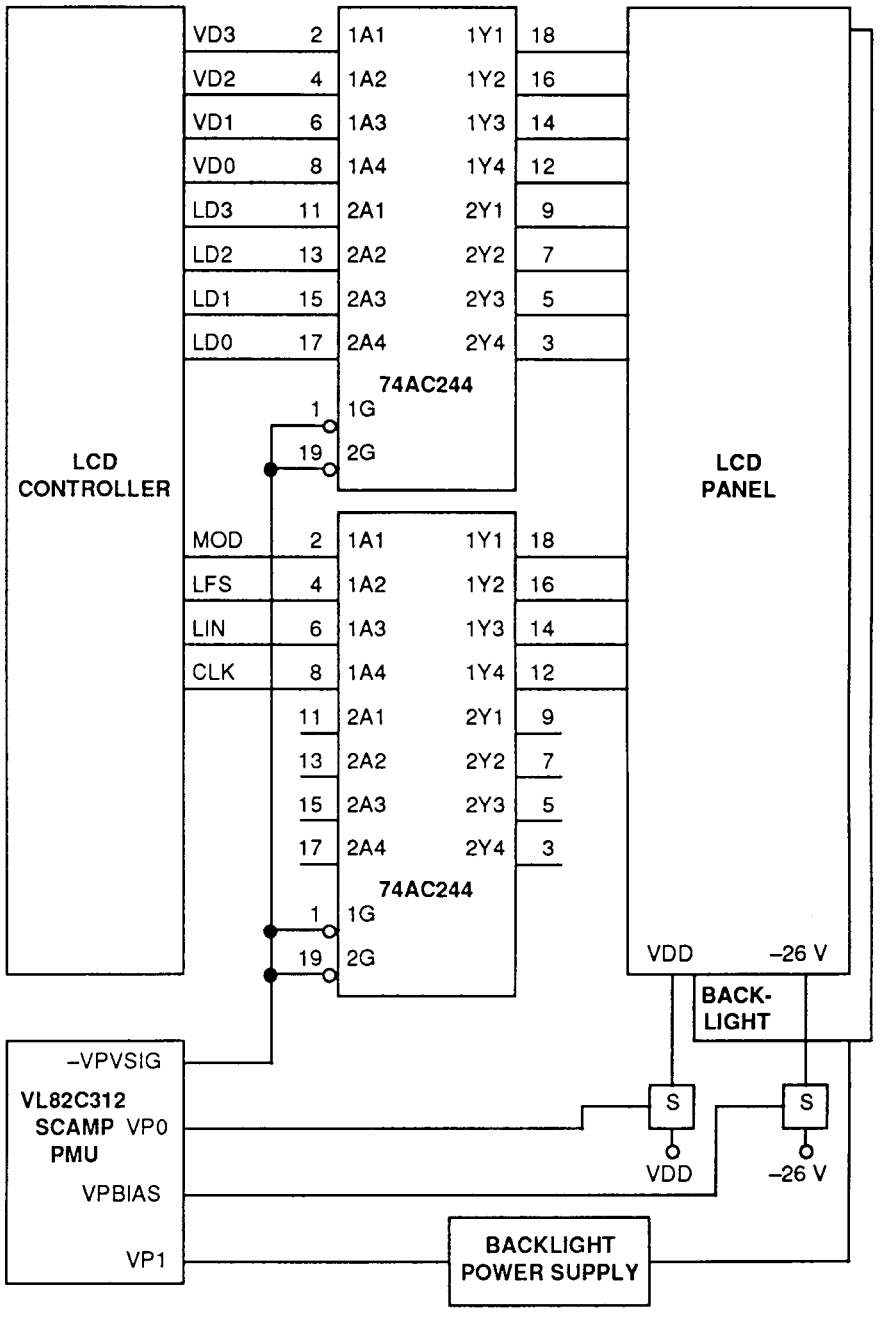
NMIMASK-II Register. This selects BIOS LCD power sequencing. VP0 and VPBIAS are active high polarity, –VPVSIG is active low, and all are inactive or in the Off Mode. From this point, LCD power sequencing may be done either by the BIOS directly manipulating these signals, or automatically by the PMU by placing the PMU in the Automatic LCD Power Sequencing Mode. See Figure 2.

Automatic LCD Power Sequencing
This is the simplest method and should be used when the panel timing requirements can be satisfied by the VL82C312.

The Automatic LCD Power Sequence Mode is enabled by setting the EN_LCDSEQ bit. When this bit is set, VP0, VPBIAS and –VPVSIG become automatically sequenced outputs and cannot be directly controlled by software. The LCDTMG1 and LCDTMG0 bits specify a power sequencing delay time (see section "Register Descriptions"). VP0 must remain inactive while these bits are programmed, otherwise the VPBIAS and –VPVSIG outputs change state. The initial conditions must be: EN_LCDSEQ, LCDTMG1 and LCDTMG0 are low and the D0 bits in the PWRON and PWRDOZE Registers are low (automatic sequencing disabled, VP0, VPBIAS, and –VPVSIG off). First, EN_LCDSEQ is set. Then LCDTMG1 and LCDTMG0 are set to the desired delay time. Finally, bit 0 in the PWRON and PWRDOZE Registers are set to allow the display to turn on in the On or Doze Mode while the LCD Timer has not timed out. VP0 goes active, –VPVSIG goes active after the programmed delay, and after another equal delay VPBIAS goes active. When the display is to be powered down, VPBIAS goes inactive, then after the delay –VPVSIG goes inactive, and after another delay VP0 goes off. If Automatic Sequencing is enabled when the VL82C312 PMU enters the Suspend or Off Mode, the LCD sequentially turns off.

BIOS Controlled LCD Power Sequencing
This method is only for special displays that cannot be handled with the Automatic Sequencing Mode. The

FIGURE 2. LCD POWER SEQUENCING/ISOLATION CIRCUITRY



BIOS has direct control over all three signals. After –RCRESET, VP0 is controlled normally via the appropriate PWR Register's bit 0. –VPVSIG can be activated by setting LCDTMG0 high, and VPBIAS can be activated by setting LCDTMG1 high. To make practical use of this hardware, the BIOS must enable some NMI's.

If MSK_LCD is cleared, the LCD Timer no longer affects VP0. When it times out, it generates NMI and the BIOS can then control VP0, –VPVSIG, and VPBIAS in the proper order and timing. Of course, one or more activity detection NMIs should also be enabled so that the BIOS can turn the LCD back on again. If EN_LCDSEQ is low, LCDTMG1 and LCDTMG0 are cleared when the VL82C312 PMU enters the Off Mode.

PMU Reset and Initialization
The VL82C312 requires the –RCRESET input signal to reset itself, when power is first applied to it. This signal is generated from an external RC network, thus a Schmitt-trigger input is used. The resistor should be a 100 kΩ pull-up tied to the VL82C312's VDD, and the capacitor should be a 1.0 µF connected to ground. The RC network must tie to the same power source as the VL82C312. The PWGIN signal does not affect the initialization of the VL82C312. For proper initialization of the power control circuitry, PWGIN must no go active until RCRESET goes inactive. After the internal registers are written by the CPU, the information remains the same regardless of the assertion or de-assertion of the PWGIN signal, until a low on the –RCRESET pin is detected or the registers are rewritten by the CPU.

AC Power Monitoring
The ACPWR input informs the VL82C312 that the system is running on AC power. If ACPWR is high, the VL82C312 disables the Doze, Sleep, and LCD Timers, thus the automatic hardware power saving features will be disabled. Since these timers are disabled, the system is running at maximum speed and peripheral devices are not turned off. Only the BL Timer is enabled for controlling the LCD backlight. Once the BL backlight is turned off, it is turned back on by any keyboard activity. However, all the power saving features can still be controlled by software when ACPWR is applied.

Low Battery Warning
The battery condition can be monitored by the power supply or by an external voltage comparison circuit. The VL82C312 has two dedicated pins, LB and LLB, to monitor the battery level. LB is the first level of a low battery warning signal. LLB is a warning signal of a "very" low battery level. If a low battery input is high, and the corresponding NMI is unmasked, the VL82C312 generates an NMI every 15 seconds. The BIOS can flash a warning message on the screen, turn on a low battery indicator, or save the current application and command the VL82C312 to enter the Suspend Mode.

The VL82C312 also has two additional GPIO pins that can be programmed as low battery inputs for more levels of battery condition detection. The low battery inputs are debounced. To be recognized, these inputs must be high for two to four seconds if the FASTDB bit in the MISC Register is cleared, or 30-60 ms if FASTDB is set. Refer to sections "NMI Generation and Handling" and "GPIO4, GPIO5/LB1 and LB2 NMI" for more details.

PWGIN and PWGOUT
The PWGIN input is an active high signal from the power supply. PWGIN does not reset the VL82C312 when it goes low. When a transition of PWGIN from low-to-high is detected, after a delay of 0.5 to 1.0 seconds, the VL82C312 asserts PWGOUT high to the VL82C310 SCAMP Controller. If the PWGIN goes low when the VL82C312 is not in the Suspend or Off Mode, the VL82C312 asserts PWGOUT low immediately and places itself into the Off Mode. The PWGOUT goes low before the PWGIN goes low if the VL82C312 is commanded to enter the Suspend or Off Mode.

NMI GENERATION AND HANDLING
There are 13 different sources of an NMI logically ORed together by the VL82C312. These can be masked off independently by bits in the NMIMASK-I and NMIMASK-II Registers. At power-on, all NMIs are masked. When an internal NMI is generated, it generates a minimum 570 ns wide pulse. The cause of the NMI is latched and can be read from NMICAUSE-I and NMICAUSE-II Registers. The NMICAUSE-I and NMICAUSE-II Registers are cleared when read. A read of the NMICAUSE-I Register also clears the NMI cause code in the Status Register. The NMI can also be read from the Status Register for INMI, Sleep NMI, activity NMI, Suspend NMI, EXT NMI, and LB, LLB NMI. If any of the NMI in the NMICAUSE-II Register are enabled, then the BIOS should read the NMICAUSE-I and NMICAUSE-II Registers for NMI information and should not rely on the Status Register. Reading the NMIMASK-I Register does not affect the NMICAUSE Registers.

A timer is provided to automatically place the VL82C312 in the Off Mode if the LLB NMI is not serviced. See section "Auto Power Off Timer".

Although this specification refers to NMI throughout, the internally generated interrupt can be routed to NMI, IRQx, both or neither. If the MSK_NMI bit in the NMIMASK-I Register is cleared, the NMI pin is driven by the OR of all internally generated interrupts and the INMI pin. If set, only the INMI drives the NMI output pin. If the MSK_IRQx bit in the NMIMASK-I Register is cleared, IRQx output is active if any other bit besides the I_NMI bit is set in either NMICAUSE Register. If set, IRQx remains inactive.

INMI
The INMI input comes from the VL82C310 SCAMP Controller for reporting PC/AT-compatible standard NMIs such as parity error or IOCHCHK. If the MSK_NMI bit in the NMIMASK-I Register is set, INMI still causes the NMI output to be active but internally generated interrupts do not.

Doze Timer NMI
When VL82C312 detects no activity and the Doze Timer times out, it generates an NMI if the MSK_DOZE bit is cleared in the NMIMASK-II Register. The VL82C312 remains in the On Mode.

Sleep Timer NMI
If MSK_SLEEP bit in the NMIMASK-I Register is cleared, the VL82C312 generates an NMI when the Sleep Timer times out and remains in Doze Mode.

Activity NMI and LCD Activity NMI
If MSK_DOZE is cleared, activity detection occurring while the VL82C312 is in the Doze Mode generates an Activity NMI. ACT_NMI in NMICAUSE-I is set, and the VL82C312 remains in the Doze Mode. If MSK_SLEEP is cleared, the VL82C312 behaves the same way in the Sleep Mode.

If MSK_LCD is cleared, and the LCD Timer has previously timed out, activity that triggers the LCD Timer causes an LCD Actvity NMI. ACT_LCD_NMI in NMICAUSE-I will be set. If EN_LCDSEQ is set, the LCD power is automatically sequenced on, otherwise the BIOS must turn it on via the power control bits.

Suspend Timer NMI
If the MSK_SUSPEND bit in the NMIMASK-I Register is cleared, the VL82C312 generates an NMI when the Suspend Timer times out, and it remains in the Sleep Mode. The BIOS saves the system status and commands the VL82C312 to enter the Suspend Mode. If the MSK_SUSPEND bit is set, the Suspend Timer is disabled. Refer to the section titled "Suspend Mode" for more information on entering the Suspend Mode.

Rescheduled Suspend NMI
When the Suspend Timer times out or the EXT pin goes high, the VL82C312 generates an NMI to inform the BIOS to start the Suspend procedure. But the application program may be in the middle of something that may cause the system to be not resumable if entering the Suspend Mode at this moment. A rescheduled Suspend NMI is provided to inform the BIOS to try to enter into the Suspend Mode whenever possible. When the MSK_RESCH bit in the NMIMASK-II Register is cleared, the VL82C312 generates the rescheduled NMI every 60 ms. This feature can also be used to generate tick interrupts for the power management software. Refer to section "Suspend Reschedule Timer" for more information.

EXT NMI
EXT is a rising edge sensitive internally debounced input and is intended for use with an external pushbutton switch. A rising transition on this input while the VL82C312 is not in the Suspend or Off Mode generates an NMI. Software can then save the status and go to the Suspend or Off Mode.

LB, LLB NMI
LB and LLB are active high inputs. The LB and LLB NMIs are masked by MSK_LB and MSK_LLB, respectively. If a low battery input is high, and the corresponding NMI is unmasked, the PMU generates an NMI every 15 seconds until it enters the Suspend or Off Mode. This is not the case for IRQx. IRQx remains active until the NMICAUSE Register is read.

GPIO4, GPIO5 / LB1 and LB2 NMI
When MSK_GPLBx bits in the NMIMASK-II Register are unmasked, GPIO4 and GPIO5 can be used as LB1 and LB2 low battery warning inputs, respectively. They are active high inputs. and are GPIO input pins at power-on reset.

LCD Timer NMI
If the MSK_LCD bit in the NMIMASK-II Register is cleared, the VL82C312 generates an NMI when the LCD Timer times out. If EN_LCDSEQ is set, the LCD power is automatically sequenced off, otherwise the BIOS must turn it off.

SYSTEM ACTIVITY MONITOR
The system activity monitor is used to monitor I/O or video activity. If no activity is detected for a period of time determined by one of several timers, the VL82C312 can generate an NMI or enter a power saving mode. If activity is detected, the VL82C312 can generate an NMI or enter the On Mode. There are eight system operations treated as a detection of activity and each of these can be masked independently in the ACTMASK Register. A bit is set in the Activity Register for each unmasked activity that has occurred since the last time the register was read. The Activity Register is cleared when read.

Parallel I/O Ports	Any read or write access to LPT1, LPT2, or LPT3 is treated as an activity. The address range for: LPT1 is 378h to 37Fh, LPT2 is 278h to 27Fh, and LPT3 is 3BCh to 3BFh.
Keyboard Ports	A read of the keyboard port 60h.
RTC Ports	Any read or write access to the RTC ports 70h and 71h.
Serial Ports	Any read or write access to the COM1-COM4 ports. The address range for: COM1 is 3F8h to 3FFh, COM2 is 2F8h to 2FFh, COM3 is 3E8h to 3EFh, and COM4 is 2E8h to 2EFh.
Floppy Disk Port	A read or write to the floppy disk data port 3F5h.
Hard Disk Port	A read or write to 1F0h to 1F7h.
Video Memory Writes	It is recommended that the video memory write signals should be connected to the –VIDCS4 - –VIDCS0 inputs of the VL82C312. When a transition from high-to-low on –VIDCS4 - –VIDCS0 is detected, it is treated as an activity and cause an exit from the Doze or Sleep Mode, if the MSK_VIDM bit in the ACTMASK Register is not masked. If it is masked, a –VIDCS4- –VIDCS0 low transition causes the –SLOWCLK pin to go high for 8 ms without exiting from the Doze or Sleep Mode, temporarily speeding up the CPU clock.
Programmable I/O	A programmable I/O range to the activity monitor allows the designer to monitor a non-standard I/O device for activity. This I/O address is specified in the IORNG Register. The I/O range can be 8 bytes long or 16 bytes long. Default programmable I/O range is 16 bytes long.
External Activity	A rising edge on the EXTACT pin is sensed as activity, however, there is no mask bit for this activity, nor is it reported in the Activity Register.

OPERATION STATES
The VL82C312 has five modes:
- On Mode
- Doze Mode
- Sleep Mode
- Suspend Mode
- Off Mode

Each mode can be entered through a timer time-out or by detection of activity. It also can be entered anytime by writing the Status Register's bits 1 and 0.

On Mode
The On Mode is entered from the Suspend or Off Mode when either the EXT, RTC, or RI pins goes high. At this time, the Doze, BL, and LCD Timers

are retriggered. When the VL82C312 is first powered up, –RCRESET is also set to the On Mode. The On Mode may also be entered from the Doze or Sleep Mode when the activity monitor detects activity. In the On Mode, all power control outputs are controlled by the PWRON Register. Entering the On Mode and activity detection in the On Mode retriggers the Doze Timer.

If ACPWR is high, the Doze Timer is disabled and causes the hardware power saving features of the VL82C312 to be disabled except for the BL Timer. Unless commanded to change modes, the VL82C312 remains in the On Mode and its –SLOWCLK output pin is high.

Doze Mode
If the MSK_DOZE bit in the NMIMASK-I Register is set, the Doze Mode is entered from the On Mode when the activity monitor has not detected activity within the time specified by the Doze Timer Register. Any unmasked activity causes an exit from the Doze Mode to the On Mode. Alternatively, if MSK_DOZE is cleared, the VL82C312 generates an NMI and remains in the On Mode until the BIOS commands it to enter the Doze Mode or another mode. Any unmasked activity causes an activity NMI. In the Doze Mode, the power control outputs are controlled by the PWRDOZE Register, the –SLOWCLK pin goes low and VL82C310 SCAMP Controller may slow down the CPU clock. Interrupts, NMIs, or video memory writes will temporarily force the –SLOWCLK output pin high, as described in the section" Clock Switching".

Sleep Mode
If the MSK_SLEEP bit in the NMIMASK-I Register is set, the Sleep Mode is automatically entered from the Doze Mode when the activity monitor has not detected activity within the time specified by the Sleep Timer Register. Any unmasked activity causes an exit from the Sleep Mode to the On Mode. Alternatively, if MSK_SLEEP is cleared, the VL82C312 generates an NMI and remains in the Doze Mode until the CPU commands it to enter the Sleep Mode. Any unmasked activity causes an activity NMI. The –SLOWCLK pin behavior is the same as when in the Doze Mode. The power control outputs are controlled by the PWRSLEEP Register.

Suspend Mode
If software support is provided for the Suspend Mode, the VL82C312 can be programmed to generate an NMI after the Suspend Timer times out, or in response to a low-to-high transition on the EXT input pin when the VL82C312 is not in the Suspend or Off Mode. After saving the system information, the BIOS can place the PMU in the Suspend Mode via the Status Register. The BIOS may halt the CPU, but it is not necessary. The BIOS must not read data or instructions from DRAM after issuing the Suspend command. The power control outputs are controlled by the PWRSUSPEND Register.

Refresh Control
The –RAS3 - –RAS0 and –CAS3 - –CAS0 lines from the VL82C310 SCAMP Controller are bused to the VL82C312. The VL82C312 three-states its outputs connected to these lines during normal operation and drives them to refresh the DRAM during Suspend, since the VL82C310 is not powered in this mode. When the VL82C312 is commanded to enter the Suspend Mode and PWRGD is driven low to the VL82C310, the VL82C312 takes over refresh of on-board DRAM. It performs CAS before RAS refresh cycles at the rate determined by the SLWREF bit in the Control Register.

Resume From Suspend
Only activity on the EXT, RI, or –RTCIRQ input pins can cause an exit from the Suspend Mode. The new mode is the On Mode. The cause of a resume can be examined in the WU0 and WU1 bits in the Status Register. The BIOS must read the RESUME bit in the Status Register to determine if a cold boot or a return from the Suspend Mode has occurred. If the RESUME bit is true, the BIOS restores all information and verifies data in the main memory and video memory is still valid. The process of reading the RESUME bit in the Status Register resets the RESUME bit.

When a wake-up event occurs, the VL82C312 enters the On Mode and turns on VDD 0.5 to 1.0 seconds later. After PWGIN goes high, the digital signals that were three-stated or held low are allowed to go to their normal levels. Once PWGOUT is driven high, the VL82C312 discontinues the on-board DRAM refresh and the VL82C310 takes over.

Off Mode
The VL82C312 enters the Off Mode after a falling edge on the PWGIN input, or when the CPU writes the code for Off (FFh) to the Status Register. The Auto Power Off Timer also causes the VL82C312 to enter the Off Mode.

The Off Mode is meaningful only when the VL82C312 is powered from a battery while the rest of the system is turned off. This type of connection is necessary only if the VL82C312 must awaken the system from the Off Mode by activating the VP outputs in response to transitions on the EXT, RI, or RTC inputs. If this function is not implemented, the VL82C312 may be powered off along with the system power (as with a switch) and the Off Mode does not exist.

In the Off Mode, all devices except battery backed up devices in the computer are powered off. Only –RCRESET or activity on the EXT, RI, or RTC inputs can cause an exit from the Off Mode and into the On Mode. When powered up from the Off Mode, the burst refresh is not activated, and if –RCRESET was not asserted, the contents of the VL82C312's internal registers are not changed after awaking from the Off Mode.

TIMERS
There are ten timers in the VL82C312. Some timers are associated with the activity monitors controlling mode transitions. A detailed description of the timers follows.

Doze Timer
The Doze Timer is programmable from 1/8 to 1 second with a resolution of 1/8 second, and from 2 to 14 seconds with a resolution of two seconds. Setting a zero value to the timer disables it and setting any non-zero value enables it. Any activity detected by the activity monitor retriggers the Doze Timer. The default value for the Doze Timer is four seconds.

Sleep Timer
The Sleep Timer is programmable from 1 to 15 minutes with a resolution of one minute. Setting a zero value to the timer disables it and setting any non-zero value enables it. Any activity detected by the activity monitor will retrigger the Sleep Timer. The Sleep Timer is triggered when the Doze Mode is entered and is cleared when the Doze Mode is exited. The default value for the Sleep Timer is two minutes.

Suspend Timer
The Suspend Timer is programmable from 5 to 75 minutes with a resolution of five minutes. Setting a zero value to the timer disables it and setting any non-zero value enables it. Any activity retriggers the Suspend Timer. The Suspend Timer is triggered when Sleep Mode is entered and is cleared when the Sleep Mode is exited. The default of the MSK_SUSPEND bit is masked, thus it disables the Suspend Timer. The default value for the Suspend Timer is five minutes.

Backlight (BL) Timer
The BL Timer is programmable from 1 to 15 minutes with a resolution of two minutes. Setting a zero value to the timer disables it and setting any non-zero value enables it. The BL Timer is always enabled and is retriggered when keyboard activity is detected. The default value for the BL Timer is two minutes.

LCD Timer
The LCD Timer is programmable from 1 to 15 minutes with a resolution of one minute. Setting a zero value to the timer disables it and setting a non-zero value enables it. It is disabled if ACPWR is true. It is triggered when the VL82C312 goes from the Off or Suspend Mode to the On Mode. It is also triggered when keyboard activity occurs or when –VIDCS4 - –VIDCS0 are asserted. The default value for the LCD Timer is two minutes.

Suspend Reschedule Timer
The Suspend Reschedule Timer is fixed at 60 ms. While the MSK_RESCH bit in the NMIMASK-II Register is cleared, the VL82C312 generates a suspend re-schedule NMI every 60 ms. This timer can be retriggered by momentarily setting and clearing the MSK_RESCH bit. This feature can be used to generate reliable tick interrupts for the power management software if the system clock timer has been reprogrammed by the application or OS software. If this timer is retriggered at each INT8, it never times out, but if other software takes over the system timer, it times out and repeatedly generates an NMI until masked.

Auto Power-Off Timer
If the LLB NMI is unmasked and is not serviced within three minutes while LLB remains continuously true, the VL82C312 automatically goes to the Off Mode.

VIDCS Timer
A fixed 8 ms timer is provided for the video memory write operations. If the MSK_VIDM bit in the ACTMASK Register is set, any –VIDCS4 - –VIDCS0 low transitions are not treated as an activity detection. The VL82C312 temporarily brings the –SLOWCLK pin high for 8 ms without exiting from either the Doze or Sleep Mode. If the MSK_VIDM bit is cleared, this timer is disabled. Default is disabled.

Low Battery Timer
The Low Battery (LB) Timer is enabled in the On, Doze and Sleep Mode. The LB Timer is fixed to 15 seconds. An NMI is generated by the LB Timer every 15 seconds until a timer period elapses during which all low battery inputs are continuously false. This is also true for IRQx, if it is active.

Power-On Fault Timer
If PWGIN fails to go high within one to two seconds after wake-up, the VL82C312 goes back to the previous mode (Off or Suspend).

Time Register
This read-only register contains the value of a counter which counts cycles of the 32 kHz clock whenever it is running. Unlike the system clock timer, it cannot be altered by the application software and can provide a reliable relative time reference for the power management software. It is cleared when –RCRESET is active.

POWER-ON
There are three power-on inputs to the VL82C312:
- RTC
- RI
- EXT

These inputs can bring the VL82C312 out of the Suspend or Off Mode and into the On Mode. Since these inputs control the power on/off for the system, care must be taken to insure these inputs never float. To insure these inputs are always driven, tie any unused inputs low.

RTC Power-On
–RTCIRQ is an edge sensitive input, intended for use with the real-time clock's wake-up alarm from VL82C107 SCAMP Combination I/O chip. Any transition on this input forces the VL82C312 into the On Mode. The VL82C312 generates an IRQ8 output to the VL82C310 SCAMP Controller to prevent leakage in the Suspend Mode.

Ring Indicator Power-On
RI is a rising edge sensitive input, intended for use with a modem ring indicator output. The number of rising edges required for this input to be recognized is specified in bits D6-D4 of the Control Register. The default is one transition. If these bits are zero, the RI input is disabled. If enabled, the programmed number of edges forces the VL82C312 into the On Mode.

External Switch Power-On
EXT is a rising edge sensitive input, intended for use with an external pushbutton. A rising transition on this input while the VL82C312 is in the Off or Suspend Mode forces it in to the On state. A transition in the On, Doze, or Sleep Mode generates an NMI.

EXT is internally debounced. A rising edge immediately generates an NMI if EXT has been sampled low at least twice by a 32 Hz debounce clock prior to the rising edge. The VL82C312 does not respond to any activity on any other wake-up input until after EXT has been sampled low twice by the debounce clock.

LEAKAGE CONTROL DURING SUSPEND AND OFF

Leakage control is active during the Suspend and Off Modes in order to provide absolute minimal current consumption. However, there is a set of signals for which the system designer must externally control leakage either because they must remain functional during the Off Mode or to prevent the design of the VL82C312 from placing restrictions on the user's circuits.

These signals are:

- LB
- LLB
- RI
- EXT
- –RTCIRQ
- ACPWR
- PWGIN
- –RCRESET
- RTCX1
- RTCX2
- GPIO9-GPIO0

GPIO

The VL82C312 has ten general purpose pins that may be individually programmed as inputs or outputs. Some can be programmed as blinking outputs, low battery inputs or AND/OR inputs or outputs. They default to general purpose inputs at power-on. If not used, the pins must be tied low to prevent leakage, alternatively they may be programmed as outputs to prevent leakage. For example, the pins could be used for monitoring the power supply status, EEPROM interface, or as software controlled VP outputs.

Blinking Option

The GPIO3 pin can be used as a programmable audio and/or blinking generator. The blinking option is enabled by setting the EN_BLK bit in the MISC Register. Default is reset. The blink generator produces an audible output frequency which blinks on and off. The frequency, blink rate, and number of blinks are programmed by the Blinking Register. When used to drive an LED rather than a speaker, the use of audio frequencies results in an LED that flashes at the blink rate, but is unaffected by the audio frequency. This feature might be useful to drive an LED indicator, speaker or both in response to a low battery indication or as an indicator of the Suspend Mode active, for example.

Low Battery Option

The GPIO4 and GPIO5 pins can be used as optional low battery warning inputs. Please refer to section "GPIO4, GPIO5 / LB1 and LB2 NMI" for a detailed description.

AND/OR Selectable Option

The GPIO8-GPIO6 pins can be used as an optional AND/OR selectable input and GPIO9 as the resulting output. This option is enabled by setting the EN_ANDOR bit in the ANDOR Register. Default is disabled. If the SEL_AND bit is set, an AND function is selected, otherwise an OR function is selected. Default is an OR function. If the EN_ANDOR bit is low, the SEL_AND bit is ignored.

CHIP SELECTS AND MISCELLANEOUS

The VL82C312 provides additional logic to optimize the glue logic for system integration and to reduce the chip count for a notebook computer design. The glue logic includes the following functions:

- chip select for the IDE, COM1, COM2, printer port and floppy disk controller
- address/data multiplex for the VGA controller
- data buffer for the UART
- glue control logic for the floppy disk controller

The chip select functions are enabled/disabled through control bits located in the Data Register which are accessible through the Index Port at address EC hex. The index address for the Chip Select Control Register is DA hex. The default values for the Control Register have been selected so as to eliminate the need to change their values in typical system configurations. The control bits are defined in Table 1.

Chip Select Control Register (CSCNTL)
Index Register: ECh
Index Address: DAh
Data Register: EDh

Bit 0 IDEEN - IDE Enable: Enables the IDE interface when set. –IDENH and –IOCS16 are active for accesses to 1F0h. –IDENL is active when either –IDECS0 or –IDECS1 are active. –IDECS0 decodes addresses 1F0h-1FFh and –IDECS1 decodes 3F6h-3F7h. When the IDE enable bit is cleared, –IDENH, –IDENL, –IDECS0, and –IDECS1 are disabled. Power-on reset default = 1.

Bit 1 COMS - Communications Port Default: Selects address decode ranges for –CS0 and –CS1. If set, –CS0 is decoded from 3F8h-3FFh and –CS1 is decoded from 2F8h-2FFh. When cleared, –CS0 is decoded from 3E8h-3EFh and –CS1 from 2E8h-2EFh. Power-on reset default = 1.

TABLE 1. CHIP SELECT CONTROL REGISTER BIT DEFINITIONS

Register (DAh)	D7	D6	D5	D4	D3	D2	D1	D0
CSCTRL	FDCEN	LPTEN	LPT1	LPT0	COMB	COMA	COMS	IDEEN

TABLE 2. DECODING RANGE FOR LINE PRINTER CHIP SELECT

LPT1	LPT0	Decode Range
0	0	3BC-3BF hex
0	1	378-37B hex
1	0	278-27B hex
1	1	Undefined

Bit 2 COMA - Primary Communication Port Enable: If set, –CS0 address decoding is enabled. Power-on reset default = 1.

Bit 3 COMB - Secondary Communication Port Enable: If set, –CS1 address decoding is enabled. Power-on reset default = 1.

Bits 4, 5 LPT0, LPT1 - Line Printer Chip Select Decode: Determines the address decoding range for the line printer chip select, –CS2. The bits are decoded as shown in Table 2.

Bit 6 LPTEN - Line Printer Chip Select Enable: If set, line printer chip select address decoding is enabled. Power-on reset default = 1.

Bit 7 FDCEN - Floppy Disk Chip Select Enable: If set, floppy disk chip select address decoding is enabled using –FDCCS, –CS3, and –CS4. Two sets of floppy disk decoding are available, which allow either a 82077 or 765 floppy disk controller to be used. The first set consists of the single –FDCCS pin, which decodes 3F0h-3F7h (82077 compatible). The second consists of the –FDCSS pin in concert with the –CS3 and –CS4 pins, with the –FDCCS pin decoding 3F4h-3F5h, the –CS3 pin decoding 3F2h, and the –CS4 pin decoding 3F7h (765-compatible). The address range selected by the –FDCCS pin is determined by the reset value of the –FDCCS pin. At the falling edge of RSTDRV if –FDCC is high, the –FDCCS pin decodes 3F0h-3F7h; if low on reset, 3F4h-3F5h is decoded. Note that even if –FDCCS is high on reset, –CS3 and –CS4 still decode their respective address ranges. Power-on reset default = 1.

Multiplexed Address/Data Bus
The address portion of the multiplexed address/data bus is generated by driving the value on the SA bus onto the AD bus pins when the –ASEL input is low. Data direction to/from the SD bus and from/to the AD bus is controlled by the VDIR and –DSELL/–DSELH pins. When VDIR is low, data is directed from AD to SD with the high and/or low byte being driven if –DSELH and/or –DSELL, respectively, are active. If VDIR is high, the SD high byte and/or low byte are driven onto the AD high byte and/or low byte if –DSELLH and/or –DSELL, respectively, are active.

Miscellaneous Gates
The logic for the VL82C312 includes generation of an inverted RSTDRV signal, –RESET, that can be used for resetting a VL16C452 (UART) and for –IDERST. In addition, generation of the –FDACK2 signal for a 82077 floppy disk controller from the –DACK2 and MFM inputs is provided, reducing the need for external gates. The logic equation for this function is:

–FDACK2 = NOT (NOT (–DACK2) AND MFM).

The PCLOCK output is the inverted MCLK for the video controller RAMDAC. A 32 kHz clock output, 32KOUT, is also provided for VGA refresh clocks during the Suspend Mode.

REGISTER DESCRIPTIONS

Tables 3 through 27 list the register contents of the VL82C312 SCAMP PMU.

TABLE 3. REGISTER DESCRIPTIONS

Register	Index		Register	Index
STATUS	C0h		LCD	CFh
SUPPLY	C1h		BL	D0h
CONTROL	C2h		NMIMASK-II	D1h
ACTMASK	C3h		NMICAUSE-I	D2h
NMIMASK-I	C4h		NMICAUSE-II	D3h
IORNG	C5h		MISC	D4h
PWRON	C6h		REVID	D5h
PWRDOZE	C7h		BLINKING	D6h
PWRSLEEP	C8h		GPDIR	D7h
PWRSUSPEND	C9h		GPEN	D8h
POLARITY	CAh		ANDOR	D9h
OUTPUT	CBh		CSCTRL	DAh
DOZE	CCh		ACTIVITY	DBh
SLEEP	CDh		TIME	DCh
SUSPEND	CEh			

TABLE 4. STATUS REGISTER (C0h)

Bit	Name	Function
D7	RESUME	Resuming from Suspend (Warm Start)
D6	WU1	Wake-up Code MSB
D5	WU0	Wake-up Code LSB
D4	NMI2	NMI Cause Code
D3	NMI1	NMI Cause Code
D2	NMI0	NMI Cause Code
D1	MODE1	Mode MSB
D0	MODE0	Mode LSB

Only D0 and D1 are affected by a write. The CPU can write the mode code to this register to put the VL82C312 into another mode. Writing 0FFh puts it in the Off Mode. The NMI cause, mode, and wake-up codes are listed in Table 5.

TABLE 5. NMI CAUSE, MODE AND WAKE-UP CODES

NMI		Mode		Wake-up	
Code	Cause	Code	Cause	Code	Cause
000	None or INMI	00	On	00	
001	EXT Input	01	Doze	01	EXT Input
010	LB	10	Sleep	10	RTC Input
011	LLB Time-out	11	Suspend	11	RI Input
100	Sleep Time-out				
101	Suspend Time-out				
110	Sleep to On (Activity)				

–RCRESET clears all bits. D4-D2 are cleared when the NMICAUSE-I Register is read. D7 is cleared after the Status Register is read.

SUPPLY REGISTER (C1h)
This register has different functions for read and write.

TABLE 6. SUPPLY REGISTER - READ

Bit	Name	Function
D7	ACPWR	
D6	GPIN2	
D5	GPIN1	
D4	GPIN0	
D3	ACTIVITY	System Activity Present
D2	LLB	Low Battery 2 (Second Warning)
D1	LB	Low Battery 1 (First Warning)
D0	LOCKOUT	PMU Registers Write-Protected

TABLE 7. SUPPLY REGISTER - WRITE

Bit	Name	Default	Function
D7	Reserved	0	
D6	GPOUT2	0	General Purpose Output
D5	GPOUT1	0	General Purpose Output
D4	GPOUT0	0	General Purpose Output
D3	Reserved	0	
D2	GPDIR2	0	General Purpose I/O Direction Control
D1	GPDIR1	0	General Purpose I/O Direction Control
D0	GPDIR0	0	General Purpose I/O Direction Control

This GPIO2-GPIO0 pins are programmed as inputs or outputs by D2-D0 and are read and written on D6-D4. For read operations, D7-4, D2, and D1 are driven directly by the input pins. D3 is set when activity is detected and is cleared when this register is read.

TABLE 8. CONTROL REGISTER (C2h)

Bit	Name	Default	Function
D7	Reserved	0	
D6	RING2	0	RI Pulse Required for Turn-on
D5	RING1	0	RI Pulse Required for Turn-on
D4	RING0	1	RI Pulse Required for Turn-on
D3	Reserved	0	
D2	SLWREF	0	1 = Slow Refresh DRAM
D1	Reserved	0	
D0	Reserved	0	

The RING2-RING0 bits are used to set the number of RI pulses required for turn-on. The default value is 1 so that only one pulse is required for turn-on. If set to 0, RI is disabled.

TABLE 9. ACTMASK REGISTER (C3h)

Bit	Name	Default	Function
D7	MSK_IORNG	1	Mask Access to 16 Ports at IORNG5-IORNG0
D6	MSK_VIDM	0	Mask Access to Video Memory
D5	MSK_HD	0	Mask Hard Disk Activity
D4	MSK_FLP	0	Mask Access to Port 3F5
D3	MSK_SIO	0	Mask Access to COM1-COM4
D2	MSK_RTC	1	Mask Access to Port 70h, 71h
D1	MSK_KBD	0	Mask Keyboard Access to Port 60h Reads
D0	MSK_PIO	0	Mask Access to LPT1-LPT3

The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources. This register affects only the ACTIVITY output.

TABLE 10. NMIMASK-I REGISTER (C4h)

Bit	Name	Default	Function
D7	MSK_IRQx	1	Mask IRQx Output
D6	MSK_NMI	0	Mask NMI Output
D5	MSK_SUSPEND	1	Mask Suspend Time-out
D4	MSK_SLEEP	1	Mask Sleep Time-out
D3	MSK_LLB	1	Mask LLB Input
D2	MSK_LB	1	Mask LB Input
D1	MSK_EXT	1	Mask EXT Input
D0	Reserved	0	

This register masks the various NMI sources. In the Default Mode, only the INMI input can generate an NMI.

TABLE 11. IORNG REGISTER (C5h)

Bit	Name	Default	Function
D7	RNGSIZE	0	1 = 8 Bytes, 0 = 16 Bytes
D6	IORNG6	0	Maskable I/O Range Base Address
D5	IORNG5	0	Maskable I/O Range Base Address
D4	IORNG4	0	Maskable I/O Range Base Address
D3	IORNG3	0	Maskable I/O Range Base Address
D2	IORNG2	0	Maskable I/O Range Base Address
D1	IORNG1	0	Maskable I/O Range Base Address
D0	IORNG0	0	Maskable I/O Range Base Address

IORNG6-IORNG0 are the base address bits SA9-SA3 for the maskable I/O port range in the activity monitor. RNGSIZE is the size of the range. IORNG0 is ignored when RNGSIZE is low.

TABLE 12. POWER REGISTERS (C6h-C9h)

Register	Default	Index
PWRON	FEh	C6h
PWRDOZE	FEh	C7h
PWRSLEEP	FCh	C8h
PWRSUSPEND	00h	C9h

The bits in these registers D7-D0 correspond directly with the power control outputs VP7-VP0. In a particular mode, the corresponding PWR Register outputs control the VP pins. The exception is VP0 and VP1 which are LCD and BL power, respectively. These outputs are ANDed with the LCD and BL Timer outputs prior to driving the pins. All bits are then exclusive NORed with the Polarity Register and the result drives the pins. VPBIAS, –VPVSIG, and VP0 are controlled as described in the "Automatic LCD Power Sequencing" section. The default values for these registers are described in Table 12, where 1 indicates that the controlled device is on.

Polarity Register (CAh)
This register controls the polarity of the VP outputs. If a logic low is required on any of VP7-VP0 pins to turn the external device on, the corresponding bit in the Polarity Register must be low. If a high is required, set the bit high. The default value is 0FFh. The polarity of VPBIAS is the same as VP0. –VPVSIG is always low true.

Output Register (CBh)
The Output Register is a read-only register. For each VP7-VP0 output that is on, the corresponding bit in the Output Register will be set.

TABLE 13. TIMER REGISTERS (CCh-D0h)

Timer	Range	Default	Index
Doze	1/8-14 sec	4 sec	CCh
Sleep	1-15 min	2 min	CDh
Suspend	5-75 min	0 (disabled)	CEh
LCD	1-15 min	2 min	CFh
BL	1-15 min	2 min	D0h

Loading a value into a timer register enables the timer and selects the time-out. All timer registers have four significant bits (0 through 3). Data written to the upper bits has no effect. The upper bits are 0 when read back. Except for the Doze Timer, all timer registers can be set for a time-out from 1 to 15 time units, where a unit is the resolution of the timer. A zero disables the timer. Reading a timer register returns the value that was last written to it, not the actual time remaining. The default values are tabulated in Table 13.

The Doze Timer programming for different time-outs is tabulated in Table 14.

TABLE 14. DOZE TIMER PROGRAMMING

D3-D0	Time	D3-D0	Time
0000	Disabled	1000	1 sec
0001	1/8 sec	1001	2 sec
0010	1/4 sec	1010	4 sec
0011	3/8 sec	1011	6 sec
0100	1/2 sec	1100	8 sec
0101	5/8 sec	1101	10 sec
0110	3/4 sec	1110	12 sec
0111	7/8 sec	1111	14 sec

TABLE 15. NMIMASK-II REGISTER (D1h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	MSK_GPLB2	1	Mask off the LB2 NMI option from GPIO5. 1 = Mask. When this bit is low, the GPIO5 is used as LB2 input.
D3	MSK_GPLB1	1	Mask off the LB1 NMI option from GPIO4. 1 = Mask. When this bit is low, the GPIO4 is used as LB1 input.
D2	MSK_RESCH	1	Mask off the Suspend reschedule NMI. 1 = Mask.
D1	MSK_LCD	1	Mask off the NMI caused by the LCD Timer time-out. 1 = Mask.
D0	MSK_DOZE	1	Mask off the NMI caused by the Doze Timer time-out. 1 = Mask.

TABLE 16. NMICAUSE-I REGISTER (D2h)

Bit	Name	Default	Function
D7	ACT_LCD_NMI	0	LCD Timer Retrigger Activity
D6	ACT_NMI	0	Activity NMI from Doze or Sleep
D5	SUSPEND_NMI	0	Suspend NMI
D4	SLEEP_NMI	0	Sleep NMI
D3	LLB_NMI	0	LLB NMI
D2	LB_NMI	0	LB NMI
D1	EXT_NMI	0	EXT Input NMI
D0	I_NMI	0	PC/AT-compatible specified NMI generated by the VL82C310 SCAMP Controller.

The NMI cause can also be examined by reading the Status Register. Additional NMICAUSE-I Registers are provided to give more flexibility of using the VL82C312. Reading the NMICAUSE-I Register clears the NMICAUSE-I Register and NMI cause codes in the Status Register. It also clears the IRQx output if it is unmasked. The NMICAUSE-I Register is cleared at the trailing edge of the –IOR signal. A double buffer method is used to prevent loss of the NMI while it is cleared. This is a read-only register. Writing any data to it indicates the end of a PMU NMI service routine.

TABLE 17. NMICAUSE-II REGISTER (D3h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	GPLB2_NMI	0	GPLB2 NMI
D3	GPLB1_NMI	0	GPLB1 NMI
D2	RESCH_NMI	0	Rescheduled NMI
D1	LCD_NMI	0	LCD NMI
D0	DOZE_NMI	0	Doze NMI

The NMICAUSE-II Register is cleared by reading it. It is a read-only register.

TABLE 18. MISC REGISTER (D4h)

Bit	Name	Default	Function
D7	FASTDB	1	Low battery NMI debouce time. Low = 2-4 seconds and high = 30-60 ms.
D6	AUTOFLUSH	0	When set, it allows automatic stack flush when entering the On Mode.
D5	FLUSH	0	When set, it flushes and inhibits the INTR stack.
D4	EN_LCDSEQ	0	When the EN_LCDSEQ bit is set, the VL82C312 performs the LCD power-up and power-down sequencing.
D3	LCDTMG1	0	LCDTMG0 and LCDTMG1 are used to select the LCD power-up and power-down sequencing if the EN_LCDSEQ bit is set. If the EN_LCDSEQ is not set, LCDTMG0 controls –VPVSIG and LCDTMG1 controls the VPBIAS outputs individually.
D2	LCDTMG0	0	**1 0 Delay** 0 0 8 ms 0 1 15 ms 1 0 31 ms 1 1 125 ms
D1	Reserved		
D0	EN_HICLK	0	When high, forces –SLOWCLK pin to go high in the Doze or Sleep Mode.

TABLE 19. REVID REGISTER (D5h)

Bit	Name	Default	Function
D7	ID3	0	Used for the ID number of the VL82C312.
D6	ID2	0	Used for the ID number of the VL82C312.
D5	ID1	0	Used for the ID number of the VL82C312.
D4	ID0	0	Used for the ID number of the VL82C312.
D3	Reserved	0	
D2	REV2	0	Used for revision number of the VL82C312.
D1	REV1	0	Used for revision number of the VL82C312.
D0	REV0	0	Used for revision number of the VL82C312.

TABLE 20. BLINKING REGISTER (D6h)

Bit	Name	Default	Function
D7	Reserved		
D6 D5	BLKPERD1 BLKPERD0	0 0	**1 0 Period** 0 0 1 Hz 0 1 2 Hz 1 0 4 Hz 1 1 8 Hz
D4 D3	BLKNBR1 BLKNBR0	0 0	**1 0 Number** 0 0 1 0 1 2 1 0 4 1 1 Continuous
D2 D1	BLKFRQ1 BLKFRQ0	0 0	**1 0 Frequency** 0 0 512 Hz 0 1 1024 Hz 1 0 1365 Hz 1 1 2048 Hz
D0	EN_BLK	0	Used to enable the blinking option of the GPIO3. 1 = enable.

EXAMPLE OF BLINKING REGISTER

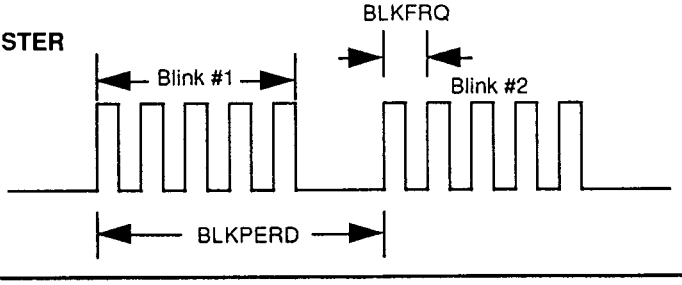


TABLE 21. GPDIR REGISTER (D7h)

Bit	Name	Default	Function
D7	Reserved		
D6	GPDIR9	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D5	GPDIR8	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D4	GPDIR7	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D3	GPDIR6	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D2	GPDIR5	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D1	GPDIR4	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D0	GPDIR3	0	General purpose I/O pin. Direction can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.

GPDATA REGISTER (D8h)
This register has different functions for read and write.

TABLE 22. GPDATA REGISTER (D8h) - WRITE

Bit	Name	Default	Function
D7	Reserved		
D6	GPOUT9	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.
D5	GPOUT8	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.
D4	GPOUT7	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.
D3	GPOUT6	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.
D2	GPOUT5	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.
D1	GPOUT4	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.
D0	GPOUT3	0	If the corresponding bit in the GPDIR register is to output, the value of the GPIO pin can be set by this register.

TABLE 23. GPDATA REGISTER (D8h) - READ

Bit	Name	Default	Function
D7	Reserved		
D6	GPIN9	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D5	GPIN8	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D4	GPIN7	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D3	GPIN6	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D2	GPIN5	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D1	GPIN4	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D0	GPIN3	0	If the corresponding bit in the GPDIR register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.

TABLE 24. AND/OR REGISTER (D9h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	Reserved		
D3	SEL_POL	1	If set, GPIO9 is the output of the AND/OR function. If cleared, GPIO9 is the output of the NAND/NOR function.
D2	SEL_AND	0	If EN_ANDOR is enabled, SEL_AND = 1 selects the AND function and SEL_AND = 0 selects the OR function.
D1	EN_AO8	0	Enable the AND/OR function for the GPIO8. When this bit and the EN_ANDOR bit are both set, GPIO8 becomes an input of the AND/OR function.
D0	EN_ANDOR	0	Enable the AND/OR option for the GPIO6, GPIO7, and GPIO9. When set, GPIO6 and GPIO7 becomes the input of the AND/OR function and GPIO9 becomes the output.

TABLE 25. CSCTRL REGISTER (DAh)

Bit	Name	Default	Function
D7	FDCEN	1	Enables –FDCCS, –CS3, and –CS4
D6	LPTEN	1	Enables –CS2
D5	LPT1	0	Selects –CS2 Decode Ranges
D4	LPT0	0	Selects –CS2 Decode Ranges
D3	COMB	1	Enables –CS1
D2	COMA	1	Enables –CS0
D1	COMS	1	Selects –CS0 and –CS1 Decode Ranges
D0	IDEEN	1	Enables IDE Interface Chip Selects and Control Pins

This register is used for the IDE and chip select control port. See section titled "Chip Selects and Misc" for more information.

TABLE 26. ACTIVITY REGISTER (DBh)

Bit	Name	Default	Function
D7	IORNG	0	I/O Range Activity
D6	VIDM	0	Video Memory Activity
D5	HD	0	Hard Disk Activity
D4	FLP	0	Floppy Disk Activity
D3	SIO	0	COM Port Activity
D2	RTC	0	Real-time Clock Access
D1	KBD	0	Keyboard Port 60h Read Activity
D0	PIO	0	LPT1-LPT3 Activity

Any unmasked activity sets the corresponding bit in this register. This register is read-only and is cleared when read and by –RCRESET.

TABLE 27. TIME REGISTER (DCh)

Bit	Significance
D7	1 s
D6	500 ms
D5	250 ms
D4	125 ms
D3	62.5 ms
D2	31.25 ms
D1	15.625 ms
D0	7.8125 ms

This register contains the relative time in units of 1/128 second. It is a read-only register and is cleared only by –RCRESET.

FIGURE 3. POWER MANAGEMENT MODE FLOW

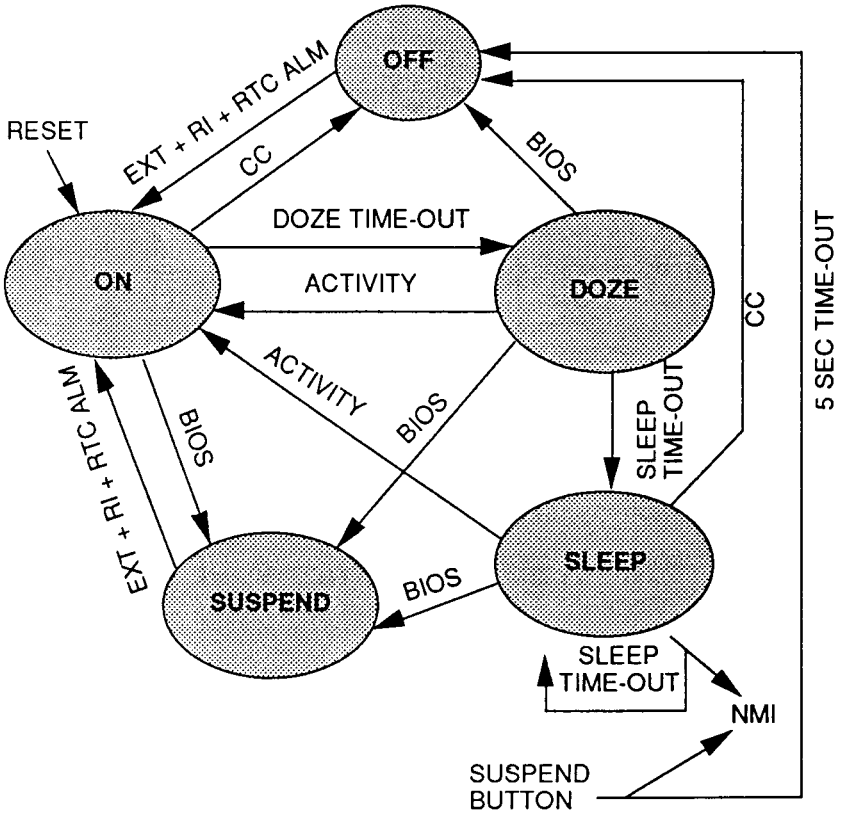
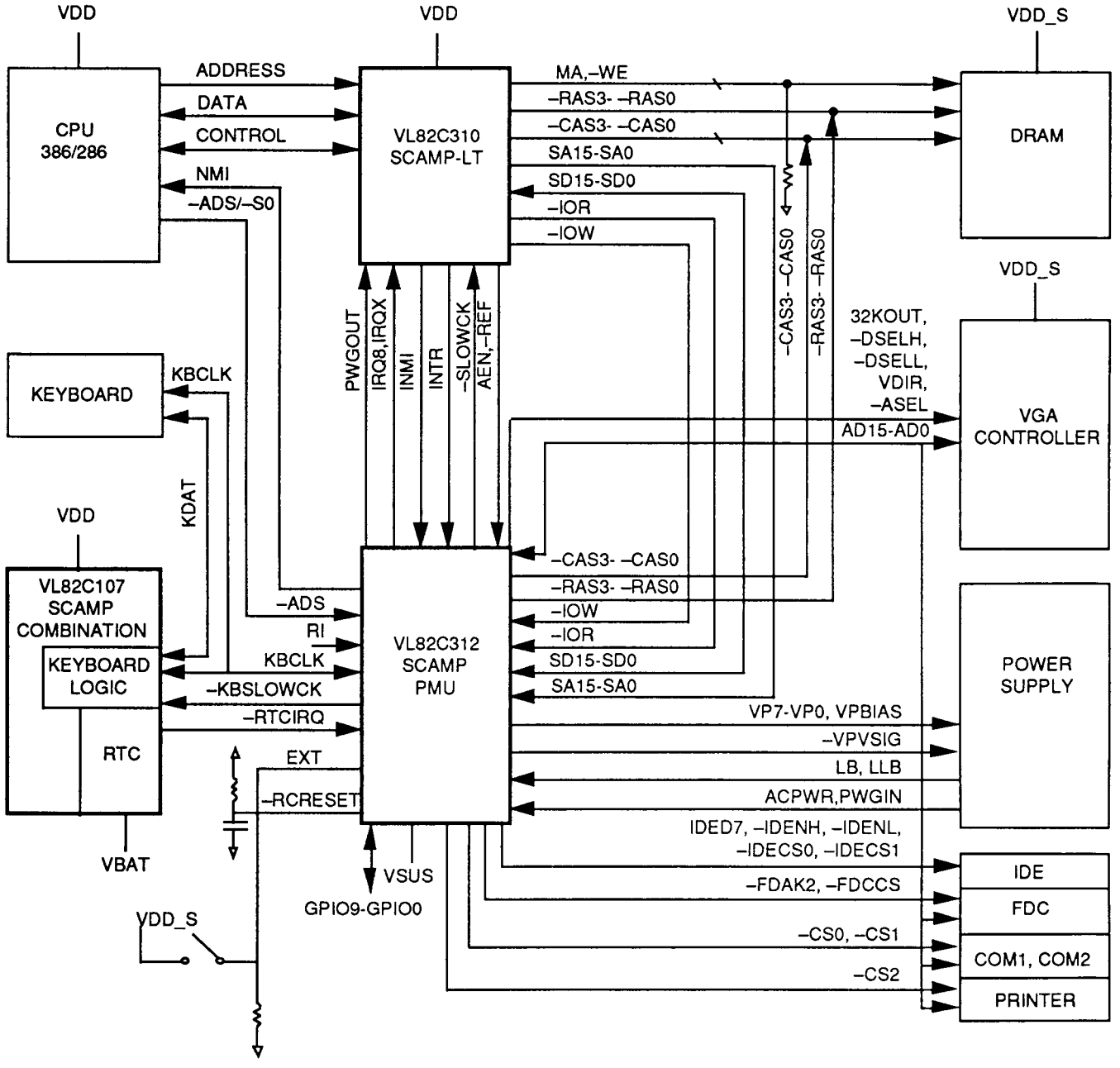


FIGURE 4. SCAMP NOTEBOOK SYSTEM BLOCK DIAGRAM

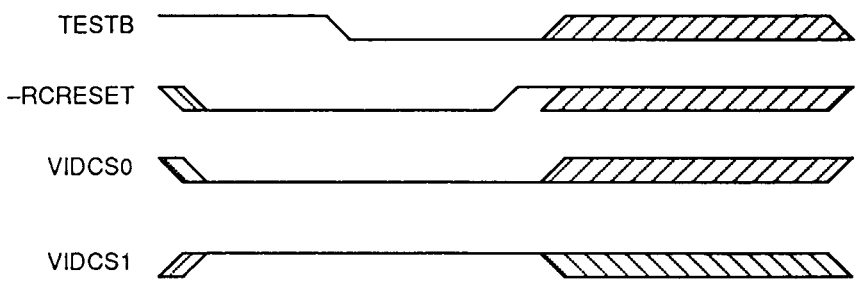


IN-CIRCUIT TEST MODE

During In-Circuit Test (ICT) each output may be toggled by one or more of the inputs. This allows a board level tester to check the solder connection of each pin.

Table 28 shows the input to output mapping for each pin while the ICT Mode is active. The "Signal Name" column shows the first of the two signals in an I/O mapping pair. As an example, pin 3 (–VIDCS1), is used as an input while VP0 is used as the output.

The sequence for enabling ICT Mode:



To clear ICT Mode –IOW and –IOR must be low, and ACPWR high.

TABLE 28. IN-CIRCUIT TEST MODE

ICT Input		ICT Output	
Sig. Name	Pin #	Sig. Name	Pin #
–VIDCS0	2	VGARST	1
–DACK2	8	–FDACK	9
MFM	7	PCLOCK	10
–CAS3	84	–CS3	12
GPIO7	87	–CS4	13
MCLK	11	–FDCCS	14
–VIDCS2	4	–VPVSIG	15
–VIDCS4	6	VPBIAS	16
–VIDCS1	3	VP0	17
–VIDCS3	5	VP1	19
LLB	30	VP2	21
PWGIN	32	VP3	22
LB	29	VP4	23
ACPWR	31	VP5	24
EXT	34	VP6	25
–RCRESET	36	VP7	26
EXTACT	33	GPIO4	27
RI	35	GPIO5	28
AEN	39	IRQX	38
–ADS	40	–IOCS16	43
SD1	45	SD8	53
SD3	47	SD9	54
SD0	44	SD10	56
SD2	46	SD11	57
SD5	49	SD12	58
SD7	52	SD13	59
SD4	48	SD14	60
SD6	50	SD15	61
RSTDRV	64	–RESET	63
INMI	69	–SLOWCK	65
–ASEL	71	PWGOUT	66
RSTDRV	64	IRQ8	67
INTR	70	NMI	68

ICT Input		ICT Output	
Sig. Name	Pin #	Sig. Name	Pin #
–DSELL	74	–RAS0	77
–RTCIRQ	76	–RAS1	78
VDIR	72	–RAS2	79
–DSELH	75	–RAS3	80
GPIO8	86	–CAS0	81
GPIO6	88	–CAS1	82
GPIO9	85	–CAS2	83
RTCX1	107	RTCX2	108
–TEST	110	–KBSLOWCK	111
KBCLK	112	CLK32K	113
–IOW	42	–CS0	114
IDED7	121	–CS1	115
GPIO1	123	–CS2	116
GPIO3	125	–IDECS0	117
GPIO0	122	–IDECS1	118
GPIO2	124	–IDENL	119
–IOR	41	–IDENH	120
SA0	89	AD0	126
SA1	91	AD1	128
SA2	93	AD2	130
SA3	94	AD3	131
SA4	95	AD4	132
SA5	96	AD5	133
SA6	97	AD6	134
SA7	98	AD7	135
SA8	99	AD8	136
SA9	100	AD9	137
SA10	101	AD10	138
SA11	102	AD11	139
SA12	103	AD12	140
SA13	104	AD13	141
SA14	105	AD14	142
SA15	106	AD15	143

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write Timing					
tSU1	Address Setup Time	55		ns	
tH2	Address Hold Time	20		ns	
tSU3	AEN Setup Time	55		ns	
tH4	AEN Hold Time	20		ns	
t5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL = 200 pF
tH9	Read Data Hold	5	60	ns	CL = 50 pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
Chip Select Timing					
tD11	Chip Select Delay from Address Signals –CS0, –CS1, –CS2, –CS3, –CS4, –FDCCS, –IDECS0, –IDECS1		35	ns	CL = 50 pF CL = 200 pF
tD13	–IOCS16 Active from Address		60	ns	
tD17	–IOCS16 Inactive from Command		55	ns	VOH = 1.5 V, 300Ω pull-up –IOCS16 open drain
IDE Interface Timing					
tD19	IDEN/IDENL Delay from Address		60	ns	CL = 50 pF
tD20	IDB7 Delay from SD7 Input		40	ns	CL = 200 pF
tD21	SD7 Delay from IDB7 Input		40	ns	CL = 200 pF
tD23	SD7 Delay from –IOR During IDE Access	0	85	ns	CL = 200 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
IDE Interface Timing (Cont.)					
tD24	SD7 Hold from –IOR Inactive	5	60	ns	CL = 50 pF
tD25	IDB7 Delay from –IOR Inactive	0	85	ns	CL = 200 pF
tD26	IDB7 Delay from –IOR Active	5	60	ns	CL = 50 pF
PMU Pins Timing					
tD131	–RAS Precharge Time (Burst Refresh)	125		ns	
tD132	–RAS On Time (Burst Refresh)	250		ns	
tD133	Burst Refresh to Suspend Refresh Delay	15	31	µs	
tD134	–RAS On Time (Suspend Refresh)	170	610	ns	
tD135A	Suspend Refresh Cycle Time (Reg. DRAM)	15		µs	
tD135B	Suspend Refresh Cycle Time (Slow Refresh DRAM)	124		µs	
tD138A	PWGIN to PWGOUT Delay	0.53	1.035	s	See Note
tD138B	–RCRESET to PWGOUT Delay	0.53	1.035	s	See Note
tD139	–RCRESET to VP7-VP2 Delay	0	40	ns	
tD140	PWGOUT to VP1 Delay				0.5 sec typical
tD141	EXT to VP7-VP2 Delay	0	40	ns	
tD142	PWGIN to PWGOUT Delay	0.53	1.03	s	

Note: –RCRESET and PWGIN, whichever activates last, 0.5 to 1.0 sec later the PMU will drive PWGOUT "HIGH"

AC CHARACTERISTICS (Cont): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
PMU Pins Timing (Cont.)					
tD143	PWGOUT to VP1 Delay				0.5 sec typical
tD144	INMI to NMI Delay	0	40	ns	
tD145	EXT Pulse Width Low	63		ms	
tD147	–SLOWCK or –KBSLOCK Low	288		ns	
tD148	–SLOWCK or –KBSLOCK High	288		ns	
tD149	EXTACT Pulse Width High	60		ns	
tD150	Resume Command to PMU Refresh Burst Delay	0.53	1.03	s	
tD151	Suspend Command to Suspend Active Delay	0.53	1.03	s	
tD152	PWGOUT Low to PMU Driving –CAS Low	560		ns	
tD153	–CAS Low to Start of 1024 Refresh Burst	150		ns	
tD154	NMI Pulse Width High	570		ns	
AD Bus Timing					
tD200	AD Delay from Address		20	ns	
tD203	SD Delay from AD - Read Cycle		25	ns	
tD201	AD Delay from SD - Write Cycle		25	ns	
tH202	AD Hold from –ASEL	80		ns	

BUS TIMING

FIGURE 5. WRITE CYCLE

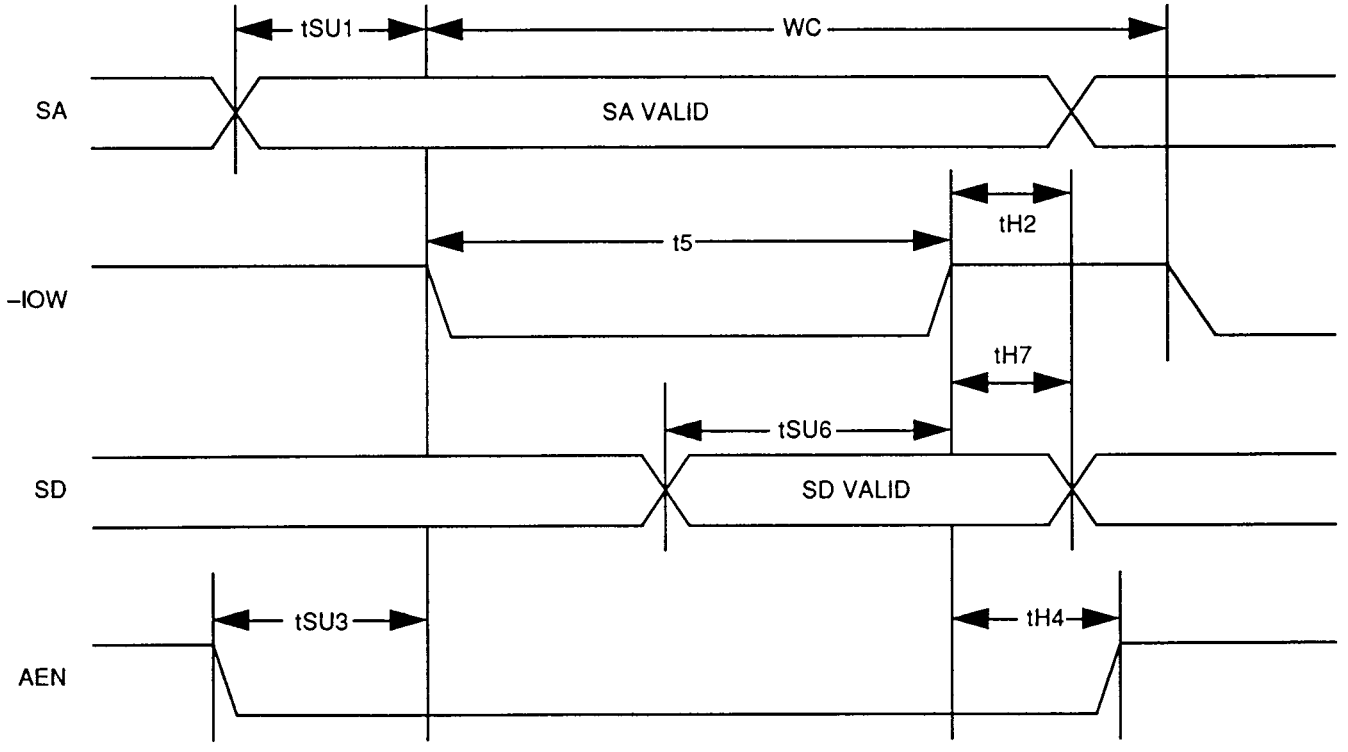
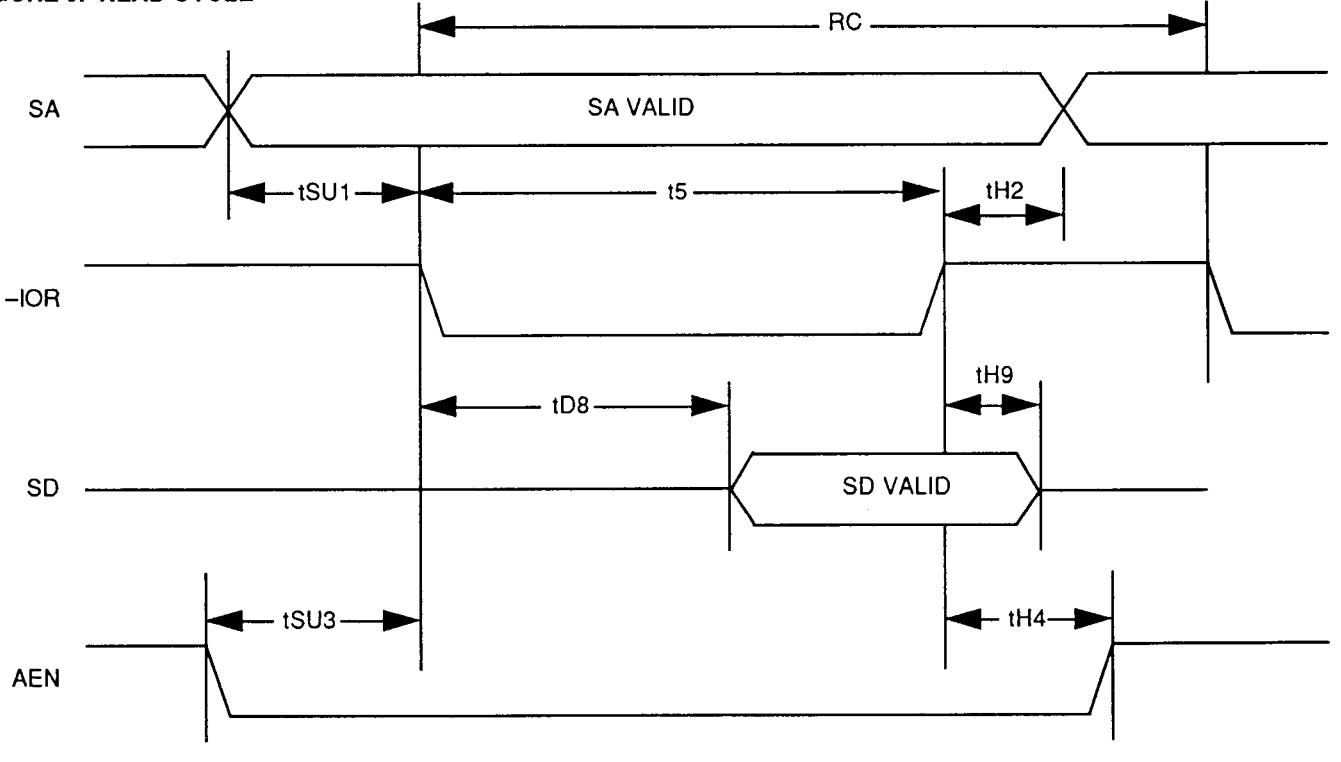
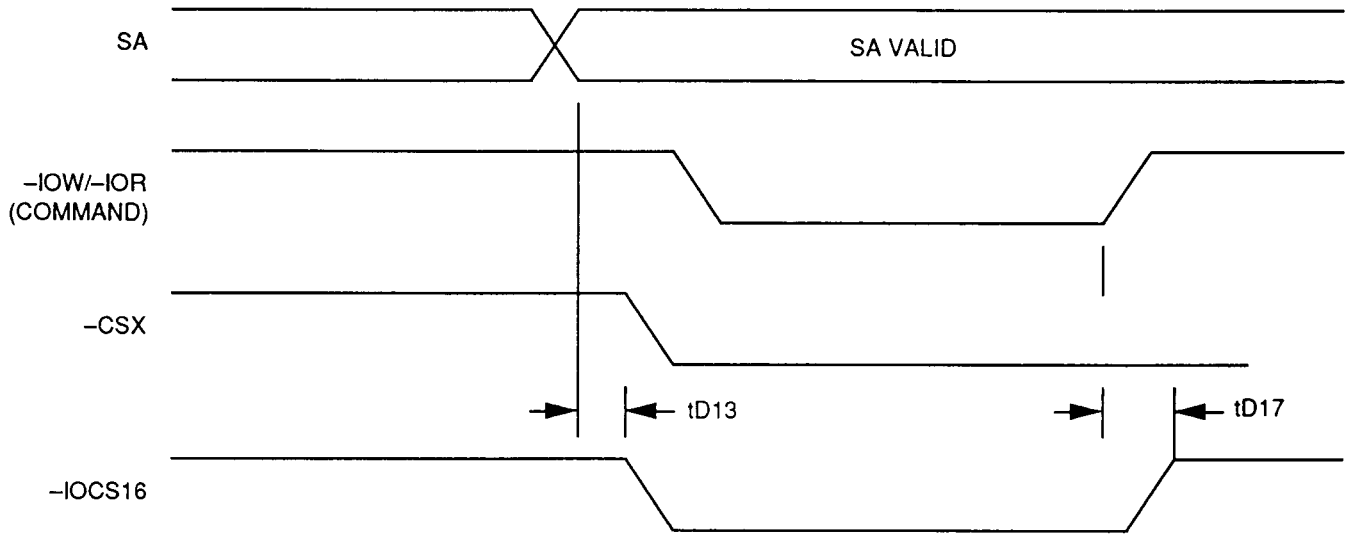


FIGURE 6. READ CYCLE



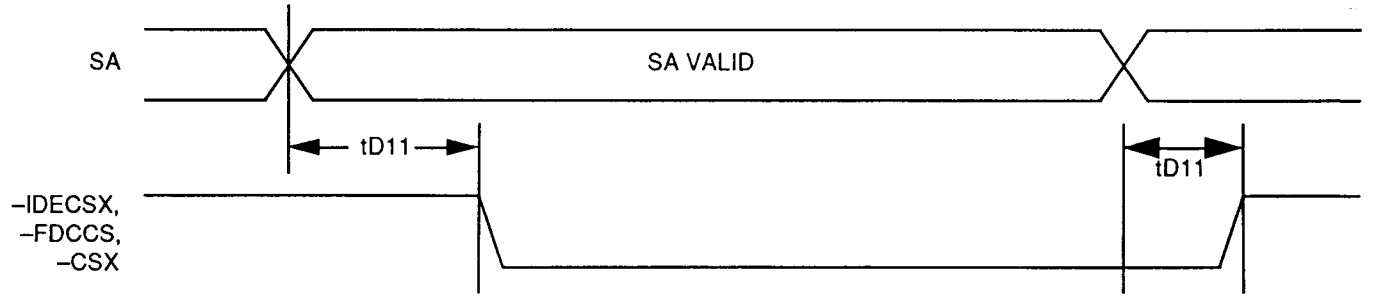
–IOCS16 TIMING

FIGURE 7. –IOCS16 CYCLE



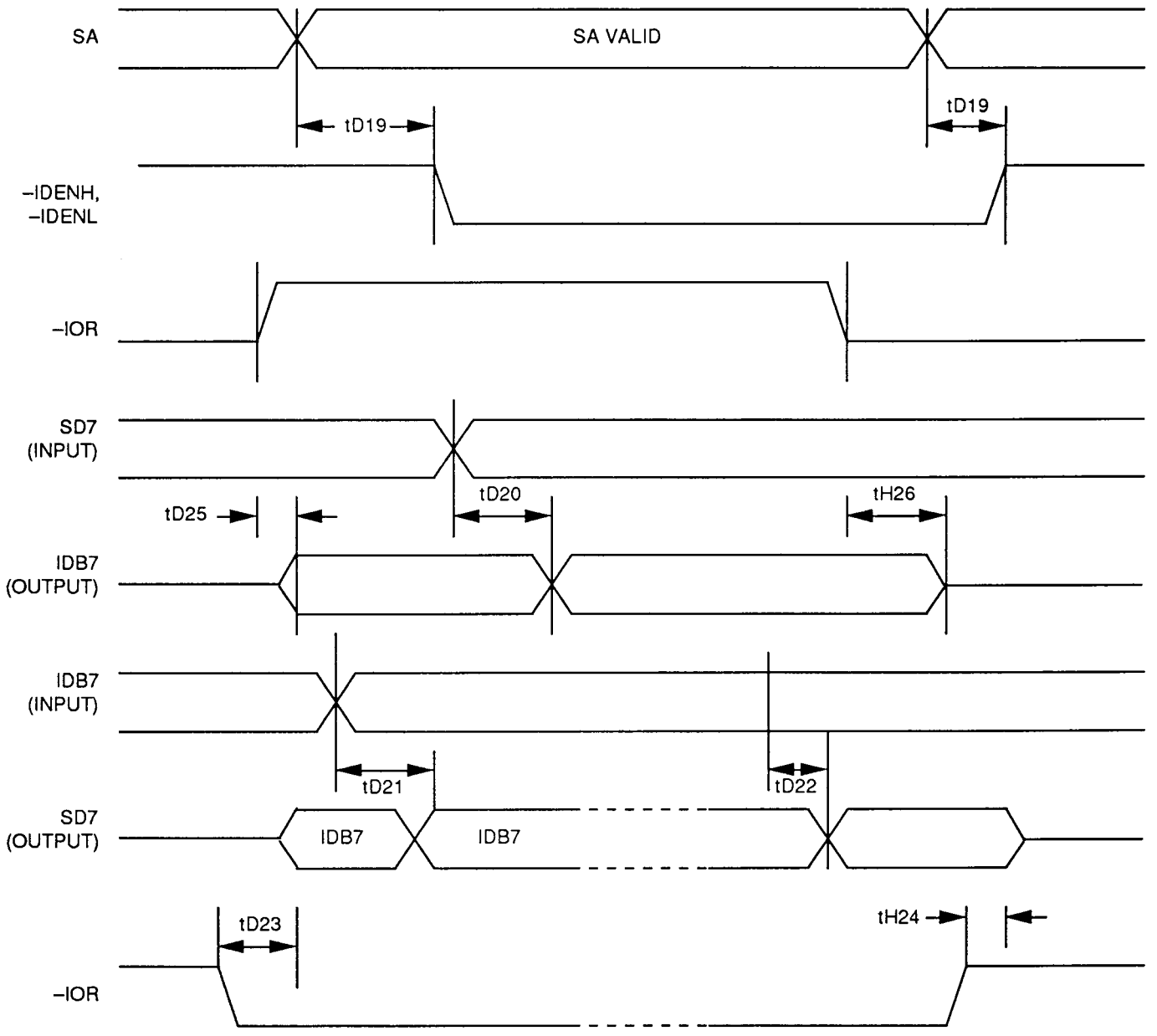
CHIP SELECT TIMING

FIGURE 8. CHIP SELECT CYCLE



IDE INTERFACE TIMING

FIGURE 9. IDE INTERFACE CYCLE



RAS TIMING

FIGURE 10. ENTERING SUSPEND RAS TIMING - ENTERING SUSPEND

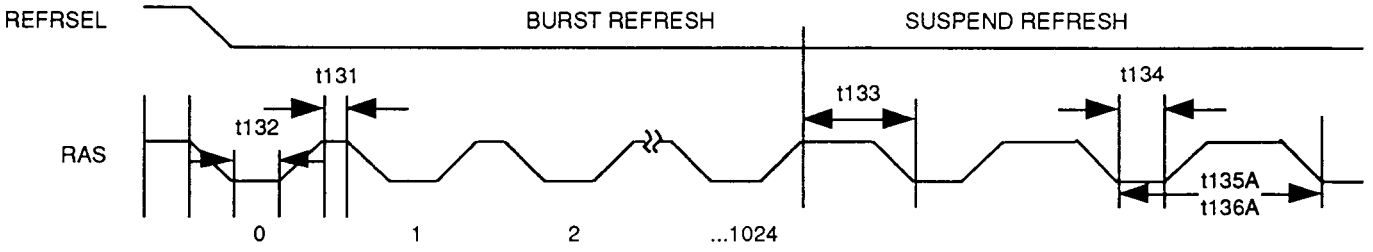


FIGURE 11. LEAVING SUSPEND

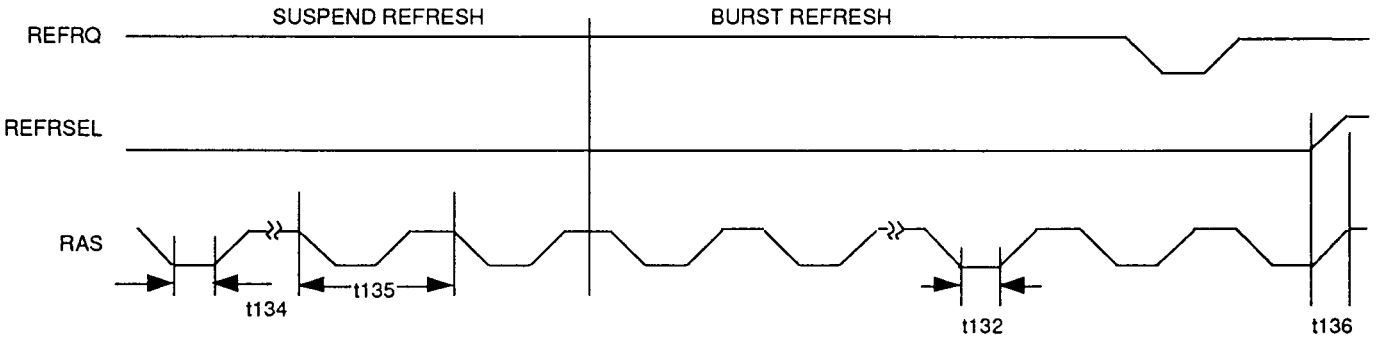
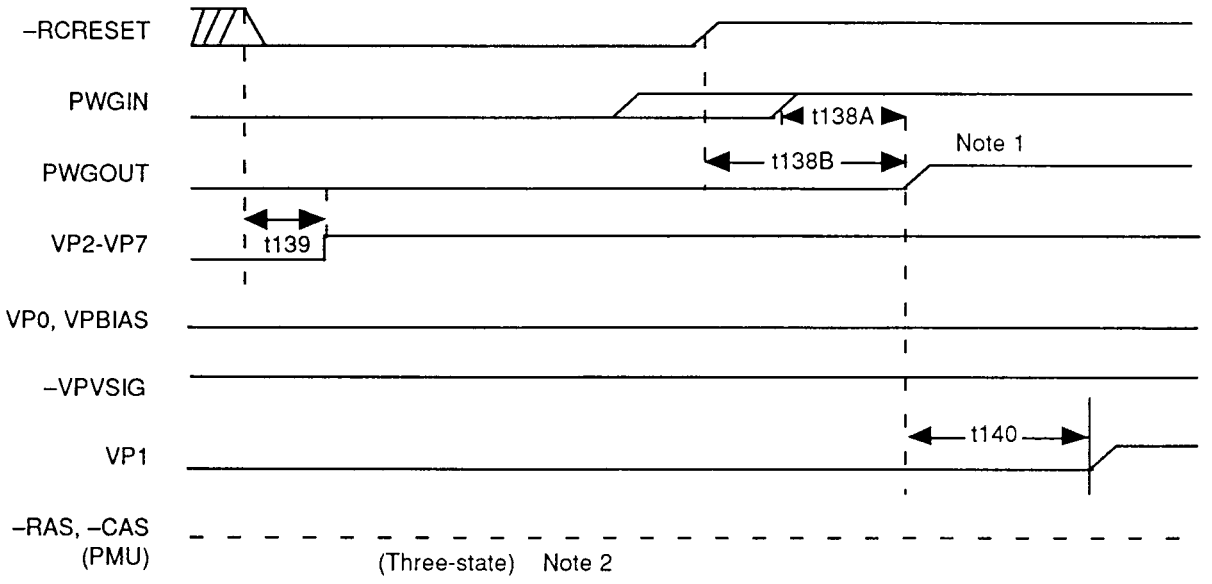


FIGURE 12. POWER-UP FROM –RCRESET (No LCD Auto-Sequencing)



Notes: 1. –RCRESET and PWGIN, whichever activates last, 0.5 to 1.0 sec, later the VL82C312 drives PWGOUT high.
2. –RAS and –CAS from VL82C312 are three-stated all the time, except when the VL82C312 enters the Suspend Mode. During the Suspend Mode, the VL82C312 will perform a –CAS before –RAS refresh.

FIGURE 13. POWER-UP FROM EXT (No LCD Auto-Sequencing)

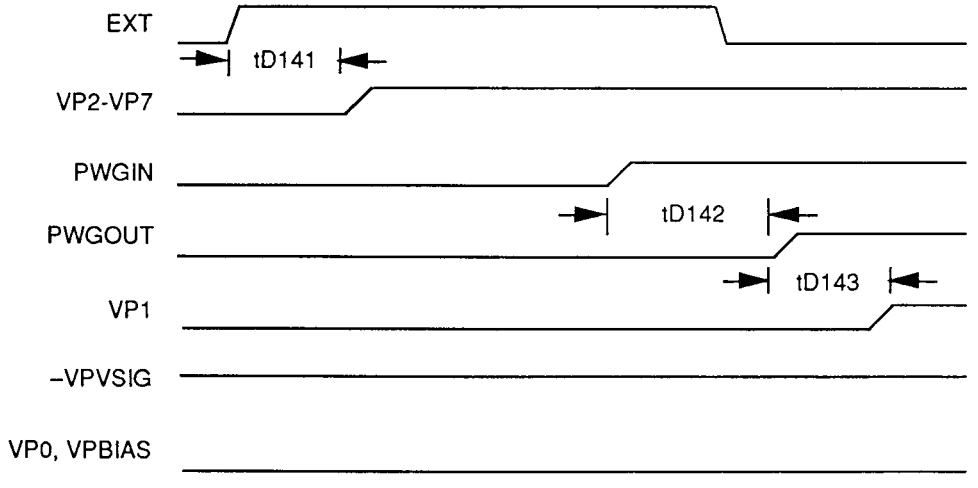
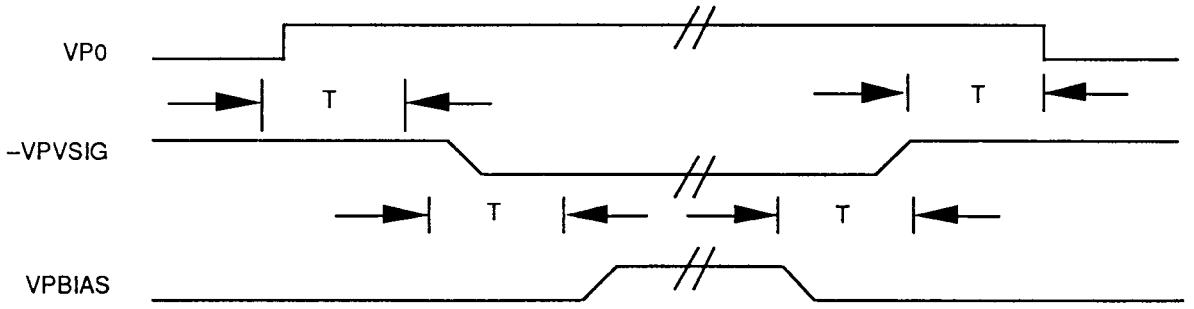


FIGURE 14. LCD AUTO-SEQUENCING



Note: T = The LCD sequencing time T is based on the setup of MISC Register D4 (data bit 4).

Enable LCD - SEQUENCING
D4 = 1

D3	D2	T Delay
0	0	8 ms
0	1	15 ms
1	0	31 ms
1	1	125 ms

FIGURE 15. INMI TO NMI TIMING

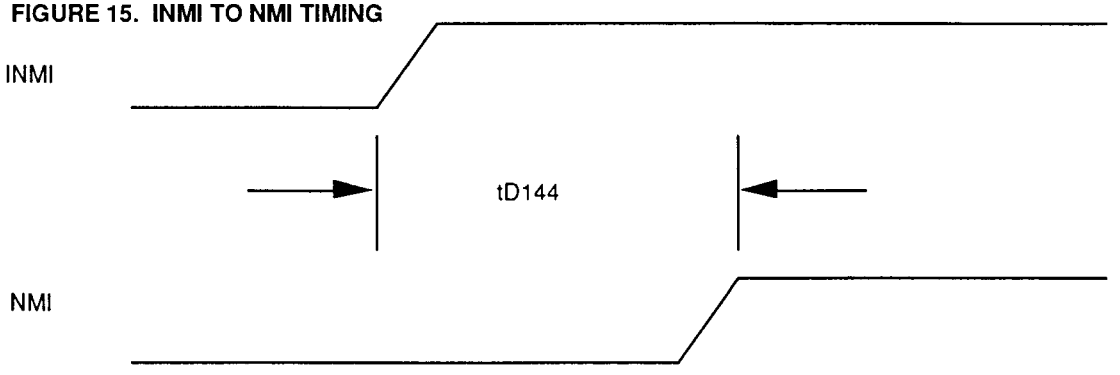
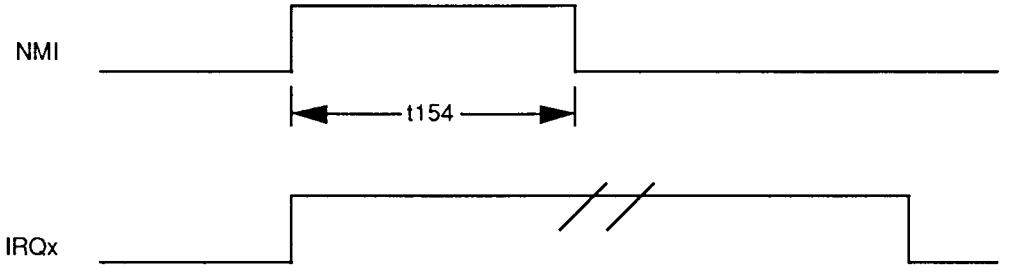
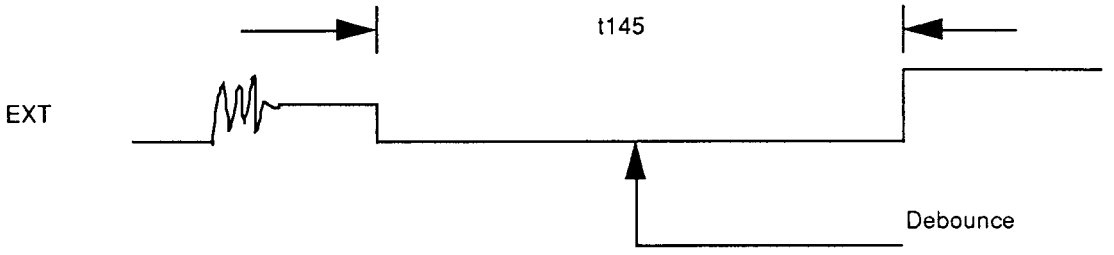


FIGURE 16. INTERNAL INTERRUPT GENERATION



Note: IRQx remains active until the NMICAUSE Register is read.

FIGURE 17. EXT TIMING (EXT causes NMI for Suspend Mode)



Note: EXT is internally debounced and it is required low for minimum 63 ms.

FIGURE 18. CLOCK SWITCHING CONTROL

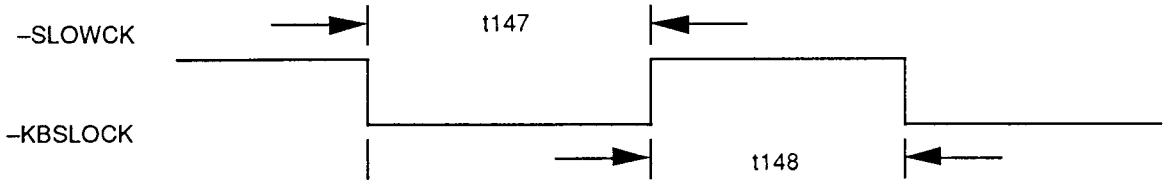
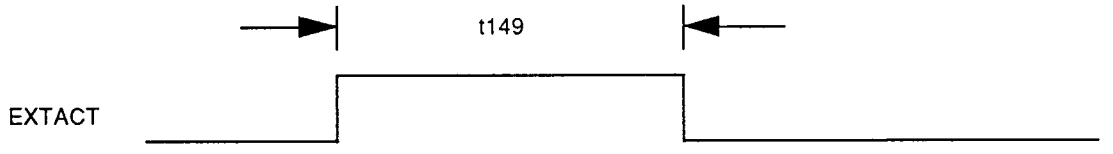


FIGURE 19. EXTACT TIMING



Note: EXTACT can remain high or low.

FIGURE 20. AD BUS TIMINGS

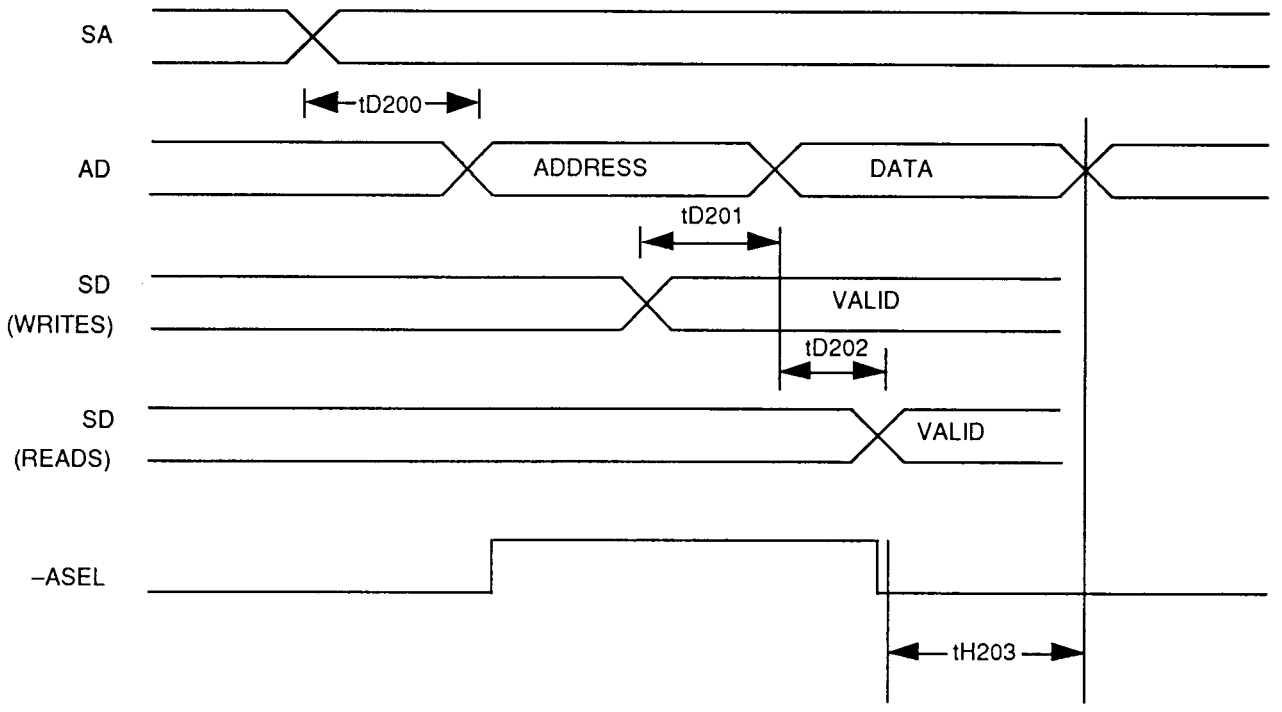
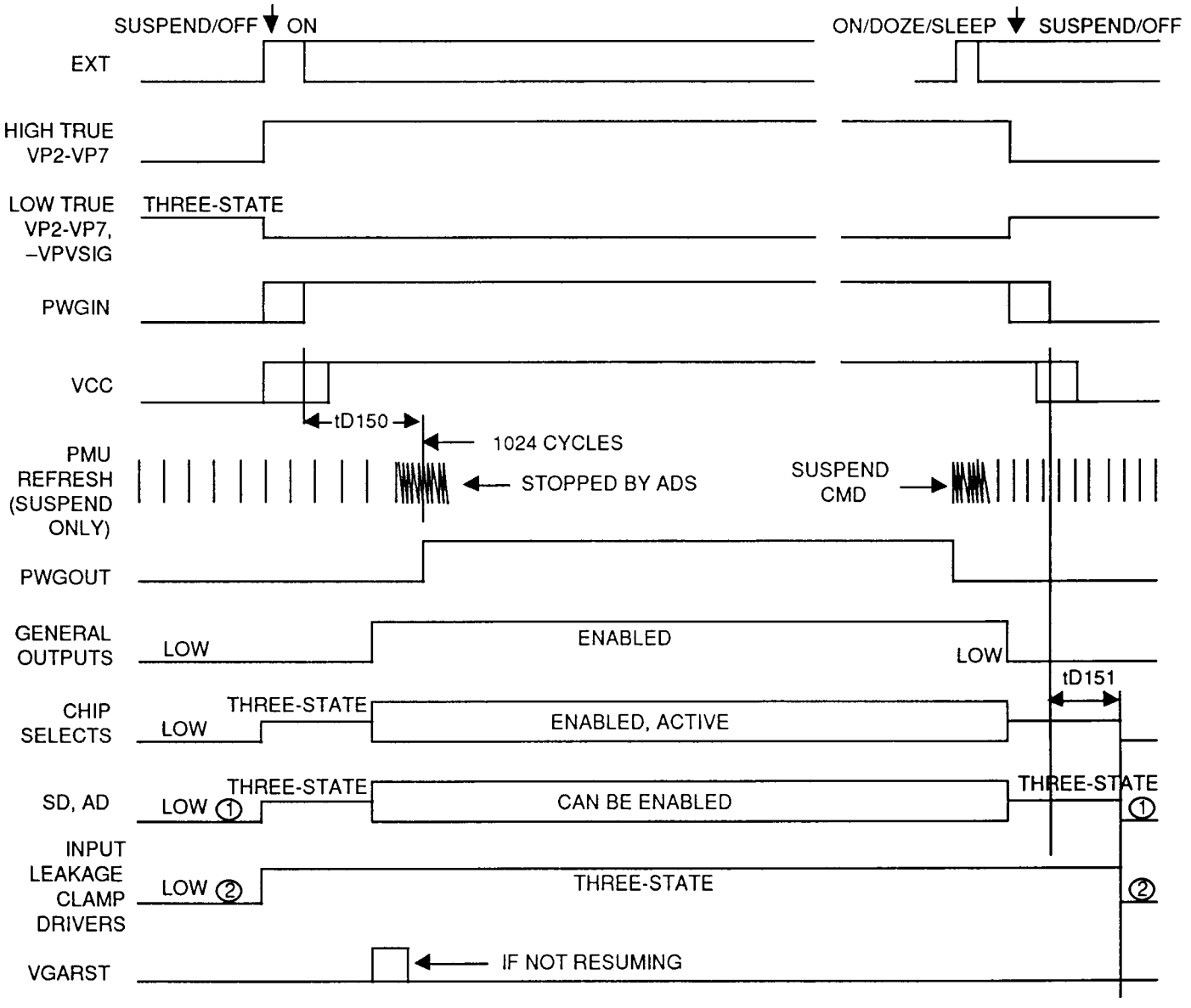
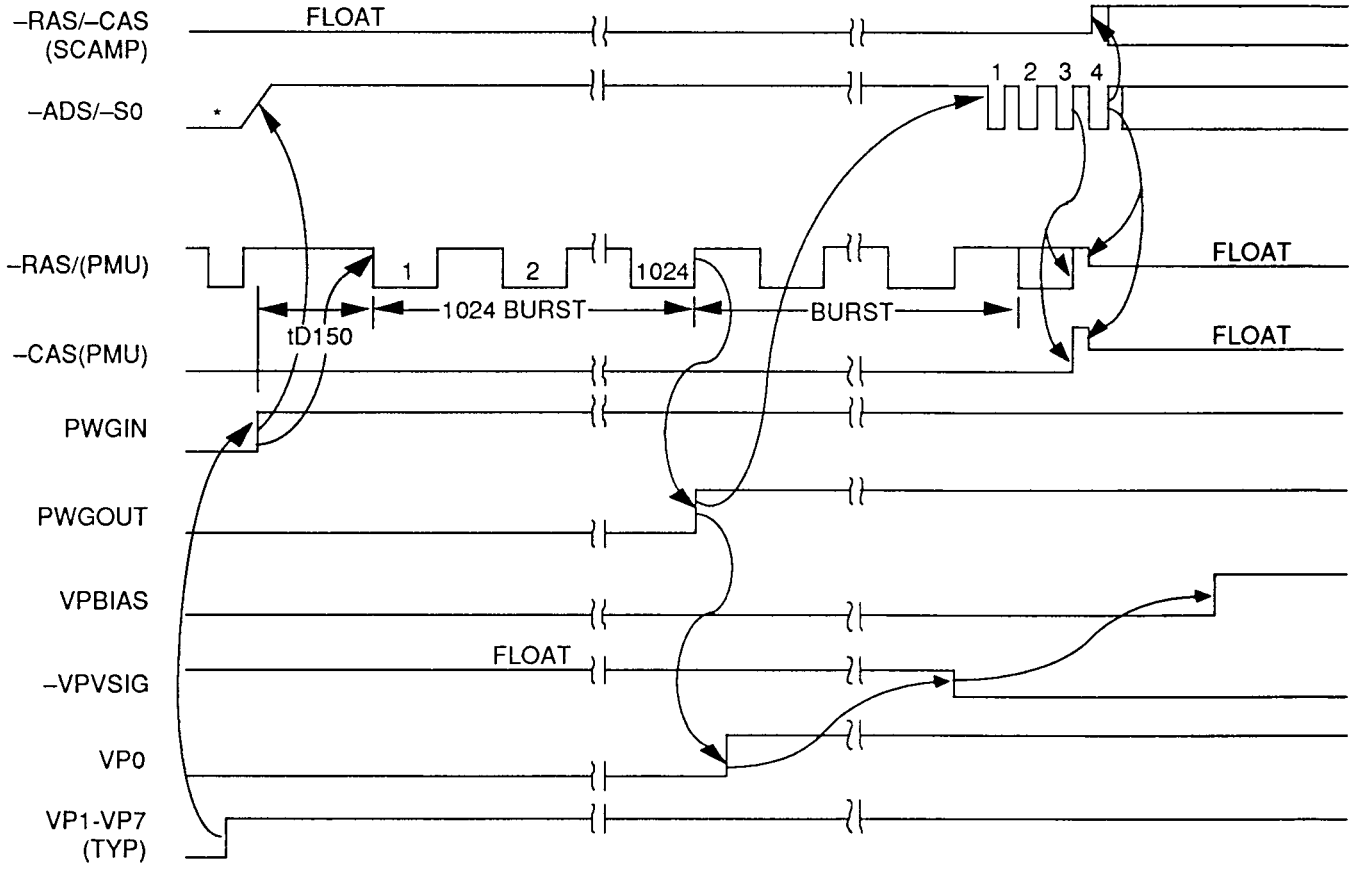


FIGURE 21. POWER MODE TIMING



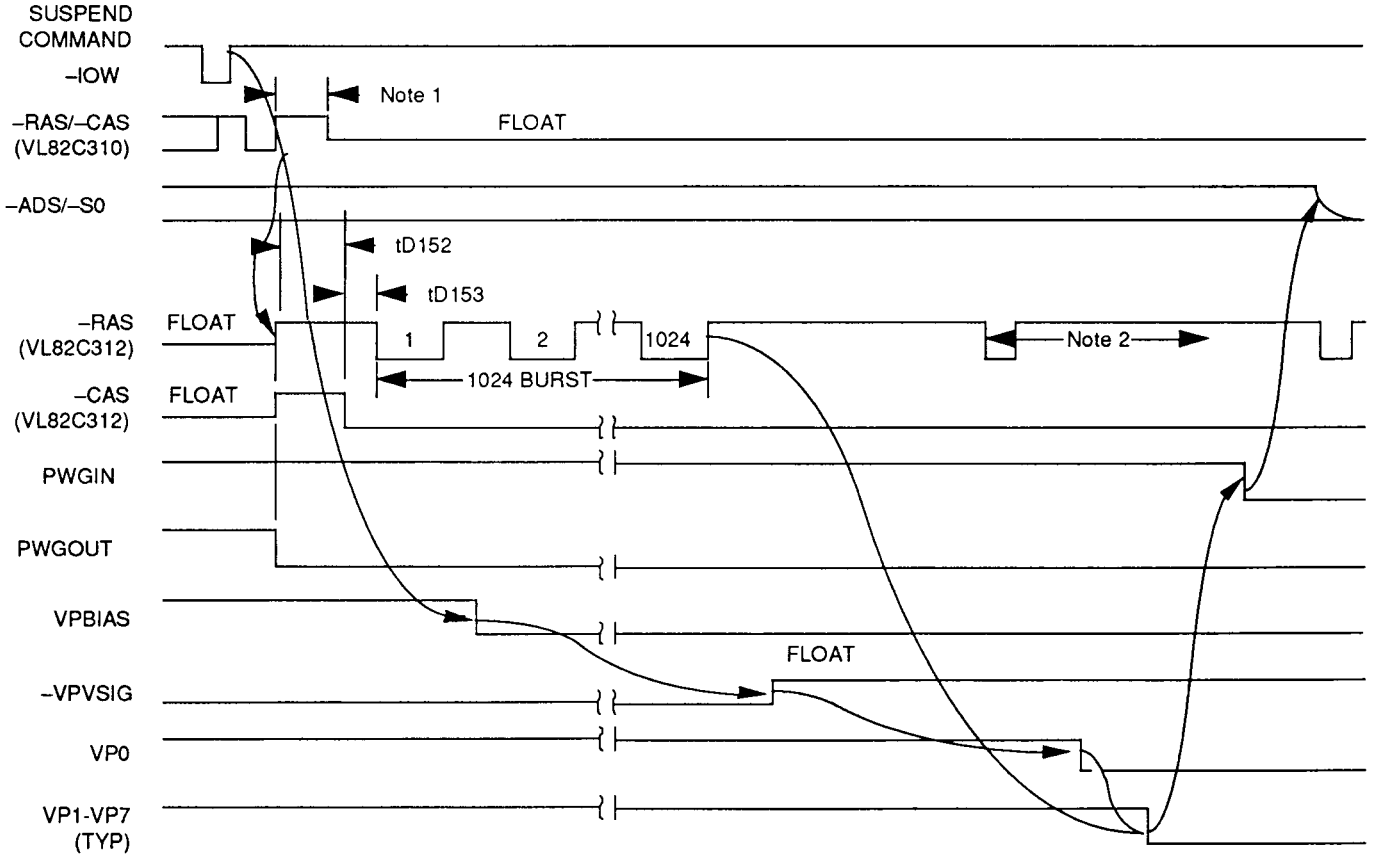
Notes: 1. AD bus enabled in Suspend Mode.
2. Inputs from VGA not clamped low in Suspend Mode.

FIGURE 22. SUSPEND ON MODE TIMING



* Driven low by VL82C312 during Suspend Mode.

FIGURE 23. ON TO SUSPEND TIMING



Notes: 1. The VL82C310 floats –RAS and –CAS line within 400 ns after falling edge of PWGOUT.
2. After completion of the 1024 cycle refresh burst, normal –CAS before –RAS refresh occurs at the programmed rate (15 or 122 ms).

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature −10°C to +70°C

Storage Temperature −65°C to 150°C

Supply Voltage to Ground Potential −0.5 V to VDD +0.3 V

Applied Output Voltage −0.5 V to VDD +0.3 V

Applied Input Voltage −0.5 V to +7.0 V

Power Dissipation 500 mW

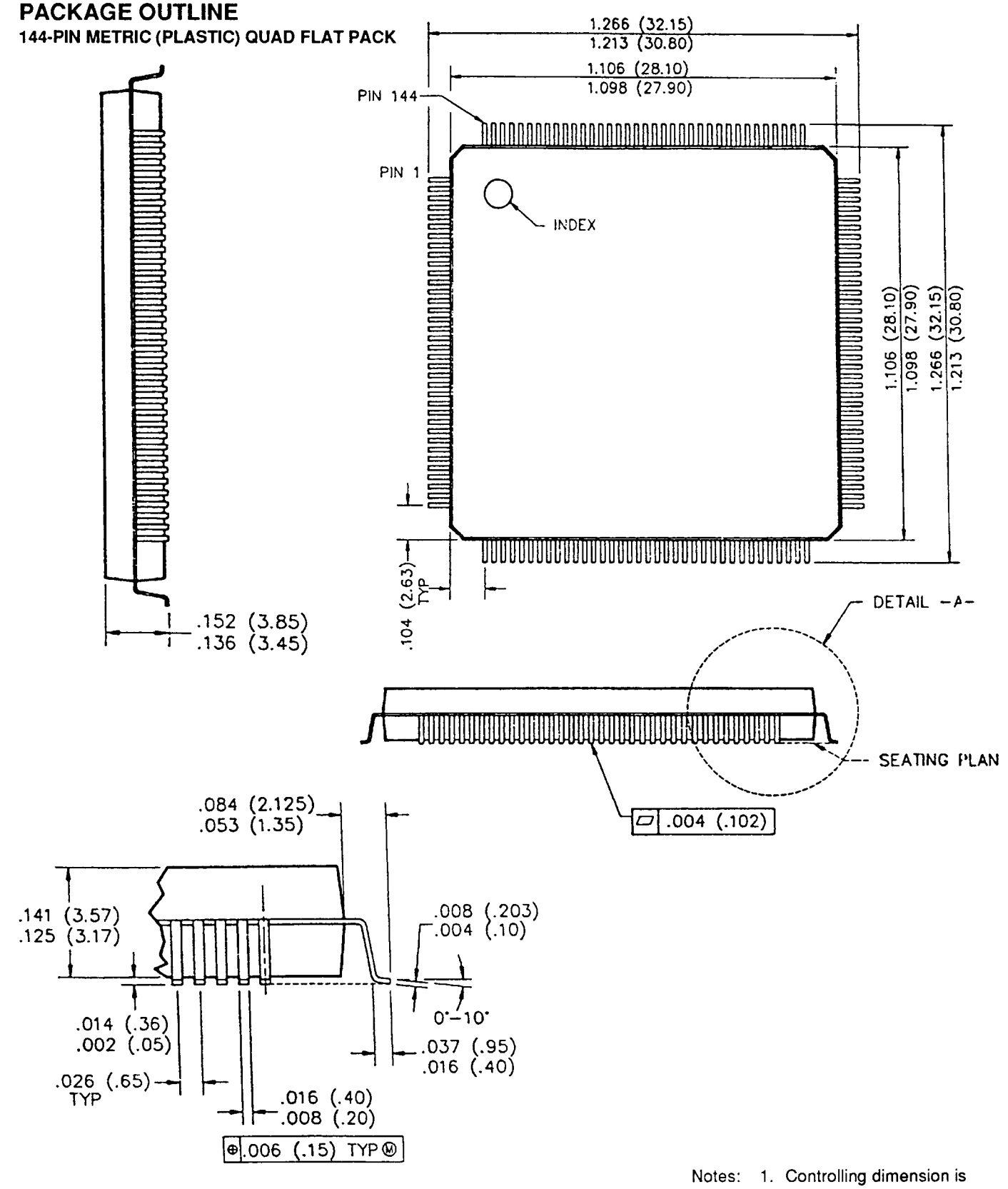
Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device as indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0° to +70°C, VDD = 5 V + 5%, VSS = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage I1, I3, IO1, IO2, IO3, IO4 I2	 2.0 2.4	 VDD + 0.5 VDD + 0.5	 V V	
VOL	Output Low Voltage O1, IO1 O2, IO4 IO3 O3, IO2		 0.45 0.45 0.45 0.45	 V V V V	 IOL = 4.0 mA IOL = 8.0 mA IOL = 12.0 mA IOL = 24.0 mA
VOH	Output High Voltage O1, IO1 O2, IO4 IO3 O3, IO2	 2.4 2.4 2.4 2.4		 V V V V	 IOH = −0.8 mA IOH = −1.4 mA IOH = −2.0 mA IOH = −2.4 mA
IIH	Input High Current I1, I2, I3		10	µA	VIN = VDD
IIL	Input Low Current I1, I2 I3	 −10 −500	 −50	 µA µA	 VIN = VSS + 0.2 V VIN = 0.8 V All other pins floating
ILOL	Three-state Leakage Current IO1, IO2, IO3, IO4	 −50		 µA	 VSS + 0.2 V
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	
IDD	Operating Current		40	mA	

PACKAGE OUTLINE

144-PIN METRIC (PLASTIC) QUAD FLAT PACK



Notes: 1. Controlling dimension is MM.

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