VL82C032

SUPER XT-COMPATIBLE I/O CONTROLLER

FEATURES

- Controls PS/2®- and PC/AT®-compatible system keyboard and mouse
- Integrates the following functions on a single device:
  - –8253-compatible timer/counter
  - –Dual 8250-compatible serial communications controller
  - –Bidirectional parallel port controller
  - –8259-compatible interrupt controller
  - –58167-compatible real-time clock
- Decodes subsystems for floppy disk, hard disk, and video
- Provides chip select logic for serial/parallel ports, disk controllers, and real-time clock.

DESCRIPTION

The VL82C032 provides the XT-compatible system with control of both the keyboard and the pointing device ("mouse"), control of two serial communication channels, a real-time clock, as well as controlling both the disk storage and display functions. It also provides the chip select logic for the functions it controls. The VL82C032 is available from VLSI Technology, Inc. in an industry-standard plastic 100-pin flatpack.

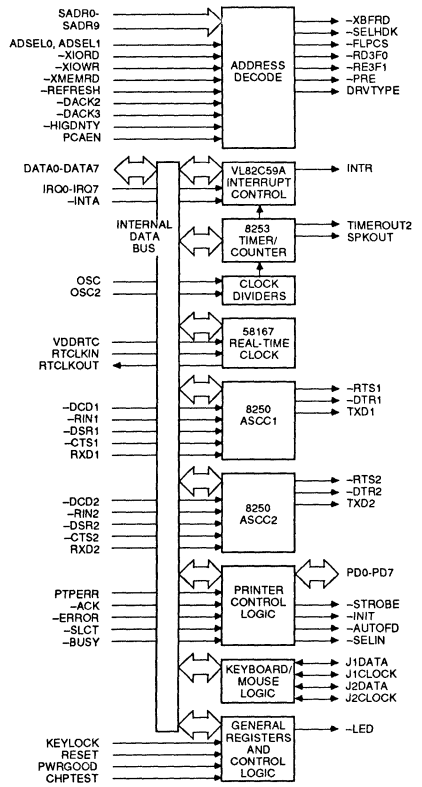
The CMOS VL82C032 is the Input/Output Controller device in the two-chip VLSI XT-compatible chip set. The other device is the VL82C031 System Controller.

The chip set integrates logic and functions on XT-compatible systems.

Further, while offering complete compatibility with the Super XT system, the VLSI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M bytes of memory using EMS (Expanded Memory Specification) 4.0, controls system speed as necessary for optimum performance, and supports a 16-bit memory data bus.

A third device, the VL82C037 VGA, Video Graphics Controller, is also used in the XT-compatible system and provides high resolution graphics of up to 800 x 600 elements with 16 colors. Graphic capabilities of this resolution are usually found only on more expensive systems.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C032-FC	Plastic Flatpack

Notes: Operating temperature range is 0°C to +70°C.
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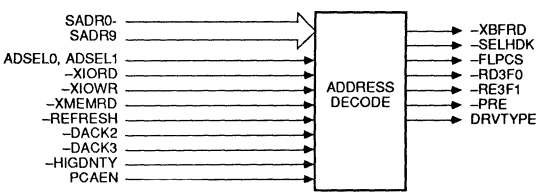

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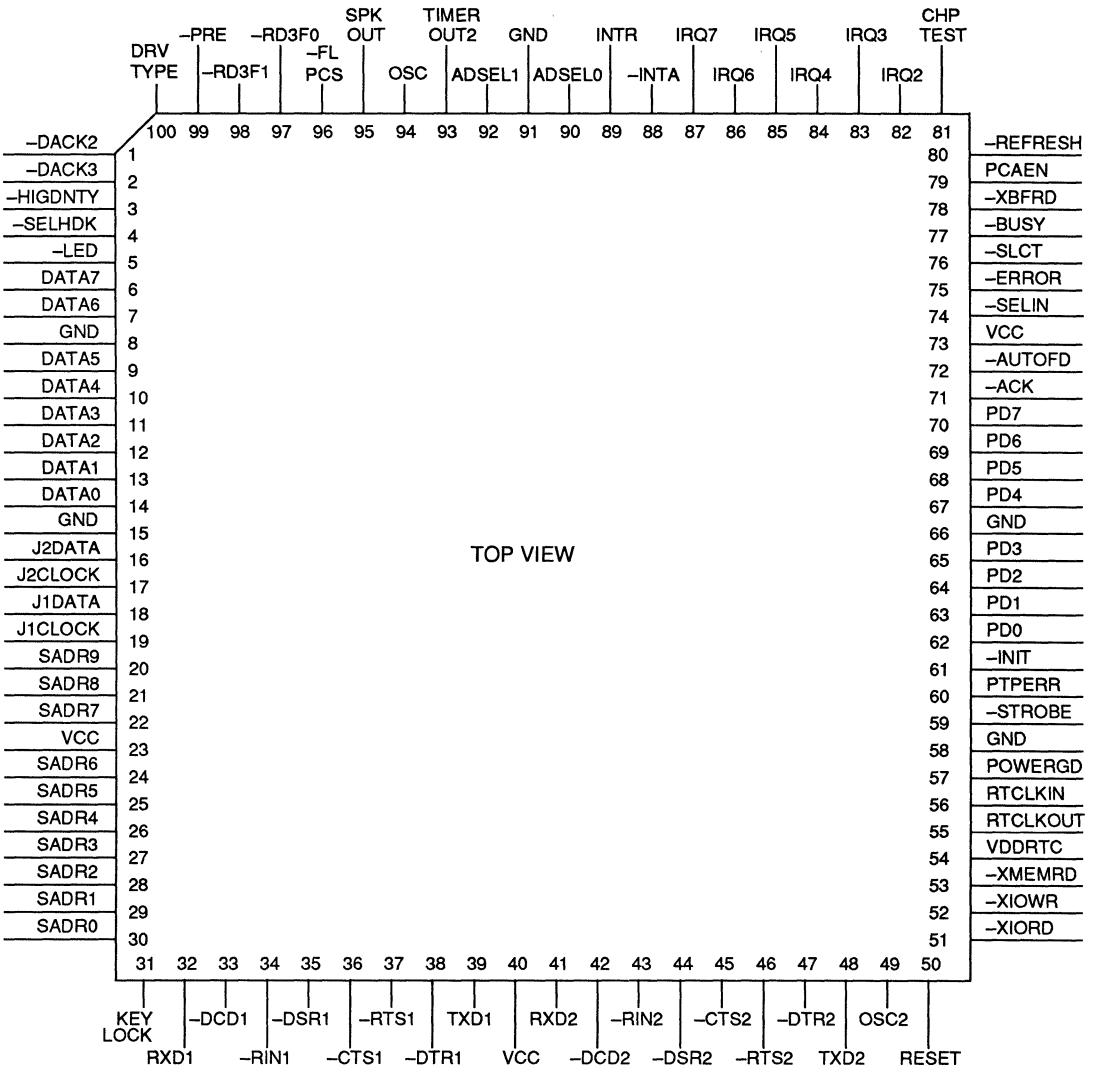
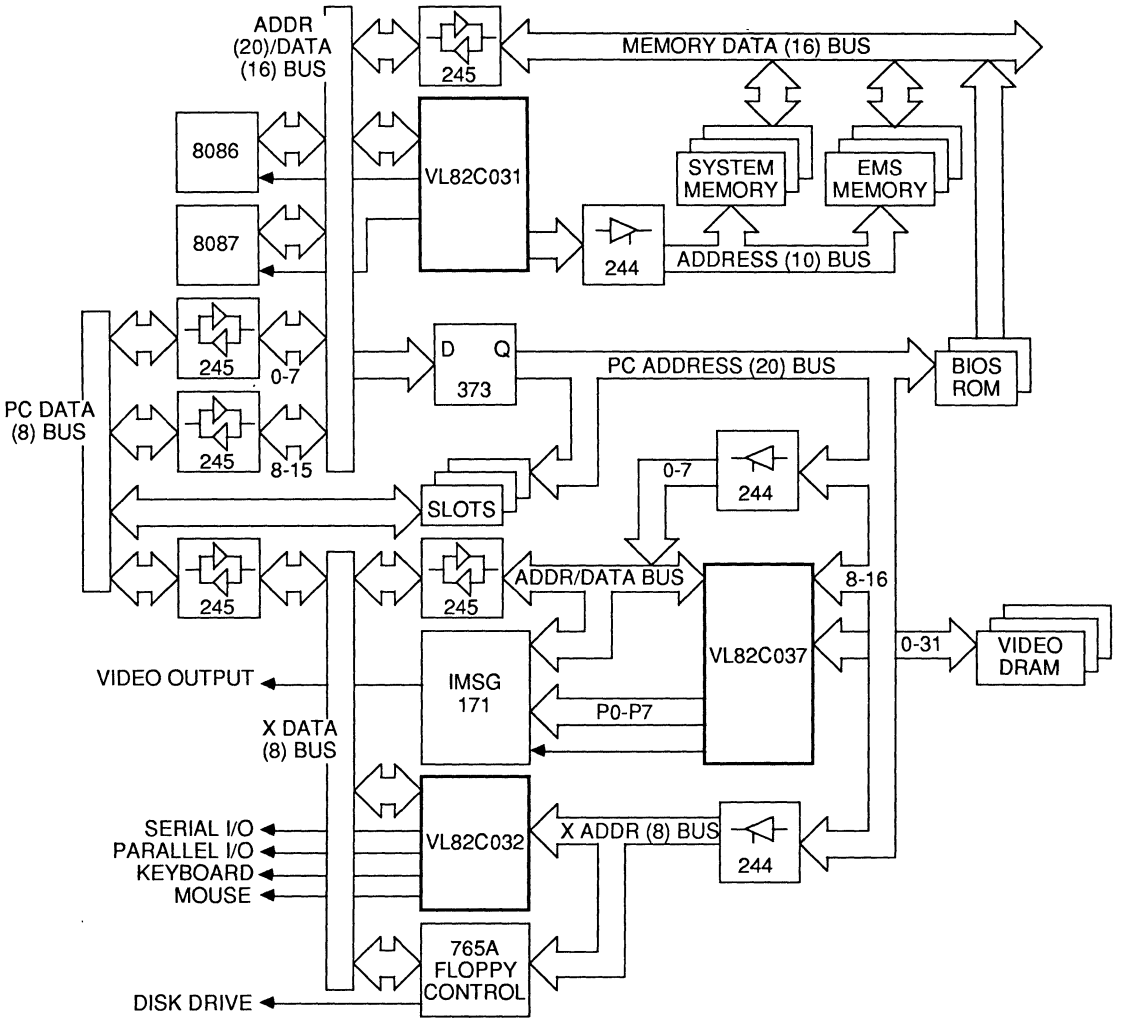
PIN DIAGRAM

VL82C032



SUPER XT-COMPATIBLE SYSTEM DIAGRAM (WITH VGA)



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SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–DACK2	1	I	DMA Acknowledge 2 - Used to notify the floppy controller that it has been granted a DMA cycle.
–DACK3	2	I	DMA Acknowledge 3 - Used to notify the on-board hard disk controller that it has been granted a DMA cycle.
–HIGDNTY	3	I	High Density - An active low signal that a high density floppy is being used.
–SELHDK	4	O	Hard Disk Select - Used to select on-board hard disk drive.
–LED	5	O	LED Output - Turns on an LED and is programmable through I/O Port D7h Bit 0.
DATA7-DATA0	6, 7 9-14	I/O	Data Bus - Bidirectional data lines to/from the CPU or I/O channel.
J2DATA	16	I/O	J2 Connector Data - A bidirectional data line for either a keyboard interface or pointing device.
J2CLOCK	17	I/O	J2 Connector Clock - A bidirectional clock for either a keyboard interface or pointing device.
J1DATA	18	I/O	J1 Connector Data - A bidirectional data line for either a keyboard interface or pointing device.
J1CLOCK	19	I/O	J1 Connector Clock - A bidirectional clock for either a keyboard interface or pointing device.
SADR9-SADR0	20-22 24-30	I	Address Bus - From I/O channel. This determines which I/O device the CPU is accessing.
KEYLOCK	31	I	Key Lock - Indicates whether the keyswitch has been locked or not. The state of this input can be read at Port 66h Bit 3.
RXD1	32	I	Receive Data 1 - Input pin for serial data to UART1.
–DCD1, –DCD2	33, 42	I	Carrier Detect - Notifies UART1 or UART2 that a carrier signal has been detected.
–RIN1, –RIN2	34, 43	I	Ring Indicator - Notifies UART1 or UART2 that a telephone ringing signal has been detected by a modem or data set.
–DSR1, –DSR2	35, 44	I	Data Set Ready - Handshake signal for UART1 and UART2, that the modem or data set is ready to transfer data.
–CTS1, –CTS2	36, 45	I	Clear To send - Handshake signal which notifies a modem or data set that UART1 or UART2 is ready to receive data.
–RTS1, –RTS2	37, 46	O	Request To Send - Handshake signal which notifies a modem or data set that UART1 or UART2 is ready to transmit data.
–DTR1, –DTR2	38, 47	O	Data Terminal Ready - Notifies a modem or data set that UART1 or UART2 is ready to transfer characters.
TXD1	39	O	Transmit Data 1 - Output pin for serial data from UART1.
RXD2	41	I	Receive Data 2 - Input pin for serial data to UART2.
TXD2	48	O	Transmit Data 2 - Output pin for serial data from UART2.
OSC2	49	I	Oscillator 2 - Is a 14.318 MHz TTL level clock input signal used to generate the clock for the 8253 internally.
RESET	50	I	Reset - An active high signal which is used to reset the internal logic of the VL82C032.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
-XIORD	51	I	I/O Read Command - Instructs the internal I/O device to drive its data on to the data bus.
-XIOWR	52	I	I/O Write Command - Instructs the internal I/O device to read the data present on the data bus.
-XMEMRD	53	I	Memory Read Command - Instructs the external memory to drive its data on to the data bus.
VDDRTC	54	I	Real Time Clock Supply - Isolated power supply input for real-time clock.
RTCLKOUT	55	O	Oscillator Output - 32.768 KHz real-time clock output to crystal.
RTCLKIN	56	I	Oscillator Input - 32.768 KHz real-time clock crystal or oscillator input.
PWRGOOD	57	I	Power Good - Indicates that power to the board is stable.
-STROBE	59	O	Printer Strobe - This pin is the "strobe" signal to a printer. Programmable through I/O Port 37Ah Bit 0.
PTPERR	60	I	Printer Paper End - Indicates that an end of paper has been detected. Readable at I/O Port 379h Bit 5.
-INIT	61	O	Printer Initialize - Initializes the printer. Programmable through I/O Port 37Ah Bit 2.
PD0-PD7	62-65 67-70	I/O	Parallel Port Data Bus - Bidirectional data lines to the parallel port device. When printer mode is selected, these lines are used as output lines. When input mode is selected, these lines are used as input lines.
-ACK	71	I	Printer Acknowledge - Indicates that data has been received by a printer. Readable at I/O Port 379h Bit 6.
-AUTOFD	72	O	Printer Auto Feed - Causes a printer to generate a line feed automatically after each line is printed. Programmable through I/O Port 37Ah Bit 1.
-SELIN	74	O	Printer Select In - Used to select the printer. Programmable through I/O Port 37Ah Bit 3.
-ERROR	75	I	Printer Error - Indicates that a printer error has occurred. Readable at I/O Port 379h Bit 3.
-SLCT	76	I	Printer Select - Indicates that the printer has been selected. Readable at I/O Port 379h Bit 4.
-BUSY	77	I	Printer Busy - This pin indicates whether the printer is able to receive data. Readable at I/O Port 379h Bit 7.
-XBFRD	78	O	Buffer Read - Controls the direction of an external data buffer. When this signal is low, data is read from the internal bus to the I/O channel. When this signal is high, data is written from the I/O channel to the internal bus.
PCAEN	79	I	Address Enable - Disables I/O devices from the I/O channel to allow DMA transfers to take place.
-REFRESH	80	I	Memory Refresh Request - Indicates that the system is in a memory refresh cycle.
CHPTEST	81	I	Chip Test Mode - When this signal is high, the VL82C032 is in a test mode. During normal operation, this pin should be tied to ground.
IRQ2-IRQ7	82-87	I	Interrupt Request Inputs - Asynchronous inputs which are the interrupt request signals to the internal 8259 interrupt controller.
-INTA	88	I	Interrupt Acknowledge - Enables the internal 8259 controller to vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
INTR	89	O	Interrupt Request - Interrupts the CPU. Generated whenever a valid IRQ is received.
ADSEL0, ADSEL1	90, 92	I	Address Select - Address range signals from the VL82C031, according to the following table:
TIMEROUT2	93	O	Timer Channel 2 Output - Provides a precision timer clock to the VL82C031.
OSC	94	I	OSC Input - A 24 MHz clock input.
SPKOUT	95	O	Speaker Data Output - Should be connected to a speaker driver to drive the speaker or beeper.
–FLPCS	96	O	Floppy Select - Chip select for a 765A floppy controller.
–RD3F0	97	O	Read Port A - A gate signal activated by a read from I/O Port 3F0h.
–RD3F1	98	O	Read Port B - A gate signal activated by a read from I/O Port 3F1h.
–PRE	99	O	Precomp - Used to select whether write precompensation is enabled in the 765A floppy controller. Programmable through I/O Port 3F7h Bit 2.
DRVTYPE	100	O	Drive Type - Used to control the data rate for the floppy controller (765A).
GND	8, 15, 58, 66, 91	I	System Ground
VCC	23, 40, 73	I	System Power: +5 V

ADSEL1	ADSEL0	Range
0	0	Don't Care
0	1	A15-A10 = 0 (I/O)
1	0	ROM
1	1	Video RAM

FUNCTIONAL DESCRIPTION

SYSTEM MEMORY AND I/O MAP

The 8086/V30 supports 16-bit operations with 20-bit addressing to directly access up to 1M byte of memory space. The system memory and an on-board expanded memory (if it's enabled) are byte and/or word accessible. Memory is mapped as follows:

Hex Address	Description	
00000 - 1FFFF	128K byte: 1st bank #1	640K System Memory
20000 - 2FFFF	64K byte: 2nd bank #2	
30000 - 3FFFF	64K byte: 2nd bank #3	
40000 - 4FFFF	64K byte: 2nd bank #4	
50000 - 5FFFF	64K byte: 2nd bank #5	
60000 - 6FFFF	64K byte: 2nd bank #6	
70000 - 7FFFF	64K byte: 2nd bank #7	
80000 - 8FFFF	64K byte: 2nd bank #8	
90000 - 9FFFF	64K byte: 2nd bank #9	
A0000 - BFFFF	128K byte: Video Buffer	
C0000 - EFFFF	192K byte: Reserved for BIOS on I/O Channel.	
F0000 - FFFFF	64K byte: System ROM	

VL82C032 I/O MAP

I/O Address	Function	Response	PC Bus Response
0020 - 0021	Interrupt Control	R/W	None
0040 -0043	System Timer	R/W	None
0060	System Data Port	R/W	None
0061	System Control	R/W	None
0062	System Status Register	R/W	None
0063	Interrupt Control	R/W	None
0065	Chip Select Control	R/W	None
0066 - 006A	Interrupt Diagnostic /Keyboard/Mouse	R/W	None
00A0 - 00AF	Interrupt Extended Status	R/W	None
00B0 - 00BF	Real-Time Clock	R/W	None
00D0 - 00DF	System Control and Status Group 2	R/W	None
00E0 - 00EF	Real-Time Clock	R/W	None
02F8-02FF	Serial Comm. Control 2	R/W	None
0320 - 032F	Fixed Disk Control	R/W*	R/W
0378 - 037A	Parallel Port	R/W	None
03F0 - 03F7	Floppy Disk Control	R/W*	R/W
03F8 - 03FF	Serial Comm. Control 1	R/W	None

***Note:** The peripheral is external to the VL82C032. It can be enabled or disabled through the Chip Select Control Register Port.

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TABLE 1. INTERRUPT REQUEST LEVEL REGISTER

Level	VL82C032 Chip	System Board	I/O Channel
IRQ0	Timer Channel 0	Not Available	Not Available
IRQ1	Keyboard Interface Pointing Device and Real-Time Clock	Not Available	Not Available
IRQ2	Not Used	Video (VL82C037)	Available
IRQ3	Serial Port 2	Not Used	Available
IRQ4	Serial Port 1	Not Used	Available
IRQ5	Not Used	Fixed Disk	Available
IRQ6	Not Used	765A Floppy Controller	Available
IRQ7	Parallel Port	Not Used	Available

TABLE 2. MODE FUNCTIONS

Address	W/R	Functions
		*** Initialization Mode***
0020	W	Initialization Command Word ICW1
0021	W	Initialization Command Word ICW2, ICW2, ICW3, ICW4
		*** Operation Mode ***
0021	W	Operation Control Word OCW1
0020	W	Operation Control Word OCW2, OCW3
		*** Read Status Register (Operation Mode) ***
0021	R	Interrupt Mask Register (IMR)
0020	R	Interrupt Request Register (IRR) and Interrupt Service Register (ISR), IRR and ISR is selected through b0 and b1 in OCW3

INTERRUPT CONTROL LOGIC

The interrupt control logic includes one Intel 8259A-compatible interrupt controller, one interrupt vector register and two interrupt extension registers.

The interrupt controller has eight levels of interrupt that are handled according to priority in the VL82C032 chip. Table 1 shows the hardware interrupts and their availability to the I/O channel (PC bus).

The I/O address for each register in the interrupt controller is defined in Table 2.

During initialization mode, when the vector address is written into ICW2 register, the same vector address will be written into the interrupt vector register. The content of interrupt vector register can be read through an I/O read from address 063h. In order to read this register, I/O Port 69h Bit 6 must be set to 1. By writing to I/O Port 63h any of the IRQ lines can be activated or the NMI line as shown in the following table:

I/O Port 63h (Write)

Bit	Function
7	IRQ7
6	IRQ6
5	IRQ5
4	IRQ4
3	IRQ3
2	IRQ2
1	Not Used
0	NMI

To write this port I/O Port 69h Bit 7 must first be set to 1. You must set Port 69h Bit 2 to 1 to allow NMI activation. To start the initialization mode of the interrupt controller, a command is issued with Bit 4 =1 to I/O address 020h which it is interpreted as ICW1. The content of the interrupt vector register is reset to 0 after power-up reset.

Regardless of the vector address initialized in ICW2, the vector address generated by interrupt IRQ1 is always hex 71. The interrupt acknowledge cycle only requires one wait state for 8 MHz or 10 MHz CPU 8086.

For detailed instructions on how to program the 8259A-compatible interrupt controller, see the VL82C59A data sheet.

TIMER CONTROLLER

This timer controller is compatible with the Intel 8253. It is a programmable interval timer/counter. The functions of the timer controller are to generate a constant system time and control the tone of the speaker. This controller contains three timer channels. Each channel is described as follows:

Channel 0:
This channel is a general purpose timer providing a constant time base for the operating system. The input clock runs at 1.19 MHz. The enable clock input is always enabled after power-up. The output of this channel is connected to interrupt channel 0 (IRQ0) of the interrupt controller (8259A).

Channel 1:
This channel is for diagnostic purposes. During power-up test, the system BIOS will use this channel to check the functions of the timer controller. The system BIOS also uses this channel to check the frequency of memory refresh. The input clock runs at 15.6 µs per cycle. The enable clock input is always enabled after power-up. The output of this channel is not connected anywhere, so CLKOUT1 is not an available pin on the VL82C032.

Channel 2:
This channel is used to control the tone of the speaker. The input clock runs at 1.19 MHz frequency. The enable clock input is turned on or off by bit 0 of system control register 061h. When bit 0 of I/O PORT 061h is set to 1, the frequency of the tone is controlled by the number in counter register 2. The output of this channel is connected to the speaker driver. After power-up reset, bit 0 of I/O port 061h is reset to 0. More detailed information is available in the system control register section (061h).

The I/O address for each register in the timer controller is defined in Table 3.

The control mode register is to select the operation mode for each channel in the timer controller. There are six

TABLE 3. REGISTERS

Address	W/R	Functions
0040	W/R	Counter Register 0
0041	W/R	Counter Register 1
0042	W/R	Counter Register 2
0043	W	Control Mode Register

different modes that can be selected. They are listed as follows:

- mode 0: interrupt on terminal count
- mode 1: programmable one-shot
- mode 2: rate generator
- mode 3: square wave rate generator
- mode 4: software triggered strobe
- mode 5: hardware triggered strobe

REAL TIME CLOCK

A real-time clock is integrated in the VL82C032 chip. Its functions are fully compatible with the National 58167A real-time clock. However, the VL82C032 is much faster than the 58167A. It can complete a read or write cycle at normal I/O speed (four wait states) in a System 30, so it is not necessary to generate the IOCHRDY to the I/O Channel. The functional block has an independent power (VDDRTC) pin which is isolated from the normal power (VCC) pin of the VL82C032 chip.

This real-time clock includes an addressable counter, eight bytes of RAM, and two interrupt outputs. A power-down input allows the real-time clock to be powered from battery power and continue its operation independently during power-down mode. The time base is derived from a 32,768 Hz crystal oscillator.

The PWRGOOD input will block the chip select signal and I/O read or write signals during power-up or hardware reset. It prevents any non-valid I/O access to the real-time clock.

The I/O address for each register and RAM in the real-time clock is defined in Table 4.

The interrupt from the real-time clock is connected to IRQ1 of the interrupt controller. IRQ1 is also shared with the keyboard and pointing device interface. The interrupt from the real-time clock can be reset by reading the interrupt status register (I/O Port B0 hex).

An auto reset will be generated in the internal logic of the real-time clock when VCC switches from 0.0 V to operating voltage. This reset signal will reset the content of RAM and the content of the interrupt registers to 0.

CMOS SRAM

There are 16 bytes of CMOS static RAM in the VL82C032, powered by the standby battery. This can be used for storing system configuration information.

The RAM can be accessed by writing an index value (0-F) to I/O Port D4h and then writing or reading I/O Port D5h.

The PWRGOOD input will block the chip select signal and I/O read or write signals during power-up or hardware reset. It prevents any non valid I/O access to the RAM.

An auto reset will be generated when VCC switches from 0.0 V to 2.0 V, which will reset the content of the SRAM to 0.

SERIAL CONTROLLER

The VL82C032 chip incorporates two serial communication controllers which are fully compatible with the NS8250A. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. These controllers support 5-, 6-, 7- and 8-bit characters with 1, 1.5 or 2 stop bits. A prioritized interrupt system controls transmit, receive, error, and line status as well as data-set interrupt. The clock applied to the serial controller is 1.84 MHz which is derived from the system clock.

Each serial port will provide the following RS232 signals:

- RXD: Receive Data
- CTS: Clear To Send
- DSR: Data Set Ready
- DCD: Data Carry Detect
- RI: Ring Indicator
- TXD: Transmit Data
- DTR: Data Terminal Ready
- RTS: Request To Send

The interrupt from serial controller 1 is connected to IRQ4 of the interrupt controller in the VL82C032. The I/O address for each register in serial controller 1 is defined in Table 5.

The interrupt from serial controller 2 is connected to IRQ3 of the interrupt controller in the VL82C032. The I/O address for each register in serial controller 2 is defined in Table 6.

TABLE 4. W/R FUNCTIONS

Address	W/R	Functions
00B0	R	Interrupt Status Register
00B1	W	Interrupt Control Register
00B2	W	Counters Reset (Data = FFH)
00B3	W	RAM Reset (Data = FFH)
00B4	R	Status Bit, d0 = 1, Counter Is Rippling The content of counters are invalid; reread.
00B5	W	Go Command (Data = XXH)
00B6	W	Standby Interrupt (1 = Enable, 0 = Disable)
00BF	W	Enable Test Mode
00E0	W/R	Counter - Ten Thousandths of Seconds
00E1	W/R	Counter - Hundredths and Tenths of Seconds
00E2	W/R	Counter - Seconds
00E3	W/R	Counter - Minutes
00E4	W/R	Counter - Hours
00E5	W/R	Counter - Day of Week
00E6	W/R	Counter - Day of Month
00E7	W/R	Counter - Month
00E8	W/R	RAM - Ten Thousandths of Seconds
00E9	W/R	RAM - Hundredths and Tenths of Seconds
00EA	W/R	RAM - Seconds
00EB	W/R	RAM - Minutes
00EC	W/R	RAM - Hours
00ED	W/R	RAM - Day of Week
00EE	W/R	RAM - Day of Month
00EF	W/R	RAM - Month

PARALLEL PORT CONTROLLER

The parallel port controller can be configured to be one of two modes. The first is "printer mode". The second is "input mode," which allows the parallel port to receive data from external devices. The input mode of the parallel port controller is selected by writing a 0 to bit 7 of the peripheral select control register 065h.

There are two output ports and three input ports in the parallel port controller. The following is a detailed description of each port.

Data Port: 378h

The data port is an 8-bit port for both the printer mode and input mode. For the printer mode, a write operation to this port immediately presents data to the connector pins. A read operation from this port in the printer port produces the data that was last written to it.

In the input mode, a write operation to this port will not affect the output of the data port. A read operation in the input mode produces the current data on the connector pins from external devices.

Status Port: 379h

The status port is a read-only port for either mode. When an interrupt is pending the interrupt status bit is set to 0. The following is the bit definition of the status port:

Bit Function

7 –BUSY: When this bit is 0, the printer is busy and cannot accept data.

6 –ACK: When this bit is 0, the printer is ready to accept data.

5 PE: When this bit is 1, the printer has detected the end of the paper.

4 SLCT: When this bit is 1, the printer has been selected.

3 –ERROR: When this bit is 0, the printer has detected an error condition.

2 –IRQ: When this bit is 0, the printer has acknowledged the previous transfer using the "–ACK" signal.

Output Control Port: 37Ah

The Output Control Port is a read or write port. The following shows the bit definition of the Output Control Port:

Bit Function

4 IRQEN: When this bit is set to 1, the interrupt logic is enabled.

3 SLCTIN: This bit controls the –SELIN signal on the VL82C032 pin 74. When this bit is set to 1, the printer is selected.

2 –INIT: This bit controls the "–INIT" signal on the VL82C032 pin 61. When this bit is set to 1, the printer starts.

1 AUTOFD: This bit controls the "–AUTOFD" signal on the VL82C032 pin 72. When this bit is set to 1, the printer will automatically line feed after each line is printed.

0 STROBE: This bit controls the "–STROBE" signal on the VL82C032 pin 59. When this bit is set to 1, data is pulse-clocked into the printer.

The interrupt from the parallel port controller is connected to IRQ7 of the interrupt controller in the VL82C032. The I/O address for each register in the parallel port controller is defined in Table 7.

KEYBOARD INTERFACE AND POINTING DEVICE INTERFACE

There are two interfaces (J1 and J2) which can be used for either keyboard or pointing device. The keyboard interface is fully compatible with the enhanced AT keyboard, and is implemented as hardware logic instead of the 8042 microcontroller. The pointing device interface is also fully compatible with IBM PS/2 mouse devices. The system BIOS will handle the following tasks:

- initialization of the interface after power-up
- define which device (keyboard or pointing device) has been connected to each interface (J1 and J2)
- receive interrupt and parity errors
- translation between keyboard scan code and ASCII code
- transmission sequences

The hardware will handle the following tasks:

- initialize both interface registers to default value after power-up reset
- generate protocol sequences (data line and clock line) between system and keyboard or mouse
- detect incoming data (start bit) from keyboard or mouse
- generate the receive interrupt and check parity error
- generate the parity bit during transmission
- handle asynchronous conditions between transmit and receive

There are two signal lines used for each interface. They are the data line and the clock line. During a receive or transmit cycle, the clock will be generated by the keyboard or pointing device.

TABLE 5. SERIAL CONTROLLER 1 I/O ADDRESSES

Address	W/R	Functions
03F8	W	Transmitter Holding Register
03F8	R	Receive Buffer Register
03F9	W/R	Interrupt Enable Register
03FA	R	Interrupt Identification Register
03FB	W/R	Line Control Register
03FC	W/R	Modem Control Register
03FD	R	Line Status Register
03FE	R	Modem Status Register
03FF	W/R	Scratch Register

TABLE 6. SERIAL CONTROLLER 2 I/O ADDRESSES

Address	W/R	Functions
02F8	W	Transmitter Holding Register
02F8	R	Receive Buffer Register
02F9	W/R	Interrupt Enable Register
02FA	R	Interrupt Identification Register
02FB	W/R	Line Control Register
02FC	W/R	Modem Control Register
02FD	R	Line Status Register
02FE	R	Modem Status Register
02FF	W/R	Scratch Register

The system only drives the clock line for handshake purposes.

The communication protocol used by the keyboard and mouse ports is compatible with the Intel 8042 chip, although the programming interface is different. Data transmission to and from the external device consist of an 11-bit data stream transferred over the data line. The clock is generated by the external device to synchronize the transmission, and is implemented as a "wire OR" signal so either the external device or the system may pull it low. The format of each data element is as follows:

1 Start Bit (Always 0)
8 Data Bits, LSB First
1 Parity Bit (Odd Parity)
1 Stop Bit (Always 1)

The eight data bits plus the parity bit always have an odd number of 1's. The external device begins transmitting information by pulling the data line low for one clock cycle, which indicates the start bit. The system can terminate the transmission at any time during the first 10 clock cycles by pulling the clock low. If the transmission has progressed beyond the tenth clock, the system must receive the data to prevent data loss. The system may transmit data to the external device by first pulling the clock low to inhibit the external device, then pulling the data line low and releasing the clock line. The external device then recognizes the first clock pulse as a start bit transmitted from the system and receives the rest of the data. Table 8 summarizes the functions of the clock and data signals for the two interfaces.

The definitions of each register for interface are described as follows.

KEYBOARD/POINTING DEVICE DATA REGISTER (060h) R/W

This register is for user interface (application) at the system BIOS level. It is a dummy register, and does not relate to the hardware logic on any particular interface. When information is to be transmited to the keyboard or pointing device, writing the data to this register and the system BIOS will take the content of this register and transmit it to the keyboard or pointing device. When either interface receives data from an external device (keyboard or pointing device), the system BIOS will check any parity error and copy the data from the receive register to this data register.

This register will be reset to 0 at power-up reset.

KEYBOARD/POINTING DEVICE TRANSMIT/RECEIVE REGISTERS (067h AND 068h)

Register 067h is the transmit/receive register for interface J1. Register 068h is the transmit/receive register for interface J2. These are eight-bit registers. Reading these registers will not affect any logic state on the interfaces. These registers can be read at any time, and will return the data from the receive buffers for their respective interfaces.

When writing to these registers, the data will be stored in the transmit buffers and generate a parity bit. Writing the data to these registers will not start the transmit sequence. To start the transmit sequence on interface J1, bit 3 of the transmit control register (069h) must be toggled (0->1->0) before writing the data to the transmit register (067h). To start the transmit sequence on interface J2, bit 4 of the transmit control register (069h) must be toggled (0->1->0) before writing the data to the transmit register (068h). The purpose of toggling bit 3 or bit 4 of the transmit control register is to ensure the clock line on the interface (J1 or J2) is in a quiescent state.

The receive buffers and transmit buffers will be reset to 0 after power-up reset.

Bit 3 of this register is for initializing the transmission logic for interface J1. Bit 4 of this register is for initializing the transmission logic for interface J2. These two bits ensure the clock lines are in the quiescent state. If the external device (keyboard or pointing device) is sending data to the system before transmission starts, the transmit sequence will not be started until bit 4 or bit 6 of the receive control register (066h) is toggled (0->1->0). When either interface receives data from an external device the hardware logic will pull the clock line low to prevent contiguous data transmission by the external device. Toggling bit 4 of the receive control register (066h) will

TABLE 7. OUTPUT AND PRINTER REGISTER

Address	W/R	Functions
0378	W/R	Data Output Register
0379	R	Printer Status Register b7 = Printer Busy (1 = Not Busy, 0 = Busy) b6 = Printer Acknowledge (1 = No –ACK, 0 = –ACK) b5 = End of Paper (1 = No Paper, 0 = Paper ok) b4 = Printer Selected (1 = Selected, 0 = Not Selected) b3 = Printer Error (1 = No –ERROR, 0 = –ERROR) b2 - b0 = Not Used
037A	W/R	Printer Control Register b7 - b5 = Not Used b4 = Enable/Disable Interrupt (1 = Enable, 0 = Disable) b3 = Select Printer Device (1 = Select, 0 = Not Select) b2 = Start Printer Device (1 = Stop, 0 = Start) b1 = Enable Line Feed (1 = Enable, 0 = Disable) b0 = Data Strobe (1 = Data Valid, 0 = Data Invalid)

TABLE 8. TRANSMIT DECODE

Clock Line	Data Line	Functions
0	X	No Transmit or Receive
1	0	System Transmit Data to Keyboard or Mouse
1	1	Keyboard or Mouse Transmit Data to System

cause the clock line on interface J1 to become quiescent. Toggling bit 6 of the receive control register (066h) will cause the clock line on interface J2 to become quiescent. If the clock line is kept low for any reason, the transmit cycle should not be started until the clock line becomes quiescent.

The bit definitions of the transmit control register are shown in Table 9.

Toggling bit 3 or bit 4 of the transmit control register will reset any parity error indication (bit 0 or bit 1 of the receive control register - 066h).

Bit 7, bit 6 and bit 2 of the transmit control register are for interrupt/NMI diagnostics. These bits are described in the section covering the interrupt controller.

Reading this register will not affect the hardware logic. These bits will be reset to 0 after power-up reset.

KEYBOARD/POINTING DEVICE RECEIVE CONTROL REGISTER (066h)

This register controls the receive logic for both interfaces. This register also indicates which interface (J2 or J2) has been connected to the keyboard, and if any parity error has occurred during a receive cycle. The bits are defined in Table 10.

When bit 5 is set to 0, the clock line on interface J1 will be forced to 0. When bit 7 is set to 0, the clock line on interface J2 will be forced to 0. At power-up reset, these two bits are reset to 0. External devices cannot send any data to the system until these two bits are set to 1.

When bit 4 is set to 1, it clears the indication of parity errors and interrupts on interface J1. When bit 6 is set to 1, it clears the indication of parity errors and interrupts on interface J2. When these two bits are 1, the clock line will not be forced low after receiving data from an external device. Normally, these two bits should be set to 0. After receiving data from an external device, bit 4 or bit 6 should be toggled to clear any parity error or interrupt. These bits will be reset to 0 on power-up reset.

Bit 3 indicates whether the keyboard has been connected to interface J1. The keyboard connection is not detected by the hardware logic on the the interface J1. It is done by the system BIOS, so the system BIOS should set or reset this bit. When this bit is set to 1, the keyboard is connected to interface J1. When this bit is 0, the keyboard is connected to interface J2. This bit will be reset to 0 at power-up reset.

Bit 0 and bit 1 indicate parity errors. When bit 0 is set to 1, it indicates a parity error occurred on interface J1 during a receive cycle. Bit 0 can be cleared by writing one to bit 4 of this register or bit 3 of the transmit control register (069h). Bit 1 can be cleared by writing 1 to bit 6 of this register or bit 4 of the transmit control register (069h). These two bits are reset to 0 at power-up reset.

Bit 2 indicates whether the system keyswitch has been locked or not. When this bit is 0, the system keyswitch is locked.

KEYBOARD/POINTING DEVICE RECEIVE STATUS REGISTER (06Ah)

Bit 5 and bit 2 of this register indicate whether data has been received from an external device or not for interface J1 and J2, respectively. When bit 5 is 1, data has been received from interface J1. Bit 5 can be cleared by setting bit 4 of the receive control register (066h) or bit 3 of the transmit control register (069h). When bit 2 is 1, data has been received from interface J2. Bit 2 can be cleared by setting bit 6 of the receive control register (066h) or bit 4 of the transmit control register (069h). After power-up reset, these bits are reset to 0.

The bits in this register are defined in Table 11.

Bit 0 indicates what type of floppy disk drive has been connected to the system. When this bit is set to 0, a high density drive (1.44M bytes) has been selected. When this bit is set to 1, a low density drive (720K bytes) has been selected. This bit reflects the state of the –HIGDNTY input (pin 3) of the VL82C032.

INTERRUPT EXTENDED CONTROL REGISTER (0A1h)

The purposes of this register is to mask out incoming interrupts from the keyboard, pointing device or real-time clock. The bit definitions for this register are described in Table 12.

When bit 3 is set to 1, interrupts from interface J2 will be masked out. When bit 2 is set to 1, interrupts from interface J1 will be masked out. When bit 0 is set to 1, interrupts from the real-time clock wil be masked out.

TABLE 9. TRANSMIT CONTROL REGISTER

Address	W/R	Functions
0069	W/R	b7 = Enable Diagnostic Through Reg. 63h b6 = Blocks Reg. 63h Read b5 = Disable J1 and J2 Clock (1 = Disable) b4 = Toggle for System to Transmit Data Through J2 b3 = Toggle for System to Transmit Data Through J1 b2 = Enable NMI Diagnostic Through Reg. 63h b1 = Not Used b0 = Not Used

TABLE 10. RECEIVE CONTROL REGISTER

Address	W/R	Functions
0066	W/R	b7 = System Drives the Clock on J2
	W/R	b6 = Toggle for System to Receive Data Through J2
	W/R	b5 = System Drives the Clock on J1
	W/R	b4 = Toggle for System to Receive Data Through J1
	W/R	b3 = J1 Has Keyboard Connection
	R	b2 = Key lock (0 = Key Is Locked)
	R	b1 = J2 Parity Error Indication
	R	b0 = J1 Parity Error Indication

Setting the bits in register 0A1 will not affect the indications on bit 2 and bit 3 of the interrupt extended status register (0A0h) and bit 2 and bit 5 of the keyboard/pointing device receive status register (06Ah). These bits are reset to 0 at power-up reset.

INTERRUPT EXTENDED STATUS REGISTER (0A0h)

IRQ1 (hardware interrupt) of the interrupt controller is shared by three devices; real-time clock, J1 interface and J2 interface. This register determines which device generated the IRQ1.

The bit functions of this register are described in Table 13.

When bit 3 is 1, it indicates a pending interrupt from interface J2 (keyboard or pointing device). Bit 3 can be reset by toggling bit 6 of register 066h or bit 4 of register 069h. When bit 2 is 1, it indicates a pending interrupt from interface J1 (keyboard or pointing device). Bit 2 can be reset by toggling bit 4 of register 066h or bit 3 of register 069h. When bit 0 is 1, it indicates a pending interrupt from the real time clock. Bit 0 can be reset by reading the interrupt status register (0B0h) on the real time clock. These bits are reset to 0 at power-up reset.

SYSTEM CONTROL REGISTER

The system control register (061h) is used as speaker control, enables the parity check on the I/O Channel and memory parity check on the system board. This register is read/write. The bits in this register are defined in Table 14.

TABLE 11. RECEIVE STATUS REGISTER

Address	W/R	Functions
006A	R	b7 = Not Used b6 = J2 Status (0 = Receive in Progress) b5 = J1 Receive Buffer Full (Interrupt Status) b4 = Not Used b3 = J1 Status (0 = Receive in Progress) b2 = J2 Receive Buffer Full (Interrupt Status) b1 = Not Used b0 = High Density Floppy Media (0 = High Density)

TABLE 12. INTERRUPT EXTENDED CONTROL REGISTER

Address	W/R	Functions
00A1	W/R	b7 = Not Used b6 = Not Used b5 = Not Used b4 = Not Used b3 = Mask Out Interrupt from J2 b2 = Mask Out Interrupt from J1 b1 = Not Used b0 = Mask Out Interrupt from Real Time Clock

TABLE 13. INTERRUPT EXTENDED STATUS REGISTER

Address	W/R	Functions
00A0	R	b7 = Not Used b6 = Not Used b5 = Not Used b4 = Not Used b3 = IRQ1 from J2 b2 = IRQ1 from J1 b1 = Not Used b0 = IRQ1 from Real Time Clock

When bit 5 is set to 1, it stops IOCHCK from generating an NMI. When cleared, an NMI is generated when IOCHCK goes active.

When bit 4 is set to 1, it stops a memory parity from generating an NMI. When cleared, an NMI is generated whenever a memory parity error is sensed.

Bit 1 is used as speaker data. This bit gates the output of timer 2. It is used to disable the timer's sound source or modify its output. When set to 1, it enables the output. When cleared, it forces the output to 0.

Bit 0 is routed to the timer input at GATE 2. When this bit is cleared, the timer operation is halted. This bit and bit 1 (speaker data) control the operation of the sound source.

At power-up reset, the contents of this register are reset to 0.

SYSTEM STATUS REGISTER (062h)

This port returns status and configuration information about the planar card. The bits are defined in Table 15.

Bit 7 - Parity Error status bit, is used to indicate that a memory error has been detected. This bit is read only and is cleared by a reset.

Bit 6 - I/O Channel Error status bit, is used to indicate the state of the IOCHCK pin. This bit is read only and is cleared by a reset.

Bit 5 - Timer 2 Output status bit, is used to reflect the current state of the output of timer channel 2. This bit is read only.

Bit 4 - Reserved, read as 0, and should be written as 0.

Bit 3 - Reserved, read as 0, and should be written as 0.

Bit 2 - Hard Disk Installed status bit, when set (1) indicates the hard disk drive is missing, and when reset (0) the hard disk is installed. This bit is set by the BIOS and defaults to 1 on reset.

Bit 1 - Coprocessor Installed status bit, when set (1) indicates that the coprocessor is installed, and when reset (0) indicates the

coprocessor is missing. This bit is set by the BIOS. This bit defaults to 0 on reset.

Bit 0 - Reserved, read as 0, and should be written as 0.

PERIPHERAL SELECT CONTROL REGISTER (065h)

This register controls the following peripherals on the system board:

- Serial Controllers
- Floppy Controller
- Video Controller
- Parallel Controller
- Fixed Disk Controller

The bits in this register are defined in Table 16.

When a bit is set to 1, that peripheral is enabled. When the peripheral is enabled, the chip select signal is generated to start a read or write operation, and the read or write signal to the I/O channel is blocked. When the peripheral is disabled, the chip select signal is not generated and all read and write operations are directed to the I/O channel. See Table 16.

After power-up reset, all the bits of this register are reset to 0.

ADDRESS DECODE FOR FLOPPY CONTROLLER

VL82C032 has the capability to decode the I/O address for an on-board floppy controller and generates the select signal for the floppy controller. From the system point of view, the floppy controller and its associated registers inside the VL82C032 are on the same bus (I/O extended bus). The VL82C032 can control the data buffers between the I/O extended bus and the I/O channel during I/O cycles or DMA cycles for the floppy controller.

Two buffer enable signals (–RD3F0 and –RD3F1) are decoded for this purpose. The bits in these buffers should be connected as shown in Table 17.

ADDRESS DECODE FOR HARD DISK CONTROLLER

VL82C032 has the capability to decode the I/O address for the on-board hard disk controller and generates the select signal for the controller. From the system point of view, the hard disk controller and its associated registers reside on the same bus (I/O extended bus) as the VL82C032. VL82C032 can control the data buffers between the I/O extended bus and the I/O channel during I/O cycles or DMA cycles for the hard disk controller. The I/O address range for the hard disk controller is between 320h and 327Fh. Accessing these addresses will activate the –SELHDK output (pin 4). It uses DMA channel 3 for DMA access.

EXTENDED CONTROL AND DIAGNOSTICS

There are several extended control and diagnostic features incorporated into the VL82C032. These include a power management function for reduced power consumption in standby mode, DMA diagnostics for hard disk controllers, and control of an external LED driver signal.

POWER MANAGEMENT REGISTERS (01E AND 01C)

The VL82C032 contains circuitry which allows it to be placed in a "standby" mode where any internal circuits which operate in a dynamic manner are placed into a static state, thereby reducing power consumption. This feature is intended primarily for use the VL82C032 system controller, but can be implemented in a stand-alone I/O controller under the right circumstances. To place the chip in standby mode, first write a 1 to register 1Eh, then perform a read from register 1Ch. As long as the I/O read line and chip select remain active, and the address remains valid, the chip will be in standby mode. When the read cycle is terminated, the chip resumes normal operation.

MISCELLANEOUS CONTROL/ STATUS REGISTER (0D0)

This register is related to the operation of the built in floppy decode logic, the real-time clock, and serial port 2. The bit assignments in this register are as follows:

Bit 7 - DRVTYPE control bit. This bit controls the state of the DRVTYPE output signal of the VL82C032 (Pin 100).

Bit 6 - RTC Clock Status. This bit indicates the current state of the internal 58167 compatible RTC input clock, and is read only.

Bit 5 - Enable Serial Port 2. When set to 1, this bit enables the operation of the second 8250 serial I/O controller.

Bit 4 - This bit, when set, forces DACK2 active.

Bit 3 - RTC Reset Status. This bit reflects the state of the reset signal to the internal 58167 compatible real-time clock, and is read only.

Bits 2-0 - Not Used

HARD DISK DIAGNOSTIC REGISTER (0D1)

This register allows diagnostics of DMA transfers and selection of the address range for the hard disk chip select. The bit assignments for this register are as follows:

Bits 7-2 - Not Used

Bit 1 - 0 = IBM IDE address range, 1 = XT controller address range.

Bit 0 - 1 = Force DACK3 active.

LED CONTROL REGISTER (0D7)

This register controls the state of the LED output of the VL82C032. A 1 in bit 0 turns on the LED, and a 0 turns it off. The remaining bits are not used.

TABLE 14. SYSTEM CONTROL REGISTER

Address	W/R	Functions
0061	W/R	b7 = Not Used (0). b6 = Not Used (0). b5 = IOCHCK, PC-Bus Memory Parity Check (1 = Disable, 0 = Enable) b4 = On-Board Memory Parity Check (1 = Disable, 0 = Enable) b3 = Not Used (0). b2 = Not Used (0). b1 = Speaker Data, Enable/Disable Output of 8253-Timer 2 (1 = Enable, 0 = Disable) b0 = Enable/Disable 8253-Timer 2 (1 = Enable, 0 = Disable)

TABLE 15. SYSTEM STATUS REGISTER

Address	W/R	Functions
0062	W/R	b7 = Parity Error (R/O) b6 = I/O Channel Error (R/O) b5 = Timer 2 Output (R/O) b4 = Reserved (0) b3 = Reserved (0) b2 = No Hard Disk (1) b1 = Coprocessor Installed (0) b0 = Reserved (0)

TABLE 16. PERIPHERAL SELECT CONTROL REGISTER

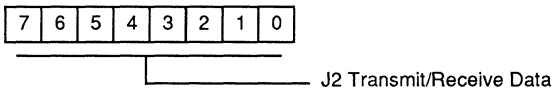
Address	W/R	Functions
065	W/R	b7 = Parallel Port Output Enable b6 = Reserve (0) b5 = Reserve (0) b4 = Serial Port 1 Select b3 = Floppy Controller Select b2 = Video Select b1 = Parallel Port Select b0 = Hard Disk Select

TABLE 17. FLOPPY CONTROL LOGIC I/O ADDRESSES

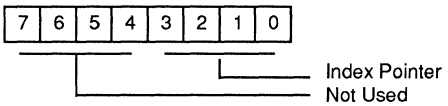
Address	W/R	Functions
03F0	R	RAS A Port b7 = IRQ6 b6 = DRQ2 b5 = Step (Latched) b4 = Track 0 b3 = Head 1 Select b2 = Index b1 = Write Protect b0 = Direction
03F1	R	RAS B Port b7 = Not Used b6 = Drive Select 1 b5 = Drive Select 0 b4 = Write Data (Latched) b3 = Read Data (Latched b2 = Write Enable (Latched) b1 = Drive Select 3 b0 = Drive Select 2

REGISTER BIT DIAGRAMS

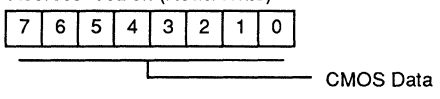
J2 TRANSMIT/RECEIVE REGISTER
Address=0068h (Read/Write)



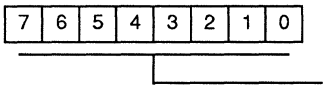
CMOS SRAM INDEX REGISTER
Address=00D4h (Read/Write)



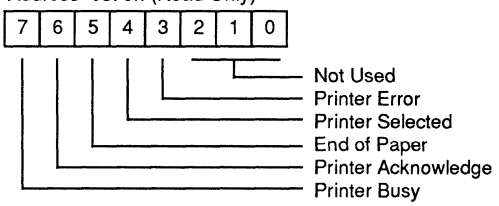
CMOS SRAM DATA PORT
Address=00D5h (Read/Write)



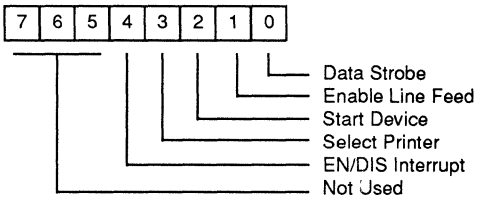
PARALLEL PORT DATA REGISTER
Address=0378h (Read/Write)



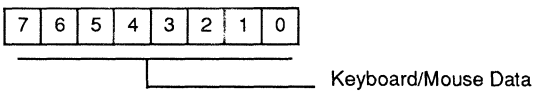
PARALLEL PORT STATUS REGISTER
Address=0379h (Read Only)



PARALLEL PORT CONTROL REGISTER
Address=-037Ah (Read/Write)

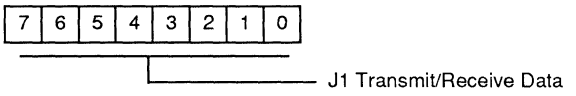


KEYBOARD/MOUSE DATA REGISTER
Address=0060h (Read/Write)

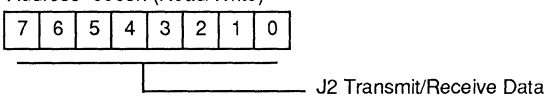


REGISTER BIT DIAGRAMS (Cont.)

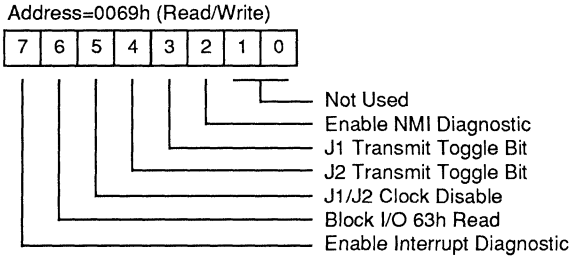
J1 TRANSMIT/RECEIVE REGISTER
Address=0067h (Read/Write)



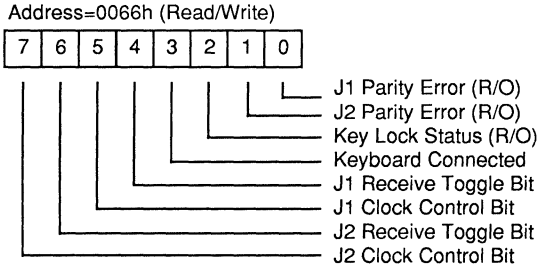
J2 TRANSMIT/RECEIVE REGISTER
Address=0068h (Read/Write)



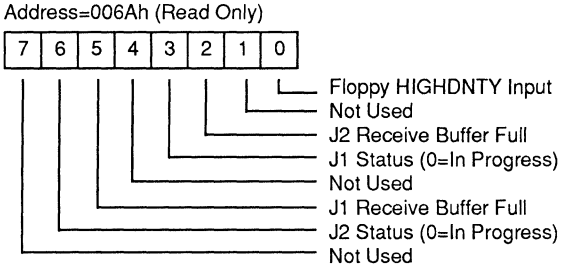
TRANSMIT CONTROL REGISTER
Address=0069h (Read/Write)



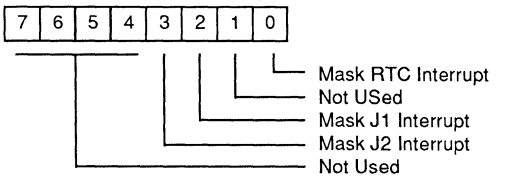
RECEIVE CONTROL REGISTER
Address=0066h (Read/Write)



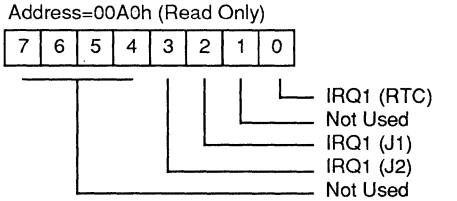
KEYBOARD/MOUSE RECEIVE STATUS REGISTER
Address=006Ah (Read Only)



INTERRUPT EXTENDED CONTROL REGISTER
Address=00A1h (Read/Write)



INTERRUPT EXTENDED STATUS REGISTER
Address=00A0h (Read Only)



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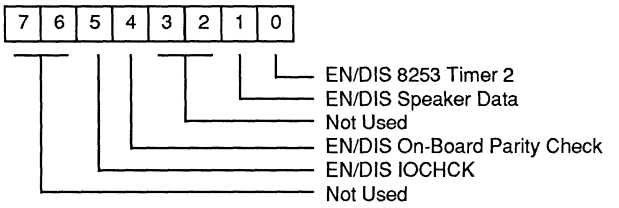
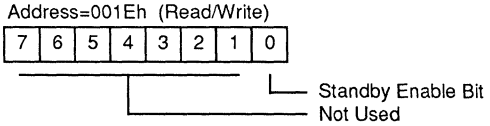
REGISTER BIT DIAGRAMS (Cont.)

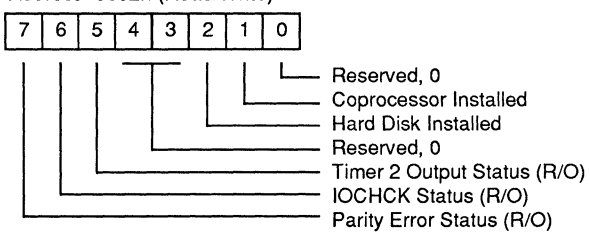
SYSTEM CONTROL REGISTER
Address=0061h (Read/Write)



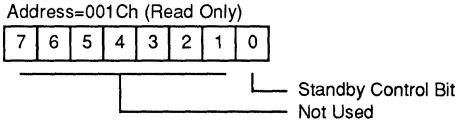
STANDBY ENABLE REGISTER
Address=001Eh (Read/Write)



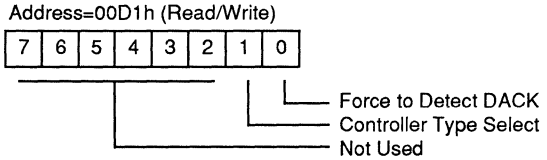
SYSTEM STATUS REGISTER
Address=0062h (Read/Write)



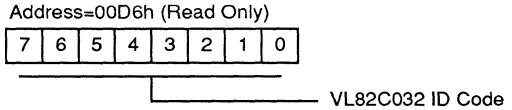
STANDBY CONTROL REGISTER
Address=001Ch (Read Only)



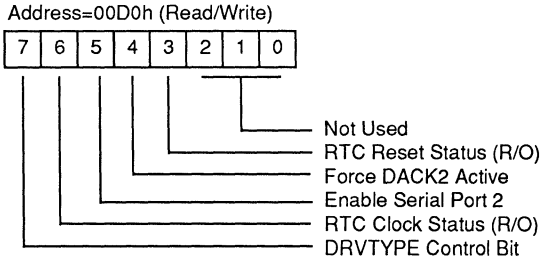
HARD DISK CONTROL/DIAGNOSTIC REGISTER
Address=00D1h (Read/Write)



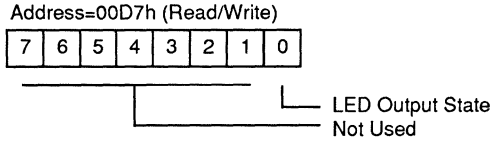
ID REGISTER
Address=00D6h (Read Only)



MISCELANEOUS CONTROL/STATUS REGISTER
Address=00D0h (Read/Write)



LED CONTROL REGISTER
Address=00D7h (Read/Write)



AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
tSU1	Address Setup Time before Command	50		ns	
tH2	Address Hold Time after Command	50		ns	
tSU3	ADSEL Setup Time before Command	30		ns	
tH4	ADSEL Hold Time after Command	50		ns	
tH5	Read Data Invalid from End of Read	5		ns	
tH6	Write Data Hold Time	20		ns	
tD7	Real Time Controller Data Valid from Read		160	ns	
tSU8	Real Time Controller Write Data Setup Time	100		ns	
tD9	Asynchronous Controller Data Valid from Read		140	ns	
tSU10	Asynchronous Controller Write Data Setup Time	160		ns	
tD11	Timer Controller Data Valid from Read		160	ns	
tD12	Timer Controller Data Valid from ADDR		260	ns	
tSU13	Timer Controller Write Data Setup Time	160		ns	
tD14	Internal Registers Data Valid from Read		110	ns	
tSU15	Internal Registers Write Data Setup Time	100		ns	
tD16	Interrupt Controller Data Valid from Read		150	ns	
tSU17	Interrupt Controller Write Data Setup Time	100		ns	
tD18	Interrupt Vector from Interrupt Acknowledge		150	ns	
tD19	Interrupt Vector Invalid after Acknowledge	5		ns	

FIGURE 1. *READ TIMING DIAGRAM FOR TIMER CONTROLLER (8253)

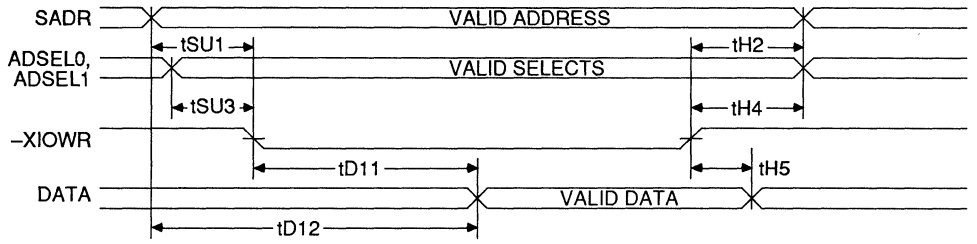


FIGURE 2. *WRITE TIMING DIAGRAM FOR TIMER CONTROLLER (8253)

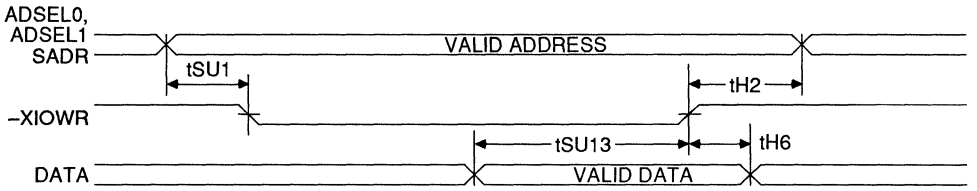


FIGURE 3. *READ TIMING DIAGRAM FOR ASYNCHRONOUS SERIAL COMMUNICATIONS CONTROLLER (8250A)

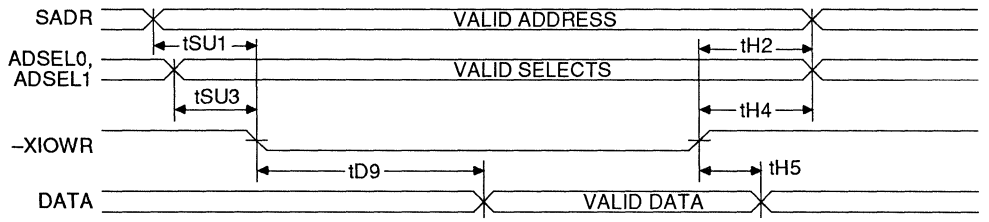
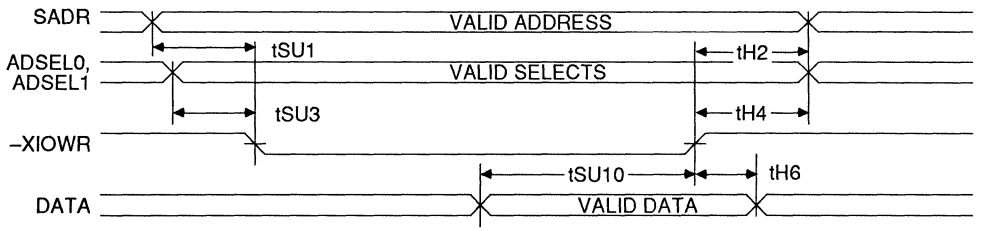


FIGURE 4. *WRITE TIMING DIAGRAM FOR ASYNCHRONOUS SERIAL COMMUNICATIONS CONTROLLER (8250A)



***Note:** Data Lines - Output Loading = 40 pF.

FIGURE 5. *READ TIMING DIAGRAM FOR INTERRUPT CONTROLLER (8259)

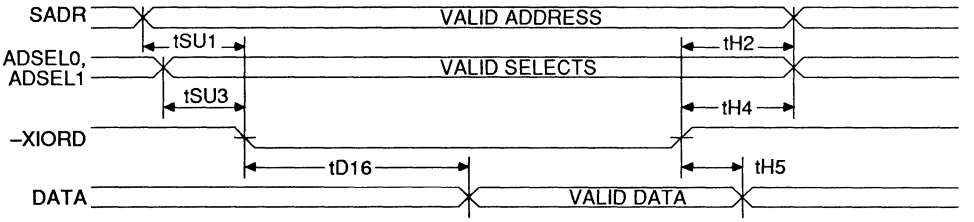


FIGURE 6. *WRITE TIMING DIAGRAM FOR INTERRUPT CONTROLLER (8259)

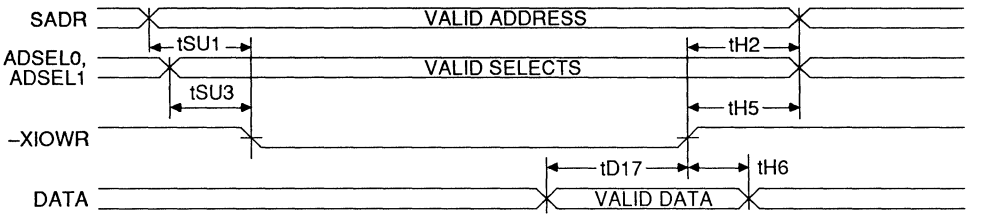


FIGURE 7. *INTERRUPT ACKNOWLEDGE TIMING DIAGRAM FOR INTERRUPT CONTROLLER (8259)

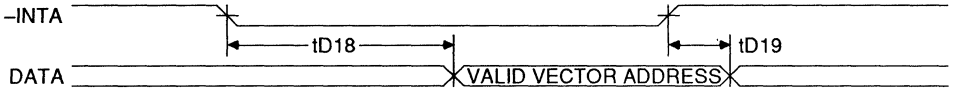
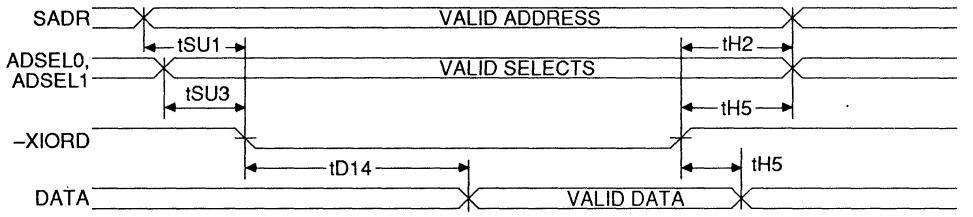


FIGURE 8. *READ TIMING DIAGRAM FOR INTERNAL REGISTERS



***Note:** Data Lines - Output Loading = 40 pF.

FIGURE 9. *WRITE TIMING DIAGRAM FOR INTERNAL REGISTERS

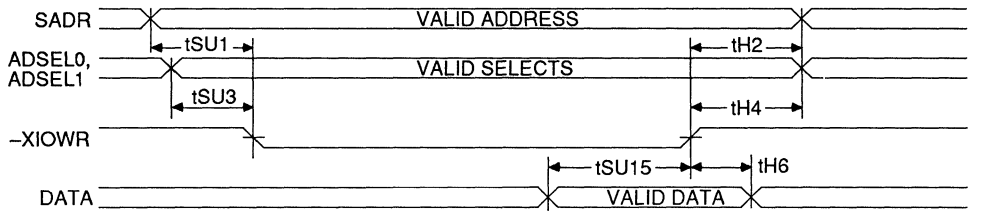


FIGURE 10. **TIMING DIAGRAM FOR FLOPPY OR HARD DISK CHIP SELECT

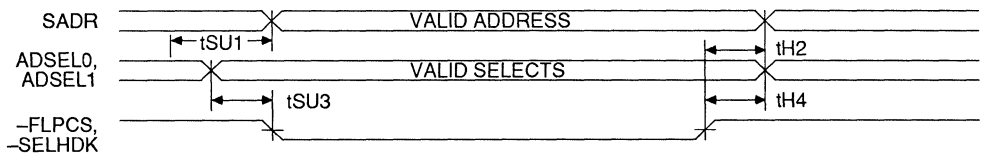


FIGURE 11. *READ TIMING DIAGRAM FOR REAL TIME CLOCK (58167A)

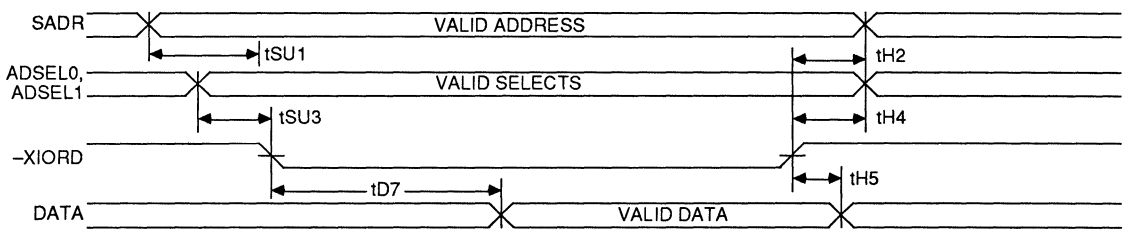
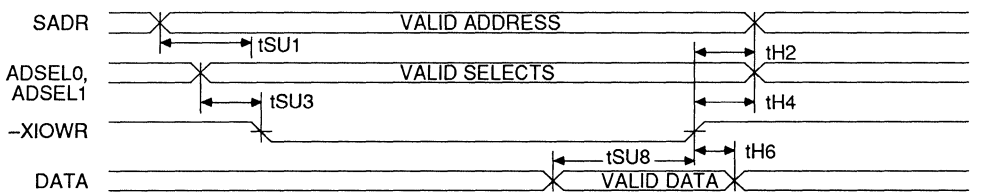


FIGURE 12. *WRITE TIMING DIAGRAM FOR REAL TIME CLOCK (58167A)



***Note:** Data Lines - Output Loading = 40 pF.
****Note:** FLPCSH - Output Loading = 20 pF. –SELHDK - Output Loading = 20 pF.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to VCC +0.3 V
Applied Output Voltage	−0.5 V to VCC +0.3 V
Applied Input Voltage	−0.5 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	Note
VOL	Output Low Voltage		0.45	V	Note
VIH	Input High Voltage	2.2	VCC + 0.5	V	Pins 16-19, 49, 94
VIH	Input High Voltage	2.0	VCC + 0.5	V	All Other Inputs*
VIL	Input Low Voltage	−0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	−150	10	µA	Pins 82-87
ILI	Input Leakage Current	−10	10	µA	All Other Inputs*
OLI	Output Leakage Current	−10	10	µA	
ICC	Operating Supply Current		40	mA	

Note: Output Current Driving Capabilities for VOH and VOL DC Parameters

IOH	IOL	VL82C032 Pins
−400 µA	20 mA	−LED, PD0-PD7
−400 µA	16 mA	J1DATA, J2DATA, J1CLOCK, J2CLOCK
−400 µA	10 mA	−INIT, −STROBE, −SELIN, −AUTOFD
−400 µA	8 mA	XD0-XD7, KEYLOCK, −SELHDK
−400 µA	4 mA	INTR, SPKOUT, −FLPCS, −XBFRD, TXD1, TXD2, −DTR1, −DTR2, −RTS1, −RTS2
−400 µA	2 mA	DRVTYPE, −PRE, −RD3F0, −RD3F1, −TIMER2

* RTCLKIN (Pin 56) is a crystal input and is not intended to conform to typical TTL input levels. For testing purposes it is driven to 4.0 V and 0.2 V for a logic high and low respectively.

NOTES: