VL82C031

SUPER XT-COMPATIBLE SYSTEM CONTROLLER

FEATURES

- Supports 8086 or V30 CPU at 8 MHz or 10 MHz zero wait state using 150 ns DRAMs
- Provides either DRAM or SRAM control
- Supports up to 8M bytes of expanded memory
- Supports 256K or 1M bit DRAMs on EMS memory
- Arbitrates the system bus among the CPU, DMA, math coprocessor, and DRAM memory refresh cycles
- Provides four channels of 8 MHz DMA as well as burst mode
- RAM pin available to select static or dynamic memory interface
- Power down mode for low power standby operation

DESCRIPTION

The VL82C031 provides the XT-compatible system with dual speed control, 8 MHz or 10 MHz, to operate the system at peak performance. The device also controls memory, I/O, parity, address paths, and data paths as well as handling four channels of direct memory access. The VL82C031 is available from VLSI Technology, Inc. in an industry-standard plastic 100-pin flatpack.

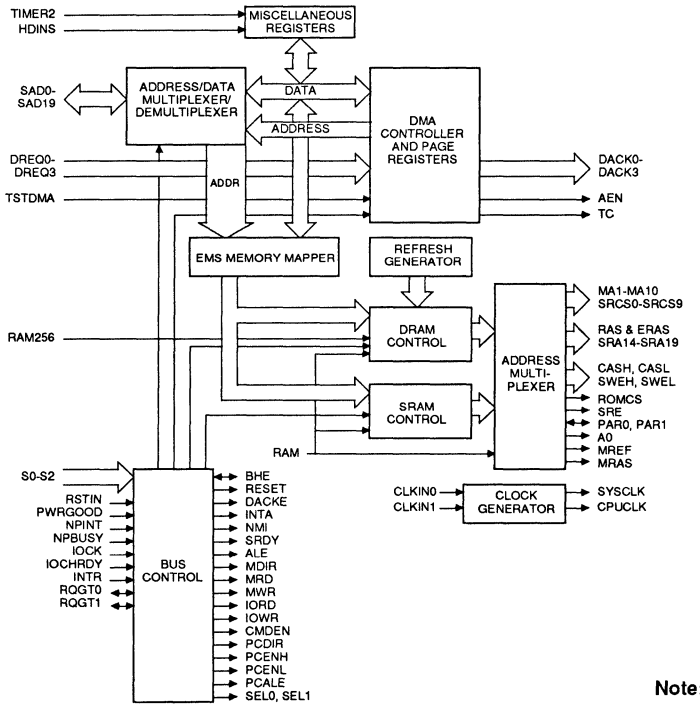
The CMOS VL82C031 is the System Controller device in the two-chip VLSI XT-compatible chip set. The other device is the VL82C032 I/O Controller.

The chip set integrates logic on XT-compatible systems. Further, while offering complete compatibility with the Super XT architecture, the VLSI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M bytes of memory using EMS (Expanded Memory Specification) 4.0, controls system speed as necessary for optimum performance, and supports a 16-bit memory data bus.

The chip can be brought to a power-down mode to conserve power. The chip can then be woke up from power-down mode by an external interrupt.

A third device, the VL82C037 VGA, Video Graphics Controller, can also be used in the Super XT-compatible system and provides high resolution graphics of up to 800 x 600 pixels with 16 colors. Graphic capabilities with this resolution are usually found only on more expensive systems.

BLOCK DIAGRAM

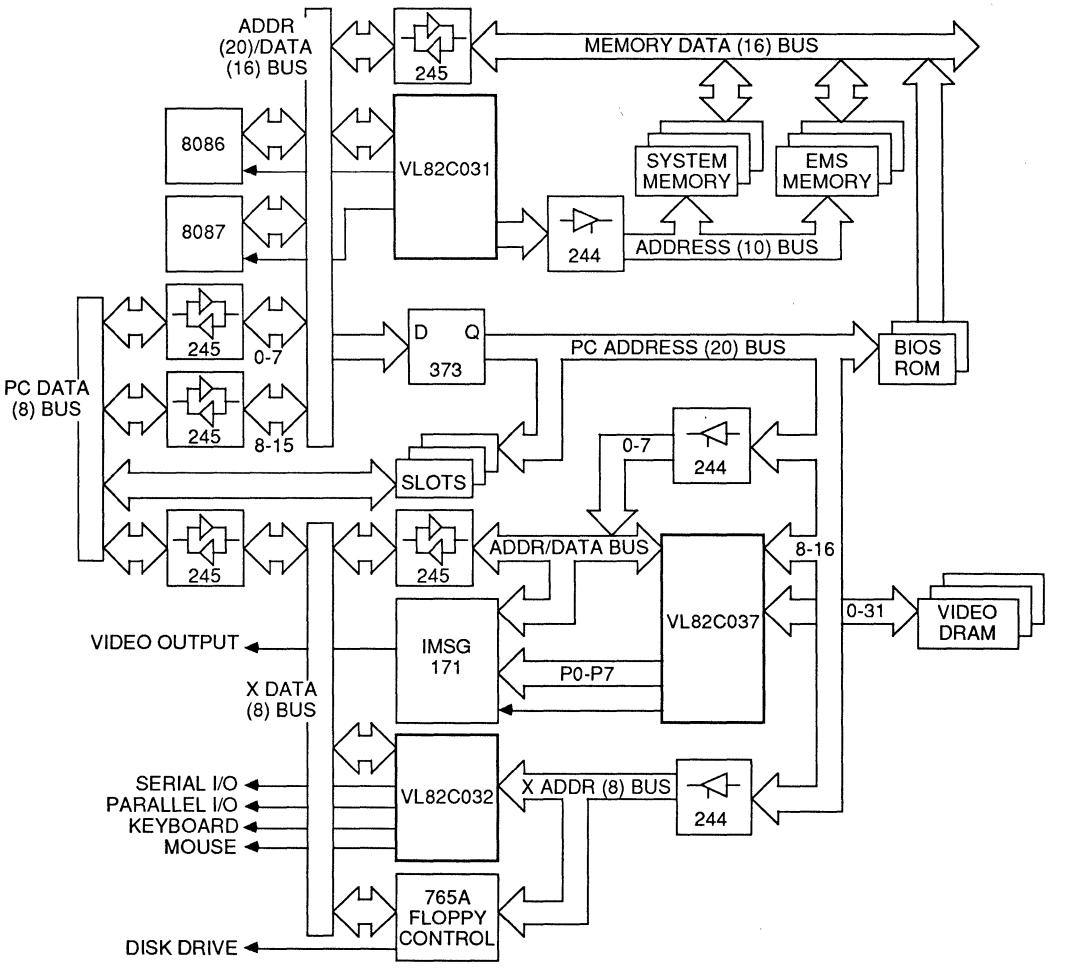


ORDER INFORMATION

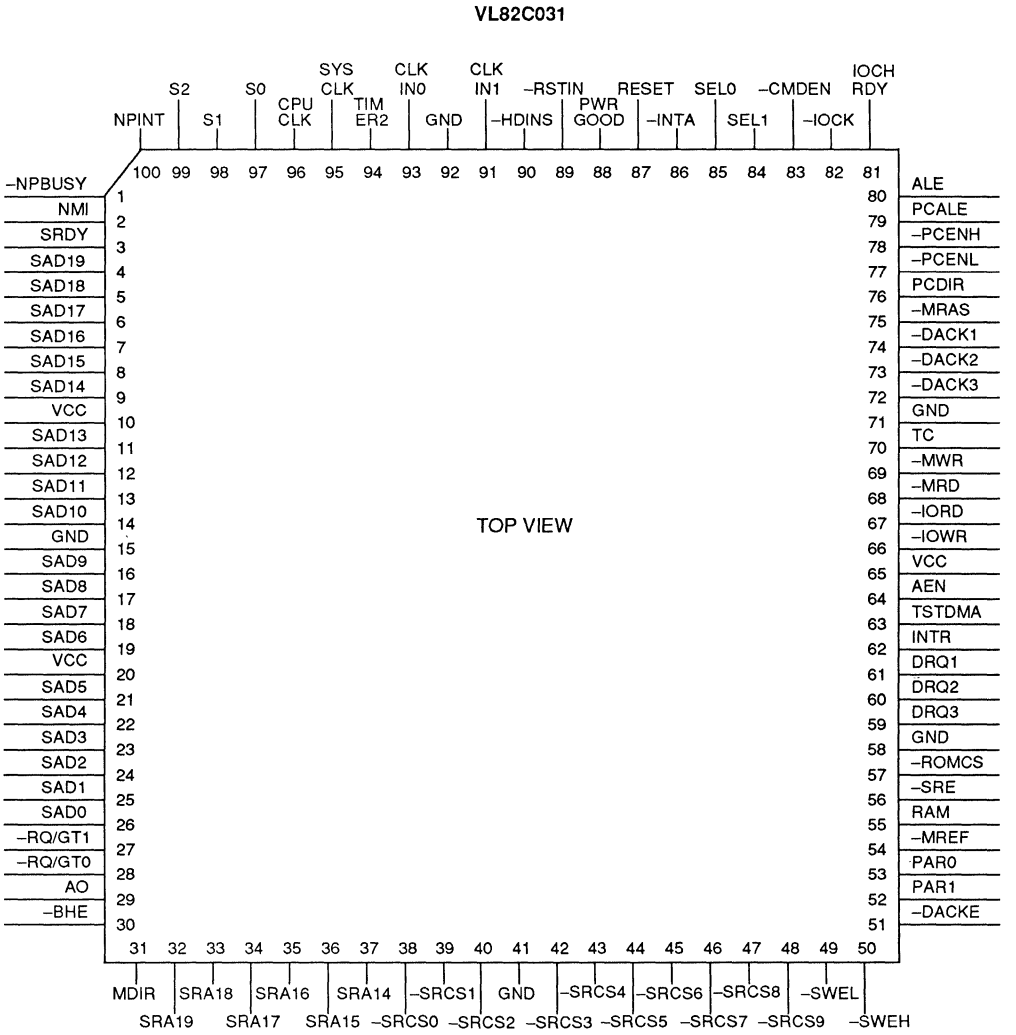
Part Number	Package
VL82C031-FC	Plastic Flatpack

Note: Operating temperature range is 0°C to +70°C.

SUPER XT-COMPATIBLE SYSTEM DIAGRAM (WITH VGA)



PIN DIAGRAM [When pin 55 (RAM) is tied low, SRAM configuration.]



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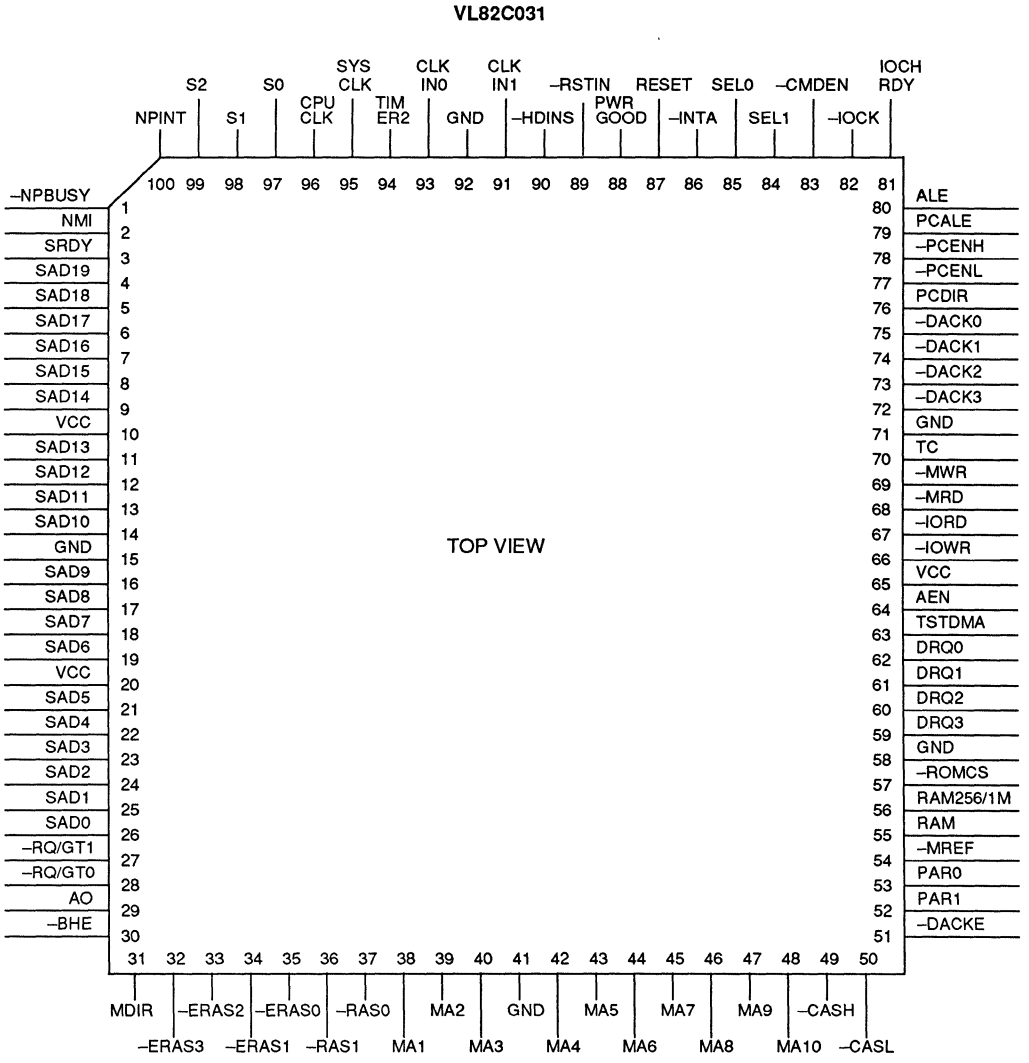
PIN DIAGRAM [When pin 55 (RAM) is tied high, DRAM configuration.]



SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low, SRAM configuration]

Signal Name	Pin Number	Signal Type	Signal Description
–NPBUSY	1	I	Busy - Is an active low signal connected directly to the –BUSY signal of NP8087 which is normally connected to the –TEST signal of the 8086 CPU. It is examined by the bus arbitrator logic internally to the VL82C031.
NMI	2	O	Non Maskable Interrupt - Is an active high signal to the CPU that there is an exception caused by one of the following: - memory parity error, - I/O channel check signaled from the PC bus, - 8087 interrupts (an unmasked exception has occurred).
SRDY	3	O	System Ready - This is an active high signal that acknowledges to the CPU or 8087 at t3 or tW before t4 time that a data transfer for either memory or I/O is complete.
SAD19-SAD16	4-7	I/O	Address Bus - These lines are the four most significant address lines for memory operation. They are input lines when the CPU or 8087 is in control. The chip starts driving these lines during DMA address time.
SAD15-SAD0	8, 9, 11-14, 16-19, 21-26	I/O	Address and Data Bus - These lines are a time multiplexed address and data bus corresponding to the AD15-ADO of 8086 and 8087 bus. The VL82C031 monitors these lines during the time the CPU or 8087 is in control of the bus. It will drive these lines during DMA address time.
–RQ/GT1	27	I/O	Request Grant Channel 1 - Is an active low pulse signal connected directly to –RQ/GT1 of the 8087. This signal is used by the chip to request the bus from the 8087. If the 8087 is not controlling the bus at that time, the request will relay through –RQ/GT0 of the 8087 which is connected to –RQ/GT1 of the CPU.
–RQ/GT0	28	I/O	Request Grant Channel 0 - Is an active low pulse signal connected directly to –RQ/GT0 of the CPU. This signal is used by the chip to request the bus from the CPU if there is no 8087, otherwise it is inactive.
A0	29	O	Address Line 0 - Is the latched version of address 0. It is used along with –BHE signal to distinguish 8/16 bit and odd/even byte operation.
–BHE	30	I/O	Byte High Enable - This is an active low signal used to enable data to the most significant half of the data bus (D15-D8). It is an input line when the CPU or 8087 is in control. The chip drives this signal during DMA time.
MDIR	31	O	Memory Direction - Controls memory write enable of memory devices and also the data direction of the transceiver between the CPU and system memory bus.
SRA16-SRA19	35-32	O	SRAM Address Bits 16-19 - If RAM is low, these bits drive an SRAM address decoder for the Expanded Memory option. The combination of SRA16-SRA19 is capable of selecting one of 15 32K X 8 SRAM banks organized as a word wide for a total of 960K bytes (15 banks of 64K each). Expanded memory is not selected if SRA16-SRA19 are 1111.
SRA14, SRA15	37, 36	O	SRAM Address Bits 14, 15 - If RAM is low, these are the two most significant address bits of the 32K X 8 SRAM.

–BHE	A0	Operation
0	0	Word (D15-D0)
0	1	Odd Byte (D15-D8)
1	0	Even Byte (D7-D0)
1	1	Not Used

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SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SRCS0- –SRCS9	38-40, 42-48	O	Static RAM Chip Select Bits 0-9 - If RAM is low, these are Static RAM Memory Chip Selects (active low). Each signal selects a bank of two 32K X 8 SRAM chips for a total of 640K bytes of system memory.
–SWEH, –SWEL	50, 49	O	SRAM Write Enable (High & Low) - If RAM is low, these are active low write enable signals for SRAM: - –SWEH for odd byte, - –SWEL for even byte.
–DACKE	51	O	DACK Enable - Is an active low control signal to enable either –DACK2 or –DACK3 to the on-board floppy and hard disk controllers respectively. This is a programmable signal based on the content of Chip Select Control Port 0065 (hex).
PAR0, PAR1	53, 52	I/O	Parity Bits 0-1 - Are the memory parity bits (odd type) for even and odd bytes of memory bank. Each parity bit is generated and written during a memory write operation. Each parity bit is checked and errors are reported by NMI to the system at the end of each memory cycle. PAR0 is the memory parity bit for even bytes. PAR1 is the memory parity bit for odd bytes.
–MREF	54	O	Memory Refresh - Is an active low signal indication of the refresh cycle. It is inhibited when RAM is low.
RAM	55	I	RAM Select - Is an input signal which indicates the memory type used in the system: - RAM = low = Static RAM, - RAM = high = Dynamic RAM.
–SRE	56	O	SRAM Read Enable - If RAM is low, it is an active low read enable signal for SRAM memory.
–ROMCS	57	O	ROM Chip Select - Is an active low signal used to enable the ROM BIOS to output data to the data bus.
DRQ1-DRQ3	61-59	I	DMA Request Bits 1-3 - Are asynchronous active high channel request inputs used by peripheral devices to obtain DMA service. –DACK will acknowledge the recognition of DRQ signals. These signals are compatible with the DRQ signals of the 8237 DMA controller.
INTR	62	I	Interrupt Signal - Is a positive edge signal to release the system from an idle state for power management.
TSTDMA	63	I	Test DMA Function - This signal is used for testing purposes of the internal DMA controller. It should be tied low.

Signal	Memory Space
–SRCS0	00000 - 0FFFF
–SRCS1	10000 - 1FFFF
–SRCS2	20000 - 2FFFF
–SRCS3	30000 - 3FFFF
–SRCS4	40000 - 4FFFF
–SRCS5	50000 - 5FFFF
–SRCS6	60000 - 6FFFF
–SRCS7	70000 - 7FFFF
–SRCS8	80000 - 8FFFF
–SRCS9	90000 - 9FFFF

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
AEN	64	O	Address Enable - Is an active high signal during the DMA cycle to disable any I/O devices from the I/O channel to allow DMA transfers to take place.
–IOWR	66	O	I/O Write Command - Is an active low signal to instruct an I/O device to read the data present on the data bus.
–IORD	67	O	I/O Read Command - Is an active low signal to instruct an I/O device to drive its data on the data bus.
–MRD	68	O	Memory Read Command - Is an active low signal to instruct the memory to drive its data on to the data bus.
–MWR	69	O	Memory Write Command - Is an active low signal to instruct the memory to store the data present on the data bus.
TC	70	I/O	Terminal Count - Is an active high pulse signal when any DMA transfer is completed. It can be driven from the I/O channel to terminate a current DMA cycle.
–DACK1- –DACK3	74-72	O	DMA Acknowledge Bits 1-3 - Are active low signals to notify the requesting peripherals when one has been granted a DMA cycle. These signals are compatible with the DACK signals of the 8237 DMA controller.
–MRAS	75	O	Memory Signal Timing - Is an active low control signal to indicate a system memory cycle.
PCDIR	76	O	PC Data Bus Direction - Is the direction signal to the data transceiver between the CPU and PC data bus: - high means the CPU drives the PC data bus (write cycle), - low means the PC drives the CPU data bus (read cycle).
–PCENL	77	O	PC Data Byte Low Bus Enable - Is the active low control signal to enable the data buffer (D7-D0) between the CPU and PC data bus.
–PCENH	78	O	PC Data Byte High Bus Enable - Is the active low control signal to enable the data buffer (D15-D8) between the CPU and PC data bus.
PCALE	79	O	PC Address Latch Enable - Is an active high pulse active during t1 of any bus cycle. It is similar to the ALE signal except that this signal is active high throughout the DMA cycle.
ALE	80	O	Address Latch Enable - Is an active high pulse active during t1 of any bus cycle including DMA and memory refresh cycles. The CPU address should be latched using the ALE falling edge.
IOCHRDY	81	I	I/O Channel Ready - Is an active high ready signal from an I/O channel. Memory or I/O devices can pull this signal low to lengthen memory or I/O cycles. For every system clock cycle this signal is low, one wait state is added.
–IOCK	82	I	I/O Channel Check - This signal should be pulled low for at least two system clock cycles to indicate an uncorrectable error on an I/O channel. This signal causes a Non Maskable Interrupt if NMI is enabled.
–CMDEN	83	O	Command Enable - Is the active low control signal to enable the command buffer going to the I/O channel bus (PC Bus). It is used to prevent bus contention between the I/O devices that share the same address space in the X bus and in the I/O channel bus.

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SEL0,SEL1	85, 84	O	Select Function (0-1) - These are special select decoders for address range according to the following table:
–INTA	86	O	Interrupt Acknowledge - This pin is an active low signal used to enable the interrupt controller's interrupt-vector data on to the data bus.
RESET	87	O	Reset - Is an active high signal synchronized to the system clock to reset the CPU and system.
PWRGOOD	88	I	Power Good - Is an active high Schmitt Trigger input signal (TTL level of 2.4 to 5.25 Vdc during normal operation, or an inactive level of 0.0 to 0.4 Vdc) coming from a power supply to indicate that power is stable.
–RSTIN	89	I	Reset Input - Is an active low signal which is used to generate the RESET signal. The VL82C031 provides a Schmitt Trigger input so that an RC connection can be used to establish the power on reset of proper duration.
–HDINS	90	I	Hard Disk Installed - Is the status signal that the hard disk is installed on the system. This can be read at I/O port 62 bit 2.
CLKIN1	91	I	Clock Input 1 - Is a 30 MHz TTL clock input with 40/60% duty cycle. It is used for a system clock with the CPU running at 10 MHz. It should be pulled high if there is no clock source to this pin.
CLKIN0	93	I	Clock Input 0 - A 24 MHz TTL clock input with 40/60% duty cycle. It is used for the system clock with the CPU running at 8 MHz, internal DMA control, and memory refresh timing.
TIMER2	94	I	Timer2 Status - Is the status signal on the 8253 Timer Channel 2 which comes from VL82C032. This is can be read at I/O port 62 bit 5.
SYSCLK	95	O	System Clock - Is the MOS driven clock signal to the 8087 and system. It has a 33% duty cycle (67-low, 33-high).
CPUCLK	96	O	CPU Clock - Is a MOS driven clock signal to 8086 or NEC V30 CPU. The clock speed can be selected through a special register. The duty cycle of CPU clock is 33% (67-low, 33-high).
S2-S0	99-97	I	System Status - These are Schmitt Trigger input signals used to decode different CPU or 8087 operations.

SEL1	SEL0	Range
0	0	Don't Care
0	1	A15-A10 = 0 (I/O)
1	0	ROM
1	1	Video RAM

S2-S0	Operation
000	Interrupt Acknowledge
001	I/O Read
010	I/O Write
011	Halt
100	Memory Read (fetch)
101	Memory Read (data)
110	Memory Write
111	Passive

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
NPINT	100	I	8087 Numerical Processor Interrupt - An active high signal that indicates that an unmasked exception has occurred during numeric instruction execution when 8087 interrupt is enabled.
VCC	65, 20, 10		Power - +5 V
GND	92, 71, 41, 58, 15		Ground

SIGNAL DESCRIPTIONS [For pins which operate differently in DRAM configuration (Pin 55 tied high)]

Signal Name	Pin Number	Signal Type	Signal Description
–ERAS0- –ERAS3	35-32	O	EMS Row Address Strobe Bits 0-3 - If RAM is high, these are active low –RAS signals for Expanded Memory option to the system:
–RAS0, –RAS1	37, 36	O	Row Address Strobe Bits 0-1 - If RAM is high, these are active low control signals to the 640K byte DRAM system memory to inform the memory that a row address is present on the address bus. –RAS0 is for the first 128K and –RAS1 is for the next 512K of memory.
MA1-MA10	38-40, 42-48	O	Memory Address Bit 1-10 - If RAM is high, these are time multiplexed row and column memory address lines for 1M memory chips (for 256K memory chips MA10 is not used.)
–CASH- –CASL	49 ,50	O	Column Address Strobe (High & Low) - If RAM is high, these are active low control signals to the on-board DRAM system and EMS memory to signal that a column address is present on the address bus: - –CASH for odd byte [D(15-8)], - –CASL for even byte [D(7-0)].
–MREF	54	O	Memory Refresh - Is the active low signal indication of the refresh cycle. It is inhibited when RAM is low.
RAM	55	I	RAM Select - Is an input signal to tell the chip of the memory type used in the system: - RAM = low = Static RAM, - RAM = high = Dynamic RAM.
RAM256/1M	56	I	256K or 1M - If RAM is high, this is the signal which informs the chip of the memory type used in expanded memory: - low means 1M chips, - high means 256K chips.

	Pin	Odd	Even
–ERAS0	35	256K (1M)	256K (1M)
–ERAS1	34	256K (1M)	256K (1M)
–ERAS2	33	256K (1M)	256K (1M)
–ERAS3	32	256K (1M)	256K (1M)

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SIGNAL DESCRIPTIONS (DRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
DRQ0-DRQ3	62-59	I	DMA Request Bits 0-3 - Are asynchronous active high channel request inputs used by peripheral devices to obtain DMA service. –DACK will acknowledge the recognition of DRQ signals. These signals are compatible with the DRQ signals of the 8237 DMA controller.
–DACK0- –DACK3	75-72	O	DMA Acknowledge Bits 0-3 - Are active low signals to notify the requesting peripherals when one has been granted a DMA cycle. These signals are compatible with the DACK signals of the 8237 DMA controller.

FUNCTIONAL DESCRIPTION

SYSTEM MEMORY AND I/O MAP

The 8086/V30 supports 16-bit operations with 20-bit addressing to directly access up to 1M byte of memory space. The system memory and an On-board Expanded Memory (if it's enabled) are byte and/or word accessible. Memory is mapped in Table 1.

MEMORY CONTROL UNIT

VL82C031 offers either Dynamic or Static RAM memory control depending on the RAM input signal with zero wait states for 150 ns memory access.

If the "RAM" pin is strapped high (to VCC), the VL82C031 will generate on-board DRAM memory control signals. It supports 640K bytes of system memory using 64K X 4 DRAM for the first 128K bytes and 256K X 1 DRAM for the next 512K bytes of memory. In addition to 640K bytes, the VL82C031 also supports EMS 4.0 which makes multi-tasking possible. The EMS logic will support either 256K or 1M byte memory chips depending on how the RAM256/1M input signal is strapped. The EMS logic will control on-board memory up to 2M bytes if 256K memory is used and up to 8M bytes if 1M chips are used (see RAM256/1M input definition in the VL82C031 Signal Descriptions).

If the "RAM" pin is strapped low (to Ground), the VL82C031 will generate SRAM memory control. It supports 640K bytes of system memory using 32K X 8 SRAM chips. It also supports an EMS SRAM up to 960K (1M minus 64K) bytes of 32K X 8 type memory. It provides four address lines (SRA16-SRA19) that can select one out of 15 banks of memory (64K bytes each). When EMS SRAM is not accessed, SRA16-SRA19 will be all 1's so only 15 banks can be selected.

The Memory Control Unit has the following five functions:

1. System Memory Control
2. EMS Control
3. Memory Refresh Control
4. Memory Parity Check and Generator
5. Row and Column Address Generator

SYSTEM MEMORY CONTROL

FOR DRAM CONTROL: The system memory controller generates RAS signals for 640K of read/write memory:

- –RAS0 is for the first 128K of memory,
- –RAS1 is for the next 512K of memory.

FOR SRAM CONTROL: The system memory controller generates 10 SRAM chip selects (–SRCS0-SRCS9) as shown in Table 2 and read/write control signals (–SRE, –SWEH, –SWEL).

TABLE 1. FUNCTIONS

Hex Address	Description	
00000 - 1FFFF	128K byte: 1st bank #1	640K System Memory
20000 - 2FFFF	64K byte: 2nd bank #2	
30000 - 3FFFF	64K byte: 2nd bank #3	
40000 - 4FFFF	64K byte: 2nd bank #4	
50000 - 5FFFF	64K byte: 2nd bank #5	
60000 - 6FFFF	64K byte: 2nd bank #6	
70000 - 7FFFF	64K byte: 2nd bank #7	
80000 - 8FFFF	64K byte: 2nd bank #8	
90000 - 9FFFF	64K byte: 2nd bank #9	
A0000 - BFFFF	128K byte: Video Buffer	
C0000 - EFFFF	192K byte: Reserved for BIOS on I/O Channel.	
F0000 - FFFFF	64K byte: System ROM	

TABLE 2. MEMORY

Signal	Memory Space
–SRCS0	00000 - 0FFFF
–SRCS1	10000 - 1FFFF
–SRCS2	20000 - 2FFFF
–SRCS3	30000 - 3FFFF
–SRCS4	40000 - 4FFFF
–SRCS5	50000 - 5FFFF
–SRCS6	60000 - 6FFFF
–SRCS7	70000 - 7FFFF
–SRCS8	80000 - 8FFFF
–SRCS9	90000 - 9FFFF

The controller can allocate system memory through the Planar RAM Control Register at Port 006B. If the first 128K bytes of memory are not installed or bad, the system can remap the next 512K bytes over. Also, each 64K block of the second bank (except the first two blocks) can be enabled or disabled so the system can allocate memory between system memory and expanded memory.

If bit 0 of the Planar RAM register is 0, –RAS0 or –SRCS0-SRCS1 will be active at memory space 00000 - 1FFFF (128K bytes), and –RAS1 or –SRCS2-–SRCS9 will be active at memory space 20000 - 9FFFF (512K byte) for 640K bytes of system memory .

If bit 0 is 1, memory bank 0 is disabled (–RAS0 or –SRCS0- –SRCS1), and the physical memory at addresses 80000 - 9FFFF will be mapped to memory space 00000 - 1FFFF. Thus, –RAS1 or –SRCS2- –SRCS9 will be active in memory space 00000 - 7FFFF for 512K bytes of system memory.

The format of the Planar RAM Control/ Status Register is as follows:

Planar RAM Control Register: I/O Port 006B (hex) R/W:

Bit	Function
7	Parity Check Pointer 1 = Lower 128K failed 0 = Upper 512K failed
6	DIS/EN– RAM, 90000 - 9FFFF
5	DIS/EN– RAM, 80000 - 8FFFF
4	DIS/EN– RAM, 70000 - 7FFFF
3	DIS/EN– RAM, 60000 - 6FFFF
2	DIS/EN– RAM, 50000 - 5FFFF
1	DIS/EN– RAM, 40000 - 4FFFF
0	MAP/UNMAP– Low Memory

At power-on or reset, this port is 00.

If the EMS memory happens to be selected in the system memory space, –RAS0 and –RAS1 or –SRCS0-–SRCS9 will be blocked. Both –RAS0 and –RAS1 will be asserted during RE-FRESH. REFRESH is inhibited if "RAM" is low.

Bit 7 of Planar RAM Control Register will be set (1) or clear (0) according to the most recent parity bit error:

– If the current memory read cycle is in the first 128K memory and caused a parity error, bit 7 will be set.
– If the current memory read cycle is in the next 512K memory and caused a parity error, bit 7 will be cleared.
– If there is no parity error, bit 7 will remain unchanged.
– Writing a 1 to bit 7 of this port will reset this bit. Writing a 0 to this bit has no effect.

This feature is primarily intended for use in memory testing and is not particularly useful for post-mortem diagnostics.

EMS CONTROL

The EMS Control consists of EMS Current Map, EMS Alternate Map, and the EMS RAS generator.

The Current and Alternate Maps are 36 word by 10 bit register files each containing an enable bit and the physical address bits 22-14 of the EMS memory. The memory space is logically broken down to 64 blocks of 16K bytes each. However, the first 256K of system memory (00000 - 3FFFF), Video memory (40000 - BFFFF), and ROM BIOS (F0000 - FFFFF) are reserved. That leaves two areas of memory: 40000 - 9FFFF and C0000 - EFFFF mappable to EMS. Each block of 16K bytes can be mapped to any of n blocks of EMS memory. (If RAM256/1M is high, n = 128. If RAM256/1M is low, n = 512.) EMS can access up to 2M or 8M bytes of DRAM depending on the state of RAM256/1M.

If SRAM is used (i.e. Pin 55 is tied low) the maximum EMS memory will be 1M minus 64K (960K) bytes of SRAM, that is n = 60.

The EMS Current Map is a 36 word by 10 bit register file that translates A14-A19 during memory cycles to an EMS memory address. The EMS Current Memory Map can be accessed through three I/O ports:

CMPR - Current Map Pointer Register
8-bit I/O R/W
CMDR - Current Map Data Register
16-bit I/O R/W

The CPU performs an I/O write to CMPR with a pointer to the current map. After that, the CPU performs I/O reads or writes to CMDR.

The CMPR and CMDR formats are:

CMPR: I/O Port 0011 R/W:

Bit	Function
7, 6	Not Used
5-0	Current Map Ponter

CMDR: I/O Port 0012 R/W word access only:

Bit	Function
15-10	Not Used
9	Map Address 22 for EMS Memory
8	Map Address 21 for EMS Memory
7	EN/DIS-
6	Map Address 20 for EMS Memory
5	Map Address 19 for EMS Memory
4	Map Address 18 for EMS Memory
3	Map Address 17 for EMS Memory
2	Map Address 16 for EMS Memory
1	Map Address 15 for EMS Memory
0	Map Address 14 for EMS Memory

The type of memory and map address bits used in EMS are determined by the RAM and RAM256/1M input pins as shown in Table 3.

TABLE 3. MEMORY CONFIGURATION OPTIONS

RAM	256/1M	Type of Memory	Map Bits Used
0	X	32K X 8 SRAM	14-19
1	0	1M DRAM	14-22
1	1	256K DRAM	14-20

X = Don't Care

When RAM is low, and during EMS memory access, SRA14-SRA19 are identical to the map address. SRA14-SRA19 are all high if the access is not in EMS memory.

CMDR bit 7: EN/DIS- is used to enable or disable mapping of the logical memory address space to the EMS memory area. If this bit is set to 1, it will use the map address 21-14 during the memory access time to map to the EMS memory, otherwise it will be unmapped and either system memory or memory on the I/O channel will be accessed.

The EMS Alternate Map is a 36 word by 10-bit register file that translates A14-A19 during DMA memory cycles to the EMS memory. The EMS Alternate Memory Map can be accessed through three I/O ports:

AMPR - Alternate Map Pointer Register
8-bit I/O R/W
AMDR - Alternate Map Data Register
16-bit I/O R/W

The CPU performs an I/O write to AMPR with a pointer to the alternate map. After that, the CPU performs I/O reads or writes to AMDR.

The AMPR and AMDR formats are:

AMPR: I/O Port 0015 R/W:

Bit	Function
7, 6	Not Used
5-0	Alternate Map Pointer

AMDR: I/O Port 0016 R/W word access only:

Bit	Function
15-10	Not Used
9	Map Address 22 for EMS Memory
8	Map Address 21 for EMS Memory
7	EN/DIS-
6	Map Address 20 for EMS Memory
5	Map Address 19 for EMS Memory
4	Map Address 18 for EMS Memory
3	Map Address 17 for EMS Memory
2	Map Address 16 for EMS Memory
1	Map Address 15 for EMS Memory
0	Map Address 14 for EMS Memory

The type of memory and map address bits used in EMS are determined by the same system as with the current map. See Table 3.

The EMSEN I/O port enables or disables the EMS Current or Alternate Memory Map during CPU or NPU accesses:

EMSEN: I/O Port 0010 R/W:

Bit	Function
7-2	Not Used
1	EN/DIS- Alternate Map
0	EN/DIS- Current Map

Bit 0 and 1 of this port are Master EMS Enable bits used to enable or disable the EMS memory access function during the CPU or NPU memory access cycles. Writing a 1 to the EMSEN port bit 0 and/or bit 1 enables the EMS Current Map and/or Alternate Map to function. Otherwise, the EMS memory is not accessible. However, the EMS Current and Alternate Memory Maps are always accessible. If both bit 0 and 1 are set to 1's, the Current Memory Map will be used. See Table 4.

If one of the maps is selected but the EN/DIS- bit for the current page is 0, the memory access will go to CPU system memory, or the I/O channel if that address space is disabled through the Planar RAM Control Register.

The EMS RAS signals are always generated during memory refresh. At power-on or reset, bits 0 and 1 are 0's.

EMDMA is an I/O port used to tag any DMA channel to the Current or Alternate Map access during the DMA cycle:

EMDMA I/O Port 0014 R/W:

Bit	Function
7	EMCDMA3 : EN/DIS- Current Map during DMA Channel 3.
6	EMCDMA2 : EN/DIS- Current Map during DMA Channel 2.
5	EMCDMA1 : EN/DIS- Current Map during DMA Channel 1.
4	EMCDMA0 : EN/DIS- Current Map during DMA Channel 0.
3	EMADMA3 : EN/DIS- Alternate Map during DMA Channel 3.
2	EMADMA2 : EN/DIS- Alternate Map during DMA Channel 2.
1	EMADMA1 : EN/DIS- Alternate Map during DMA Channel 1.
0	EMADMA0 : EN/DIS- Alternate Map during DMA Channel 0.

There are four pairs of bits: 0,4; 1,5; 2,6; 3,7 that are related directly to each channel of the DMA in map selection

TABLE 4. GLOBAL EMS MAPPING

EMSEN Bit 1	EMSEN Bit 0	Map of EMS Memory Access During CPU or NPU Access cycles
0	0	None
0	1	Current Map
1	0	Alternate Map
1	1	Current Map

TABLE 5. EMS DMA ASSIGNMENT

EMDMA Bits 0,4; 1,5; 2,6; 3,7	Map of Memory Access During DMA Cycles
0, 0	None (map to system memory or I/O channel)
1, 0	Alternate Map
0, 1	Current Map
1, 1	Alternate Map

At power-on or reset, EMDMA = 00.

during each DMA cycle. The function of those bits are defined in Table 5.

If one of the maps is selected but the EN/DIS- bit for the current page is 0, the memory access will go to CPU system memory, or the I/O channel if that address space is disabled through the Planar RAM Control Register.

The EMS RAS Generator takes the content of CMDR or AMDR during memory access and generates the EMS RAS signals:

- ERAS0 : For EMS Bank 0.
- ERAS1 : For EMS Bank 1.
- ERAS2 : For EMS Bank 2.
- ERAS3 : For EMS Bank 3.

EMST: The EMS Parity Status Port Register is an eight bit I/O read only port used to identify the source of EMS parity errors if the EMS function is enabled:

EMST: I/O Port 0018 Read:

Bit	Function
7	EMSERR : EMS memory parity error.
6	Not Used
5	ODDBYTE : Odd byte is bad, if EMSERR is set.
4	EVENBYTE : Even byte is bad, if EMSERR is set.
3	EMSBNK3 : EMS memory bank 3 is bad, if EMSERR is set.
2	EMSBNK2 : EMS memory bank 2 is bad, if EMSERR is set.
1	EMSBNK1 : EMS memory bank 1 is bad, if EMSERR is set.
0	EMSBNK0 : EMS memory bank 0 is bad, if EMSERR is set.

EMST: I/O Port 0018 Write:

Bit	Function
7	EN/DIS- : EMS memory parity error.
6	Not Used
5	EN/DIS- : Odd parity byte, if EMSERR is set.
4	EN/DIS- : Even parity byte, if EMSERR is set.
3	EN/DIS- : EMS memory parity bank 3, if EMSERR is set.
2	EN/DIS- : EMS memory parity bank 1, if EMSERR is set.
1	EN/DIS- : EMS memory parity bank 1, if EMSERR is set.
0	EN/DIS- : EMS memory parity bank 0, if EMSERR is set.

Writing 0 to these bits will reset the corresponding parity bits to 0.

At power-on or reset, EMST = 00.

The mapping registers are implemented internally as static RAM register files, and can be disabled to reduce power consumption for applications such as laptop computers. This is done by writing a 1 to I/O Port IEh to enable the funtion, and then writing a 1 or 0 to I/O Port 1Ch to enable or disable the register banks, respectively. Reading I/O Port 1Ch at this point will disable the register banks and stop the CPUCLK output. An active signal on the INTR input (pin 62) will then restart the CPU clock. During the shutdown period the SYSCLK output continues to run.

CLOCK CONTROL

The speed and duty cycle of the clock outputs can be controlled through the Clock Control Register which resides at I/O Port 19h.

Clock Control: I/O Port 0019 R/W:

Bit	Function
7-3	Not Used
2	CPUCLK Duty Cycle - 0 = 33%, 1 = 50%
1	Divider Select - 0 = ÷6, 1 = ÷3
0	Clock Select - 0 = CLKIN0, 1 = CLKIN1

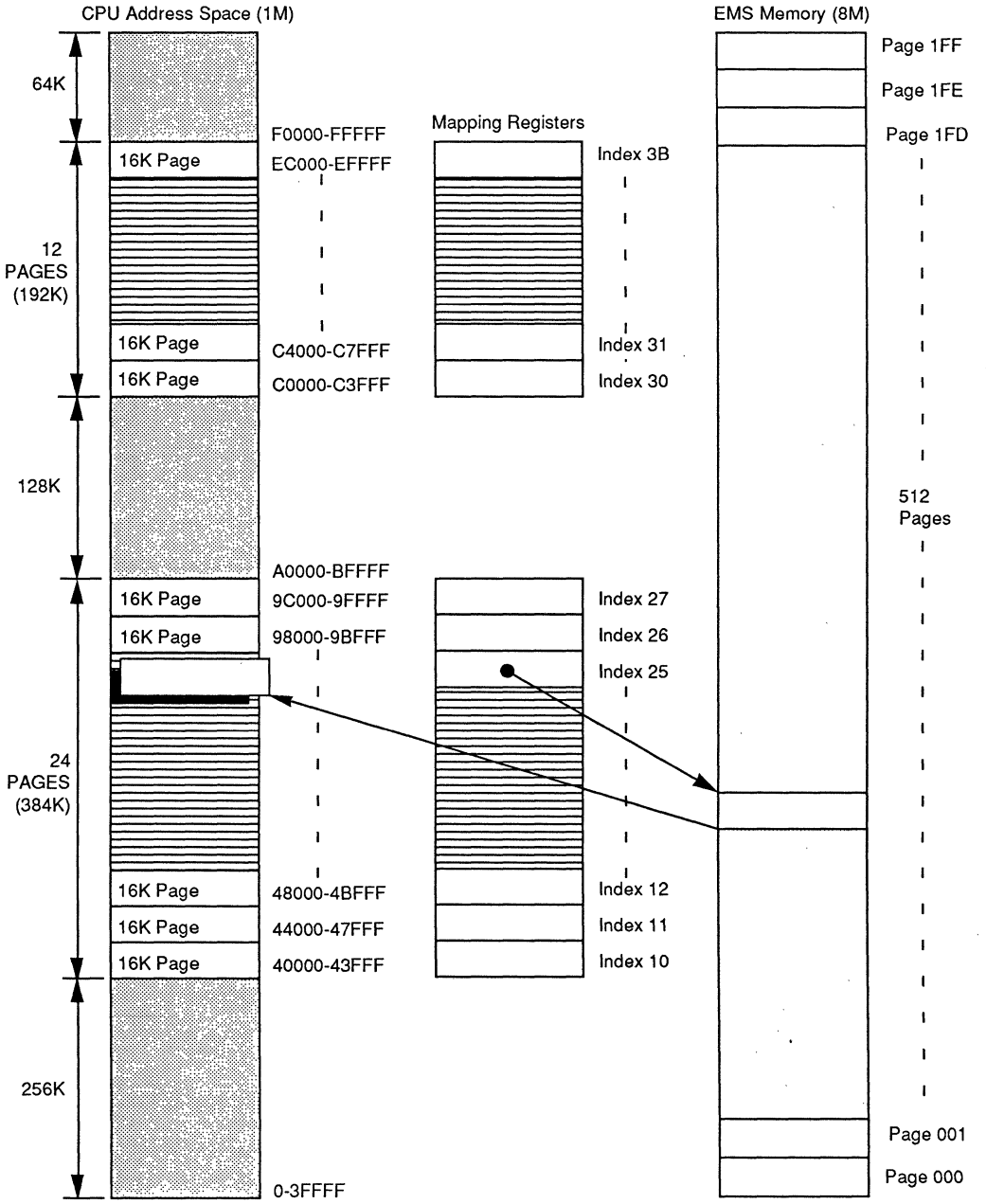
Both of the clock outputs (CPUCLK and SYSCLK) are affected by clock input and clock divider selection. Only the CPUCLK is affected by duty cycle selection.

5

VL82C031 I/O MAP

I/O Address	Function	Response
0000 - 000F	DMA Controller	R/W
0010 - 001F	System Control and Status Group 1	R/W
006B	Planar RAM Control	R/W
0081 - 0087	DMA Page Registers	R/W
03B0 - 03DF	Video System	On-Board Decoder

FIGURE 1. EMS MAPPING REGISTERS



MEMORY REFRESH CONTROL

The Memory Refresh Timer generates a request every 15.6 µs to the Refresh Controller. Once the Refresh Controller grants the cycle (–MREF is asserted), it outputs the ALE, PCALE, and –MRD signals. The minimum refresh cycle is five system clocks for a system running at 8 MHz or six system clocks for a system running at 10 MHz.

The Memory Refresh Address Generator drives all 20 address lines through the CPU bus during memory refresh cycle time (–MREF is low). Address 0-8 comes from a 9-bit binary counter (which will increment at the end of the cycle), and A9-A19 is driven low during the memory refresh cycle.

DMA CONTROL

DMA Control consists of two blocks:

- 8237-Compatible DMA Controller
- DMA Page Registers

The DMA Controller is a four channel DMA operating at 8 MHz which supports byte (8-bits) transfer operations between memory and peripherals. Its function is equivalent to the 8237 DMA chip. The DMA channels are assigned as shown in Table 6.

Each channel can transfer data throughout the 1M byte system address space up to 64K bytes at a time. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller
Address	A19 ◄——► A16	A15 ◄—► A0

Note: The addressing signal, 'byte high enable' (–BHE), is generated by inverting address line A0.

Three DMA channels (1, 2, 3) are available on the I/O channel. The 8237 DMA controller command code addresses are shown in Table 8.

DMA PAGE REGISTER

DMA Page Registers can be accessed through four 8-bit I/O ports. These ports are read/write and only data bits 0-3 are significant. Table 7 shows the addresses for the page registers.

Addresses for all DMA channels cannot increase or decrease through page boundaries (64K bytes).

TABLE 6. DMA CHANNELS

Channel	Assignment
Channel0: DRQ0	Reserved
Channel1: DRQ1	Not Used
Channel2: DRQ2	Diskette
Channel3: DRQ3	Fixed Disk

TABLE 7. PAGE REGISTERS

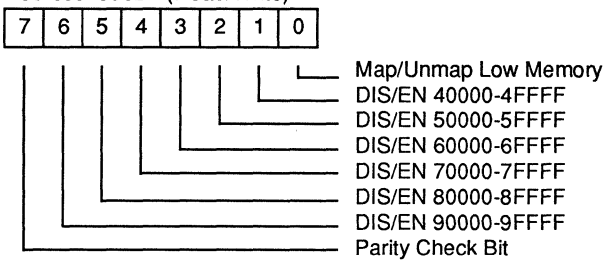
Page Register	I/O Address (In Hex)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082

TABLE 8. DMA CONTROLLER REGISTER FUNCTIONS

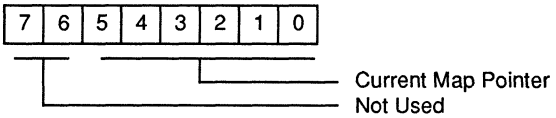
I/O Address (In Hex)	Register Function
0000	Channel 0 Base and Current Address Register
0001	Channel 0 Base and Current Word Count
0002	Channel 1 Base and Current Address Register
0003	Channel 1 Base and Current Word Count
0004	Channel 2 Base and Current Address Register
0005	Channel 2 Base and Current Word Count
0006	Channel 3 Base and Current Address Register
0007	Channel 3 Base and Current Word Count
0008	Read Status Register/Write Command Register
0009	Write Request Register
000A	Write Single Mask Register Bit
000B	Write Mode Register
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Register/Write Master Clear
000E	Clear Mask Register
000F	Write All Mask Register Bits

REGISTER BIT DIAGRAMS

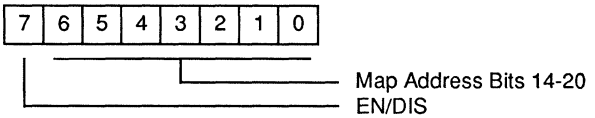
PLANAR RAM CONTROL REGISTER
Address=006Bh (Read/Write)



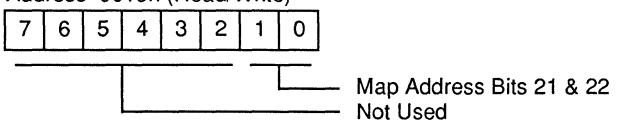
CURRENT MAP POINTER REGISTER
Address=0011h (Read/Write)



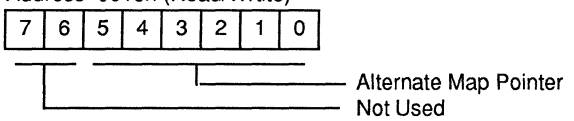
CURRENT MAP DATA REGISTER LOW
Address=0012h (Read/Write)



CURRENT MAP DATA REGISTER HIGH
Address=0013h (Read/Write)

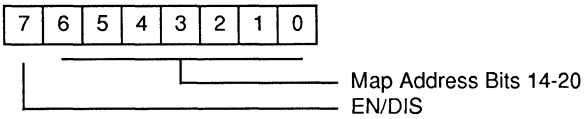


ALTERNATE MAP POINTER REGISTER
Address=0015h (Read/Wrtite)

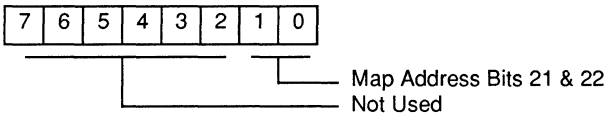


REGISTER BIT DIAGRAMS (Cont.)

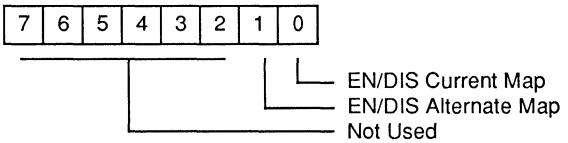
ALTERNATE MAP DATA REGISTER LOW
Address=0016h (Read/Write)



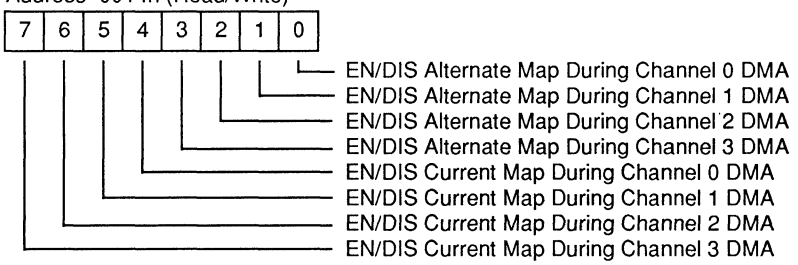
ALTERNATE MAP DATA REGHISTER HIGH
Address=0017h (Read/Write)



EMS ENABLE REGISTER
Address=0010h (Read/Write)



EMS DMA ASSIGNMENT REGISTER
Address=0014h (Read/Write)



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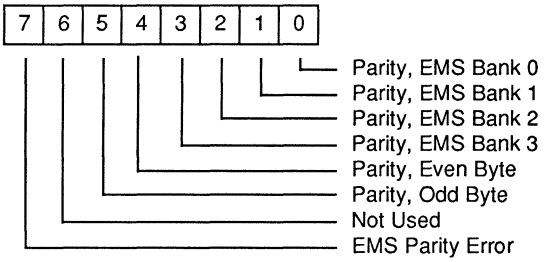
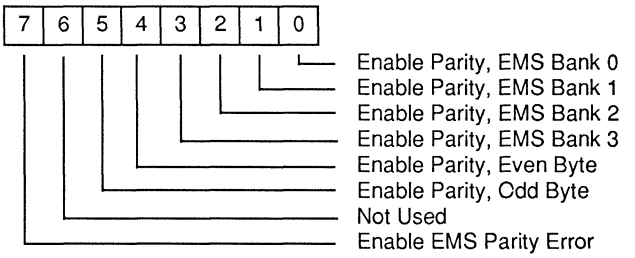
REGISTER BIT DIAGRAMS (Cont.)

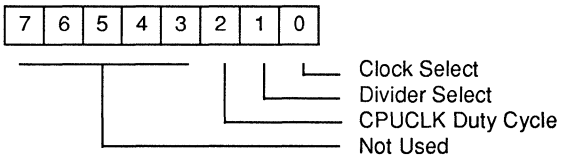
EMS PARITY STATUS REGISTER
Address=0018h (Read Only)



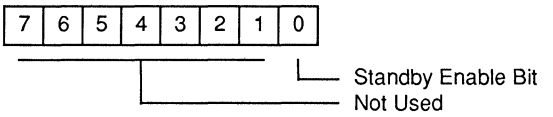
EMS PARITY ENABLE REGISTER
Address=0018 (Write Only)



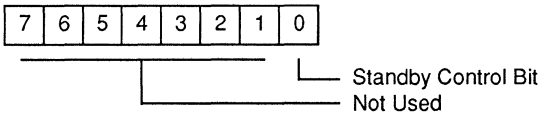
CLOCK CONTROL REGISTER
Address=0019h (Read/Write)



STANDBY ENABLE REGISTER
Address=001Eh (Read/Write)



STANDBY CONTROL REGISTER
Address=001Ch (Read/Write)



AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
tCYC	SYSCLK, CPUCLK Cycle Time	100		ns	
tC1	CLKIN0 Cycle Time	42		ns	24 MHz
tC2	CLKIN1 Cycle Time	33		ns	30 MHz
tC3	SYSCLK High Time	33		ns	33% Duty Cycle
tC4	SYSCLK Low Time	60		ns	33% Duty Cycle
tC5	CPUCLK High Time	33		ns	33% Duty Cycle
		47		ns	50% Duty Cycle
tC6	CPUCLK Low Time	60		ns	33% Duty Cycle
		47		ns	50% Duty Cycle
t7	SYSCLK to Command		25	ns	
tD8	SYSCLK Low to ALE, PCALE High		42	ns	
tD9	SYSCLK High to ALE, PCALE Low		30	ns	
tD10	SYSCLK to SRDY		35	ns	
tD11	SYSCLK Low to Address on I/O Channel		75	ns	
tSU12	Data Valid before t4 during Read	25		ns	
tH13	Data Invalid after End of t3 during Read	5		ns	
tD14	Data from End of t1 during Write		75	ns	
tD15	Memory Row Address Valid from SYSCLK Low		100	ns	
tD16	Memory Column Address Valid from SYSCLK Low		43	ns	
tD17	SYSCLK to –RAS		20	ns	
tD18	SYSCLK to –CAS		20	ns	
tD19	Memory Data Valid from –RAS		155	ns	
tD20	Memory Data Valid from –CAS		75	ns	
tSU21	Memory Data Valid before t4	20		ns	
tH22	Memory Data Invalid after –CAS	20		ns	
tD23	Memory Data Valid after SYSCLK Low during Write		75	ns	
tH24	Memory Data Hold Time after –CAS	20		ns	
tD25	Request/Grant from SYSCLK Low		25	ns	
tD26	Refresh after SYSCLK Low		40	ns	
tD27	PCALE after SYSCLK High during Refresh		30	ns	
tD28	Memory Refresh Address after PCALE		25	ns	
tD29	–RQ/GT Request from DRQ		2 tCYC	ns	
t30	DRQ Hold Time after –DACK		0	ns	
tD31	PCALE High from –RQ/GT Grant		30	ns	

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AC CHARACTERISTICS: (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
tH32	Data Hold Time from t4 SYSCLK High during Write	35		ns	
tD33	PCALE Low from End of DMA Command		2 1/2 tDCY +35	ns	tDCY=DMA Cycle Time Min 125 ns
tD34	AEN High from –RQ/GT Grant		1/2 tDCY +35	ns	
tD35	AEN Low from End of DMA Command		2 1/2 tDCY +35	ns	
tD36	–DACK Low from AEN		3 tDCY +70	ns	
tD37	–DACK High from End of DMA Command		1/2 tDCY +40	ns	
tD38	DMA Address Valid from AEN		3 tDCY +30	ns	
tD39	–MRD, –IORD Active from AEN		3 1/2 tDCY +35	ns	
tD40	–MWR, –IOWR Active from –MRD, –IORD		2 tDCY	ns	
t41	–MWR, –IOWR Command Width	4 tDCY		ns	
t42	–MRD, –IORD Command Width	6 tDCY		ns	
tD43	End of DMA Command to –RQ/GT Release		2 tDCY	ns	

MAXIMUM OUTPUT CAPACITANCE LOADING

Pinout	Capacitance Loading (pF)
CPUCLK	20
SYSCLK	20
RESET	200
–INTA	15
SEL0	30
SEL1	30
–CMDEN	15
ALE	20
PCALE	15
–PCENH	15
–PCENL	15
PCDIR	20
–DACK3- –DACK0	200
TC	15
–MWR	25

Pinout	Capacitance Loading (pF)
–MRD	25
–IORD	25
–IOWR	25
AEN	200
–ROMCS	20
–MREF	200
PAR0	100
PAR1	100
–DACKE	15
–CASL	45
–CASH	45
MA1-MA10	20
–RAS0	20
–RAS1	20
–ERAS0	20

Pinout	Capacitance Loading (pF)
–ERAS1	20
–ERAS2	20
–ERAS3	20
MDIR	15
–BHE	15
A0	15
–RQ/GT0	20
–RQ/GT1	20
SAD19-SAD0	40
SRDY	35
NMI	20

TIMING CHARACTERISTICS

FIGURE 2. CLOCK TIMING

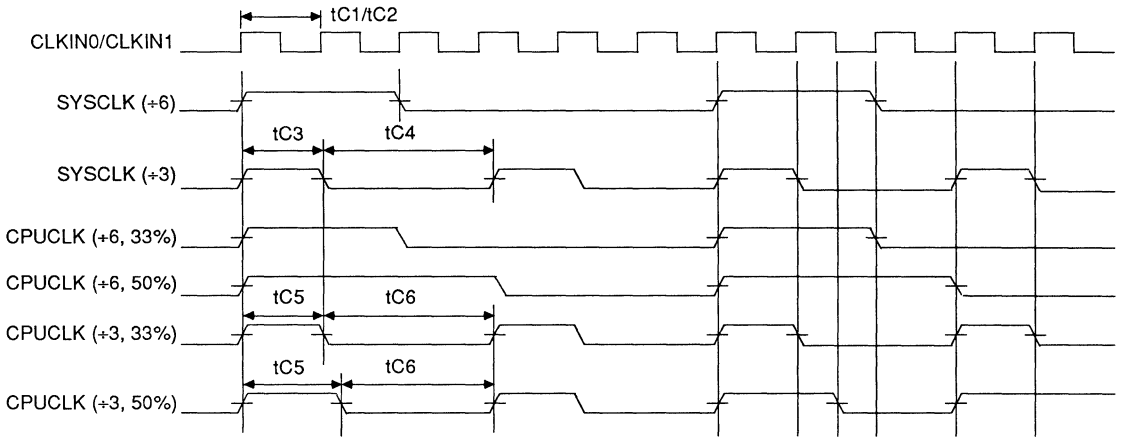

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FIGURE 3. READ CYCLE TIMING DIAGRAM FOR I/O CHANNEL

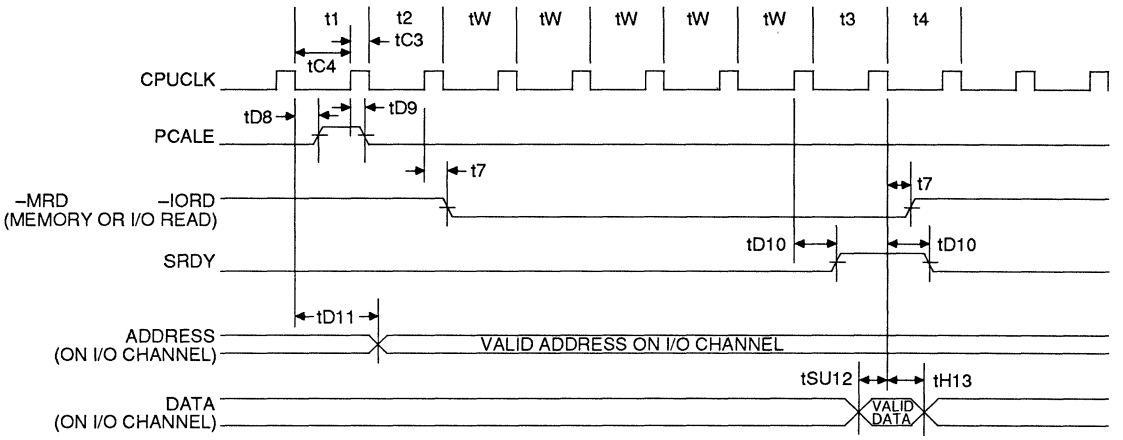

FIGURE 3. WRITE CYCLE TIMING DIAGRAM FOR I/O CHANNEL

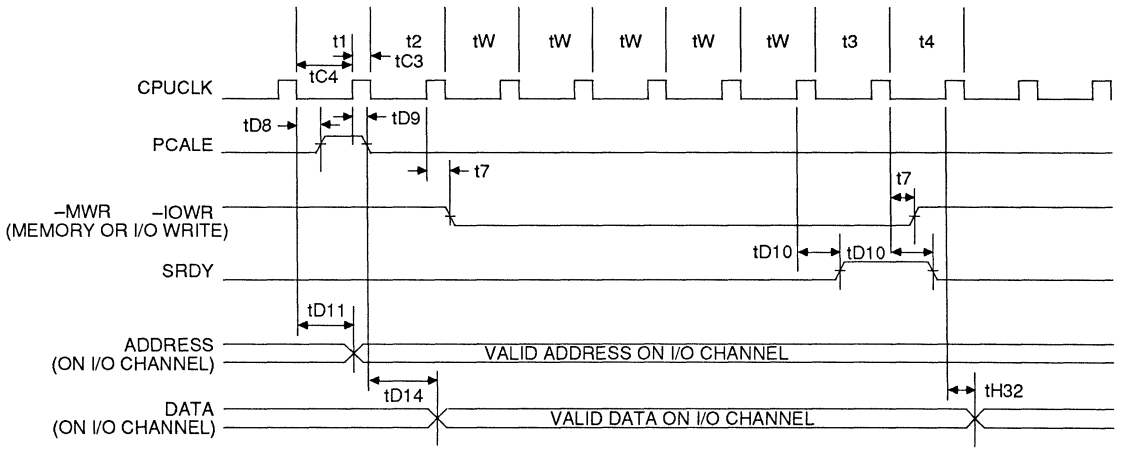

FIGURE 5. READ CYCLE TIMING DIAGRAM FOR ON-BOARD MEMORY (0 WAIT, 150 NS DRAM)

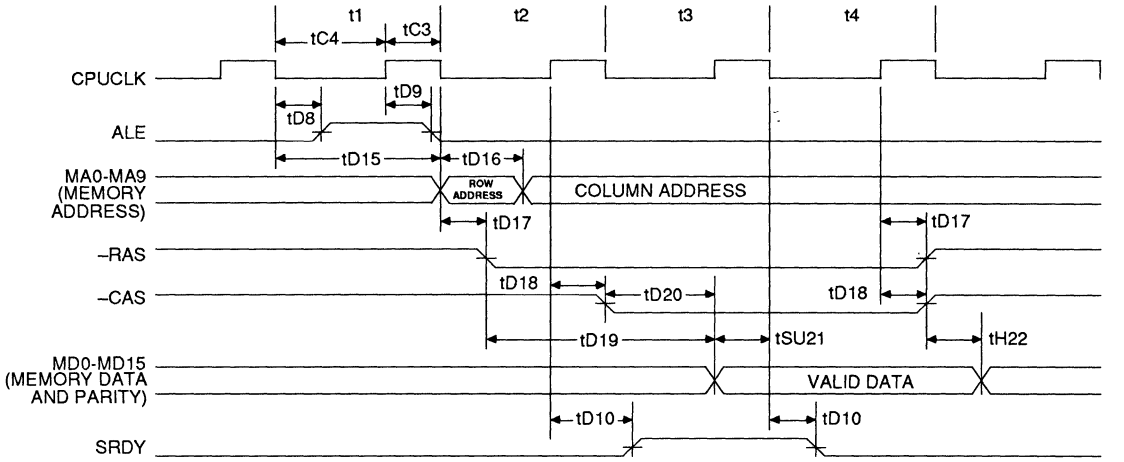

FIGURE 6. WRITE CYCLE TIMING DIAGRAM FOR ON-BOARD MEMORY (0 WAIT, 150 NS DRAM)

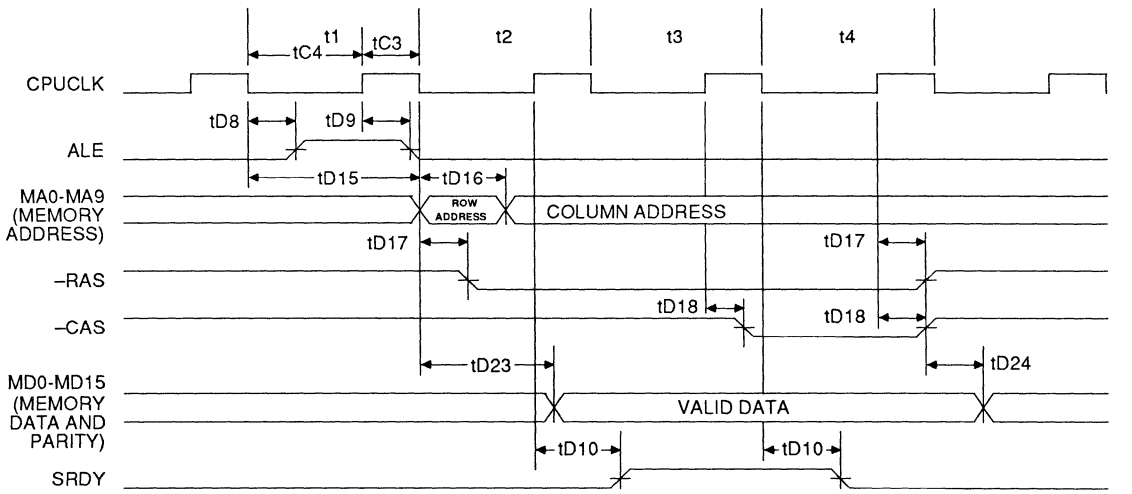

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FIGURE 7. MEMORY REFRESH CYCLE TIMING DIAGRAM

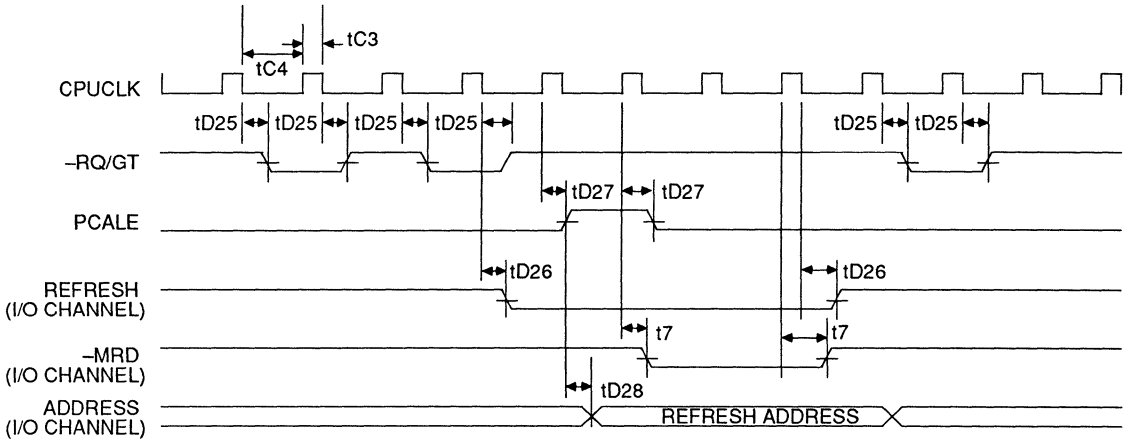
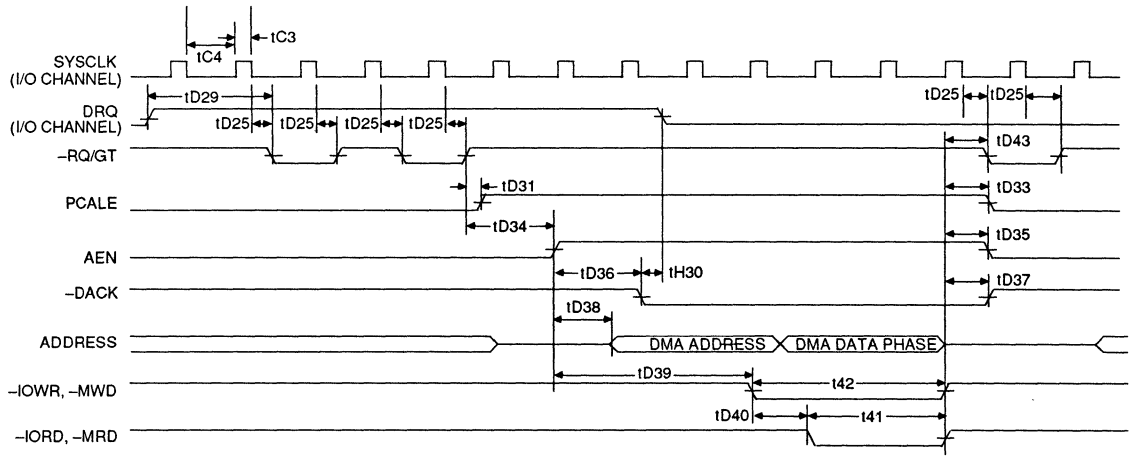


FIGURE 8. DMA TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VCC +0.3 V
Applied Output Voltage	–0.5 V to VCC +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = 400 µA
VOL	Output Low Voltage		0.45	V	IOL = 20 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 12 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 8 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 2 mA, Note 1
VIH	Input High Voltage	2.0	VCC + 0.5	V	TTL
VIL	Input Low Voltage	–0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	–10	10	µA	
OLI	Output Leakage Current	–10	10	µA	
ICC	Operating Supply Current		250	mA	

Note 1: Output Current Driving Capabilities.

IOH	IOL	VL82C031 Pins
–3.3 mA	20 mA	RESET,–DACK1, –-DACK3, AEN, –MREF
–1 mA	8 mA	PAR0, PAR1
–200 µA	4 mA	CPUCLK, SYSCLK, MDIR, –ERAS3 - –ERAS0, –RAS1, –RAS0, –CASH, –CASL, MA1-MA10, SAD0-SAD19, A0, ALE, –DACK0/–MRAS, –MWR, –MRD, –IOWR, –IORD, RAM256/1M, –ROMCS
–200 µA	2 mA	–INTA, SEL0, SEL1, –CMDEN, NMI, SRDY, –RQ/GT0, –RQ/GT1, –BHE, PCALE, –PCENH, –PCENL, PCDIR, TC, –DACKE

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NOTES: