Data Sheet

VT1636
LVDS Transmitter

Preliminary Revision 1.0
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VIA TECHNOLOGIES, INC.

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VT1636

LVDS Transmitter

PRODUCT FEATURES

- **Supports Single / Dual LVDS Transmitter Function**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Supports LVDS 18-bit and 24-bit Output**
- **Supports Dual Channel UXGA Panel Display**
- **Supports 2D Dither for 18-bit Panel**
- **Supports Option for 24-bit Color Mappings with Conventional (LSB) or Non-Conventional (MSB) Format Output**
- **Supports DVO Input Mode with 25 to 165 MHz Input Clock**
- **Programmable Input Clock and Strobe Select**
- **Narrow Bus Reduces Cable Size and Cost**
- **PLL Requires No External Components**
- **Two-Wire Serial Communication**
- **Panel Protection and Power Down Sequencing**
- **Panel Power Sequencing Control**
- **Supply Voltage 2.25 - 2.75V**
- **64-pin LQFP Package (10x10x1.4 mm)**

OVERVIEW

The VIA VT1636 is a powerful LVDS transmitter. The input format can be DVO (12 data pin per port) digital interface. Operating on DVO mode, its output can support single / dual channels with 18-bit or 24-bit color type panel. The VT1636 implements a 2D dithering engine option for 18-bit / 36-bit color type panel.

Figure 1 shows the functional block diagram for VT1636 LVDS Transmitter.

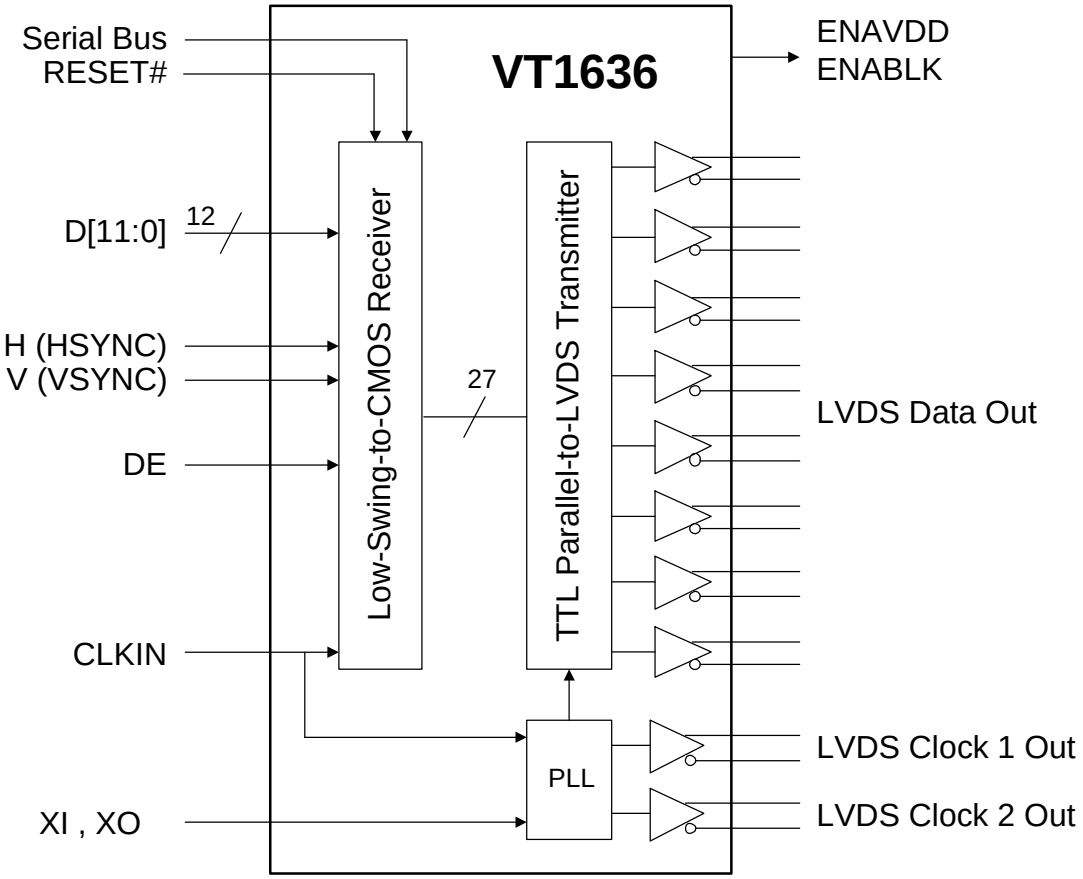


Figure 1. Functional Block Diagram

The LVDS transmitter operates at pixel speed up to 165 MHz per link, supporting UXGA panel display. It converts 24 / 48 bits of CMOS/TTL data into 3-8 LVDS data streams. The LVDS transmitter supports dither function for 18-bit panel. Data is encoded into commonly used formats. A phase-locked transmit clock is transmitted in parallel with the data streams over 3-8 LVDS link.

All features can be software programmable through a serial bus interface that provides read / write access to all registers or by hardware strapping pins setting.

PINOUTS

Pin Diagram

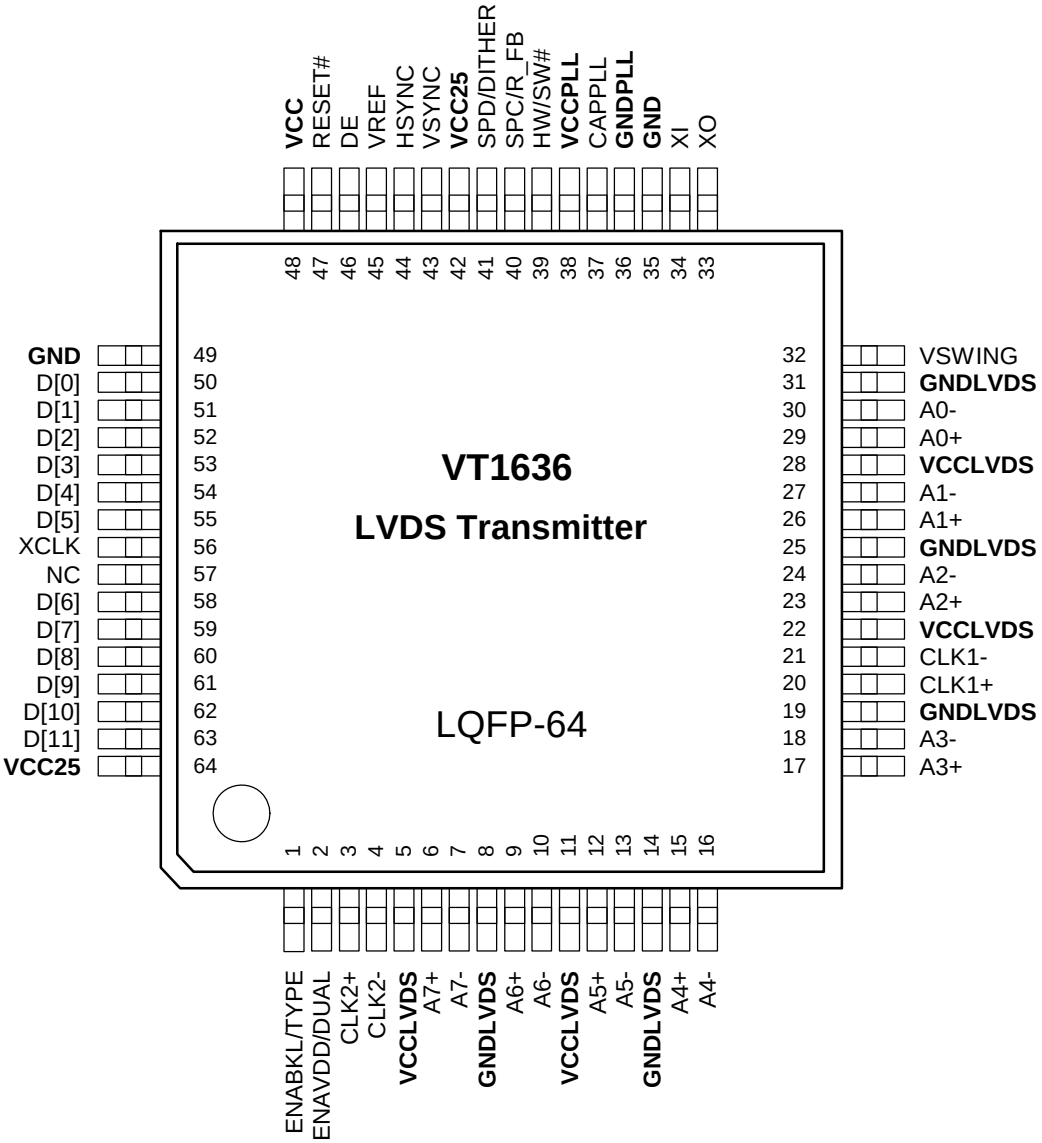


Figure 2. Pin Diagram (Top View)

Pin Lists

Table 1. Pin List (Alphabetical Order)

Pin	Pin Name	Pin	Pin Name
30	A0-	63	D[11]
29	A0+	46	DE
27	A1-	1	ENABKL / TYPE
26	A1+	2	ENAVDD / DUAL
24	A2-	**35**	**GND**
23	A2+	**49**	**GND**
18	A3-	**8**	**GNDLVDS**
17	A3+	**14**	**GNDLVDS**
16	A4-	**19**	**GNDLVDS**
15	A4+	**25**	**GNDLVDS**
13	A5-	**31**	**GNDLVDS**
12	A5+	**36**	**GNDPLL**
10	A6-	44	HSYNC
9	A6+	39	HW/SW#
7	A7-	57	NC
6	A7+	47	RESET#
37	CAPPLL	40	SPC / R_FB
21	CLK1-	41	SPD / DITHER
20	CLK1+	**48**	**VCC**
4	CLK2-	**42**	**VCC25**
3	CLK2+	**64**	**VCC25**
50	D[00]	**5**	**VCCLVDS**
51	D[01]	**11**	**VCCLVDS**
52	D[02]	**22**	**VCCLVDS**
53	D[03]	**28**	**VCCLVDS**
54	D[04]	**38**	**VCCPLL**
55	D[05]	45	VREF
58	D[06]	32	VSWING
59	D[07]	43	VSYNC
60	D[08]	56	XCLK
61	D[09]	34	XI
62	D[10]	33	XO

Pin Descriptions

Table 2. Pin Descriptions

Pixel Data Input			
Signal Name	**Pin #**	**Type**	**Description**
D[11-00]	63, 62, 61, 60, 59, 58, 55, 54, 53, 52, 51, 50	I	**Channel Data Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.
DE	46	I	**Data Enable Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.
HSYNC	44	I	**HSYNC Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.
VSYNC	43	I	**VSYNC Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.

Control Pins			
Signal Name	**Pin #**	**Type**	**Description**
ENAVDD/ DUAL	2	I/O	**Enable Panel Power Supply 2.5V** LVDS single or dual channel select pin. S/W mode: ENAVDD; H/W mode: Dual DUAL = L, chip is for single channel. DUAL = H, chip is for dual channel.
ENABLK/ TYPE	1	I/O	**Enable Back-Light of LCD Panel** Conventional / Non-Conventional Output Format Mode select pin. S/W mode: ENABLK; H/W mode: TYPE TYPE = L, chip is for output of Conventional (LSB) color mapping format. TYPE = H, chip is for output of Non-Conventional (MSB) color mapping format.
HW/SW#	39	I	

Two-Wire Serial Bus Interface			
Signal Name	**Pin #**	**Type**	**Description**
SPD / DITHER	41	I/O	**Two-Wire Serial Communication Interface** This pin functions as bi-direction data pin. S/W mode: SPD; H/W mode: Dither Dither = H, dither function enabled Dither = L, disabled.
SPC / R_FB	40	I	**Two-Wire Serial Communication Interface** This pin functions as clock pin. S/W mode: SPC; H/W mode: R_FB Rising / Falling sample select pin R_FB = H, rising sample R_FB = L, falling sample.

Clock			
Signal Name	**Pin #**	**Type**	**Description**
XCLK	56	I	**External Clock Input** This input clock signals to the device for use with H1, V1 and D[11-00].
XI	34	I	A 14.31818 MHz crystal is attached between XI and XO. This pin can also be connected to oscillator.
XO	33	O	A 14.31818 MHz crystal is attached between XI and XO. If an external oscillator is attached to XI, this pin should be no connected.

Reserved and NC Pin			
Signal Name	**Pin #**	**Type**	**Description**
NC	57	-	**Not Connected.** Reserved for future use.

Power and Ground			
Signal Name	**Pin #**	**Type**	**Description**
CAPPLL	37	O	**LVDS PLL Capacitor**
GND	35, 49	P	**Digital Ground Pin**
GNDLVDS	8, 14, 19, 25, 31	P	**LVDS Ground Pin for LVDS Outputs**
GNDPLL	36	P	**LVDS PLL Ground**
VCC	48	P	**I/O Supply Voltage (1.5V - 3.3V)**
VCC25	42, 64	P	**Digital Power Supply Pin (2.5V)**
VCCLVDS	5, 11, 22, 28	P	**LVDS Power Supply Pin for LVDS Outputs (2.5V)**
VCCPLL	38	P	**LVDS PLL Power Supply (2.5V)**

REGISTERS

Register Overview

Table 3 below summarizes all on-chip registers. The table also documents the power-on default value ("Default") and access type for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved (essentially the same as RO) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits. Refer to individual register descriptions for details.

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 3. Register Mapping

Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	VND_IDL (RO)								**06h**
0x01	VND_IDH (RO)								**11h**
0x02	DEV_IDL (RO)								**45h**
0x03	DEV_IDH (RO)								**33h**
0x04	DEV_REV (RO)								**00h**
0x05	RSVD								**00h**
0x06	FRQ_LOW (RO)								**19h**
0x07	FRQ_HIGH (RO)								**A5h**
0x08	MODE_IN[2:0] (RW)			TYPE (RW)	CLK_SEL_ST2[3:0] (RW)				**F0h**
0x09	PWDB (RW)	RSVD		CLK_SEL_ST1[4:0] (RW)					**00h**
0x0A	DC_EN (RW)	DI[2:0] (RW)			DLY_P2S (RW)	PANEL_PRO[2:0] (RW)			**00h**
0x0B	T5[3:0] (RW)				T1[9:8] (RW)		T4[9:8] (RW)		**10h**
0x0C	T1[7:0] (RW)								**01h**
0x0D	T4[7:0] (RW)								**01h**
0x0E	T2[7:0] (RW)								**01h**
0x0F	T3[7:0] (RW)								**01h**
0x10	T2[8] (RW)	T3[8] (RW)	LVDSRDY (RW)	EN_ENABKL (RW)	PRE (RW)	EMP (RW)	IS[1:0] (RW)		**00h**
0x11	RSVD								**3ch**
0x12	RSVD								**3ch**
0x13	RSVD								**00h**
0x14	RSVD								**00h**
0x15	RSVD								**00h**

LVDS Transmitter Register Descriptions

Series Bus Device Address: 80h

Vendor Identification

Address Offset: 00–01h **Default Value: 1106h**

Bit	Attr.	Description
15:0	RO	**VND_IDL, VND_IDH (Vendor Identification Number)**

Device Identification

Address Offset: 02–03h **Default Value: 3345h**

Bit	Attr.	Description
15:0	RO	**DEV_IDL, DEV_IDH (Device Identification Number)**

Device Revision

Address Offset: 04h **Default Value: 00h**

Bit	Attr.	Description
7:0	RO	**DEV_REV (Device Revision)**

Low Frequency Limit

Address Offset: 06h **Default Value: 19h**

Bit	Attr.	Description
7:0	RO	**FRQ_LOW (Low Frequency Limit)** 25 MHz. 1-pixel per clock mode.

High Frequency Limit

Address Offset: 07h **Default Value: A5h**

Bit	Attr.	Description
7:0	RO	**FRQ_HIGH (High Frequency Limit)** 165 MHz. 1-pixel per clock mode.

Panel Data Select

Address Offset: 08h **Default Value: F0h**

Bit	Attr.	Description
7:5	RW	**MODE_IN[2:0] (Single 12-bit DDR Input to Single/Dual Channel Output)** 000 single channel output 111 dual channel output
4	RW	**TYPE (Output Signal Mapping Select)** 0 24-bit Conventional (LSB) color mapping format output. **1** 24-bit Non-Conventional (MSB) color mapping format output.
3:0	RW	**CLK_SEL_ST2[3:0] (Clock Deskew Phase Select of Data Latch Stage 2)** There are 14 PLL phases available to select.

Power Down Mode and Clock Deskew Phase Select

Address Offset: 09h **Default Value: 00h**

Bit	Attr.	Description
7	RW	**PWDB (Power Down Mode)** 0 Power down 1 Normal operation
6:5	-	**-reserved-**
4:0	RW	**CLK_SEL_ST1[4:0] (Clock Deskew Phase Select of Data Latch Stage 1)** There are 16 external clocks and 14 PLL phases available to select.

Miscellaneous Control

Address Offset: 0Ah **Default Value: 00h**

Bit	Attr.	Description
7	RW	**DC_EN (DC Balance Function Enable)** **0** Disable 1 Enable
6:4	RW	**DI[2:0] (Dithering Function Select)** **6-5:** Programmable dithering select: Default = 10b **4:** Function 0 Disable 1 Enable
3	RW	**DLY_P2S (P2S Clock Deskew Select)** 0 Disable 1 Enable
2:0	RW	**PANEL_PRO[2:0] (Panel Protection)** **2:** PLL lock detection circuit select: 0 Disable 1 Enable **1:** HSYNC missing detection circuit select: 0 Disable 1 Enable **0:** VSYNC missing detection circuit select: 0 Disable 1 Enable

Panel Power Sequencing Timing

Address Offset: 0Bh **Default Value: 10h**

Bit	Attr.	Description
7:4	RW	**T5[3:0] (Power Sequencing Timing Parameter T5[3:0])** Range: 100-1600ms Increment: 100ms
3:2	RW	**T1[9:8] (Power Sequencing Timing Parameter T1[9:8])** Range: 1-1024ms Increment: 1ms
1:0	RW	**T4[9:8] (Power Sequencing Timing Parameter T4[9:8])** Range: 1-1024ms Increment: 1ms

Panel Power Sequencing Timing 1

Address Offset: 0Ch **Default Value: 01h**

Bit	Attr.	Description
7:0	RW	**T1[7:0] (Power Sequencing Timing Parameter T1[7:0])** Range: 1-1024ms Increment: 1ms

Panel Power Sequencing Timing 4

Address Offset: 0Dh **Default Value: 01h**

Bit	Attr.	Description
7:0	RW	**T4[7:0] (Power Sequencing Timing Parameter T4[7:0])** Range: 1-1024ms Increment: 1ms

Panel Power Sequencing Timing 2

Address Offset: 0Eh **Default Value: 01h**

Bit	Attr.	Description
7:0	RW	**T2[7:0] (Power Sequencing Timing Parameter T2[7:0])** Range: 2-1024ms Increment: 2ms

Panel Power Sequencing Timing 3

Address Offset: 0Fh **Default Value: 01h**

Bit	Attr.	Description
7:0	RW	**T3[7:0] (Power Sequencing Timing Parameter T3[7:0])** Range: 2-1024ms Increment: 2ms

Panel Power Sequencing Timing and Pre-emphasis

Address Offset: 10h **Default Value: 00h**

Bit	Attr.	Description
7	RW	**T2[8] (Power Sequencing Timing Parameter T2[8])** Range: 2-1024ms Increment: 2ms
6	RW	**T3[8] (Power Sequencing Timing Parameter T3[8])** Range: 2-1024ms Increment: 2ms
5	RW	**LVDSRDY (LVDS Ready Input)** This bit is used to test the timing requirements on panel sequencing.
4	RW	**EN_ENABKL (Enable Output Pin ENABKL, Back-Light of LCD panel)**
3	RW	**PRE (Pre-emphasis)** 0 Disable 1 Enable
2	RW	**EMP (Pre-emphasis Enhance)** 0 Disable 1 Enable
1:0	RW	**IS[1:0] (Swing Control)** 0 Disable 1 Enable

FUNCTIONAL DESCRIPTIONS

LVDS Transmitter

Power Sequencing

The internal signal Lvds_rdy represents that the state of LVDS TX is ready to transmit. Power-on sequence starts when Lvds_rdy goes high, and ends when the panel is ready. T1 is the time duration between Lvds_rdy to valid LVDS clocks and data. T2 is the waiting time after valid LVDS clocks and data before enabling the LVDS panel back light.

Power-off sequence starts when Lvds_rdy goes low, and ends when the panel power is off after a period of time. T3 is the required time after disabling the backlight before the valid LVDS clocks and data become tri-state or ground. T4 is the time duration prior to panel power off after the valid LVDS clocks and data become tri-state or ground. T5 is the waiting time required prior to enabling power on after power has been off.

Once power sequence starts, the internal state machine would complete the sequence.

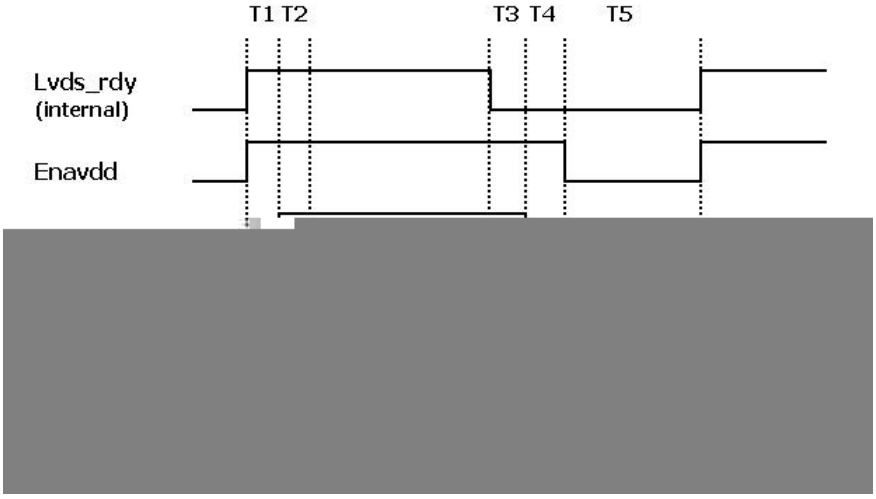


Figure 3. Power Sequencing Timing Definition

Table 4. Power Sequencing Timing Definition

	Range	Increment
T1[9:0]	1-1024ms	1ms
T2[8:0]	2-1024ms	2ms
T3[8:0]	2-1024ms	2ms
T4[9:0]	1-1024ms	1ms
T5[3:0]	100-1600ms	100ms

LVDS Interface Data Mapping

Table 6. 12-bit DVO Mode (DDR), "Two Data per Clock" Input Color Data Mapping

MODE_IN=000	P0		P1	
	P0L	P0H	P1L	P1H
Pin Name	Low	High	Low	High
D[11]	G0[3]	R0[7]	G1[3]	R1[7]
D[10]	G0[2]	R0[6]	G1[2]	R1[6]
D[09]	G0[1]	R0[5]	G1[1]	R1[5]
D[08]	G0[0]	R0[4]	G1[0]	R1[4]
D[07]	B0[7]	R0[3]	B1[7]	R1[3]
D[06]	B0[6]	R0[2]	B1[6]	R1[2]
D[05]	B0[5]	R0[1]	B1[5]	R1[1]
D[04]	B0[4]	R0[0]	B1[4]	R1[0]
D[03]	B0[3]	G0[7]	B1[3]	G1[7]
D[02]	B0[2]	G0[6]	B1[2]	G1[6]
D[01]	B0[1]	G0[5]	B1[1]	G1[5]
D[00]	B0[0]	G0[4]	B1[0]	G1[4]

Table 7. Single Channel Color Mapping for Single LVDS Channel

Pin Name	24-bit MSB Color Mapping Format TYPE = 1	24-bit LSB Color Mapping Format TYPE = 0
LDC[0](1)	R0	R2
LDC[0](2)	R1	R3
LDC[0](3)	R2	R4
LDC[0](4)	R3	R5
LDC[0](5)	R4	R6
LDC[0](6)	R5	R7
LDC[0](7)	G0	G2
LDC[1](1)	G1	G3
LDC[1](2)	G2	G4
LDC[1](3)	G3	G5
LDC[1](4)	G4	G6
LDC[1](5)	G5	G7
LDC[1](6)	B0	B2
LDC[1](7)	B1	B3
LDC[2](1)	B2	B4
LDC[2](2)	B3	B5
LDC[2](3)	B4	B6
LDC[2](4)	B5	B7
LDC[2](5)	HSYNC(H2)	HSYNC(H2)
LDC[2](6)	VSYNC(V2)	VSYNC(V2)
LDC[2](7)	DE(DE2)	DE(DE2)
LDC[3](1)	R6	R0
LDC[3](2)	R7	R1
LDC[3](3)	G6	G0
LDC[3](4)	G7	G1
LDC[3](5)	B6	B0
LDC[3](6)	B7	B1
LDC[3](7)	RES	RES

The dither engine converts 24-bit per pixel to 18-bit per pixel. For 18-bit type panel, the outputs use 3 data sets, leaving LDC[3] unused.

18-bit type panel color mapping is similar to 24-bit LSB color mapping. No LDC[3] channel.

Dual channel output color mapping is same as single channel. LDC[0-3] for P0 (pixel 0), LDC[4-7] for P1 (pixel 1).

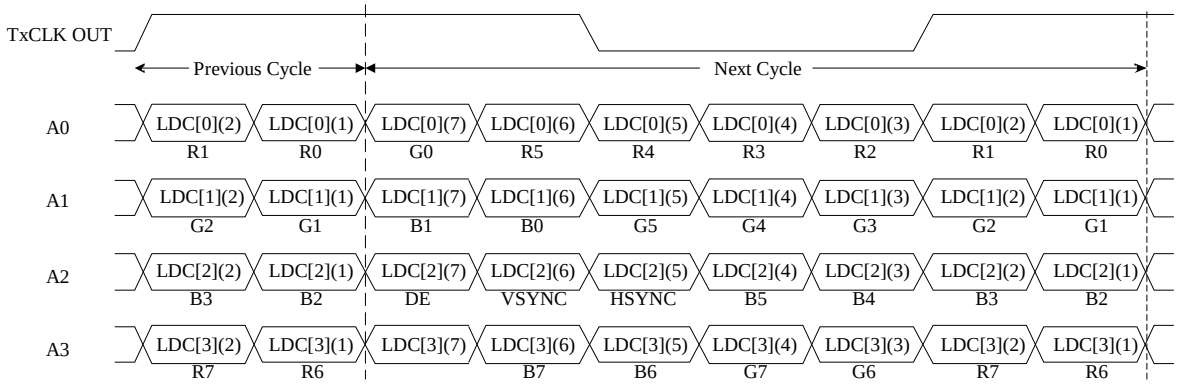
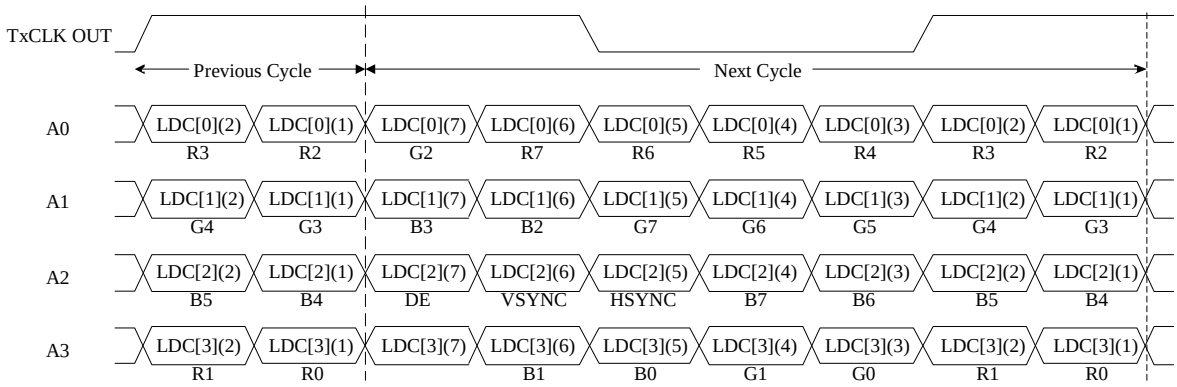


Figure 5. 24-bit Non-Conventional (MSB) Input Data Color Mapping to LVDS Outputs



Note: For 18-bit panel (R*, G*, B*) display, R*[0-5] = R[2-7], G*[0-5] = G[2-7] , B*[0-5] = B[2-7];
A3 channel is unused.

Figure 6. 24-bit Conventional (LSB) Input Data Color Mapping to LVDS Outputs

ELECTRICAL SPECIFICATIONS

CMOS/TTL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage	-	2.0	-	V_{DD}	V
V_{IL}	Low Level Input Voltage	-	GND	-	0.8	V
I_{IN}	Input Current	V_{IN}=GND or V_{DD}	-	±5.1	±10	uA

LVDS Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential Output Voltage	R_L=100Ω	-	275	-	mV
$\Delta\|V_{OD}\|$	Change in Differential Output Voltage		-	25	-	mV
V_{OS}	Common Mode Output Voltage		-	1.250	-	V
$\Delta\|V_{OS}\|$	Change in Common Mode Output Voltage		-	25	-	mV
I_{IN}	Input Current	V_{IN}=3.3V	-	-	+10	uA
		V_{IN}=GND	-10	-	-	uA
$\|I_{OS}\|$	Short Circuit Output Current	V_{OUT}=0V; R_L=100Ω	-	3.5	-	mA
$\|I_{OZ}\|$	High Impedance State Output Current	PDB= 0V V_{OUT}=GND or VCC25	-	1	-	uA
P_{TOTAL}	Total power consumption	-	-	-	225	mW

Low Voltage Mode DC Specification (Pixel Data Input)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ref}	Differential Input Reference Voltage, VCC25=2.25V	Low Swing, V_{ref}=1/2Vddq	-	1/2Vddq	-	V
V_{IHLS}	Low Swing High Level Input Voltage, VCC25=2.25V	-	V_{ref} +100mV	-	1.5	V
V_{ILLS}	Low Swing High Level Input Voltage, VCC25=2.25V		GND	-	V_{ref} -100mV	V

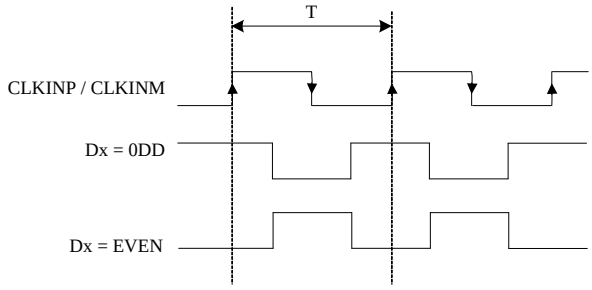


Figure 7. Worst Case Test Pattern

Figure 8. Tx Input Clock Transition Time

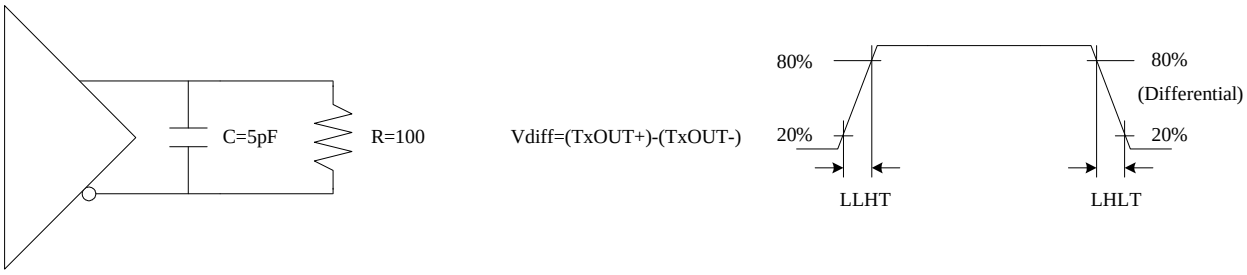


Figure 9. LVDS Output Load and Transition Time

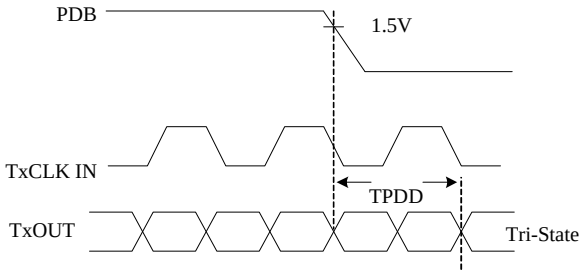


Figure 10. Tx Power Down Delay

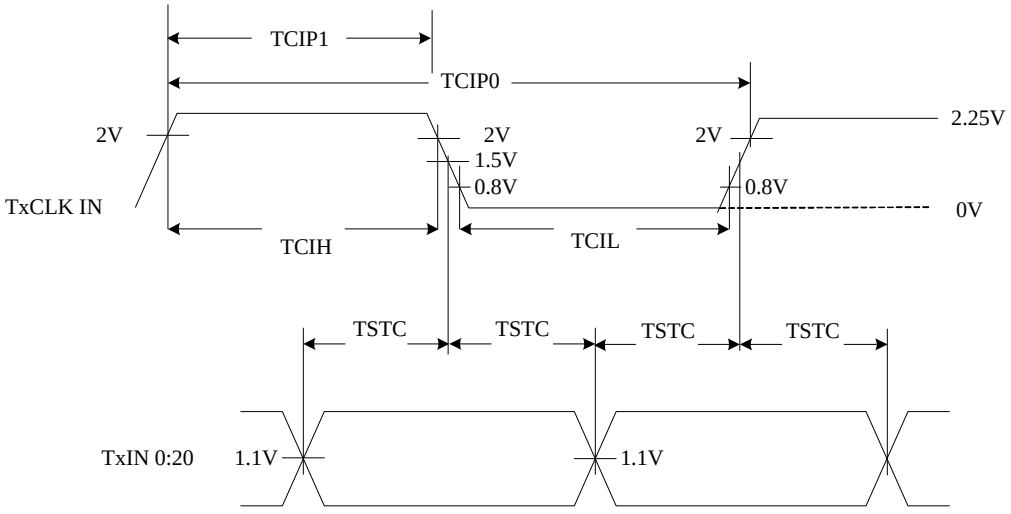


Figure 11. Tx Setup/Hold and High/Low Time

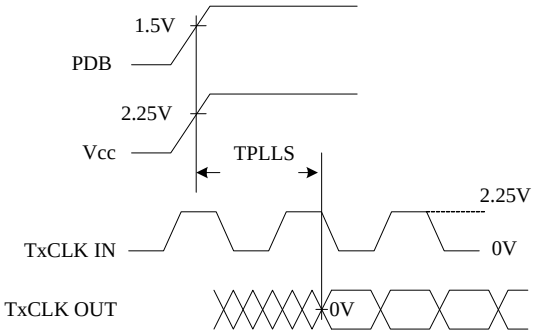


Figure 12. Tx PLL Set Time

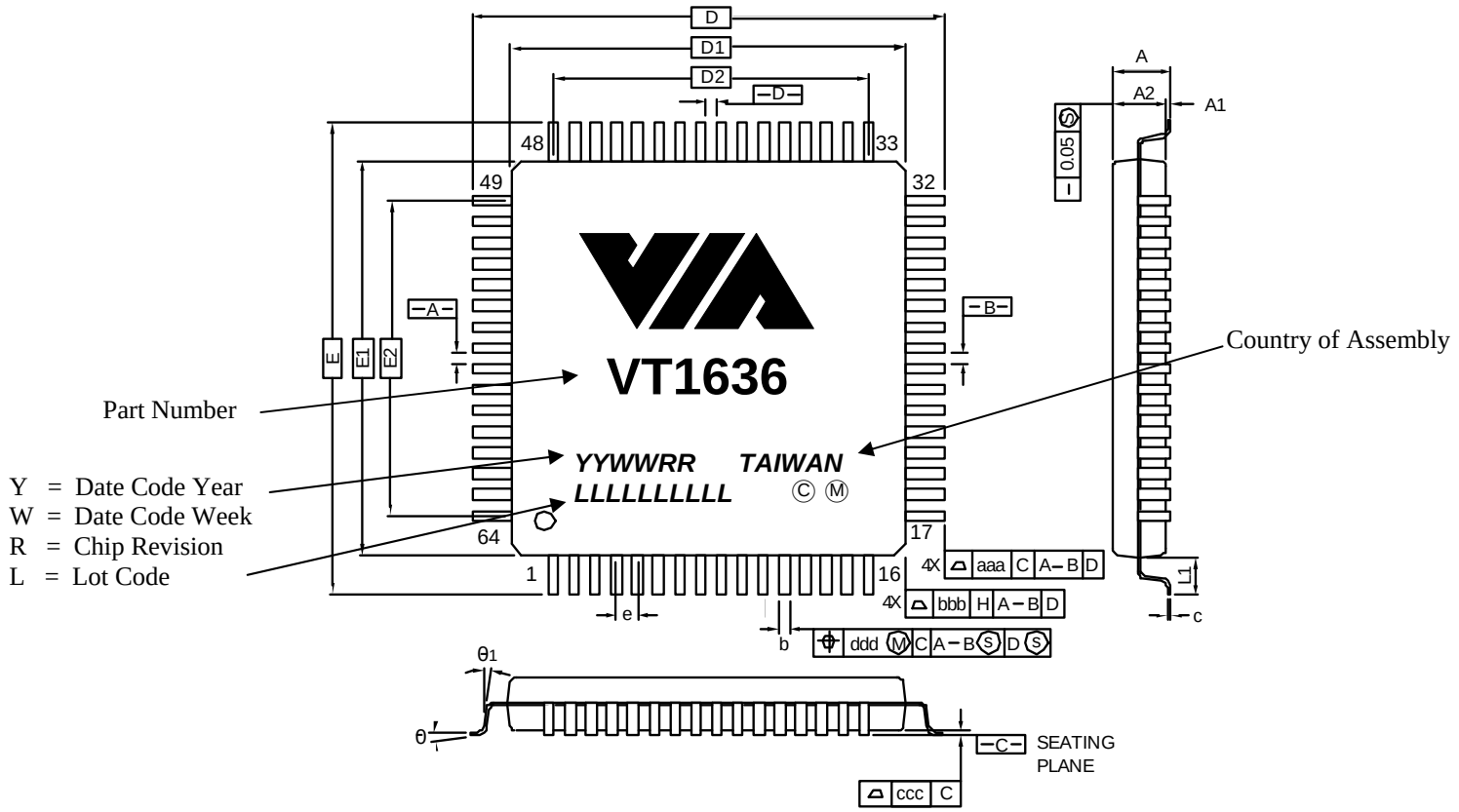
Recommended Operating Conditions

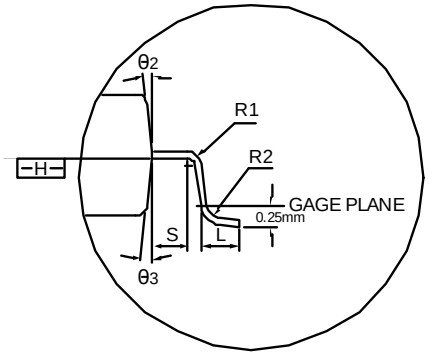
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{cc}	Supply voltage	2.25	2.5	2.75	V
T_A	Operating free air temperature	0	25	85	°C

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{STG}	Storage temperature	-25	-	150	°C
V_{ESD}	Electrostatic Discharge (Human Body)	-	-	2.5	KV
T_{VPS}	Vapor Phase Soldering (1 min.)	-	-	255	°C

Package Mechanical Specifications





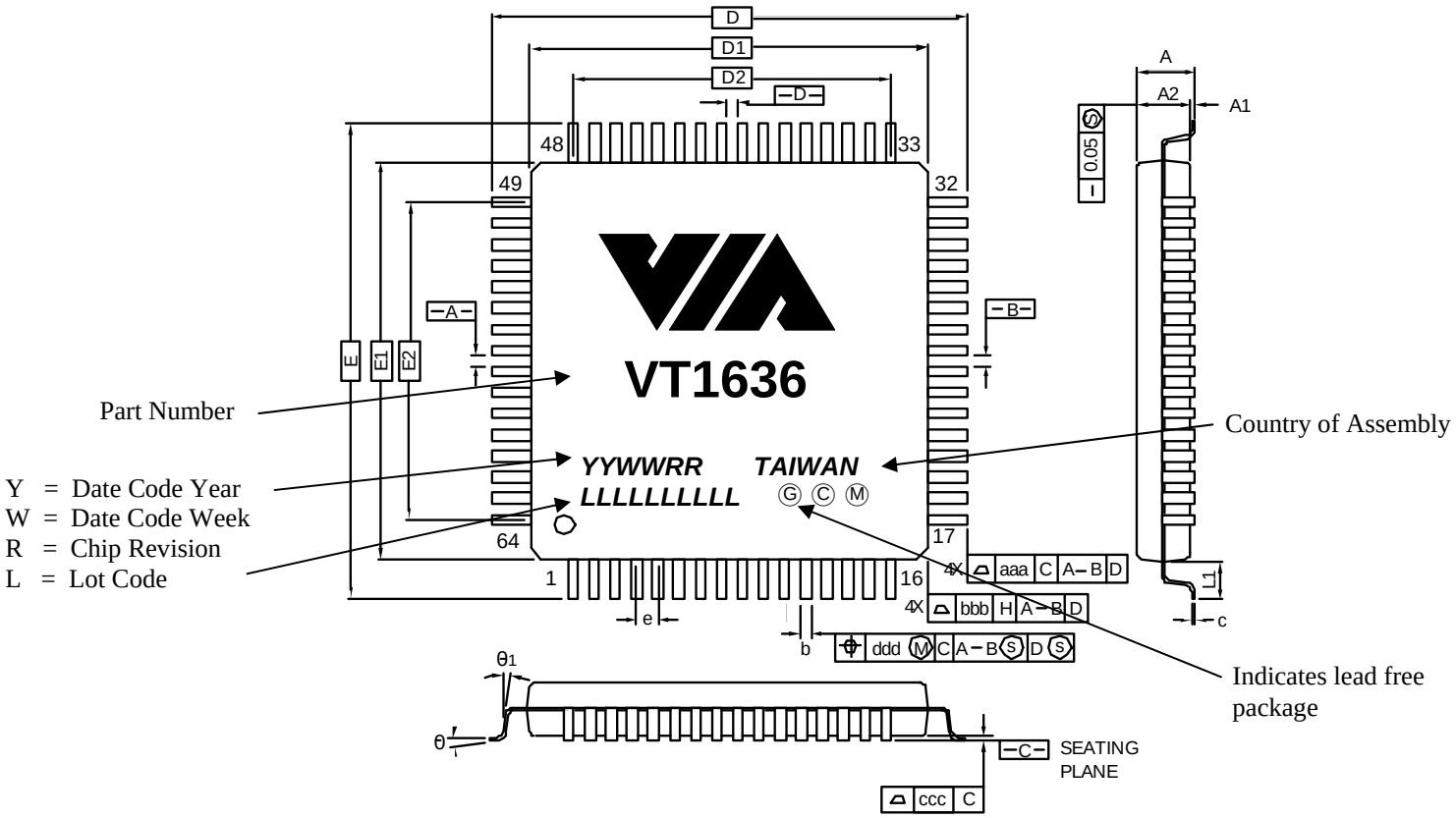
CONTROLDIMENSIONSAREINMILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00BASIC			0.472BASIC		
E	12.00BASIC			0.472BASIC		
D1	10.00BASIC			0.393BASIC		
E1	10.00BASIC			0.393BASIC		
D2	7.50BASIC			0.295BASIC		
E2	7.50BASIC			0.295BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50BASIC			0.020BASIC		
TOLERANCESOFFORMANDPOSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 13. Mechanical Specification – 64-Pin LQFP



CONTROLDIMENSIONSAREINMILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00BASIC			0.472BASIC		
E	12.00BASIC			0.472BASIC		
D1	10.00BASIC			0.393BASIC		
E1	10.00BASIC			0.393BASIC		
D2	7.50BASIC			0.295BASIC		
E2	7.50BASIC			0.295BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50BASIC			0.020BASIC		
TOLERANCESOFFORMANDPOSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 14. Mechanical Specification for Lead-Free – 64-Pin LQFP