



Preliminary Data Sheet

CX700 Series

*Advanced All-in-One
System Processor*

Preliminary Revision 0.951
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VIA TECHNOLOGIES, INC.

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CX700 / CX700M

ALL-IN-ONE SYSTEM PROCESSOR

533 / 400 MHz FSB VIA C7 and Intel Pentium-M Processor
 DDR2 533 / 400, DDR400 / 333 SDRAM Controller
 Integrated UniChrome Pro II 3D / 2D Graphics & Video Processor
 Unified Video Decoding Accelerator
 Integrated HDTV Encoder and LVDS / DVI Transmitter
 High Definition Audio Controller
 Two Serial ATA Ports
 One UltraDMA-133 EIDE Channel
 Six USB 2.0 / 1.1 Ports
 PCI 32-bit 33MHz Bus
 Two RS-232 Serial Ports
 RTC and LPC, SMBus, Modem Interfaces
 ACPI and Sophisticated Power Management

PRODUCT FEATURES

- **Process Technology and Package**
 - 0.15um, 1.5V core voltage
 - 37.5mm x 37.5mm Flip Chip BGA
- **CPU Interface**
 - Supports 533 / 400 MHz FSB VIA C7 and Intel Pentium-M processors
- **Memory System**
 - Supports DDR2 and DDR SDRAM
 - DDR2 Mode
 - Supports DDR2 533 / 400 SDRAM
 - Supports 64Mb / 128Mb / 256Mb / 512Mb / 1024Mb (x8 / x16 / x32)
 - Supports CL 2 / 3 / 4 / 5
 - Supports ECC for DDR2 400 only
 - DDR Mode
 - Supports DDR 400 / 333 SDRAM
 - Supports 64Mb / 128Mb / 256Mb / 512Mb / 1024Mb (x8 / x16 / x32)
 - Supports CL 2 / 2.5 for DDR 333, CL 2.5 / 3 for DDR 400
 - Supports ECC
 - Supports 1 or 2 unbuffered or register double-sided DIMMs with different clock buffering scheme
 - Supports 64/32-bit data width

- **Integrated 3D / 2D / Video Processors**

- Optimized Unified Memory Architecture (UMA)
- Supports 32 / 64 / 128 MB Frame Buffer sizes
- 200 MHz Graphics Engine Clock

2D Graphics Processor

- 128-bit 2D graphics engine
- Hardware 2D rotation
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit BLock Transfer) functions including alpha BLTs
- True-color hardware cursor (64x64x32bpp) with 256-level blending effect
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Graphics Processor

3D Graphics Processor

- 128-bit 3D graphics engine
- Dual pixel rendering pipelines and dual texture units
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 8K Texture Cache

Capability

- Supports ROP2
- Supports various texture formats including 16/32bpp ARGB, 8bpp Palletized (ARGB), YUV 422/420 and compressed texture (DXTC)
- Texture sizes up to 2048x2048 with Microsoft DirectX texture compression
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending
- Bump mapping and cubic mapping
- Hardware back-face culling
- Specular lighting

Performance

- Two textures per pass
- Triangle rate up to 4.5 million triangles per second
- Pixel rate up to 200 million pixels per second per texture
- Texel bilinear fill rate up to 400 million texels per second
- High quality dithering

Hi-Def Video Processor

High Quality Video Processor

- RGB555, RGB565, RGB8888 and YUV422 video playback formats
- High quality 5-tap horizontal and 5-tap vertical scaler for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
- Independent graphics and video gamma tables
- 2 sets of Color and Chroma Key support
- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Display rotation in clockwise and counter-clockwise directions
- Bob, Weave, Median-filter and Adaptive de-interlacing modes
- 3:2 / 2:2 pull-down detection
- De-blocking mode support
- Combining of many special effects such as filter, scaling up or down, sub-picture blending, de-interlacing and deblocking to one pass process
- Tear-free double / triple buffer flipping
- Input video vertical blanking or line interrupt
- Video gamma correction

Video Overlay Engine

- Simultaneous graphics and TV video playback overlay
- Supports video window overlays
- Supports Microsoft VMR™ Through Front-End Video Scaling, Color Space Conversion and Blending
- Supports both YUV and RGB format Chroma Key
- Supports 16 operations for Color and Chroma Key
- Hardware sub-picture blending

Video Capture Capability

- Dual Transport Stream inputs or dual 8-bit or one 16-bit CCIR656/601 input
- Video capture and playback tear free auto flipping
- External Hsync / Vsync support

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- **External Display Support**

- **CRT / HDTV (CX700M) Display Interface**

- 30-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability
- Supports RGB / YPbPr (CX700M) / CompYC (CX700M)
- Supports CRT resolutions up to 2048x1536
- Supports TV resolutions up to 1920x1080i (CX700M)
- Support Macrovision copy protection, GCMS/A and CC (CX700M)

- **LVDS Panel Interface**

- Compatible with TIA/EIA-644
- Support panel resolution from VGA through UXGA (1600 x 1200)
- Supports 1 x Dual-Channel / 2 x Single-Channel LVDS panel

- **DVI Panel Interface (optional)**

- Standard compliant with DVI 1.0
- Supports panel resolution from VGA through UXGA (1600 x 1200)
- Supports 1 x Single-Channel DVI panel
- Hot Plug detection input

- **TV-Out Interface (DVP1)**

- 12-bit interface to external TV encoder for NTSC or PAL TV or HDTV display
- Optional 20-bit interface to external TV encoder
- Supports simultaneous SDTV and HDTV display output with the integrated HDTV encoder. (CX700M)

- **12-bit DVI Transmitter Interface (DVP1)**

- Double-data-rate data transfer with clock rates up to 165 MHz
- Built-in digital phase adjuster to fine-tune signal timing between clock and data bus
- Optional 16-bit ARGB interface (DVP1)

- **DuoView+™ Dual Image Capability**

- WinXP, WinME and Win98 multi-monitor, extended desktop support
- Two independent display engines which can display completely different information at different resolutions, pixel depths, and refresh rates
- CRT, LVDS/DVI panel and TV refresh rates are independently programmable for optimum image quality
- Improved display flexibility with simultaneous CRT / LVDS (or DVI), TV / LVDS (or DVI), TV / HDTV and other combined operations

- **Full Software Support**

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible
- Microsoft DirectX Texture Compression (DXTC / S3TC)
- Supports OpenGL™
- Drivers for major operating systems and APIs: Windows® 9x / ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™, DirectShow™ and OpenGL™ ICD for Windows 9x / ME and XP
- Windows NT 4.0 Standard VGA driver

- **Graphics Power Management Support**

- Built-in reference voltage generator and monitor sense circuits
- Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
- External I/O signal controls enabling of graphics accelerator into standby / suspend-off state
- Dynamic clock gating for inactive functions to achieve maximum power saving
- I2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

- **Unified Video Decoding Accelerator**

- **MPEG-2 Decoding Mode**

- Supports VLD (Various Length Decode)
 - Supports iDCT
 - Supports motion compensation
 - Supports MP@HL

- **MPEG-4 Decoding Mode (CX700M)**

- Supports ASP (Advanced Simple Profile) Level 5
 - Supports GMC (Global Motion Compensation) L0 / L1
 - Supports ¼-pixel MC support
 - High video quality and performance

- **WMV9 Decoding Mode (CX700M)**

- Accelerates MP@HL decoding from iDCT to motion compensation
 - Supports adaptive macroblock quantization
 - Supports variable-sized iDCT Transform
 - Supports pre-processing function
 - Supports intensity compensation
 - Supports 4 MVs and long motion vector mode
 - Supports V9 loop filter
 - Supports simple and full quarter-pixel motion compensation
 - Video auto-flipping
 - Hardware DVD sub-picture blending

- **Integrated HDTV Encoder (CX700M)**

- VIA Advance ProScale Technology for studio grade HDTV output
 - HDTV tri-level synchronization and broad pulse insertion
 - Separate adjustable Y U V delay
 - Programmable 2D scaling
 - Adaptive deflicker filter to enhance TV image quality
 - Programmable sharpness / adaptive filter control
 - Support for CGMS-A / Wide Screen Signaling (WSS) / Closed Captioning for variable clock rates adheres to EIAJ-1204, 1204-1, 1204-2 and EN 300 294 standards
 - Multiple Chroma and Luma filters
 - Programmable power save management
 - P:P2 clocking mode or fixed clock mode for full TV screen
 - Automatic detection of TV presence
 - Hot plug interrupt support
 - DAC auto adjustment
 - High Quality 3x10-Bit Video DAC (shared with CRT output)
 - Three flexible and programmable DACs for each specific video signal output
 - Output format
 - Compliant with NTSC (M and J) or PAL (B, D, G, H, I, M, N and Nc) TV system
 - Composite, S-Video, Component (YPbPr) with interlaced or non-interlaced scan output
 - SDTV output mode (525p or 625p) compliant with EIA770-1 and EIA770-2
 - HDTV support for 1080i (D3) and 720p (D4) compliant with EIA770-1, EIA770-2, EIA770-3 and ITU-RBT 709-4
 - Output resolution support NTSC - 525i (480i), 525p (480p), PAL - 625i (576i), 625p (576p), HDTV - 1080i, 720p
 - D-Terminal support from D1 ~ D4 stage
 - Macrovision
 - Macrovision™ 7.1.L1 copy protection support
 - Macrovision™ 1.2 AGC copy protection with 525p / 625p progressive scan output

- **Integrated LVDS / DVI Transmitter**

- **LVDS transmitter**

- Compatible with TIA/EIA-644
 - Support panel resolution from VGA through UXGA (1600 x 1200)
 - Supports one Dual-Channel and two Single-Channel LVDS panel(s)

- **DVI transmitter**

- Standard compliant with DVI 1.0
 - Supports panel resolution from VGA through UXGA (1600 x 1200)
 - Supports one Single-Channel DVI panel
 - Hot Plug detection input

- **High Definition (HD) Audio Controller**

- High performance audio controller with 192 KHz sample rate, 32-bit per sample and up to 8 channels
 - Microsoft UAA (Universal Audio Architecture) driver support
 - Up to two independent playback streams and audio codecs
 - Multiple recording channels for array microphone
 - Supports jack sensing / retasking

- **MC'97 Controller**

- MC'97 modem controller supports up to V.92 standard
 - Modem controller supported by all HSP modem companies

- **Serial ATA Controller**

- Supports up to 2 SATA devices
 - Integrated SATA PHY supporting 1.5 Gbit/s and 3 Gbit/s transfer rate
 - Complies with Serial ATA II PHY Specification
 - Complies with Serial ATA Specification Revision 1.0
 - Supports SATA port multiplier functions

- **Ultra DMA-133 / 100 / 66 / 33 Bus Master EIDE**

- Single channel EIDE controller supporting 2 Enhanced IDE devices
 - Data transfer rate up to 133 MB/sec to cover PIO mode 4, multi-word DMA mode 2, and UltraDMA-133 interface
 - Full scatter gather capability
 - Supports ATAPI compliant devices including DVD devices
 - Supports PCI native and ATA compatibility modes

- **Universal Serial Bus Controller**

- Six USB 2.0 ports, one USB 2.0 root hub, and three USB 1.1 root hubs
 - USB 2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compliant
 - USB 1.1 and Universal Host Controller Interface (UHCI) v1.1 compliant
 - Legacy keyboard and PS/2 mouse support
 - One USB 2.0 debug port

- **Concurrent PCI Bus Controller**
 - PCI 2.3 compliant, 33MHz, 32 bit, 3.3V PCI interface with 5V tolerant inputs
 - Supports up to four PCI masters
 - Zero wait state PCI master and slave burst transfer rate, with up to 132 MB/sec data transfer rate
 - PCI master snoop ahead and snoop filtering
 - Byte merging in the write buffers to reduce the number of PCI cycles
 - Supports delay transaction
 - Transaction timer for fair arbitration between PCI masters
 - Symmetric arbitration between Host / PCI bus for optimized system performance
 - Complete steerable PCI interrupts
 - Supports PC / PCI DMA
- **System Management Bus Interface**
 - Compliant with System Management Bus (SMBus) Revision 2.0
 - I2C devices compatible
 - Supports SMBus Address Resolution Protocol (ARP) by using host commands through software
 - Supports slave interface for external SMBus masters to control resume events
 - Supports Alarm-On-LAN 2 through a SMBus-interfaced register
- **Plug and Play Functions**
 - Steerable PCI interrupts
 - Steerable interrupts for integrated peripheral controllers
 - Microsoft Windows XP, Windows NT, Windows 2000, Windows 98 and plug and play BIOS compliant
- **Integrated Legacy Functions**
 - Integrated Keyboard Controller with PS2 mouse and password wake-up support
 - Integrated two RS-232 serial ports (optional)
 - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM, Day / Month Alarm and century field
 - Integrated DMA, timer, and interrupt controller
 - Fast reset and Gate A20 operation
- **Sophisticated Power Management**
 - ACPI 2.0 and APM v1.2 Compliant
 - Supports CPU clock throttling and clock stop during ACPI C2 / C3 / C4 states
 - Supports PCI clock run, Power Management Enable (PME) control, and PCI / CPU clock generator stop control
 - Supports multiple system suspend types: Power-on Suspend (POS) with flexible CPU / PCI bus reset options, Suspend to DRAM (STR), and Suspend to Disk (soft-off), all with hardware automatic wake-up
 - Multiple suspend power plane controls and suspend status indicators
 - Integrates an idle timer, a peripheral timer and a general purpose timer, plus a 24/32-bit ACPI compliant timer
 - Supports normal, doze, sleep, suspend and conserve modes
 - Global and local device power control
 - Supports system event monitoring with two event classes
 - Primary and secondary interrupt differentiation for individual channels
 - Dedicated input pins for power and sleep buttons, and external modem ring indicator
 - Multiple internal and external SMI sources for flexible power management models
 - Thermal alarm on external temperature sensing circuit
 - Dynamic clock gating control on functional blocks
 - Dynamic I/O pad driving control
 - I/O pad leakage control
- **Built-in NAND-tree pin scan test capability**

CX700 / CX700M SYSTEM OVERVIEW

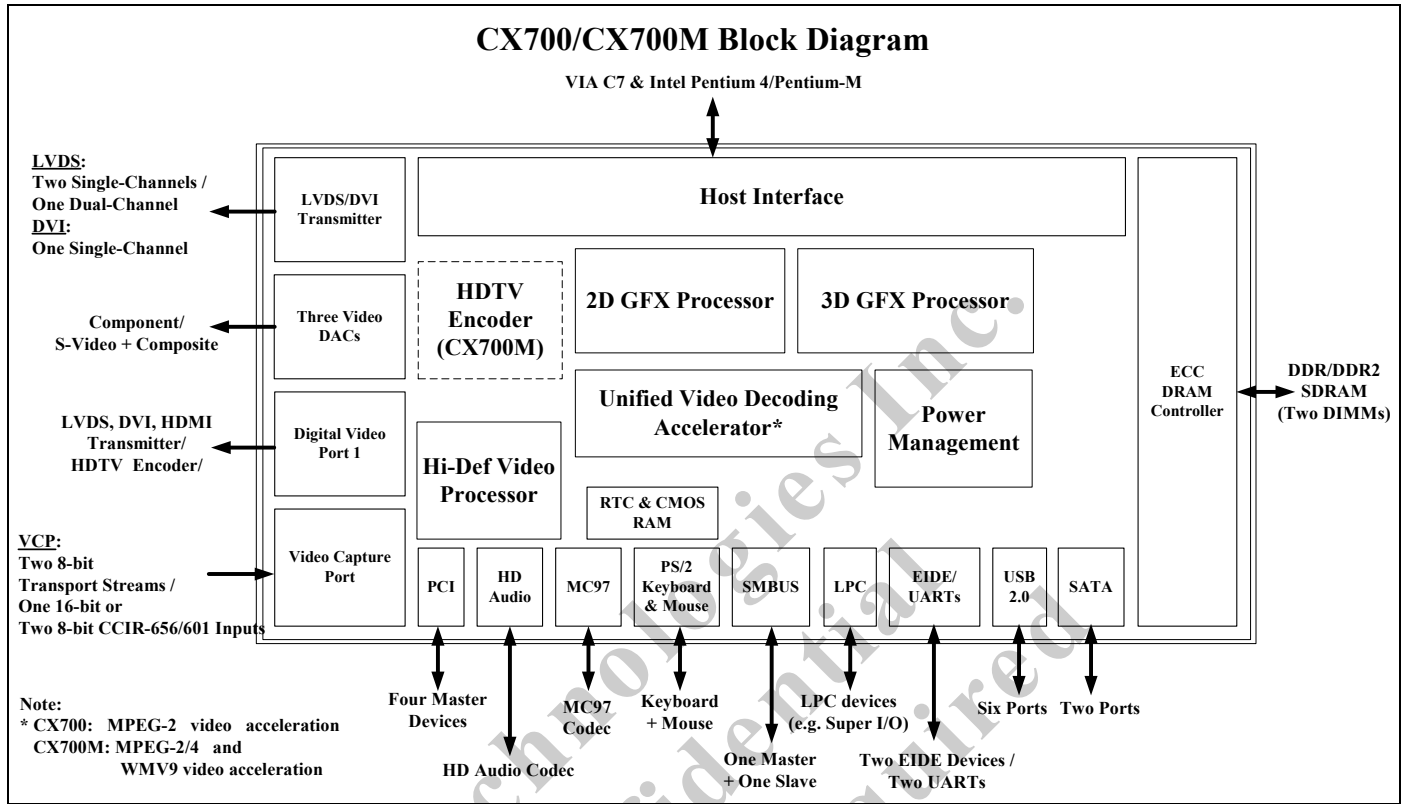


Figure 1. System Block Diagram

The VIA CX700/CX700M is the most advanced and complete all-in-one x86 system processor for today and next generation computing and media processing platforms. From quadruple host data bus, DDR2 memory controller, HDTV interface to Serial ATA and USB ports, the CX700/CX700M integrates all the desired, high quality, high performance controllers of modern media and computing platforms:

Host Interface

The CX700/CX700M supports VIA C7 and Intel Pentium-M processors with up to 533MHz data transfer speed. The host bus protocol is determined through automatic negotiation between CPU and the system processor during reset.

Memory Controller

The CX700/CX700M memory controller supports two DDR/DDR2 DIMMs, up to 4GB system memory. A memory clock buffer is integrated for 1-DIMM system memory architecture. For applications that do not require large system memory or high memory bandwidth, CX700/CX700M supports 32-bit memory data width to reduce total system cost while maintaining adequate memory performance. The memory ECC scheme is integrated to improve the system robustness in applications where high reliability is a priority.

2D / 3D Graphics Processor

The integrated 200MHz, 128-bit UniChrome Pro II graphics processor is implemented on Unified Memory Architecture with frame buffer size of up to 128MB. 32bpp color depth, hardware 2D rotation, true-color hardware cursor and window clipping functions are supported. The high performance 3D graphics processor includes dual pixel rendering pipelines and dual texture units. It delivers up to 4.5 million/second triangle rate, 200 million pixels/second per texture and 400 million texels/second bilinear fill rate for advanced 3D applications.

Unified Video Decoding Accelerator (CX700M)

The CX700M integrates an industry unique, high performance “Unified Video Decoding Accelerator” for high definition MPEG-2/4 as well as the latest WMV9 HD video stream decoding. This feature significantly reduces host processor utilization rate enabling advanced media applications to be implemented without the needs of high frequency CPU, and further reduces the power consumption of the overall platform.

High Quality Video Processor

The video processor supports RGB555 / 565 / 8888 and YUV422 video formats, and it provides complete video processing capability such as 5-tap horizontal and vertical scaling, clockwise / counter-clockwise display rotation, video de-interlacing / interlacing, de-blocking and video gamma correction. Advanced video display features such as video window overlays, sub-picture blending and Microsoft VMR™ support are also implemented for new generation media applications.

Display Interface

The CX700/CX700M provides several types of display interfaces for different applications:

CRT Interface: Three 10-bit 350MHz RAMDAC are integrated for high quality, high resolution (up to 2048x1536 @75Hz refresh rate) monitor.

TV Interface: The CX700M integrates a high definition TV Encoder, and supports YpbPr and CompYC TV interface modes through the three RAMDACs. Supported TV resolutions include NTSC - 525i (480i), 525p (480p), PAL - 625i (576i), 625p (576p), and HDTV - 1080i, 720p.

LCD Panel Interface: A LVDS/DVI Transmitter is integrated, which supports LCD Panel in three different modes:

- One Dual-Channel LVDS Interface
- Two Single-Channel LVDS Interface
- One Single-Channel DVI Interface
- DVO Interface: Two 16-bit DVO interfaces are provided for interfacing to external TV Encoder or DVI Transmitter.

The DuoView+™ feature is implemented with two independent display engines. Each engine can display completely different contents at different resolution, pixel depth and refresh rate. DuoView+™ includes WinXP, WinME and Win98 multi-monitor, extended desktop support; the CRT, LVDS/DVI LCD panel, TV refresh rates are independently programmable for optimum image quality.

High Definition Audio Interface

A high definition audio controller with up to 32-Bit Sample Size @192KHz Sampling Rate is implemented in CX700/CX700M for high-end media applications with up to 8 high definition audio channels.

Storage Device Interface

The CX700/CX700M integrates the Serial ATA and EIDE Controllers. These two controllers provide maximum flexibility in selecting storage devices (both HD and Optical drives). The Serial ATA controller is Serial ATA II PHY compliant and supports up to two SATA IDE devices with 3Gb/s data transfer rate. The EIDE controller supports up to two EIDE devices in PIO mode 4, multi-word DMA mode 2, and UltraDMA-33/66/100/133 modes.

USB Interface

Six USB 2.0/1.1 ports are integrated to support wide ranging connectivity needs on the platform.

In addition, the CX700/CX700M supports PCI bus, LPC bus, MC97, UART as well as legacy functions, such as PS/2 keyboard/mouse and RTC CMOS RAM. Through sophisticated power management scheme and state-of-the-art system functions, VIA CX700/CX700M makes High Performance, Low Power, Thin-&-Light computing/media processing a reality!

BALLOUTS

Ball Map

Figure 2. CX700/CX700M Ball Map (C7 and P4 CPU Interface) – Left Side Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	HD62#	HD STB3N#	HD STB3P#	HD52#	HD49#	HD53#	HD34#	HD35#	HD38#	HDBI2#	HD18#	HD30#	HD31#	HD23#	HD20#	HD22#	HD3#	HIT#
B	GND	HD51#	HD55#	GND	GND	HD57#	GND	HD STB2P#	HD37#	GND	HD STB1P#	GND	GND	HD25#	HD16#	GND	GND	RS1#
C	HD58#	HD59#	HD60#	HD61#	HD56#	HD54#	GND	HD STB2N#	HD36#	GND	HD19#	HD STB1N#	HD24#	HDBI1#	HD21#	HD9#	HD13#	RS0#
D	CPURST#	GND	GND	HDBI3#	GND	HD63#	HD41#	HD47#	HD44#	HD39#	HD28#	GND	GND	HD29#	HD17#	GND	GND	DEFER#
E	VTT	VTT	VTT	VTT	GND	HD50#	HD42#	HD32#	HD33#	HD43#		HD27#	HD26#	HD14#	HD STB0P#	HD2#	HD7#	DRDY#
F	VTT	VTT	VTT	VTT	VTT	VTT	HD48#	GND	HD40#	GND		GND	GND	HD STB0N#	HD4#	GND	GND	DPWR#
G	VTT	VTT	VTT	VTT	VTT	VTT	VTT	GND	HD46#	HD45#	GND	GND	GND	HD10#	HD1#	HD11#	HD6#	GND
H	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT						TP3	HD5#	GND	HDBI0#	HD8#
J	LCD2 DO0+	LCD2 DO0-		VTT	VTT	VTT	VTT	VTT	VTT		TP1		TP2	GTL VREF1				
K	GND LVDS	LCD2 DO1+	LCD2 DO1-	GND LVDS	VTT	VTT	VTT	VTT			GCLK				HD12#	GND	HD15#	HD0#
L	LCD2 CLK-	LCD2 CLK+	LCD2 DO2+	LCD2 DO2-		VTT	VTT	VTT										
M	LCD2 DO3+	LCD2 DO3-	LCD1 DO3+	LCD1 DO3-	GND LVDSPLL	VCC33 LVDS												
N	GND LVDS	LCD1 CLK+	LCD1 CLK-	GND LVDS	VCCA33 LVDSPLL1	VCC33 LVDS	GND LVDS											
P	LCD1 DO2+	LCD1 DO2-	VCCA33 LVDS	VCCA33 LVDSPLL2	GND LVDSPLL	VCC33 LVDS	GND LVDS											
R	LCD1 DO1-	LCD1 DO1+	GND LVDS	GND LVDS	GND LVDS	VCC33 LVDS	GND LVDS											
T	GND LVDS	LCD1 DO0-	LCD1 DO0+	GND LVDS	SW_REXT	VCC33 LVDS	GND LVDS											
U	AB	AG	GND DAC	VCCA33 DAC1	VCCA33 DAC2	GND DAC												
V	AR	GND DAC	RSET	VCCA33 PLL3	GND PLL	VCCA33 PLL2	GND PLL											
W	VCCA33 TVPLL	GND TVPLL	VCCA33 PLL1	GND PLL														
Y	TVX0	TVX1	ENVDD1	ENVBLD1	ENVDD2	ENVBLD2												
AA	SPD1	SPCLK1	SPCLK2	SPD2	BISTIN	HSYNC	VSU33											
AB		DVP1 D0	DVP1 HS	DIS PCLKO2	DIS PCLKI2	GPIOB	GPIOA	XIN										
AC	DVP1 D4	DVP1 D1	DVP1 D2	DVP1 VS		RSVD3	RSVD4	RSVD2										
AD	DVP1 D6	DVP1 CLK	DVP1 D5	DVP1 D3														
AE		DVP1 D8	DVP1 TVCLKR	DVP1 DET														
AF		DVP1 D10	DVP1 D15	DVP1 D7														
AG	DVP1 D12	DVP1 TVFLD	DVP1 D11	DVP1 DE	DVP1 D9	VCP0VS	VCP0D2	VCP0HS	VCP0D0									
AH	DVP1 D13	DVP1 D14	VCP0D5	VCP0D4	VCP0CLK	VCP0D3	VCP0D1		TP8			GND	GND					
AJ	VCP0D7	TS0ERR	VCP1CLK	VCP1D0	VCP0D6	VCP1D7	VCP1D2	VCP1D3				VSUS15	VSUS15		PWRBTN#	TP7		
AK	VCP1D1	VCP1HS	VCP1VS	VCP1D4	VCP1D5	VCP1D6	TS1ERR	PCIDGNT	PCIDREQ			VSUS33	VSUS33	VSUS33	TESTIN#	SMB CLK2	CPUSTP#	
AL	INTA#	INTC#	INTB#	AD27	AD26	AD24	DEVSEL#	PERR#	AD12	PCICLK		MC RST	KB CK	RING#	PME#	SMB DATA2	VRDRLP	SPKR
AM	INTD#	GNT1#	GNT2#	AD25	TRDY#	STOP#	AD13	AD10	CBE0#	AD1		MC SYNC	KB DT	SUSC#	SUSA#	SMB CLK1	SERIRQ	VGATE
AN	GNT0#	AD30	REQ0#	REQ3#	AD20	AD16	AD11	AD9	AD8	AD0		MC SDIN	MS CK	AOL	EXTSMI#	SMB DATA1	INTRU DER#	PCISTP#
AP	REQ1#	REQ2#	AD31	CBE3#	AD18	IRDY#	CBE1#	AD7	AD4		AZ SYNC	AZ SDIN1	MC BCLK	MS DT	BATLOW#	SMB ALRT#	THR#	RSMRST#
AR	GNT3#	AD28	AD22	PAR	CBE2#	SERR#	AD15	AD6	AD3		AZ RST#	AZ BITCLK	MC SDOUT	SUSB#			RTCX2	PWRGD
AT	AD29	AD23	AD21	AD17	FRAME#	AD19	AD14	AD5	AD2		PCIRST#	AZ SDIN0	MC SDOUT	LID#			RTCX1	VBAT

Signal Ball List

Table 1. CX700/CX700M Signal Ball List (Listed by Ball Name)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
F30	A20M#	AM22	DCD2	AP14	GPI4	F17	HD07#	D20	HITM#	AI12	MCRST
U01	AB	D18	DEFER#	AN15	GPI5	H17	HD08#	E19	HLOCK#	AN12	MCSDIN
AN10	AD0	AL07	DEVSEL#	AN17	GPI6	C16	HD09#	C21	HREQ0#	AR12	MCS DOUT
AM10	AD1	B31	DFTIN#	AT13	GPI7	G14	HD10#	D22	HREQ1#	AM12	MCSYNC
AT09	AD2	AB06	DISPCLKI2	AL14	GPI8	G16	HD11#	A22	HREQ2#	AC27	MD0
AR09	AD3	AB05	DISPCLKO2	AP16	GPI9	J14	HD12#	A20	HREQ3#	AB29	MD1
AP09	AD4	A31	DMCOMP	C28	GPI10	C17	HD13#	A21	HREQ4#	AC32	MD2
AT08	AD5	B30	DPSLP#	AM18	GPI11	E14	HD14#	AA06	HSYNC	AB32	MD3
AR08	AD6	F18	DPWR#	AL16	GPI00	J16	HD15#	D19	HTRDY#	AB27	MD4
AP08	AD7	AC30	DOM0	AK16	GPI01	B15	HD16#	E29	IGNNE#	AB28	MD05
AN09	AD8	W32	DQM1	AK09	GPI02	D15	HD17#	B29	INIT#	AC31	MD06
AN08	AD9	AB36	DQM2	AK08	GPI03	A11	HD18#	AL01	INTA#	AB31	MD07
AM08	AD10	W33	DQM3	AB08	GPI0A	C11	HD19#	AL03	INTB#	W28	MD08
AN07	AD11	M34	DQM4	AB07	GPI0B	A15	HD20#	AL02	INTC#	W29	MD09
AL09	AD12	H36	DQM5	AB06	GPI0C	C15	HD21#	AM01	INTD#	V33	MD10
AM07	AD13	D36	DQM6	AB05	GPI0D	A16	HD22#	A30	INTR	V30	MD11
AT07	AD14	C33	DQM7	AL22	GPO0	A14	HD23#	AN17	INTRUDER#	V29	MD12
AR07	AD15	AB30	DQS0	AT20	GPO1	C13	HD24#	AP06	IRDY#	W30	MD13
AN06	AD16	W31	DQS1	AT22	GPO2	B14	HD25#	AH22	IRQ15	V31	MD14
AT04	AD17	AB33	DQS2	AG22	GPO3	E13	HD26#	AL13	KBCK	V32	MD15
AP05	AD18	W36	DQS3	AR22	GPO4	E12	HD27#	AM13	KBDT	AC34	MD16
AT06	AD19	M35	DQS4	AM12	GPO5	D11	HD28#	N03	LCD1CLK-	AC36	MD17
AN05	AD20	H33	DQS5	AL12	GPO6	D14	HD29#	N02	LCD1CLK+	AA34	MD18
AT03	AD21	D35	DQS6	AL18	GPO7	A12	HD30#	T02	LCD1DO0-	AA36	MD19
AR03	AD22	A33	DQS7	AM15	GPO8	A13	HD31#	T03	LCD1DO0+	AC33	MD20
AT02	AD23	P32	DQS8	AR13	GPO9	E08	HD32#	R01	LCD1DO1-	AC35	MD21
AL06	AD24	E18	DRDY#	AM14	GPO10	E09	HD33#	R02	LCD1DO1+	AA35	MD22
AM04	AD25	AP21	DSR1	H20	GTLVREF0	A07	HD34#	P02	LCD1DO2-	AA33	MD23
AL05	AD26	AH20	DSR2	J12	GTLVREF1	A08	HD35#	P01	LCD1DO2+	Y34	MD24
AL04	AD27	AN20	DTR1	B21	HA03#	C09	HD36#	M04	LCD1DO3-	Y35	MD25
AR02	AD28	AL20	DTR2	D25	HA04#	B09	HD37#	M03	LCD1DO3+	U33	MD26
AT01	AD29	AD02	DVP1CLK	A24	HA05#	A09	HD38#	L01	LCD2CLK-	U34	MD27
AN02	AD30	AB03	DVP1D0	D24	HA06#	D10	HD39#	L02	LCD2CLK+	Y36	MD28
AP03	AD31	AC02	DVP1D1	B24	HA07#	F09	HD40#	J02	LCD2D00-	Y33	MD29
A19	ADS#	AC03	DVP1D2	C25	HA08#	D07	HD41#	J01	LCD2D00+	V36	MD30
U02	AG	AD04	DVP1D3	C24	HA09#	E07	HD42#	K03	LCD2DO1-	U35	MD31
AN14	AOL	AC01	DVP1D4	A25	HA10#	E10	HD43#	K02	LCD2DO1+	N36	MD32
V01	AR	AD03	DVP1D5	B25	HA11#	D09	HD44#	L04	LCD2DO2-	M33	MD33
AR11	AZBITCLK	AD01	DVP1D6	A26	HA12#	G10	HD45#	L03	LCD2DO2+	L36	MD34
AR10	AZRST#	AF05	DVP1D7	E25	HA13#	G09	HD46#	M02	LCD2DO3-	K33	MD35
AT11	AZSDIN0	AE03	DVP1D8	D26	HA14#	D08	HD47#	M01	LCD2DO3+	N35	MD36
AP11	AZSDIN1	AG05	DVP1D9	E26	HA15#	F07	HD48#	AT13	LID#	M36	MD37
AT12	AZSDOUT	AF03	DVP1D10	E27	HA16#	A05	HD49#	AR19	LPCAD0	L33	MD38
AP10	AZSYNC	AG03	DVP1D11	A27	HA17#	E06	HD50#	AT19	LPCAD1	K36	MD39
L29	BA0	AG01	DVP1D12	F27	HA18#	B02	HD51#	AN19	LPCAD2	J36	MD40
L32	BA1	AH01	DVP1D13	D21	HA19#	A04	HD52#	AM19	LPCAD3	J33	MD41
AP14	BATLOW#	AH02	DVP1D14	E24	HA20#	A06	HD53#	AK19	LPCDRQ0#	G35	MD42
AA05	BISTIN	AF04	DVP1D15	E23	HA21#	C06	HD54#	AL19	LPCDRQ1#	G34	MD43
F19	BNR#	AG04	DVP1DE	G23	HA22#	B03	HD55#	AP19	LPCFRAME#	J34	MD44
E20	BPRI#	AE05	DVP1DET	F22	HA23#	C05	HD56#	L30	MA0	J35	MD45
C19	BREQ0#	AB04	DVP1HS	E22	HA24#	B06	HD57#	L28	MA1	G36	MD46
AM09	CBE0#	AE04	DVP1TVCLKR	J22	HA25#	C01	HD58#	N27	MA2	F33	MD47
AP07	CBE1#	AG02	DVP1TVFLD	H21	HA26#	C02	HD59#	N30	MA3	F36	MD48
AR05	CBE2#	AC04	DVP1VS	H22	HA27#	C03	HD60#	N32	MA4	F35	MD49
AP04	CBE3#	Y04	ENVBLD1	E21	HA28#	C04	HD61#	P30	MA5	D33	MD50
T31	CKE0	Y06	ENVBLD2	F23	HA29#	A01	HD62#	N31	MA6	A36	MD51
T30	CKE1	Y03	ENVDD1	B27	HA30#	D06	HD63#	P28	MA7	F34	MD52
T32	CKE2	Y05	ENVDD2	H23	HA31#	H16	HDBI0#	P29	MA8	E36	MD53
T33	CKE3	AN15	EXTSMI#	A23	HADSTB0N#	C14	HDBI1#	P27	MA9	D34	MD54
AP18	CLKRUN#	D30	FERR#	C23	HADSTB0P#	A10	HDBI2#	L31	MA10	C36	MD55
D01	CPURST#	AT05	FRAME#	G22	HADSTB1#	D04	HDBI3#	T28	MA11	B35	MD56
AK17	CPUSTP#	K11	GCLK	K23	HCLK-	F14	HDSTB0N#	T29	MA12	A34	MD57
K29	CS0#	AN01	GNT0#	L23	HCLK+	E15	HDSTB0P#	G30	MA13	C32	MD58
H32	CS1#	AM02	GNT1#	J17	HD00#	C12	HDSTB1N#	AP12	MCBCLK	A32	MD59
G32	CS2#	AM03	GNT2#	G15	HD01#	B11	HDSTB1P#	AD35	MCLKO0-	A35	MD60
G31	CS3#	AR01	GNT3#	E16	HD02#	C08	HDSTB2N#	AD34	MCLKO0+	D32	MD61
AP20	CTS1	AH22	GPI0	A17	HD03#	B08	HDSTB2P#	R35	MCLKO1-	B33	MD62
AG20	CTS2	AP12	GPI1	F15	HD04#	A02	HDSTB3N#	R34	MCLKO1+	D31	MD63
B19	DBSY#	AN12	GPI2	H14	HD05#	A03	HDSTB3P#	E33	MCLKO2-	K28	MEMVREF0
AH21	DCD1	AN14	GPI3	G17	HD06#	A18	HIT#	E32	MCLKO2+	V27	MEMVREF1

CX700/CX700M Signal Ball List Continued (Listed by Ball Name)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
T35	MPD0	AH21	PDD6	J25	RSVD1	AR35	SRX0+	R01	TX0-	AH06	VCP0D3
T36	MPD1	AG21	PDD7	AC08	RSVD2	AT33	SRX1-	R02	TX0+	AH04	VCP0D4
P33	MPD2	AG20	PDD8	AC06	RSVD3	AR33	SRX1+	P02	TX1-	AH03	VCP0D5
N34	MPD3	AH20	PDD9	AC07	RSVD4	AM06	STOP#	P01	TX1+	AJ05	VCP0D6
U36	MPD4	AJ20	PDD10	AT16	RTCX1	C29	STPCLK#	N03	TX2-	AJ01	VCP0D7
T34	MPD5	AL20	PDD11	AR16	RTCX2	AN35	STX0-	N02	TX2+	AG08	VCP0HS
P36	MPD6	AL21	PDD12	AN21	RTS1	AM35	STX0+	T02	TXC-	AG06	VCP0VS
N33	MPD7	AK21	PDD13	AJ20	RTS2	AN33	STX1-	T03	TXC+	AJ03	VCP1CLK
AN13	MSCK	AM22	PDD14	AJ23	SATALED#	AM33	STX1+	AT23	USBCLK	AJ04	VCP1D0
AP13	MSDT	AT21	PDD15	AJ33	SATA50COMP	AM15	SUSA#	AL23	USBOC0#	AK01	VCP1D1
C30	NMI	AJ22	PDDACK#	K30	SCAS#	AR13	SUSB#	AP23	USBOC1#	AJ07	VCP1D2
H29	ODT0	AR20	PDDREO	AM20	SDOUT1	AM14	SUSC#	AN23	USBOC2#	AJ08	VCP1D3
G33	ODT1	AL22	PDIOR#	AK21	SDOUT2	T05	SW_REXT	AM23	USBOC3#	AK04	VCP1D4
F32	ODT2	AK22	PDIORDY	AM17	SERIRQ	K31	SWE#	AK23	USBOC4#	AK05	VCP1D5
F30	ODT3	AT20	PDIOW#	AR06	SERR#	AK35	SXI	AK24	USBOC5#	AK06	VCP1D6
AR04	PAR	AL08	PERR#	AK20	SIN1	AK36	SXO	AN29	USBP0-	AJ06	VCP1D7
AL10	PCICLK	AL15	PME#	AL21	SIN2	AK15	TESTIN#	AM29	USBP0+	AK02	VCP1HS
AK08	PCIDGNT	AJ15	PWRBTN#	B28	SLP#	AP16	THR#	AR29	USBP1-	AK03	VCP1VS
AK09	PCIDREQ	AR17	PWRGD	AP15	SMBALRT#	C28	THRMTRIP#	AT29	USBP1+	AM18	VGATE
AT10	PCIRST#	AN03	REO0#	AM16	SMBCLK1	J10	TP1	AR27	USBP2-	AL17	VRDSLP
AN18	PCISTP#	AP01	REQ1#	AK16	SMBCLK2	J11	TP2	AT27	USBP2+	AA07	VSYNC
AT22	PDA0	AP02	REQ2#	AN16	SMBDATA1	H12	TP3	AN27	USBP3-	AB09	XIN
AG22	PDA1	AN04	REQ3#	AL16	SMBDATA2	J24	TP4	AM27	USBP3+		
AR22	PDA2	AG21	RI1	D29	SMI#	H24	TP5	AR25	USBP4-		
AN22	PDCS1#	AT21	RI2	AA02	SPCLK1	AJ19	TP6	AT25	USBP4+		
AP22	PDCS3#	AL14	RING#	AA03	SPCLK2	AJ16	TP7	AN25	USBP5-		
AP20	PDD0	C18	RS0#	AA01	SPD1	AH09	TP8	AM25	USBP5+		
AP21	PDD1	B18	RS1#	AA04	SPD2	AM05	TRDY#	AR23	USBREXT		
AN21	PDD2	G19	RS2#	AL18	SPKR	AJ02	TS0ERR	AH05	VCP0CLK		
AN20	PDD3	V03	RSET	K32	SRAS#	AK07	TS1ERR	AG09	VCP0D0		
AK20	PDD4	AP17	RSMRST#	AJ34	SREXT	Y02	TVXI	AH07	VCP0D1		
AM20	PDD5	K25	RSVD0	AT35	SRX0-	Y01	TVXO	AG07	VCP0D2		

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Table 2. Power / Ground Ball List

Ball Name	Ball Numbers
GND	B01, B04, B05, B07, B10, B12, B13, B16, B17, B20, B22, B23, B26, B32, B34, B36 C07, C10, C20, C22, C26, C27, C31, C34, C35, D02, D03, D05, D12, D13, D16, D17, D23, D27 E05, E31, E34, E35, F08, F10, F12, F13, F16, F17, F20, F21, F24, F25, F26, G08, G11, G12, G13, G18, G20, G21, G24 H15, H34, H35, J15, J18, J21, K34, K35, L34, L35, P34, P35, R33, R36, T16, T18, T20, U17, U19, U21, U30, U31 V16, V18, V20, V34, V35, W17, W19, W21, W27, W34, W35, Y16, Y18, Y20, Y28, Y30, Y31 AA17, AA19, AA28, AA30, AA31, AB34, AB35, AC28, AC29, AD32, AD33, AD36, AF21, AH12, AH13, AJ21, AM21, AR21
GND A15SATA	AK34, AL32, AL33, AL34, AL35, AL36, AM32, AM34, AM36, AN32, AN34, AN36, AP32, AP33, AP34, AP35, AP36, AR32, AR34, AR36, AT32, AT34, AT36
GND A15PLLUSB	AH23
GND A33SATA	AK31, AL31, AM31
GND A33PLLUSB	AG23
GND ADAC	U03, U06, V02
GND AHCK	L24
GND ALVDS	R04
GND ALVDSPLL	M05, P05
GND APLL	V05, V07, W04
GND APLLSATA	AK32
GND ASXO	AJ35
GND ATVPLL	W02
GND LVDS	K01, K04, N01, N04, N07, P07, P14, P15, R03, R05, R07, R14, R15, T01, T04, T07, T14, T15
GND USB	AL24, AL25, AL26, AL27, AL28, AL29, AL30, AM24, AM26, AM28, AM30 AN24, AN26, AN28, AN30, AP24, AP25, AP26, AP27, AP28, AP29, AP30 AR24, AR26, AR28, AR30, AT24, AT26, AT28, AT30
VBAT	AT17
VCC15	T17, T19, T21, U16, U18, U20, V17, V19, V21, W16, W18, W20, Y17, Y19, Y21 AA16, AA18, AA20, AA21, AA22, AA23, AB21, AB22, AB23, AC21, AC22, AC23, AD28, AD29, AD30, AD31 AE28, AE29, AE30, AE31, AE32, AE33, AE34, AE35, AE36, AF28, AF29, AF30, AF31, AF32, AF33, AF34, AF35, AF36 AG28, AG29, AG30, AG31, AG32, AG33, AG34, AG35, AG36, AH28, AH29, AH30, AH31, AH32, AH33, AH34, AH35, AH36
VCC33	Y14, Y15, AA14, AA15, AB14, AB15, AB16, AB17, AB19, AB20, AC14, AC15, AC16, AC17, AC19, AC20
VCC33CPU	P23
VCC33LVDS	M06, N06, P06, R06, T06
VCC33USB	AJ25, AJ26, AJ27, AK25, AK26, AK27
VCCA15SATA	AJ28, AJ29, AK28, AK29
VCCA15SXO	AJ36
VCCA15PLLUSB	AJ24
VCCA33DAC[2:1]	U05, U04
VCCA33HCK	K24
VCCA33LVDS	P03
VCCA33LVDSPLL[2:1]	P04, N05
VCCA33PLL[3:1]	V04, V06, W03
VCCA33SATA	AN31, AP31, AR31, AT31
VCCA33PLLSATA	AK33
VCCA33TVPLL	W01
VCCA33PLLUSB	AH24
VCCMEM	F31, H30, H31, J29, J30, J31, M28, M29, M30, M31, N28, N29, P31, R23, R28, R29, R31, R32 T22, T23, U22, U23, V22, V23, W22, W23, Y22, Y23
VSUS15	AJ12, AJ13
VSUS15MEM	V26
VSUS15USB	AG24
VSUS33	AB18, AK11, AK12, AK13
VTT	E01, E02, E03, E04, F01, F02, F03, F04, F05, F06, G01, G02, G03, G04, G05, G06, G07 H01, H02, H03, H04, H05, H06, H07, H08, J03, J04, J05, J06, J07, J08, K05, K06, K07, K08 L06, L07, L08, P16, P17, P18, P19, P20, P21, P22, R16, R17, R18, R19, R20, R21, R22

Signal Descriptions

CPU Interface

The CPU interface supports two possible host protocols: VIA V4 and Intel P4. Strapping ball TP[7:5] are used to select the operating mode for the interface. See the Strapping Table for the setup.

CPU Interface (VIA V4 or Intel P4 Host Protocol)				
Signal Name	Ball #	I/O	Signal Description	Power Plane
HCLK+/-	L23, K23	I	Host Clock. CPU clock (100 / 133 MHz).	VTT
HA[31:3]#	(see ball list)	IO	P4 Host Data Address. (P4 Host Protocol) HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by CX700 during cache snooping operations. (V4 Host Protocol) Signal balls HA[30] and HA[16:3] are used. Host data addresses are transferred in 4X rate in V4 host protocol. On beat 0 and 2, address bits HA[30, 16:3] are transferred on signal balls HA[30, 16:3]. On beat 1 and 3, address bits HA[31, HAP, 29:17] are transferred on signal balls HA[30, 16:3].	VTT
HD[63:0]#	(see ball list)	IO	Host Data. These signals are connected to the CPU data bus.	VTT
ADS#	A19	IO	Address Strobe. The CPU asserts ADS# in T1 of the CPU bus cycle.	VTT
BNR#	F19	IO	Block Next Request. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.	VTT
BPRI#	E20	IO	Priority Agent Bus Request. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted.	VTT
DBSY#	B19	IO	Data Bus Busy. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.	VTT
DEFER#	D18	IO	Defer. A dynamic deferring policy is used to optimize system performance. The DEFER# signal is also used to indicate a processor retry response.	VTT
DRDY#	E18	IO	Data Ready. Asserted for each cycle that data is transferred.	VTT
HIT#	A18	IO	Hit. Indicates that a caching agent holds the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.	VTT
HITM#	D20	I	Hit Modified. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.	VTT
HLOCK#	E19	I	Host Lock. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.	VTT
HREQ[4:0]#	A21, A20, A22, D22, C21	IO	Host Request Command. (P4 Host Protocol) Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. (V4 Host Protocol) Signal balls HREQ[2:0] are used. Host request commands are transferred in 4X rate in V4 host protocol. On beat 0 and 2, host request bits HREQ[2:0] are transferred on signal balls HREQ[2:0]. On beat 1 and 3, host request bits HREQ[4:3] are transferred on signal balls HREQ[1:0].	VTT

CPU Interface (VIA V4 or Intel P4 Host Protocol) – continued				
Signal Name	Ball #	I/O	Signal Description	Power Plane
HTRDY#	D19	IO	Host Target Ready. Indicates that the target of the processor transaction is able to enter the data transfer phase.	VTT
RS[2:0]#	G19, B18, C18	IO	Response Signals. Indicates the type of response per the table below: RS[2:0]# Response type 000 Idle State 001 Retry Response 010 Defer Response 011 Reserved 100 Hard Failure 101 Normal Without Data 110 Implicit Writeback 111 Normal With Data	VTT
CPURST#	D01	O	CPU Reset. Reset output to CPU. External pull-up and filter capacitor to ground should be provided per CPU manufacturer's recommendations.	VTT
BREQ0#	C19	I	Bus Request 0. Connect to CPU bus request 0.	VTT
HDBI[3:0]#	D04, A10, C14, H16	IO	Host Dynamic Bus Inversion. Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data signal group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted to limit the number of switching data signals simultaneously.	VTT
HADSTB0P# HADSTB0N# HADSTB1#	C23 A23 G22	IO	Host Address Strobe. (P4 Host Protocol) Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HADSTB1# is the strobe for HA[31:17]# and HADSTB0P# is the strobe for HA[16:3] and HREQ[4:0]#. (V4 Host Protocol) HADSTB0P# / HADSTB0N# are differential synchronous strobes used to transfer HA[30, 16:3]# and HREQ[2:0]# at a 4x transfer rate.	VTT
HDSTB[3:0]P# HDSTB[3:0]N#	A03, B08, B11, E15 A02, C08, C12, F14	IO	Host Differential Data Strobes. Source synchronous strobes used to transfer HD[63:0]# & HDBI[3:0]# at a 4x transfer rate. HDSTB3P# / HDSTB3N# are the strobes for HD[63:48]# & HDBI3#; HDSTB2P# / HDSTB2N# are the strobes for HD[47:32]# & HDBI2#; HDSTB1P# / HDSTB1N# are the strobes for HD[31:16]# & HDBI1#; and HDSTB0P# / HDSTB0N# are the strobes for HD[15:0]# & HDBI0#.	VTT
DPWR#	F18	O	Data Bus Power Reduction. Request to reduce power on the mobile CPU data bus input buffer. HIGH will disable the CPU data bus input buffer.	VTT

CPU Control Interface (VIA V4 and Intel P4 Host Protocols)				
Signal Name	Ball #	I/O	Signal Description	Power Plane
A20M#	E30	OD	A20 Mask. Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port92 bit-1 (Fast A20).	VCC33CPU
FERR#	D30	I	Numerical Coprocessor Error. This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.	VCC33CPU
IGNNE#	E29	OD	Ignore Numeric Error. This signal is connected to the CPU "ignore error" signal.	VCC33CPU

CPU Control Interface (VIA V4 and Intel P4 Host Protocols) - continued				
Signal Name	Ball #	I/O	Signal Description	Power Plane
INIT#	B29	OD	Initialization. INIT# is asserted if a shut-down special cycle on the PCI bus is detected or if a soft reset is initiated by the register.	VCC33CPU
INTR	A30	OD	CPU Interrupt. INTR is driven by the CX700 to signal the CPU that an interrupt request is pending and needs service.	VCC33CPU
NMI	C30	OD	Non-Maskable Interrupt. NMI is used to force a non-maskable interrupt to the CPU. CX700 generates an NMI when PCI bus SERR# is asserted.	VCC33CPU
SLP#	B28	OD	Sleep. Used to put the CPU into a sleep state.	VCC33CPU
SMI#	D29	OD	System Management Interrupt. SMI# is asserted by CX700 to the CPU in response to power management events.	VCC33CPU
STPCLK#	C29	OD	Stop Clock. This signal is asserted by the CX700 to throttle the processor clock.	VCC33CPU
THRMTRIP# / GPI10	C28	I	Thermal Detect Power Down. This signal indicates a thermal trip from the processor. THRMSTRIP# can optionally be used as GPI10.	VCC33CPU
DPSLP#	B30	OD	CPU Deep Sleep. Used to put the CPU into a deeper sleep mode.	VCC33CPU

DDR/DDR2 SDRAM Memory Interface

SDRAM Memory Interface supports two operating modes: DDR or DDR2 mode. Signal ball TP8 is used to select the operating mode for the interface. See the Strapping Table for the setup.

DDR/DDR2 SDRAM Memory Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
MA[13:0]	(see ball list)	O	DRAM Row/Column Address.	VCCMEM
BA[1:0]	L32, L29	O	DRAM Bank Address.	VCCMEM
SRAS#	K32	O	DRAM Row Address Strobe.	VCCMEM
SCAS#	K30	O	DRAM Column Address Strobe.	VCCMEM
SWE#	K31	O	DRAM Write Enable.	VCCMEM
MD[63:0]	(see ball list)	IO	Memory Data. In 32-bit memory interface mode, connect memory data lines to MD[31:0].	VCCMEM
MPD[7:0]	(see ball list)	IO	Memory Parity Data Bits. For ECC function.	VCCMEM
DQM[7:0]	(see ball list)	O	Memory Data Mask. Data mask for the eight data bytes.	VCCMEM
ODT[3:0]	F30, F32, G33, H29	O	DDR2 On-Die Termination Enable. For the four DDR2 memory banks. Not used in DDR mode.	VCCMEM
DQS[8:0]	(see ball list)	IO	DDR/DDR2 Memory Data Strobes. Data strobe for the eight data bytes and the MPD[7:0] byte.	VCCMEM
CS[3:0]#	G31, G32, H32, K29	O	Memory Chip Select. Chip select for the four memory banks.	VCCMEM
CKE[3:0]	T33, T32, T30, T31	O	Memory Clock Enable. For the four memory banks to enable DRAM power down mode.	VCCMEM
MCLKO[2:0]+ MCLKO[2:0]-	E32, R34, AD34 E33, R35, AD35	O	Differential Memory Clock Output. In one DIMM system memory configuration, connect memory clock outputs to the DIMM socket directly. Use Zero Delay buffer for two DIMM system memory configurations.	VCCMEM

LVDS / DVI Interface

LVDS/DVI interface supports three possible operating modes: one dual-channel LVDS mode, two single-channel LVDS mode or one single-channel DVI mode. Signal balls DVP1D[15:14] are used to select the operating mode for the interface. See the Strapping Table for the setup.

LVDS Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
LCD1DO0+/- TXC+/-	T03, T02	O	LVDS Single Channel Mode: LVDS Differential Data Output 0 for Panel 1. LVDS Dual Channel Mode: LVDS Differential Data Output 0. In DVI Mode, used as DVI Differential Clock Output.	VCC33LVDS
LCD1DO1+/- TX0+/-	R02, R01	O	Single Channel Mode: LVDS Differential Data Output 1 for Panel 1. Dual Channel Mode: LVDS Differential Data Output 1. In DVI Mode, used as DVI Differential Data Output 0.	VCC33LVDS
LCD1DO2+/- TX1+/-	P01, P02	O	Single Channel Mode: LVDS Differential Data Output 2 for Panel 1. Dual Channel Mode: LVDS Differential Data Output 2. In DVI Mode, used as DVI Differential Data Output 1.	VCC33LVDS
LCD1DO3+/-	M03, M04	O	Single Channel Mode: LVDS Differential Data Output 3 for Panel 1. Dual Channel Mode: LVDS Differential Data Output 3.	VCC33LVDS
LCD2DO0+/-	J01, J02	O	Single Channel Mode: LVDS Differential Data Output 0 for Panel 2. Dual Channel Mode: LVDS Differential Data Output 4.	VCC33LVDS
LCD2DO1+/-	K02, K03	O	Single Channel Mode: LVDS Differential Data Output 1 for Panel 2. Dual Channel Mode: LVDS Differential Data Output 5.	VCC33LVDS
LCD2DO2+/-	L03, L04	O	Single Channel Mode: LVDS Differential Data Output 2 for Panel 2 Dual Channel Mode: LVDS Differential Data Output 6.	VCC33LVDS
LCD2DO3+/-	M01, M02	O	Single Channel Mode: LVDS Differential Data Output 3 for Panel 2 Dual Channel Mode: LVDS Differential Data Output 7.	VCC33LVDS
LCD1CLK+/- TX2+/-	N02, N03	O	Single Channel Mode: LVDS Differential Clock Output for Panel 1. Dual Channel Mode: Not Connected. In DVI mode, used as DVI Differential Data Output 2.	VCC33LVDS
LCD2CLK+/-	L02, L01	O	Single Channel Mode: LVDS Differential Clock Output for Panel 2. Dual Channel Mode: LVDS Differential Clock Output.	VCC33LVDS

DVI Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
TXC+/- LCD1DO0+/-	T03, T02	O	DVI Differential Clock Output. In LVDS mode, used as Channel 1 differential data output 0.	VCC33LVDS
TX0+/- LCD1DO1+/-	R02, R01	O	DVI Differential Data Output 0. In LVDS mode, used as Channel 1 differential data output 1.	VCC33LVDS
TX1+/- LCD1DO2+/-	P01, P02	O	DVI Differential Data Output 1. In LVDS mode, used as Channel 1 differential data output 2.	VCC33LVDS
TX2+/- LCD1CLK+/-	N02, N03	O	DVI Differential Data Output 2. In LVDS mode, used as Channel 1 differential clock output.	VCC33LVDS
SW_REXT	T05	AI	Voltage Swing Adjustment of Pixel Channel in DVI Mode This signal controls the amplitude of the DVI output voltage swing. A 410 ohm pull-up resistor should connect this ball to VCCA33LVDS. If DVI interface is not needed, leave it unconnected.	VCC33LVDS

LCD Panel Power Control				
Signal Name	Ball #	I/O	Signal Description	Power Plane
ENVDD[2:1]	Y05, Y03	O	Enable Panel VDD Power. For the two panels.	VCC33
ENVBLD[2:1]	Y06, Y04	O	Enable Panel Back Light. For the two panels.	VCC33

CRT / TV Monitor Interface

The CRT / TV Interface supports 5 possible operating modes, signal balls DVP1D[10:8] should be strapped to a defined state for the desired operating mode. Please see the Strapping Table for the setup of DVP1D[10:8].

CRT / TV Monitor Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
AR, AG, AB	V01, U02, U01	AO	CRT Mode: Analog Red / Green / Blue. DAC outputs. TV Mode: The AR / AG / AB outputs could be used as C / Y / CVBS or C / Y / Y or R / G / B or Pr / Y / Pb outputs depends on the strapping settings. See the Strapping Table for DVP1D[10:8] strapping setup for the desired DAC operating mode.	VCCA33DAC
HSYNC	AA06	O	Horizontal Sync.	VCC33
VSNC	AA07	O	Vertical Sync.	VCC33
RSET	V03	AI	Reference Resistor. Tie to GNDADAC through an external resistor to control the RAMDAC full-scale current.	VCCA33DAC
SPCLK2 SPD2 SPCLK1 SPD1	AA03 AA04 AA02 AA01	IO	Serial Port (SMBus) Clock and Data. The SPCLKn signals are the clocks for serial data transfer. The SPDn signals are the data signals used for serial data transfer. SPCLK1/SPD1 is typically used for DVI monitor communications and SPCLK2/SPD2 is typically used for DDC for CRT monitor communications.	VCC33

Video Capture Port Interface

VCP Interface supports multiple operating modes, signal balls DVP1D[7:0] are used to select the operating mode for the interface. See the Strapping Table for the setup.

Video Capture Port (VCP)				
Signal Name	Ball #	I/O	Signal Description	Power Plane
VCP1D[7:0] / TS1D[7:0] VCP0D[7:0] / TS0D[7:0]	(see ball list)	IO	Video Capture Mode: VCP1D[7:0] is 8-bit CCIR-601/656 Port 1 or Upper half of 16-bit CCIR-601/656. VCP0D[7:0] is 8-bit CCIR-601/656 Port 0 or Lower half of 16-bit CCIR-601/656. VCP1D[7:0] plus VCP0D[7:0] can be used for 16-bit CCIR-601/656. Transport Stream Input Mode: TS1D[7:0] is 8-bit Transport Stream Port 1. TS0D[7:0] is 8-bit Transport Stream Port 0.	VCC33
VCP0HS / TS0VLD	AG08	IO	Video Capture Mode: VCP0HS: Video Capture Port 0 Horizontal Sync. Transport Stream Input Mode: TS0VLD: Transport Stream Port 0 Data Valid.	VCC33
VCP0VS / TS0SYNC	AG06	IO	Video Capture Mode: VCP0VS: Video Capture Port 0 Vertical Sync. Transport Stream Input Mode: TS0SYNC: Transport Stream Port 0 Data Sync.	VCC33
VCP1HS / TS1VLD	AK02	I	Video Capture Mode: VCP1HS: Video Capture Port 1 Horizontal Sync. Transport Stream Input Mode: TS1VLD: Transport Stream Port 1 Data Valid. If the interface is not needed, leave it unconnected.	VCC33
VCP1VS / TS1SYNC	AK03	I	Video Capture Mode: VCP1VS: Video Capture Port 1 Vertical Sync. Transport Stream Input Mode: TS1SYNC: Transport Stream Port 1 Data Sync. If the interface is not needed, leave it unconnected.	VCC33
NC / TS0ERR	AJ02	IO	Video Capture Mode: NC: Not Connected. Transport Stream Input Mode: TS0ERR: Transport Stream Port 0 Error.	VCC33
VCP0CLK / TS0CLK	AH05	IO	Video Capture Mode: VCP0CLK: Video Capture Port 0 Clock. Transport Stream Input Mode: TS0CLK: Transport Stream Port 0 Clock.	VCC33
VCP1CLK / TS1CLK	AJ03	IO	Video Capture Mode: VCP1CLK: Video Capture Port 1 Clock. Transport Stream Input Mode: TS1CLK: Transport Stream Port 1 Clock.	VCC33
NC / TS1ERR	AK07	I	Video Capture Mode: NC: Not Connected. Transport Stream Input Mode: TS1ERR: Transport Stream Port 1 Error. If the interface is not needed, leave it unconnected.	VCC33

Note: Please use the **bold signal name** to find the ball location in the signal ball list.

Digital Video Port 1 (DVP1) Interface

DVP1 Interface supports multiple operating modes, signal balls VCP1D[5:3] are used to select the operating mode for the interface. See the Strapping Table for the setup.

Digital Video Port 1 (DVP1) Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
DVP1D [15:0]	(see ball list)	O	12-Bit Digital Video Output Mode: DVP1D [11:0] is for 12-Bit DVO Interface. 20-Bit TV Output Mode: DVP1D [15:0] is the first 16 Bits of the TV Interface. ARGB Mode: DVP1D[15:0] supports 16-bit ARGB interface.	VCC33
DVP1HS / DVP1D[16]	AB04	O	12-Bit Digital Video Output Mode: DVP1HS is Digital Video Port 1 Horizontal Sync. 20-Bit TV Output Mode: DVP1D[16] is the 17 th Bit of the TV Interface.	VCC33
DVP1VS / DVP1D[17]	AC04	O	12-Bit Digital Video Output Mode: DVP1VS is Digital Video Port 1 Vertical Sync. 20-Bit TV Output Mode: DVP1D[17] is the 18 th Bit of the TV Interface.	VCC33
DVP1DE / DVP1D[18]	AG04	O	12-Bit Digital Video Output Mode: DVP1DE is Digital Video Port 1 Data Enable. 20-Bit TV Output Mode: DVP1D[18] is the 19 th Bit of the TV Interface.	VCC33
DVP1TVFLD / DVP1D[19]	AG02	IO	12-Bit Digital Video Output Mode: DVP1TVFLD is Digital Video Port 1 Field Out. 20-Bit TV Output Mode: DVP1D[19] is the 20 th Bit of the TV Interface.	VCC33
DVP1DET	AE05	I	Display Detect. Tie to GND if not used.	VCC33
DVP1CLK	AD02	O	Digital Video Port 1 Clock / TV Clock	VCC33
DVP1TVCLKR	AE04	I	TV Return Clock. Tie to GND if not used.	VCC33

Note: Please use the **bold signal name** to find the ball location in the signal ball list.

PCI Bus Interface

PCI Bus Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
AD[31:0]	(see ball list)	IO	Address / Data Bus. Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.	VCC33
CBE[3:0]#	AP04, AR05, AP07, AM09	IO	Command / Byte Enable. The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.	VCC33
DEVSEL#	AL07	IO	Device Select. The CX700 asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a CX700-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]).	VCC33
FRAME#	AT05	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one additional data transfer is desired by the cycle initiator. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]).	VCC33
IRDY#	AP06	IO	Initiator Ready. Asserted when the initiator is ready for data transfer. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]).	VCC33
TRDY#	AM05	IO	Target Ready. Asserted when the target is ready for data transfer. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]).	VCC33
STOP#	AM06	IO	Stop. Asserted by the target to request the master to stop the current transaction. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]).	VCC33
SERR#	AR06	I	System Error. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the CX700 can be programmed to generate an NMI to the CPU. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]). If internal pull-up is used, this signal can be left unconnected.	VCC33
PERR#	AL08	-	Parity Error. PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[0]). If internal pull-up is used, this signal can be left unconnected.	VCC33
PAR	AR04	IO	Parity. A single parity bit is provided over AD[31:0] and C/BE[3:0]#.	VCC33

PCI Bus Interface - continued																													
Signal Name	Ball #	I/O	Signal Description	Power Plane																									
INTA# INTB# INTC# INTD#	AL01 AL03 AL02 AM01	I	<p>PCI Interrupt Request. The INTA# through INTD# signal balls are typically connected to the PCI bus INTA#-INTD# signals per the table below. BIOS settings must match the physical connection method.</p> <table border="0" style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;"><u>INTA#</u></td> <td style="text-align: center;"><u>INTB#</u></td> <td style="text-align: center;"><u>INTC#</u></td> <td style="text-align: center;"><u>INTD#</u></td> </tr> <tr> <td>PCI Slot 1</td> <td style="text-align: center;">INTA#</td> <td style="text-align: center;">INTB#</td> <td style="text-align: center;">INTC#</td> <td style="text-align: center;">INTD#</td> </tr> <tr> <td>PCI Slot 2</td> <td style="text-align: center;">INTB#</td> <td style="text-align: center;">INTC#</td> <td style="text-align: center;">INTD#</td> <td style="text-align: center;">INTA#</td> </tr> <tr> <td>PCI Slot 3</td> <td style="text-align: center;">INTC#</td> <td style="text-align: center;">INTD#</td> <td style="text-align: center;">INTA#</td> <td style="text-align: center;">INTB#</td> </tr> <tr> <td>PCI Slot 4</td> <td style="text-align: center;">INTD#</td> <td style="text-align: center;">INTA#</td> <td style="text-align: center;">INTB#</td> <td style="text-align: center;">INTC#</td> </tr> </table> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[1]). If internal pull-up is used, this signal can be left unconnected.</p>		<u>INTA#</u>	<u>INTB#</u>	<u>INTC#</u>	<u>INTD#</u>	PCI Slot 1	INTA#	INTB#	INTC#	INTD#	PCI Slot 2	INTB#	INTC#	INTD#	INTA#	PCI Slot 3	INTC#	INTD#	INTA#	INTB#	PCI Slot 4	INTD#	INTA#	INTB#	INTC#	VCC33
	<u>INTA#</u>	<u>INTB#</u>	<u>INTC#</u>	<u>INTD#</u>																									
PCI Slot 1	INTA#	INTB#	INTC#	INTD#																									
PCI Slot 2	INTB#	INTC#	INTD#	INTA#																									
PCI Slot 3	INTC#	INTD#	INTA#	INTB#																									
PCI Slot 4	INTD#	INTA#	INTB#	INTC#																									
REQ3# , REQ2# , REQ1# , REQ0#	AN04 AP02 AP01 AN03	I	<p>PCI Request. These signals connect to the CX700 from each PCI slot (or each PCI master) for access request to the PCI bus.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[1]). If internal pull-up is used, this signal can be left unconnected.</p>	VCC33																									
GNT3# , GNT2# , GNT1# , GNT0#	AR01 AM03 AM02 AN01	O	<p>PCI Grant. These signals are driven by the CX700 to grant PCI bus access to a specific PCI master.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[1]).</p>	VCC33																									
PCIRST#	AT10	O	PCI Reset. This signal is used to reset devices attached to the PCI bus.	VCC33																									
PCICLK	AL10	I	PCI Clock. This signal provides timing for all transactions on the PCI Bus. This clock is necessary even if the system does not need PCI interface.	VCC33																									

USB 2.0 Interface

USB 2.0 Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
USBP0+/-	AM29, AN29	IO	USB Port 0 Differential Data	VCC33USB
USBP1+/-	AT29, AR29	IO	USB Port 1 Differential Data	VCC33USB
USBP2+/-	AT27, AR27	IO	USB Port 2 Differential Data	VCC33USB
USBP3+/-	AM27, AN27	IO	USB Port 3 Differential Data	VCC33USB
USBP4+/-	AT25, AR25	IO	USB Port 4 Differential Data	VCC33USB
USBP5+/-	AM25, AN25	IO	USB Port 5 Differential Data	VCC33USB
USBCLK	AT23	I	USB Clock. 48 MHz clock input for the USB and HD Audio. If USB and HD Audio interfaces are not used, leave it unconnected.	VCC33USB
USBOC0#	AL23	I	USB Port 0 Over Current Detect. Port 0 is disabled if low. If it is not used, leave it unconnected.	VCC33USB
USBOC1#	AP23	I	USB Port 1 Over Current Detect. Port 1 is disabled if low. If it is not used, leave it unconnected.	VCC33USB
USBOC2#	AN23	I	USB Port 2 Over Current Detect. Port 2 is disabled if low. If it is not used, leave it unconnected.	VCC33USB
USBOC3#	AM23	I	USB Port 3 Over Current Detect. Port 3 is disabled if low. If it is not used, leave it unconnected.	VCC33USB
USBOC4#	AK23	I	USB Port 4 Over Current Detect. Port 4 is disabled if low. If it is not used, leave it unconnected.	VCC33USB
USBOC5#	AK24	I	USB Port 5 Over Current Detect. Port 5 is disabled if low. If it is not used, leave it unconnected.	VCC33USB
USBREXT	AR23	AI	USB External Resistor If USB interface is not needed, leave it unconnected.	VCC33USB

SATA Interface

SATA Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
SRX0+/-	AR35, AT35	I	SATA Port 0 Differential Receiver	VCCA33SATA
SRX1+/-	AR33, AT33	I	SATA Port 1 Differential Receiver	VCCA33SATA
STX0+/-	AM35, AN35	O	SATA Port 0 Differential Transmitter	VCCA33SATA
STX1+/-	AM33, AN33	O	SATA Port 1 Differential Transmitter	VCCA33SATA
SXI	AK35	I	SATA Crystal Input. 25MHz Crystal Input. If SATA interface is not needed, SATA crystal can be removed. Tie to GND if not used.	VCCA33SATA
SXO	AK36	O	SATA Crystal Output. 25MHz crystal output. If SATA interface is not needed, SATA crystal can be removed.	VCCA33SATA
SREXT	AJ34	AI	SATA External Resistor. If SATA interface is not needed, leave it unconnected.	VCCA33SATA
SATALED#	AJ23	O	SATA LED.	VCC33

SMBus Interface

SMBus Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
SMBCLK1	AM16	OD	SMB Channel 1 Clock. Master Mode.	VSUS33
SMBDATA1	AN16	OD	SMB Channel 1 Data. Master Mode.	VSUS33
SMBCLK2 / GPIO1	AK16	OD	SMB Channel 2 Clock. Slave Mode. SMBCLK2 can optionally be used as GPIO1.	VSUS33
SMBDATA2 / GPIO0	AL16	OD	SMB Channel 2 Data. Slave Mode. SMBDATA2 can optionally be used as GPIO0.	VSUS33
SMBALRT#	AP15	I	SMB Alert. (With optional 10K ohms built-in pull-up resistor) Enabled by System Management Bus I/O space. When enabled, SMBALRT# assertion generates an IRQ or SMI interrupt or a power management resume event. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If internal pull-up is used, this signal can be left unconnected.	VSUS33

Enhanced IDE Interface

Enhanced IDE is enabled when signal ball PDDACK# is strapped HIGH.

Enhanced IDE Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
PDIORDY	AK22	I	EIDE Mode: PDIORDY: Device ready indicator UltraDMA Mode: (Write) PDDMARDY: Output flow control. The device may assert PDDMARDY to pause output transfers (Read) PDSTROBE: Input data strobe (both edges). The device may stop assertion of PDSTROBE to pause input data transfers	VCC33
PDIOR# / GPO0	AL22	O	EIDE Mode: PDIOR#: Device read strobe UltraDMA Mode: (Write) PHSTROBE: Output data strobe (both edges). The host may stop assertion of PHSTROBE to pause output data transfers (Read) PHDMARDY: Input flow control. The host may assert PHDMARDY to pause input transfers PDIOR# can optionally be used as GPO0.	VCC33
PDIOW# / GPO1	AT20	O	EIDE Mode: PDIOW#: Device write strobe UltraDMA Mode: PSTOP: Stop transfer. Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of PSTOP by the host during or after data transfer signals the termination of the burst. PDIOW# can optionally be used as GPO1.	VCC33
PDDREQ	AR20	I	IDE Device DMA Request.	VCC33
PDDACK#	AJ22	O	IDE Device DMA Acknowledge.	VCC33

Enhanced IDE Interface - continued				
Signal Name	Ball #	I/O	Signal Description	Power Plane
PDCS1#	AN22	O	IDE Master Chip Select. This signal has an internal 10K ohms pull-up resistor.	VCC33
PDCS3#	AP22	O	IDE Slave Chip Select.	VCC33
PDA[2:0] / GPO[4:2]	AR22, AG22, AT22	O	IDE Disk Address. PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. PDA[2:0] can optionally be used as GPO[4:2].	VCC33
PDD[15:0]	(see ball list)	IO	IDE Data Bus.	VCC33
IRQ15 / GPIO	AH22	I	IDE Channel Interrupt Request. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F7 Rx55[2]). If it is not used, leave it unconnected.	VCC33

LPC Bus Interface

LPC Bus Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
LPCAD[3:0]	AM19, AN19, AT19, AR19	IO	LPC Address / Data. This signal has an internal 10K ohms pull-up resistor.	VCC33
LPCFRAME#	AP19	O	LPC Frame. This signal has an internal 10K ohms pull-up resistor.	VCC33
LPCDRQ0#	AK19	I	LPC DMA / Bus Master Request 0. Pull up 10K ohms to VCC33 if not used.	VCC33
LPCDRQ1#	AL19	I	LPC DMA / Bus Master Request 1. Pull up 10K ohms to VCC33 if not used.	VCC33

Serial Port Interface

Serial ports are enabled when signal ball PDDACK# is strapped LOW.

Serial Port Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
SDOUT1 / PDD5	AM20	O	Transmit Data for Serial Port 1. SDOUT1 can optionally be used as PDD5.	VCC33
SDOUT2 / PDD13	AK21	O	Transmit Data for Serial Port 2. SDOUT2 can optionally be used as PDD13.	VCC33
SIN1 / PDD4	AK20	I	Receive Data for Serial Port 1. SIN1 can optionally be used as PDD4.	VCC33
SIN2 / PDD12	AL21	I	Receive Data for Serial Port 2. SIN2 can optionally be used as PDD12.	VCC33
RTS1 / PDD2	AN21	O	Request To Send for Serial Port 1. RTS1 can optionally be used as PDD2.	VCC33
RTS2 / PDD10	AJ20	O	Request To Send for Serial Port 2. RTS2 can optionally be used as PDD10.	VCC33
CTS1 / PDD0	AP20	I	Clear To Send for Serial Port 1. CTS1 can optionally be used as PDD0.	VCC33
CTS2 / PDD8	AG20	I	Clear To Send for Serial Port 2. CTS2 can optionally be used as PDD8.	VCC33
DTR1 / PDD3	AN20	O	Data Terminal Ready for Serial Port 1. DTR1 can optionally be used as PDD3.	VCC33
DTR2 / PDD11	AL20	O	Data Terminal Ready for Serial Port 2. DTR2 can optionally be used as PDD11.	VCC33
DSR1 / PDD1	AP21	I	Data Set Ready for Serial Port 1. DSR1 can optionally be used as PDD1.	VCC33
DSR2 / PDD9	AH20	I	Data Set Ready for Serial Port 2. DSR2 can optionally be used as PDD9.	VCC33
DCD1 / PDD6	AH21	I	Data Carrier Detect for Serial Port 1. DCD1 can optionally be used as PDD6.	VCC33
DCD2 / PDD14	AM22	I	Data Carrier Detect for Serial Port 2. DCD2 can optionally be used as PDD14.	VCC33
RI1 / PDD7	AG21	I	Ring Indicator for Serial Port 1. RI1 can optionally be used as PDD7.	VCC33
RI2 / PDD15	AT21	I	Ring Indicator for Serial Port 2. RI2 can optionally be used as PDD15.	VCC33

High Definition Audio and MC97 Interface

Signal Name	Ball #	I/O	Signal Description	Power Plane
High Definition Audio				
AZRST#	AR10	O	High Definition Audio Reset.	VSUS33
AZBITCLK	AR11	O	High Definition Audio Bit Clock. 24.00 MHz.	VCC33
AZSYNC	AP10	O	High Definition Audio Sync. 48 KHz Frame Sync and outbound tag signal.	VCC33
AZSDOUT	AT12	O	High Definition Audio Serial Data Output.	VCC33
AZSDIN[1:0]	AP11, AT11	I	High Definition Audio Serial Data Input. Tie to GND if not used.	VSUS33
MC97				
MCSDOU / GPO11	AR12	O	MC97 Serial Data Output MCSDOU can optionally be used as GPO11.	VCC33
MCBCLK / GPI1	AP12	I	MC97 Bit Clock MCBCLK can optionally be used as GPI1. If it is not used, leave it unconnected.	VCC33
MCS DIN / GPI2	AN12	I	MC97 Serial Data Input MCS DIN can optionally be used as GPI2. Tie to GND if not used.	VSUS33
MCSYNC / GPO5	AM12	O	MC97 Sync Signal. MCSYNC can optionally be used as GPO5.	VCC33
MCRST / GPO6	AL12	O	MC97 Reset. MCRST can optionally be used as GPO6.	VSUS33

Speaker Interface

Speaker Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
SPKR / GPO7	AL18	O	Speaker Out. SPKR can optionally be used as GPO7.	VCC33

Internal Keyboard Controller Interface

Internal Keyboard Controller Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
MSCK	AN13	IO	Mouse Clock. From internal mouse controller. This signal has an internal 10K ohms pull-up resistor.	VSUS33
MSDT	AP13	IO	Mouse Data. From internal mouse controller. This signal has an internal 10K ohms pull-up resistor.	VSUS33
KBCK / A20GATE	AL13	IO	Keyboard Clock. From internal keyboard controller. This signal has an internal 10K ohms pull-up resistor. This signal is used as A20GATE to connect to external keyboard controller's A20Gate signal if external KBC is used.	VSUS33
KBDT / KBC_CPURST#	AM13	IO	Keyboard Data. From internal keyboard controller. This signal has an internal 10K ohms pull-up resistor. This signal is used as KBC_CPURST# to connect to external keyboard controller's CPURST# signal if external KBC is used.	VSUS33

Note: Please use the **bold signal name** to find the ball location in the signal ball list.

Serial IRQ Interface

Serial IRQ Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
SERIRQ	AM17	I	Serial IRQ. This signal has an internal 10K ohms pull-up resistor. If it is not used, leave it unconnected.	VCC33

PC / PCI DMA Interface

PC / PCI DMA Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
PCIDREQ / GPIO2	AK09	I	PC / PCI DMA Request. PCIDREQ can optionally be used as GPIO2. Tie to GND if not used.	VCC33
PCIDGNT / GPIO3	AK08	O	PC / PCI DMA Grant. PCIDGNT can optionally be used as GPIO3.	VCC33

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General Purpose Input Interface

General Purpose Input Interface – Signal Attributes										
Signal Name	Ball #	I/O	Default Function	Signal State					Interrupt Triggered by GPI	Power Plane
				Reset	After Reset	POS	STR	STD		
GPI0 / IRQ15	AH22	I	IRQ15	IRQ15	IRQ15	Driven	Off	Off	SCI/SMI	VCC33
GPI1 / MCBCLK	AP12	I	MCBCLK	Reserved for TV/CRT output select function HIGH: TV, LOW: CRT					SCI/SMI	VCC33
GPI2 / MCSDIN	AN12	I	MCSDIN	MCSDIN	MCSDIN	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI3 / AOL	AN14	I	—	—	—	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI4 / BATLOW#	AP14	I	GPI4	Static	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI5 / EXTSMI#	AN15	I	GPI5	Static	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI6 / INTRUDER#	AN17	I	GPI6	Static	Driven	Driven	Driven	Driven	SCI/SMI	VBAT
GPI7 / LID#	AT13	I	GPI7	Static	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI8 / RING#	AL14	I	GPI8	Static	Driven	Driven	Driven	Driven	No	VSUS33
GPI9 / THRM#	AP16	I	GPI9	Static	Driven	Driven	Driven	Driven	No	VSUS33
GPI10 / THRMTRIP#	C28	I	THRMTRIP#	THRMTRIP#	THRMTRIP#	Driven	Off	Off	No	VCC33
GPI11 / VGATE	AM18	I	GPI11	Static	Driven	Driven	Driven	Driven	Generate Wakeup Event Then SCI/SMI	VSUS33

GPI Signal States:

- Static:** The input signal must remain static, either high or low.
- Driven:** The input signal is driven from outside. It is allowed to change.
- Off:** The power plane of the input signal is off.

System States:

- Reset:** During <RSMRST#, PCIRST#> is <0, 0>
- After Reset:** Immediately after <RSMRST#, PCIRST#> is <1, 1>

General Purpose Input Interface – Signal Control Registers				
Signal Name	Control Register	GPI Status Register	GPI SCI/SMI Register	Status Change Register
GPI0	B0D17F0 RxE4[3] = 1	PMIO Rx48[0]	PMIO Rx52[0] = 1, B0D17F0 RxE0[0], B0D17F0 RxE1[0]	PMIO Rx50[0]
GPI1	B0D17F0 Rx94[3] = 1	PMIO Rx48[1]	PMIO Rx52[1] = 1, B0D17F0 RxE0[1], B0D17F0 RxE1[1]	PMIO Rx50[1]
GPI2	B0D17F0 Rx94[3] = 1	PMIO Rx48[2]	PMIO Rx52[2] = 1, B0D17F0 RxE0[2], B0D17F0 RxE1[2]	PMIO Rx50[2]
GPI3	B0D17F0 Rx95[1] = 1	PMIO Rx48[3]	PMIO Rx52[3] = 1, B0D17F0 RxE0[3], B0D17F0 RxE1[3]	PMIO Rx50[3]
GPI4	PMIO Rx25[4] = 0 & PMIO Rx23[4] = 0	PMIO Rx48[4]	PMIO Rx52[4] = 1, B0D17F0 RxE0[4], B0D17F0 RxE1[4]	PMIO Rx50[4]
GPI5	PMIO Rx24[4] = 0 & PMIO Rx22[4] = 0	PMIO Rx48[5]	PMIO Rx52[5] = 1, B0D17F0 RxE0[5], B0D17F0 RxE1[5]	PMIO Rx50[5]
GPI6	PMIO Rx24[6] = 0 & PMIO Rx22[6] = 0	PMIO Rx48[6]	PMIO Rx52[6] = 1, B0D17F0 RxE0[6], B0D17F0 RxE1[6]	PMIO Rx50[6]
GPI7	PMIO Rx25[3] = 0 & PMIO Rx23[3] = 0	PMIO Rx48[7]	PMIO Rx52[7] = 1, B0D17F0 RxE0[7], B0D17F0 RxE1[7]	PMIO Rx50[7]
GPI8	PMIO Rx25[0] = 0 & PMIO Rx23[0] = 0	PMIO Rx49[0]	N/A	N/A
GPI9	PMIO Rx25[2] = 0 & PMIO Rx23[2] = 0 & B0D17F0 Rx8C[3] = 0	PMIO Rx49[1]	N/A	N/A
GPI10	PMIO Rx2B[1] = 0	PMIO Rx49[2]	N/A	N/A
GPI11	B0D17F0 RxE5[4] = 0	PMIO Rx49[3]	PMIO Rx22[1] or PMIO Rx24[1]	PMIO Rx20[1]

General Purpose Output Interface

General Purpose Output Interface – Signal Attributes									
Signal Name	Ball #	I/O	Default Function	Signal State					Power Plane
				Reset	After Reset	POS	STR	STD	
GPO0 / PDIOR#	AL22	O	PDIOR#	PDIOR#	PDIOR#	Defined	Off	Off	VCC33
GPO1 / PDIOW#	AT20	O	PDIOW#	PDIOW#	PDIOW#	Defined	Off	Off	VCC33
GPO2 / PDA0	AT22	O	PDA0	PDA0	PDA0	Defined	Off	Off	VCC33
GPO3 / PDA1	AG22	O	PDA1	PDA1	PDA1	Defined	Off	Off	VCC33
GPO4 / PDA2	AR22	O	PDA2	PDA2	PDA2	Defined	Off	Off	VCC33
GPO5 / MCSYNC	AM12	O	MCSYNC	MCSYNC	MCSYNC	Defined	Off	Off	VCC33
GPO6 / MCRST	AL12	O	MCRST	MCRST	MCRST	Defined	Defined	Defined	VSUS33
GPO7 / SPKR	AL18	O	SPKR	SPKR	SPKR	Defined	Off	Off	VCC33
GPO8 / SUSA#	AM15	O	SUSA#	SUSA#	SUSA#	Defined	Defined	Defined	VSUS33
GPO9 / SUSB#	AR13	O	SUSB#	SUSB#	SUSB#	Defined	Defined	Defined	VSUS33
GPO10 / SUSC#	AM14	O	SUSC#	SUSC#	SUSC#	Defined	Defined	Defined	VSUS33
GPO11 / MCSDOUT	AR12	O	MCSDOUT	MCSDOUT	MCSDOUT	Defined	Off	Off	VCC33

GPO Signal States:

1. **High-Z:** Tri-State.
2. **High:** The output signal is logic “1”.
3. **Low:** The output signal is logic “0”.
4. **Defined:** The output signal can be high or low, defined by the GPO function.
5. **Undefined:** The output signal is undetermined.
6. **Off:** The power plane of output signal is off.

System States:

1. **Reset:** During <RSMRST#, PCIRST#> is <0, 0>
2. **After Reset:** Immediately after <RSMRST#, PCIRST#> is <1, 1>

General Purpose Output Interface – Signal Control Registers		
Signal Name	Control Register	GPO Output Register
GPO0	B0D17F0 RxE4[3] = 1	PMIO Rx4C[0]
GPO1	B0D17F0 RxE4[3] = 1	PMIO Rx4C[1]
GPO2	B0D17F0 RxE4[3] = 1	PMIO Rx4C[2]
GPO3	B0D17F0 RxE4[3] = 1	PMIO Rx4C[3]
GPO4	B0D17F0 RxE4[3] = 1	PMIO Rx4C[4]
GPO5	B0D17F0 Rx94[3] = 1	PMIO Rx4C[5]
GPO6	B0D17F0 Rx94[3] = 1	PMIO Rx4C[6]
GPO7	B0D17F0 RxE4[4] = 1	PMIO Rx4C[7]
GPO8	B0D17F0 Rx94[2] = 1	PMIO Rx4D[0]
GPO9	B0D17F0 Rx94[2] = 1	PMIO Rx4D[1]
GPO10	B0D17F0 Rx94[2] = 1	PMIO Rx4D[2]
GPO11	B0D17F0 Rx94[3] = 1	PMIO Rx4D[3]

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General Purpose Input/Output Interface

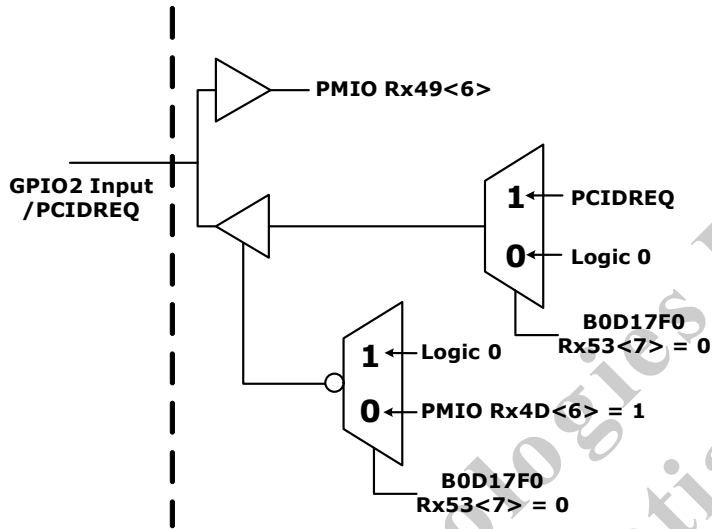
General Purpose Input/Output Interface – Signal Attributes									
Signal Name	Ball #	I/O	Default Function	Signal State					Power Plane
				Reset	After Reset	POS (GPO)	STR (GPO)	STD (GPO)	
GPIO0 / SMBDATA2	AL16	IO	GPI Mode	Static	Driven	Defined	Defined	Defined	VSUS33
GPIO1 / SMBCLK2	AK16	IO	GPI Mode	Static	Driven	Defined	Defined	Defined	VSUS33
GPIO2 / PCIDREQ	AK09	IO	GPI Mode	Static	Driven	Defined	Off	Off	VCC33
GPIO3 / PCIDGNT	AK08	IO	GPI Mode	Static	Driven	Defined	Off	Off	VCC33
GPIOA	AB08	IO	-	Reserved for display					VCC33
GPIOB	AB07	IO	-	Reserved for display					VCC33
GPIOC / DISPCLKI2	AB06	IO	DISPCLKI2	Reserved for display					VCC33
GPIOD / DISPCLKO2	AB05	IO	DISPCLKO2	Reserved for display					VCC33

General Purpose Input/Output Interface – Signal Registers			
Signal Name	Control Register	GPI Status Register	GPO Output Register
GPIO0	B0D17F0 Rx95[3] = 1 B0D17F0 Rx95[2] = 1	PMIO Rx49[4]	PMIO Rx4D[4]
GPIO1	B0D17F0 Rx95[3] = 1 B0D17F0 Rx95[2] = 1	PMIO Rx49[5]	PMIO Rx4D[5]
GPIO2	B0D17F0 Rx53[7] = 0	PMIO Rx49[6]	PMIO Rx4D[6]
GPIO3	B0D17F0 Rx53[7] = 0	PMIO Rx49[7]	PMIO Rx4D[7]

GPIO Programming Sequence

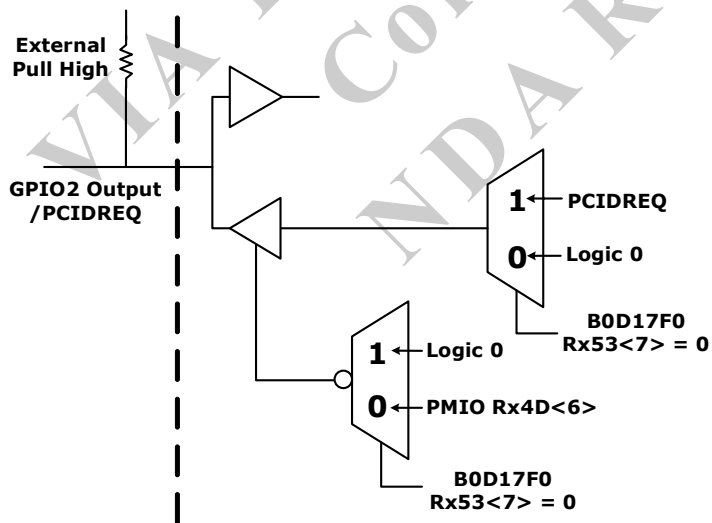
1. To Input from a GPIO[3:0] signal:
 - Enable the control register and write “1” to the corresponding PMIO Rx4D<7:4> register bit:
 - Read the corresponding input register to retrieve the current signal state.

Example: GPIO2 I/O Pad Circuit Diagram (Input Mode)



2. To Output through a GPIO[3:0] signal:
 - Enable the control register
 - Program the corresponding output register bit, PMIO Rx4D<7:4>, to the desired state.

Example: GPIO2 I/O Pad Circuit Diagram (Output Mode)



Power Management Control and Event Signals

Power Management Control and Event Signals				
Signal Name	Ball #	I/O	Signal Description	Power Plane
PWRBTN#	AJ15	I	<p>Power Button. Used by the Power Management subsystem to monitor an external system on/off button or switch. Internal logic powered by VSUS33.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If internal pull-up is used, this signal can be left unconnected.</p>	VSUS33
EXTSMI# / GPI5	AN15	IO	<p>External System Management Interrupt. When enabled, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode.</p> <p>EXTSMI# can optionally be used as GPI5.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]).</p>	VSUS33
PME#	AL15	I	<p>Power Management Event. This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If it is not used, leave it unconnected.</p>	VSUS33
LID# / GPI7	AT13	I	<p>Notebook Computer Display Lid Open / Closed Monitor. Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#.</p> <p>LID# can optionally be used as GPI7.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If it is not used, leave it unconnected.</p>	VSUS33
INTRUDER# / GPI6	AN17	I	<p>Intrusion Indicator.</p> <p>INTRUDER# can optionally be used as GPI6.</p> <p>If it is not used, leave it unconnected.</p>	VBAT
THRM# / GPI9	AP16	I	<p>Thermal Alarm Monitor. This signal is to enable the throttling mode of the STPCLK# signal for thermal control.</p> <p>THRM# can optionally be used as GPI9.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If it is not used, leave it unconnected.</p>	VSUS33
RING# / GPI8	AL14	I	<p>Ring Indicator. May be connected to external modem circuitry to allow the system to be re-activated by a received phone call.</p> <p>RING# can optionally be used as GPI8.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If it is not used, leave it unconnected.</p>	VSUS33
BATLOW# / GPI4	AP14	I	<p>Battery Low Indicator.</p> <p>BATLOW# can optionally be used as GPI4.</p> <p>This signal has a programmable internal 10K ohms pull-up resistor (default enable, B0D17F0 Rx97[1]). If it is not used, leave it unconnected.</p>	VSUS33

Power Management Control and Event Signals - continued				
Signal Name	Ball #	I/O	Signal Description	Power Plane
CPUSTP#	AK17	O	CPU Clock Stop. Signals the system clock generator to disable the CPU clock outputs.	VCC33
PCISTP#	AN18	O	PCI Clock Stop. Signals the system clock generator to disable the PCI clock outputs.	VCC33
SUSA# / GPO8	AM15	O	Suspend Plane A Control. Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. SUSA# can optionally be used as GPO8.	VSUS33
SUSB# / GPO9	AR13	O	Suspend Plane B Control. Asserted during power management STR and STD suspend states. Used to control the secondary power plane. SUSB# can optionally be used as GPO9.	VSUS33
SUSC# / GPO10	AM14	O	Suspend Plane C Control. Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. SUSC# can optionally be used as GPO10.	VSUS33
AOL / GPI3	AN14	I	Alert On LAN. AOL may optionally be used as GPI3. If it is not used, leave it unconnected.	VSUS33
CLKRUN#	AP18	IO	PCI Clock Run. Suspend PCICLK when CLKRUN# is high. See PCI Specification for CLKRUN# protocol.	VCC33
VGATE / GPI11	AM18	I	Voltage Gate. This signal is not implemented. VGATE may optionally be used as GPI11. If it is not used, leave it unconnected.	VSUS33
VRDSLP	AL17	OD	Voltage Regulator Deep Sleep. Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode.	VCC33

Clock, Test and Miscellaneous Signals

Signal Name	Ball #	I/O	Signal Description	Power Plane
Clock Signals of Graphics & Video Processors				
DISPCLKI2 / GPIOC	AB06	I	SSC Dot Clock 2 (Pixel Clock) In. DISPCLKI2 can optionally be used as GPIOC.	VCC33
DISPCLKO2 / GPIOD	AB05	O	Dot Clock 2 (Pixel Clock) Out. DISPCLKO2 can optionally be used as GPIOD.	VCC33
GCLK	K11	I	Graphics clock (66Mhz)	VCC33
TVXI	Y02	I	TV Encoder Crystal Input. 27 MHz Crystal Input. If TV interface is not needed, TV crystal can be removed. Tie to GND if not used.	VCCA33TVPLL
TVXO	Y01	O	TV Encoder Crystal Output. 27 MHz Crystal Output. If TV interface is not needed, TV crystal can be removed.	VCCA33TVPLL
XIN	AB09	I	14.31818MHz Reference Frequency Input. External 14.31818 MHz clock source. All internal graphics controller clocks and internal timer are synthesized on chip using this frequency as a reference.	VCC33
RTC Crystal Interface				
RTCX1	AT16	I	RTC Crystal Input: 32.768 KHz Crystal Input.	VBAT
RTCX2	AR16	O	RTC Crystal Output: 32.768 KHz Crystal Output.	VBAT
Power State and System Reset				
PWRGD	AR17	I	Power Good. Connected to the Power Good signal on the Power Supply. Internal logic powered by VBAT.	VBAT
RSMRST#	AP17	I	Resume Reset. When asserted, this signal resets the CX700 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	VBAT
Test and Miscellaneous Signals				
TESTIN#	AK15	I	Test In. This signal is used for testing.	VSUS33
DFTIN#	B31	I	DFT In. This signal is used for testing.	VCCMEM
BISTIN	AA05	I	BIST In. This signal is used for testing.	VCC33
TP1	J10	-	Test Pad. Also serve as a strapping pin.	VTT
TP2	J11	-	Test Pad. Also serve as a strapping pin.	VTT
TP3	H12	-	Test Pad. Also serve as a strapping pin.	VTT
TP4	J24	-	Test Pad. Also serve as a strapping pin.	VCC33CPU
TP5	H24	-	Test Pad. Also serve as a strapping pin.	VCCMEM
TP6	AJ19	-	Test Pad. Also serve as a strapping pin.	VCC33
TP7	AJ16	-	Test Pad. Also serve as a strapping pin.	VCC33
TP8	AH09	-	Test Pad. Also serve as a strapping pin.	VCC33
RSVD[4:0]	AC07, AC06, AC08, J25, K25	-	Reserved. No connection.	-

Compensation and Reference Voltage Signals

Compensation				
Signal Name	Ball #	I/O	Signal Description	Power Plane
DMCOMP	A31	AI	DRAM Compensation.	VCCMEM
SATAR50COMP	AJ33	AI	Serial ATA Auto Compensation. If SATA interface is not needed, leave it unconnected.	VCCA33SATA

Reference Voltages				
Signal Name	Ball #	I/O	Signal Description	
GTLVREF[1:0]	J12, H20	AI	Host CPU Interface AGTL+ Voltage Reference. Set it to 2/3 of VTT.	
MEMVREF[1:0]	V27, K28	AI	Memory Voltage Reference. Set it to 1/2 of VCCMEM.	

Power / Ground Signals

Analog Power / Ground		
Signal Name	Ball #	Signal Description
Host Interface		
VCCA33HCK	K24	Power for Host CPU Clock PLL. 3.3V ±5%.
GNDAHCK	L24	Ground for Host CPU Clock PLL
Graphics and Video		
VCCA33PLL[3:1]	V04, V06, W03	Power for Graphics Controller PLL. 3.3V ±5%.
GNDAPLL	V05, V07, W04	Ground for Graphics Controller PLL.
VCCA33DAC[2:1]	U05, U04	Power for DAC. 3.3V ±5%.
GNDADAC	U03, U06, V02	Ground for DAC.
LVDS Transmitter		
VCCA33LVDSPLL[2:1]	P04, N05	LVDS PLL Power. 3.3V ±5%
GNDALVDSPLL	M05, P05	LVDS PLL Ground.
VCCA33LVDS	P03	LVDS Analog Power. 3.3V ±5%
GNDALVDS	R04	LVDS Analog Ground.
TV Encoder		
VCCA33TVPLL	W01	TV Encoder PLL Power. 3.3V ±5%
GNDATVPLL	W02	TV Encoder PLL Ground.
SATA Controller		
VCCA15SXO	AJ36	SATA Oscillator Power. 1.5V ±5%.
GNDASXO	AJ35	SATA Oscillator Ground.
VCCA15SATA	(see ball list)	SATA Analog Power. 1.5V ±5%.
GND15SATA	(see ball list)	SATA Analog Ground.
VCCA33SATA	AN31, AP31, AR31, AT31	SATA Analog Power. 3.3V ±5%.
GND33SATA	AK31, AL31, AM31	SATA Analog Ground.
VCCA33PLLSATA	AK33	SATA PLL Analog Power. 3.3V ±5%.
GNDAPLLSATA	AK32	SATA PLL Analog Ground.
USB Controller		
VCCA15PLLUSB	AJ24	USB PLL Analog Voltage. 1.5V ±5%.
GND15PLLUSB	AH23	USB PLL Analog Ground.
VCCA33PLLUSB	AH24	USB PLL Analog Voltage. 3.3V ±5%.
GND33PLLUSB	AG23	USB PLL Analog Ground.

Digital Power / Ground		
Signal Name	Ball #	Signal Description
VTT	(see ball list)	Power for CPU I/O Interface. Voltage is CPU dependent.
VCCMEM	(see ball list)	Power for Memory I/O Interface. 2.5V (DDR) /1.8V (DDR2) $\pm 5\%$.
VSUS15MEM	V26	Suspend Power for Memory Module. 1.5V $\pm 5\%$
VSUS15	AJ12, AJ13	Suspend Power. 1.5V $\pm 5\%$
VSUS15USB	AG24	Suspend Power for USB. 1.5V $\pm 5\%$
VSUS33	AB18, AK11, AK12, AK13	Suspend Power. 3.3V $\pm 5\%$. Always available unless the mechanical switch of the power supply is turned off. If the “soft-off” state is not implemented, then these signal balls can be connected to VCC33.
VCC15	(see ball list)	Core Power. 1.5V $\pm 5\%$. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.
VCC33	(see ball list)	I/O Power. 3.3V $\pm 5\%$
VCC33CPU	P23	Power for 3.3V CPU Interface. 3.3V $\pm 5\%$
VBAT	AT17	RTC Battery. Battery input for internal RTC (RTCX1, RTCX2).
GND	(see ball list)	Ground. Connect to primary motherboard ground plane.
VCC33LVDS	(see ball list)	Power for LVDS Transmitter. 3.3V $\pm 5\%$.
GNDLVDS	(see ball list)	Ground for LVDS Transmitter.
VCC33USB	(see ball list)	Power for USB. 3.3V $\pm 5\%$.
GNDUSB	(see ball list)	Ground for USB.

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Strapping Signal Table

Strapping Signal													
(External pull-up / pulldown straps are required to select "H" / "L". "X" means the strapping is ignored.)													
Signal	Ball #	Function	Description										
TP[2:1]	J11, J10	FSB Clock	<table border="0" style="width: 100%;"> <tr> <td style="text-align: center;"><u>State (TP[2:1])</u></td> <td style="text-align: center;"><u>Mode (MHz)</u></td> </tr> <tr> <td style="text-align: center;">LL</td> <td style="text-align: center;">100 Mhz</td> </tr> <tr> <td style="text-align: center;">LH</td> <td style="text-align: center;">133 Mhz</td> </tr> <tr> <td style="text-align: center;">HL</td> <td style="text-align: center;">Reserved</td> </tr> <tr> <td style="text-align: center;">HH</td> <td style="text-align: center;">Auto</td> </tr> </table>	<u>State (TP[2:1])</u>	<u>Mode (MHz)</u>	LL	100 Mhz	LH	133 Mhz	HL	Reserved	HH	Auto
<u>State (TP[2:1])</u>	<u>Mode (MHz)</u>												
LL	100 Mhz												
LH	133 Mhz												
HL	Reserved												
HH	Auto												
TP3	H12	IO Queue Depth	L: 8-level deep H: 1-level deep										
TP4	J24	GTL Pull-up	L: Enable internal GTL Pull-up H: Disable internal GTL Pull-up										
TP[5:6]	H24 AJ19	Host Protocol Mode V4 or P4	LL: P4 LH: V4										
TP7	AJ16	Host Protocol Mode 2: V4 Data Width	L: 64 bit H: 32 bit TP7 strapping is valid if TP[6:5] == [H, L].										
PDCS1#	AN22	Dual Processor Configuration	L: Single Processor H: Dual Processor										
TP8	AH09	Memory Type	L: DDR H: DDR2										
SPKR	AL18	CPU Frequency Strapping	L: Enable H: Disable										
AZSDOUT	AT12	Auto Reboot	L: Enable H: Disable										
AZSYNC	AP10	LPC FWH Command	L: Enable H: Disable										
PDDACK#	AJ22	COM Port Enable	L: Enable COM ports H: Enable EIDE port										
LPCFRAME#	AP19	Reserved	Always strapped HIGH.										

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Strapping Signal - continued (External pull-up / pulldown straps are required to select "H" / "L". "X" means the strapping is ignored.)			
Signal	Ball #	Function	Description
VCP1D[5:3]	AK05 AK04 AJ08	DVP1 Output Selection	LLX: DVP-TV output LHX: DVP with alpha output HLL: DCVI 10-bit data output HLH: DCVI 8-bit data output HHL: DCVI 20-bit data output HHH: DCVI 16-bit data output
VCP1D2	AJ07	Reserved	Always strapped LOW.
VCP1D1	AK01	Reserved	Always strapped LOW.
VCP1D0	AJ04	Reserved	Always strapped HIGH.
VCP0D7	AJ01	Reserved	Always strapped LOW.
VCP0D6	AJ05	Reserved	Always strapped LOW.
VCP0D[3:0]	AH06 AG07 AH07 AG09	Panel Type Selection	
DVP1D[15:14]	AF04 AH02	LVDS/DVI Mode Selection	LL: Two Single LVDS Channel: LVDS1 + LVDS2 LH: Reserved HL: One Dual LVDS Channel (High resolution panel) HH: One DVI only
DVP1D[10:8]	AF03 AG05 AE03	DAC (CRT/TV) Output Mode Selection	LXX: DAC A/B/C = R/G/B for CRT HLL: DAC A/B/C = C/Y/CVBS for TV HLH: DAC A/B/C = C/Y/Y for TV HHL: DAC A/B/C = R/G/B for TV HHH: DAC A/B/C = Pr/Y/Pb for TV
DVP1D[7:4]	AF05 AD01 AD03 AC01	Video Capture Port 1 Type Selection	LLLL: CAP 8 bit CCIR656 LLLH: CAP 8 bit CCIR601 LLHL: CAP 8 bit VIP 1.1 LLHH: CAP 8 bit VIP 2.0 LHLL: CAP 16 bit CCIR656 LHLH: CAP 16 bit CCIR601 LHHL: CAP 16 bit VIP 1.1 LHHH: CAP 16 bit VIP 2.0 HXXX: TS 8 bit
DVP1D[3:0]	AD04 AC03 AC02 AB03	Video Capture Port 0 Type Selection	LLLL: CAP 8 bit CCIR656 LLLH: CAP 8 bit CCIR601 LLHL: CAP 8 bit VIP 1.1 LLHH: CAP 8 bit VIP 2.0 LHLL: CAP 16 bit CCIR656 LHLH: CAP 16 bit CCIR601 LHHL: CAP 16 bit VIP 1.1 LHHH: CAP 16 bit VIP 2.0 HXXX: TS 8 bit

IO Pads with Integrated Pull Up Resistors

Some of the CX700/CX700M IO pads, as listed below, are integrated with internal 10K Ohms \pm 30% Pull Up resistor to reduce component counts on the motherboards.

1. IO pads with hardwired Pull Up: LPCFRAME#, LPCAD[3:0], MSCK, MSDT, KBCK, KBDT, PDCS1#, SERIRQ
2. IO pads with programmable Pull Up:
 - PCI bus signals: FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PERR#, SERR#
 - PCI bus signals: INT[A, B, C, D]#, REQ[0-3]#, GNT[0-3]#
 - EIDE signals: IRQ15
 - Power management event signals: BATLOW#, THRM#, PME#, RING#, EXTSMI#, LID#, SMBALRT#, PWRBTN#

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T _C	Operating case temperature	0	85	°C	1
T _S	Storage temperature	-55	125	°C	1
V _{IN}	Input voltage	-0.5	V _{RAIL} + 10%	Volts	1, 2
V _{OUT}	Output voltage	-0.5	V _{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface voltage is CPU dependent. Memory is 2.5V (DDR) or 1.8V (DDR2). Graphics / Display is 3.3V.

DC Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ±5%, V_{CORE} = 1.5V ±5%, GND=0V

Table 4. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V _{IL}	Input Low Voltage	-0.50	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage	-	0.55	V	I _{OL} = 4.0mA
V _{OH}	Output High Voltage	2.4	-	V	I _{OH} = -1.0mA
I _{IL}	Input Leakage Current	-	±10	uA	0 < V _{IN} < V _{CC}
I _{OZ}	Tristate Leakage Current	-	±20	uA	0.55 < V _{OUT} < V _{CC}

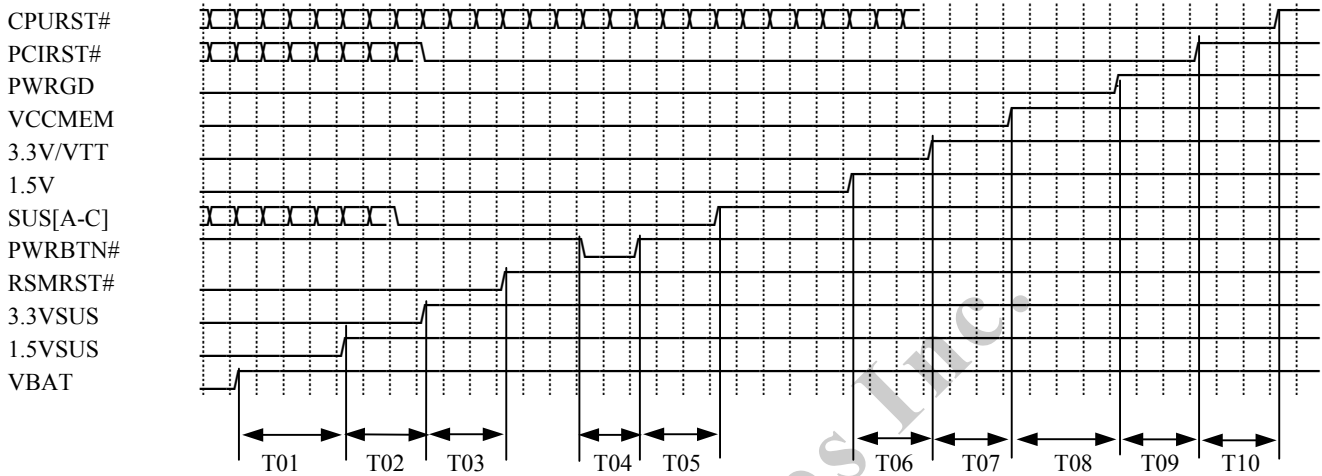
Package Weight Specifications

Table 5. Package Weight Specifications

To Be Provided

Power Sequence

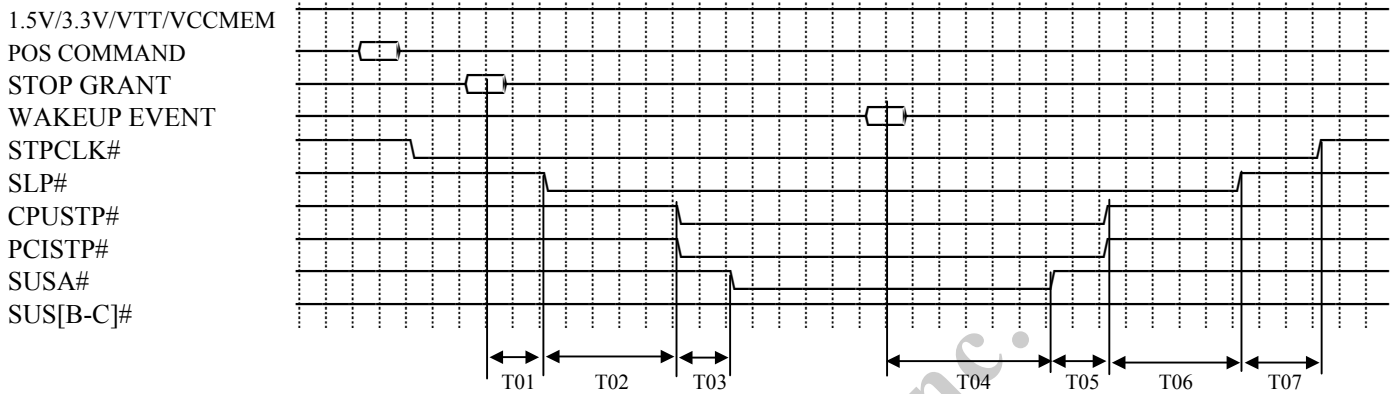
Figure 4. Power On Sequence and Reset Signal Timing



Symbol	Parameter	Min	Max	Unit	Note
T01	VBAT supply active to 5VSUS supply active	0	—	ms	
T02	1.5VSUS supply active to 3.3VSUS supply active	0.5	—	ms	
T03	3.3VSUS supply active to RSMRST# inactive	5	—	ms	
T04	PWRBTN# active width	1	—	RTCCLK	
T05	PWRBTN# rising to SUS[A-C]# inactive	4	5	RTCCLK	
T06	1.5V supply active to 3.3V/VTT supply active	0.5	—	ms	
T07	3.3V supply active to VCCMEM supply active	0	20	ms	
T08	VCCMEM supply active to PWRGD active	99	—	ms	
T09	PWRGD active to PCIRST# inactive	7	—	ms	
T10	PCIRST# inactive to CPURST# inactive	12	—	us	1

1. CPURST# is de-asserted after the completion of the ROMSIP cycle.

Figure 5. Power On Suspend (S1) and Resume Sequence

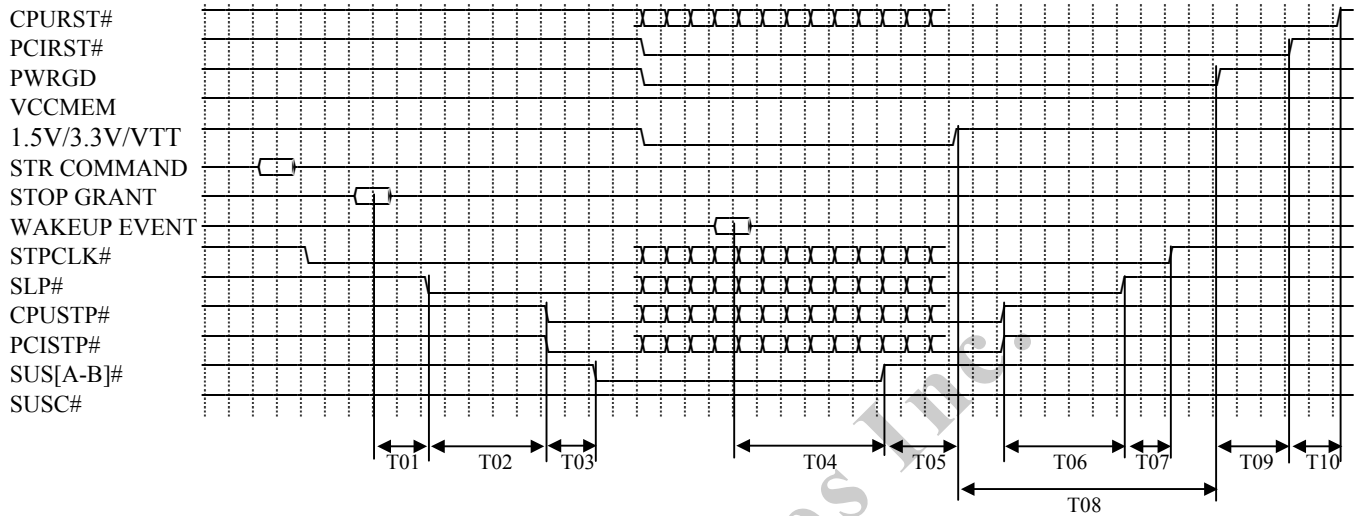


Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	1	RTCCLK	
T02	SLP# active to CPUTSTP# and PCISTP# active	—	2	RTCCLK	
T03	CPUTSTP# and PCISTP# active to SUSA# active	—	1	RTCCLK	
T04	Wakeup Event to SUSA# inactive	—	2	RTCCLK	
T05	SUSA# inactive to CPUTSTP# and PCISTP# inactive	16	32	ms	1
T06	CPUTSTP# and PCISTP# inactive to SLP# inactive	1.03	2.03	ms	2
T07	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	

1. 1. If B0D17F0 Rx95[7] = 1, the minimum delay is 1ms and the maximum delay is 2ms.
2. 2. If B0D17F0 Rx95[7] = 1, the minimum delay is 155us and the maximum delay is 280us.

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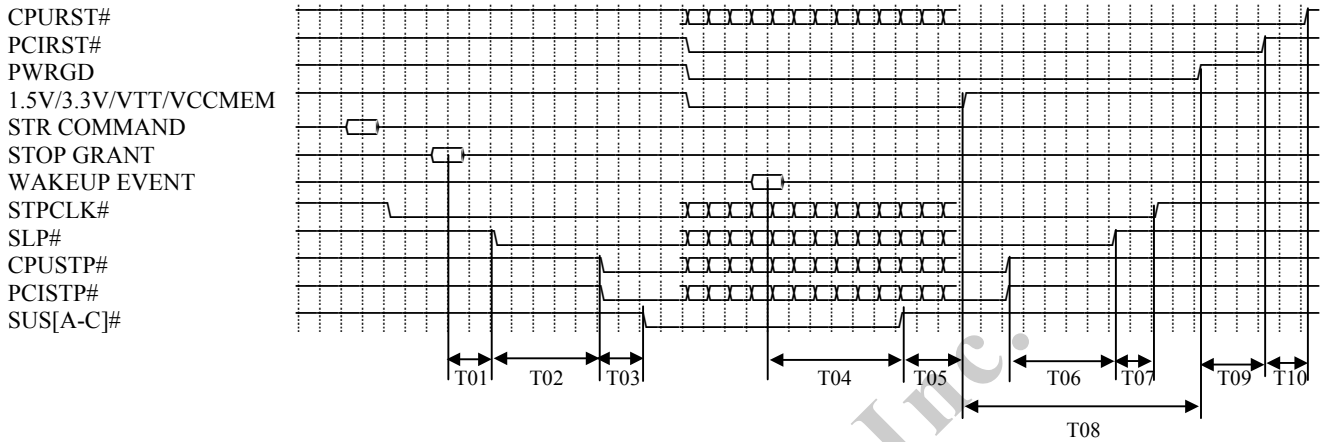
Figure 6. Suspend to RAM (S3) and Resume Sequence



Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	1	RTCCLK	
T02	SLP# active to CPUTSTP# and PCISTP# active	—	2	RTCCLK	
T03	CPUTSTP# and PCISTP# active to SUS[A-B]# active	—	1	RTCCLK	
T04	Wakeup Event to SUS[A-B]# inactive	—	2	RTCCLK	
T05	SUS[A-B]# inactive to 1.5V/3.3V/VTT supplies active	—	16	ms	1
T06	CPUTSTP# and PCISTP# inactive to SLP# inactive	1.03	2.03	ms	2
T07	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	
T08	1.5V/3.3V/VTT supplies active to PWRGD active	99	—	ms	
T09	PWRGD active to PCIRST# inactive	7	—	ms	
T10	PCIRST# inactive to CPURST# inactive	12	—	us	3

1. If B0D17F0 Rx95[7] = 1, the delay from SUS[A-B]# inactive to 1.5V/3.3V/VTT supplies active must be less or equal to 1ms.
2. If B0D17F0 Rx95[7] = 1, the minimum delay is 155us and the maximum delay is 280us.
3. CPURST# is de-asserted at the completion of the ROMSIP cycle.

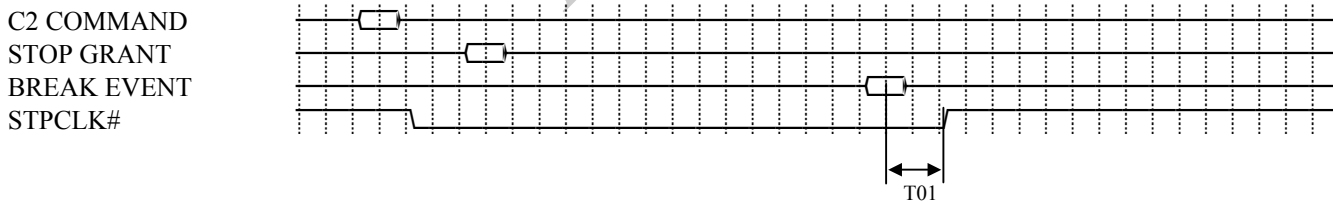
Figure 7. Suspend to DISK (S4) and Resume Sequence



Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	1	RTCCLK	
T02	SLP# active to CPUSTP# and PCISTP# active	—	2	RTCCLK	
T03	CPUSTP# and PCISTP# active to SUS[A-C]# active	—	1	RTCCLK	
T04	Wakeup Event to SUS[A-C]# inactive	—	2	RTCCLK	
T05	SUS[A-C]# inactive to 1.5V/3.3V/VTT/VCCMEM supplies active	—	16	ms	1
T06	CPUSTP# and PCISTP# inactive to SLP# inactive	1.03	2.03	ms	2
T07	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	
T08	1.5V/3.3V/VTT/VCCMEM supplies active to PWRGD active	99	—	ms	
T09	PWRGD active to PCIRST# inactive	7	—	ms	
T10	PCIRST# inactive to CPURST# inactive	12	—	us	3

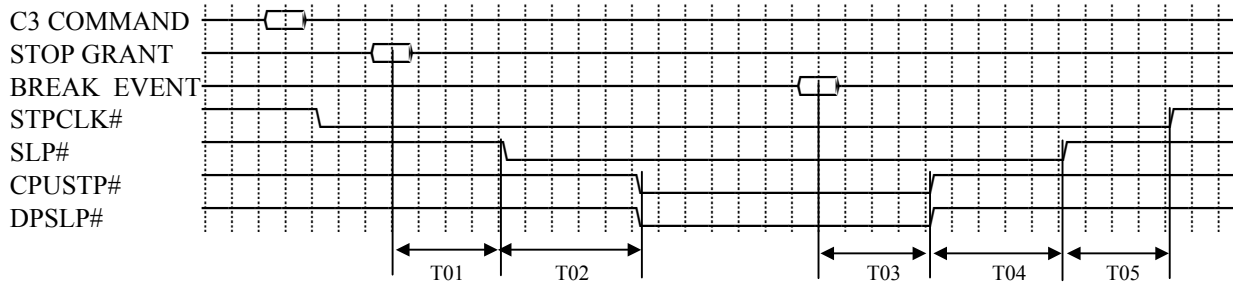
1. If B0D17F0 Rx95[7] = 1, the delay from SUS[A-C]# inactive to 1.5V/3.3V/VTT/VCCMEM supplies active must be less or equal to 1ms.
2. If B0D17F0 Rx95[7] = 1, the minimum delay is 155us and the maximum delay is 280us.
3. CPURST# is de-asserted at the completion of the ROMSIP cycle.

Figure 8. CPU C2 Sequence



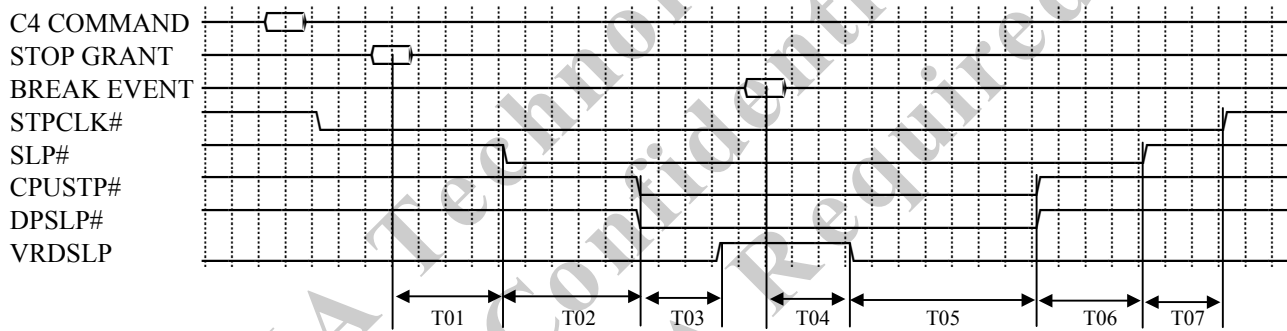
Symbol	Parameter	Min	Max	Unit	Note
T01	Break Event to STPCLK# inactive	2	—	PCICLK	

Figure 9. CPU C3 Sequence



Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	7.5	—	us	
T02	SLP# active to CPUSTP# and DPSLP# active	11.25	—	us	
T03	Break Event to CPUSTP# and DPSLP# inactive	7.5	—	us	
T04	CPUSTP# and DPSLP# inactive to SLP# inactive	7.5	—	us	
T05	SLP# inactive to STPCLK# inactive	7.5	—	us	

Figure 10. CPU C4 Sequence



Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	7.5	—	us	
T02	SLP# active to CPUSTP# and DPSLP# active	11.25	—	us	
T03	CPUSTP# and DPSLP# active to VRDSLP active	3.75	—	us	
T04	Break Event to VRDSLP inactive	—	7.5	us	
T05	VRDSLP inactive to CPUSTP# and DPSLP# inactive	50	—	us	
T06	CPUSTP# and DPSLP# inactive to SLP# inactive	7.5	—	us	
T07	SLP# inactive to STPCLK# inactive	7.5	—	us	

MECHANICAL SPECIFICATIONS

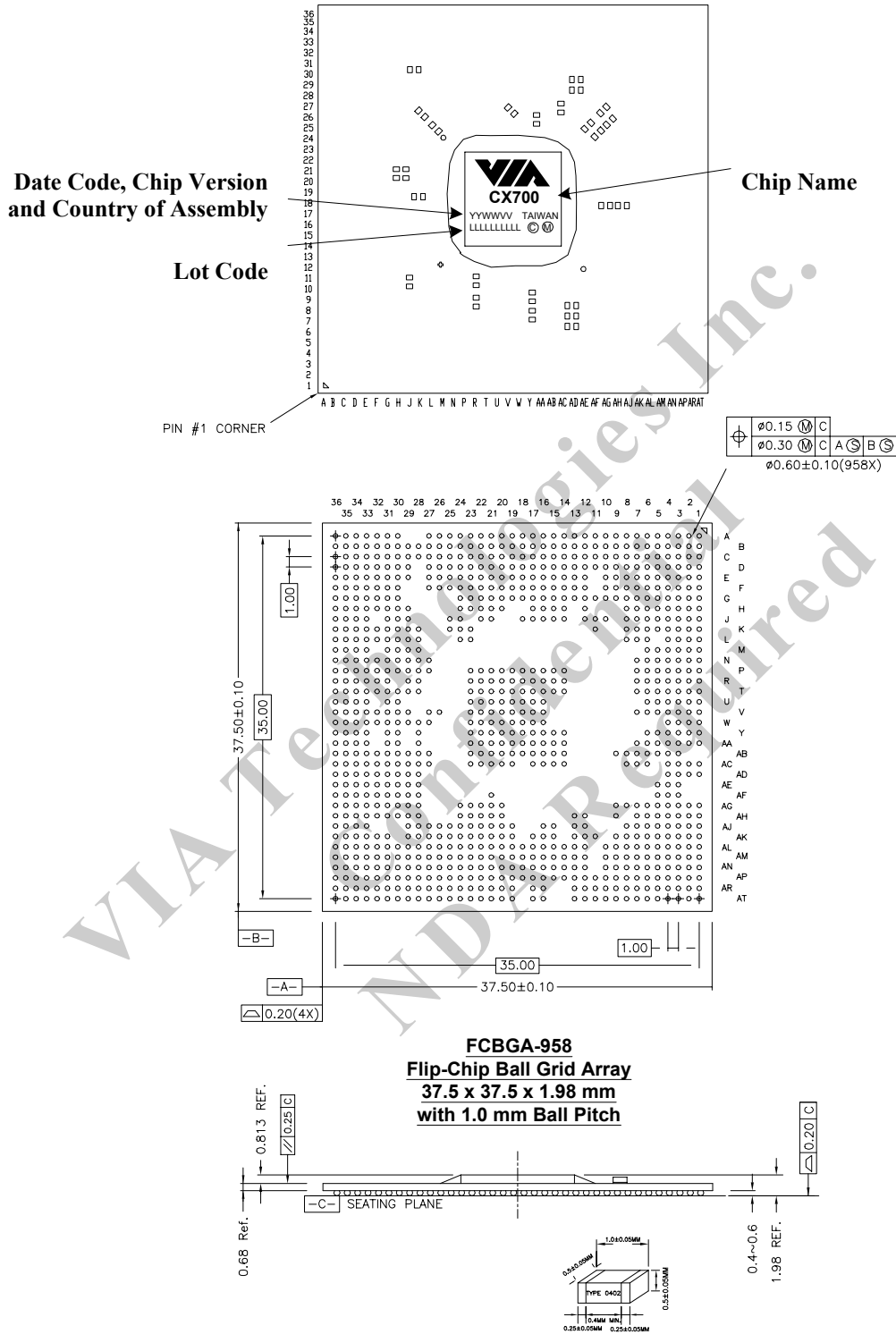
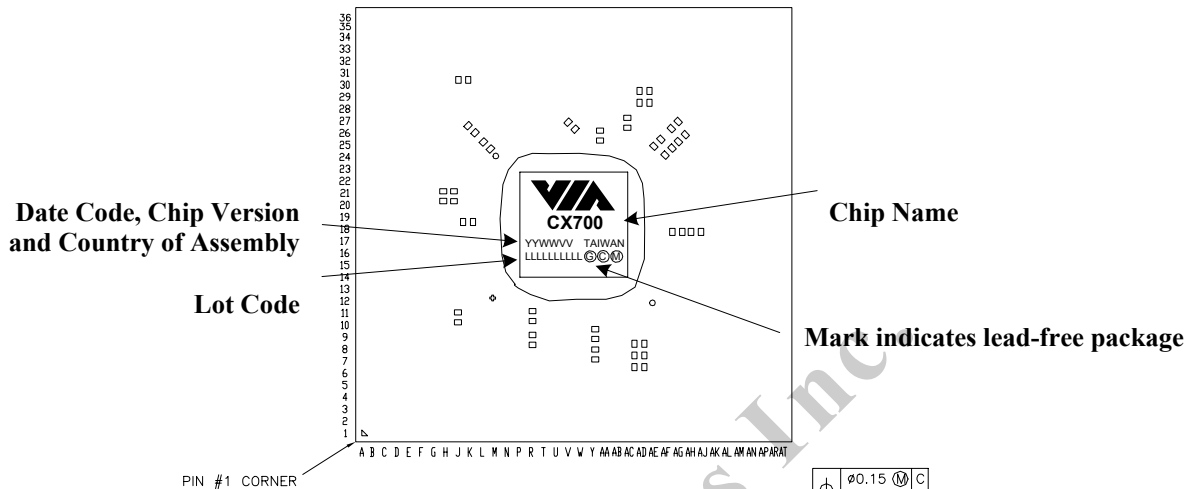
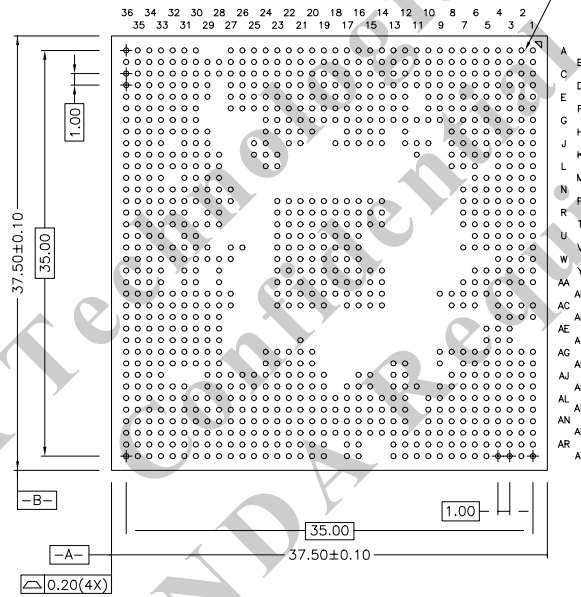


Figure 11. Mechanical Specifications – FCBGA-958 Ball Grid Array Package



⌀0.15	Ⓜ	Ⓢ	Ⓢ
⌀0.30	Ⓜ	Ⓢ	Ⓢ
⌀0.60±0.10(958X)			



FCBGA-958
Flip-Chip Ball Grid Array
37.5 x 37.5 x 1.98 mm
with 1.0 mm Ball Pitch

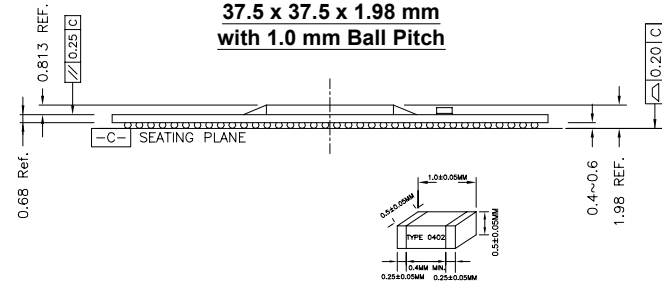


Figure 12. Lead-Free Mechanical Specifications – FCBGA-958 Ball Grid Array Package