μPD7201A
Multiprotocol, Serial Communications Controller

Description

The μPD7201A is a dual-channel, multiprotocol, serial communications controller (MPSCC) that satisfies a wide variety of serial data communication requirements in computer systems. Its basic function is as a serial-to-parallel, parallel-to-serial converter/controller, and it is software configurable for serial data communications applications.

The μPD7201A can handle asynchronous and synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. It also supports virtually any other serial protocol for applications other than data communications.

The μPD7201A can generate and check cyclic redundancy check (CRC) codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where modem controls are not needed, they can be used for general-purpose I/O.

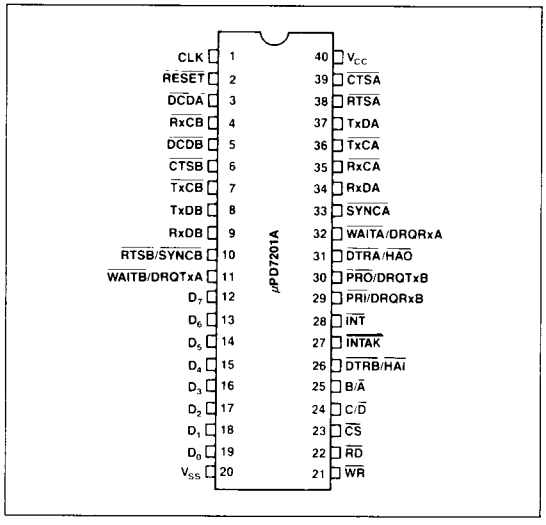
Features

- ☐ Two independent full-duplex serial channels
- ☐ Four independent DMA channels for send/receive data for both serial inputs/outputs
- ☐ Programmable interrupt vectors and interrupt priorities
- ☐ Modem control signals
- ☐ Variable software programmable data rate, up to 1 Mb/s at 5-MHz system clock
- ☐ Double-buffered transmitter data and quadruple-buffered receive data
- ☐ Selectable CRC algorithm
- ☐ Selection of interrupt, DMA, or polling mode of operation
- ☐ Asynchronous operation
  - — Character length: 5, 6, 7, or 8 bits
  - — Data clock frequency: 1x, 16x, 32x, or 64x data rate
  - — Parity: odd, even, or disable
  - — Break generation and detection
  - — Interrupt on parity, overrun, or framing errors
- ☐ Monosync, bisync, and external sync operations
  - — Software selectable sync characters
  - — Automatic sync insertion
  - — CRC generation and checking
- ☐ HDLC and SDLC operations
  - — Abort sequence generation and detection
  - — Automatic zero insertion and detection
  - — Address field recognition
  - — CRC generation and checking
  - — I-field residue handling
- ☐ N-channel MOS technology
- ☐ Single +5V power supply; interface to most microprocessors including 8080, 8085, 8086, and others.
- ☐ Single-phase TTL system clock: up to 5 MHz
- ☐ Plastic and ceramic dual-in-line packages

Ordering Information

Part Number	Package Type
μPD7201AC	40-pin plastic DIP
μPD7201AD	40-pin ceramic DIP

Pin Configuration



Pin Identification

No.	Symbol	Function
1	CLK	System clock input
2	$\overline{RESET}$	Reset input
3	$\overline{DCDA}$	Data carrier detect input A
4	$\overline{RxCB}$	Receiver clock input B
5	$\overline{DCDB}$	Data carrier detect input B
6	$\overline{CTSB}$	Clear to send input B
7	$\overline{TxCB}$	Transmitter clock input B
8	TxDB	Transmit data output B
9	RxDB	Receive data input B
10	$\overline{RTSB}/\overline{SYNCB}$	Request to send output B/Synchronization input/output B
11	$\overline{WAITB}$/DRQTxA	Wait output B/Transmit DMA request output A
12–19	D_7-D_0	Data Bus
20	V_{SS}	Ground
21	$\overline{WR}$	Write strobe input
22	$\overline{RD}$	Read strobe input
23	$\overline{CS}$	Chip select input
24	C/$\overline{D}$	Control/data input
25	B/$\overline{A}$	Channel select input
26	$\overline{DTRB}/\overline{HAI}$	Data terminal output B/Hold acknowledge input
27	$\overline{INTAK}$	Interrupt acknowledge input
28	$\overline{INT}$	Interrupt request output
29	$\overline{PRI}$/DRQRxB	Interrupt priority input/Receive DMA request output B
30	$\overline{PRO}$/DRQTxB	Interrupt priority output/Transmit DMA request output B
31	$\overline{DTRA}/\overline{HAO}$	Data terminal output A/Hold acknowledge output
32	$\overline{WAITA}$/DRQRxA	Wait output A/Receive DMA request output A
33	$\overline{SYNCA}$	Synchronization input/output A
34	RxDA	Receive data input A
35	$\overline{RxCA}$	Receiver clock input A
36	$\overline{TxCA}$	Transmitter clock input A
37	TxDA	Transmit data output A
38	$\overline{RTSA}$	Request to send output A
39	$\overline{CTSA}$	Clear to send input A
40	V_{CC}	+5 V

Pin Functions

CLK [System Clock]

A TTL-level clock signal is applied to the CLK input. The system clock frequency must be at least 4.5 times the data rate.

$\overline{RESET}$ [Reset]

A low on the $\overline{RESET}$ input (one complete CLK cycle minimum) initializes the MPSCC to the following conditions: receivers and transmitters disabled, TxDA and TxDB set to marking (high), and modem controls ($\overline{DTRA}$, $\overline{DTRB}$, $\overline{RTSA}$, $\overline{RTSB}$) set high.

In addition, all interrupts are disabled and all interrupt and DMA requests are cleared. All control registers must be rewritten after a reset before transmission or reception can be restarted.

$\overline{DCDA}$, $\overline{DCDB}$ [Data Carrier Detect]

The $\overline{DCDA}$ and $\overline{DCDB}$ inputs go low to indicate the presence of valid serial data at RxD. The MPSCC may be programmed so that the receiver is enabled only when $\overline{DCD}$ is low, and so that any change in state that lasts longer than the minium specified pulse width causes an interrupt and latches the $\overline{DCD}$ status bit to the new state.

$\overline{RxCA}$, $\overline{RxCB}$ [Receiver Clock]

The $\overline{RxCA}$ and $\overline{RxCB}$ inputs control sampling and shifting serial data at RxDA and RxDB. The MPSCC can be programmed so that the clock rate is 1, 16, 32, or 64 times the data rate. RxD is sampled on the rising edge of $\overline{RxC}$. $\overline{RxC}$ features a Schmitt-trigger input for relaxed rise and fall time requirements.

$\overline{TxCA}$, $\overline{TxCB}$ [Transmitter Clock]

The $\overline{TxCA}$ and $\overline{TxCB}$ inputs control the rate at which data is shifted out at TxDA and TxDB. The MPSCC can be programmed so that the clock rate is 1, 16, 32, or 64 times the data rate. Data changes on the falling edge of $\overline{TxC}$. $\overline{TxC}$ features a Schmitt-trigger input for relaxed rise and fall time requirements.

TxDA, TxDB [Transmit Data]

TxDA and TxDB output serial data from the MPSCC. (Marking high).

RxDA, RxDB [Receive Data]

RxDA and RxDB input serial data to the MPSCC. (Marking high.)

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ [Clear to Send]

The $\overline{\text{CTSA}}$ and $\overline{\text{CTSB}}$ inputs go low to indicate that the receiving modem or peripheral is ready to receive data from the MPSCC. The MPSCC can be programmed so that the transmitter is enabled only when CTS is low. As with $\overline{\text{DCD}}$, the MPSCC can be programmed to cause an interrupt and latch the new state when $\overline{\text{CTS}}$ changes state for longer than the minimum specified pulse width.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$ [Request to Send]

When the MPSCC is in one of the synchronous modes, $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ are general-purpose outputs that can be set or reset with commands to the MPSCC. In asynchronous mode, $\overline{\text{RTS}}$ is active (low) as soon as it is programmed on. However, when programmed off, $\overline{\text{RTS}}$ remains active until the transmitter is completely empty. This feature simplifies the programming required to perform modem control.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$ [Synchronization]

The function of the $\overline{\text{SYNCA}}$ and $\overline{\text{SYNCB}}$ pins depends on the MPSCC operating mode. In asynchronous mode, $\overline{\text{SYNC}}$ is used as an input that the processor can read. It can be programmed to generate an interrupt in the same manner as $\overline{\text{DCD}}$ or $\overline{\text{CTS}}$.

In external sync mode, $\overline{\text{SYNC}}$ is an active-low input that notifies the MPSCC that synchronization has been achieved (see timing waveforms for details). Once synchronization is achieved, $\overline{\text{SYNC}}$ should be held low until synchronization is lost or a new message is about to start.

In internal synchronization modes (monosync, bisync, HDLC), $\overline{\text{SYNC}}$ is an output which is active (low) whenever a SYNC character match is made. There is no qualifying logic associated with this function. Regardless of character boundaries, $\overline{\text{SYNC}}$ is active on any match.

DRQTxA, DRQTxB, DRQRxA, DRQRxB [DMA Request]

When a DRQTxA, DRQTxB, DRQRxA, or DRQRxB output is active (high), it indicates to a DMA controller that a transmitter or receiver is requesting a DMA data transfer.

$\overline{\text{WAITA}}$, $\overline{\text{WAITB}}$ [Wait]

The $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ outputs synchronize the processor with the MPSCC when block transfer mode is used. It can be programmed to operate with either the receiver or transmitter, but not both simutaneously. $\overline{\text{WAIT}}$ is normally inactive (high). If the processor tries, for example, to perform an inappropriate data transfer such as a write to the transmitter when the transmitter buffer is full, the $\overline{\text{WAIT}}$ output for the channel will go active (low) until the MPSCC is ready to accept the data. The $\overline{\text{CS}}$, C/$\overline{\text{D}}$, B/$\overline{\text{A}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ inputs must remain stable while wait is active. (Open drain.)

D_0-D_7 [Data Bus]

The three-state data bus lines are connected to the system data bus. Data or status from the MPSCC is output on these lines when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are active (low). Data and commands are latched into the MPSCC on the rising edge of $\overline{\text{WR}}$ when $\overline{\text{CS}}$ is active.

$\overline{\text{WR}}$ [Write Strobe]

A low on the $\overline{\text{WR}}$ input (with either CS during the read cycle or HAI during a DMA cycle) notifies the MPSCC to write data or control information to the device.

$\overline{\text{RD}}$ [Read Strobe]

A low on the $\overline{\text{RD}}$ input (with either $\overline{\text{CS}}$ during a read cycle or $\overline{\text{HAI}}$ during a DMA cycle) notifies the MPSCC to read data or status from the device.

$\overline{\text{CS}}$ [Chip Select]

A low on the $\overline{\text{CS}}$ input allows the MPSCC to transfer data or commands during a read or write cycle.

C/$\overline{\text{D}}$ [Control/Data]

The C/$\overline{\text{D}}$ input, with $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and B/$\overline{\text{A}}$ selects the data register (C/D = 0) or the control and status registers (C/D = 1) for access over the data bus.

B/$\overline{\text{A}}$ [Channel Select]

B/$\overline{\text{A}}$ input low selects channel A and B/$\overline{\text{A}}$ high selects channel B for access during a read or write cycle.

$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$ [Data Terminal]

The $\overline{\text{DTRA}}$ and $\overline{\text{DTRB}}$ outputs are general-purpose, active-low outputs which may be set or reset with commands to the MPSCC.

$\overline{\text{INTAK}}$ [Interrupt Acknowledge]

The processor generates two or three $\overline{\text{INTAK}}$ low pulses (depending on the processor type) to signal all peripheral devices that an interrupt acknowledge sequence is taking place. During the interrupt acknowledge sequence, the MPSCC, if so programmed, places information on the data bus to vector the processor to the appropriate interrupt service location.

$\overline{\text{INT}}$ [Interrupt Request]

The $\overline{\text{INT}}$ output is pulled low when an internal interrupt request is accepted. (Open drain.)

$\overline{\text{PRI}}$ [Interrupt Priority In]

The $\overline{\text{PRI}}$ input informs the MPSCC that the highest priority device is requesting an interrupt. It is used with $\overline{\text{PRO}}$ to implement a priority-resolution daisychain when there is more than one interrupting device. The state of $\overline{\text{PRI}}$ and the programmed interrupt mode determine the MPSCC's response to an interrupt acknowledge sequence.

$\overline{\text{PRO}}$ [Interrupt Priority Out]

The $\overline{\text{PRO}}$ output is active (low) when $\overline{\text{PRI}}$ is active (low) and the MPSCC is not requesting an interrupt ($\overline{\text{INT}}$ is not active).

The active state informs the next lower priority device that there are no higher priority interrupt requests pending during an acknowledge sequence.

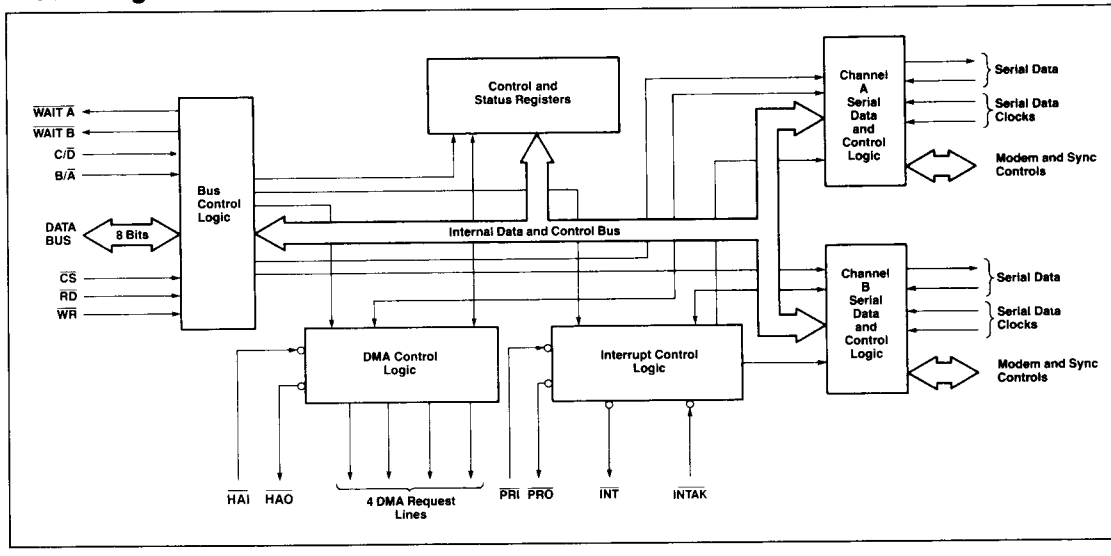
$\overline{\text{HAI}}$ [Hold Acknowledge In]

The $\overline{\text{HAI}}$ input goes low to notify the MPSCC that the host processor has acknowledged the DMA request and has placed itself in the hold state. The MPSCC then performs a DMA cycle for the highest priority outstanding DMA request, if any.

$\overline{\text{HAO}}$ [Hold Acknowledge Out]

The $\overline{\text{HAO}}$ output, with $\overline{\text{HAI}}$, implements a priority-resolution daisychain for multiple DMA devices. $\overline{\text{HAO}}$ is active (low) when $\overline{\text{HAI}}$ is active and there are no DMA requests pending in the MPSCC.

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power Supply, V_{CC}	−0.5 to + 7.0 V
Input Voltage, V_I	−0.5 to + 7.0 V
Output Voltage, V_O	−0.5 to + 7.0 V
Operating temperature, T_{OPT}	0°C to + 70°C
Storage Temperature, T_{STG}	−65°C to + 150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; V_{CC} = GND = OV

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input Capacitance	C_{IN}		10	pF	fc = 1MHz
Output Capacitance	C_{OUT}		15	pF	Unmeasured pins
I/O Capacitance	$C_{I/O}$		20	pF	returned to GND.

DC Characteristics

T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input low voltage	V_{IL}	−0.5	+0.8	V	
Input high voltage	V_{IH}	+2.0	V_{CC}+0.5	V	
Output low voltage	V_{OL}		+0.45	V	I_{OL} = +2.0 mA
Output high Voltage	V_{OH}	+2.4		V	I_{OH} = 200μA
Input leakage current	I_{IL}		±10	μA	$V_{IN}=V_{CC}$ to 0 V
Output leakage current	I_{OL}		±10	μA	$V_{OUT}=V_{CC}$ to 0 V
V_{CC} supply current	I_{CC}		230	mA	

AC Characteristics

T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock cycle	t_{CY}	200	4000	ns	
Clock high width	t_{CH}	70	2000	ns	
Clock low width	t_{CL}	70	2000	ns	

AC Characteristics (cont)

T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock rise time	t_r	0	30	ns	
Clock fall time	t_f	0	30	ns	
Address setup to $\overline{RD}$	t_{AR}	0		ns	
Address hold from $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ pulse width	t_{RR}	200		ns	
Data output delay from address	t_{AD}		200	ns	
Data output delay from $\overline{RD}$	t_{RD}		200	ns	
Data float delay from $\overline{RD}$	t_{DF}	10	100	ns	
Address setup from $\overline{WR}$	t_{AW}	0		ns	
Address hold from $\overline{WR}$	t_{WA}	0		ns	
$\overline{WR}$ pulse width	t_{WW}	200		ns	
Data setup to $\overline{WR}$	t_{DW}	130		ns	
Data hold from $\overline{WR}$	t_{WD}	0		ns	
PRO delay from $\overline{PRI}$	t_{PIPO}		100	ns	
PRO delay from $\overline{INTAK}$	t_{IAPO}		200	ns	
PRI setup to $\overline{INTAK}$	t_{PHA}	0		ns	
PRI hold from $\overline{INTAK}$	t_{IAPI}	20		ns	
$\overline{INTAK}$ pulse width	t_{IAIA}	200		ns	
Data output delay from $\overline{INTAK}$	t_{IAD}		200	ns	
Data float delay from $\overline{INTAK}$	t_{DF}	10	100	ns	
Request hold from $\overline{RD}/\overline{WR}$	t_{CQ}		150	ns	
$\overline{HAI}$ setup to $\overline{RD}/\overline{WR}$	t_{HIC}	300		ns	
$\overline{HAI}$ hold from $\overline{RD}/\overline{WR}$	t_{CHI}	0		ns	
$\overline{HAO}$ delay from $\overline{HAI}$	t_{HIHO}		100	ns	
Data clock cycle	t_{DCY}	400		ns	RxC, TxC

2

AC Characteristics (cont)

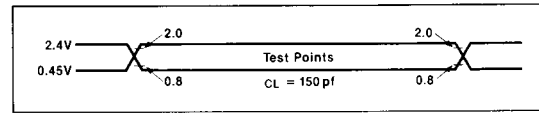
T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Data clock high width	t_{DCH}	180		ns	RxC, TxC
Data clock low width	t_{DCL}	180		ns	RxC, TxC
Tx data delay from TxC	t_{TCTD}		300	ns	x1 Mode
			1000	ns	x16, x32, x64 Mode
Rx data setup to RxC	t_{RDRC}	0		ns	
Rx Data hold from RxC	t_{RCRD}	140		ns	
INT delay Time from Tx Data	t_{IDI}		4–6	t_{CY}	
INT delay Time from RxC	t_{RCI}		7–11	t_{CY}	
CTS, DCD, SYNC high pulse width	t_{MH}	200		ns	
CTS, DCD, SYNC low pulse width	t_{ML}	200		ns	
External INT from CTS, DCD, SYNC	t_{MF}		500	ns	
Recovery time between controls	t_{RV}	300		ns	
WAIT delay time from Address	t_{AWT}		120	ns	
SYNC setup to RxC	t_{RCS}		100	ns	

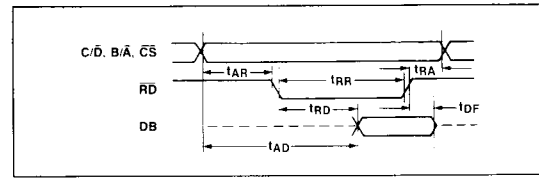
Note: 1. RESET must be active for a minimum of one complete CLK cycle.
2. In all modes system clock rate must be 4.5 times data rate.

Timing Waveforms

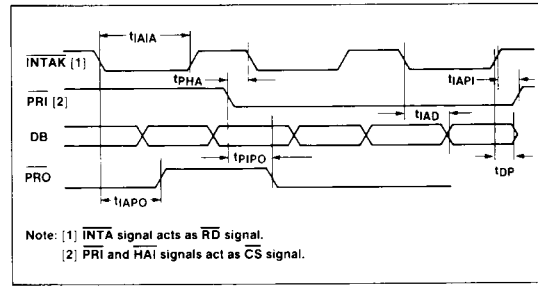
AC Waveform Measurement Points



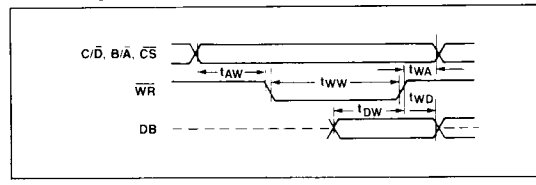
Read Cycle



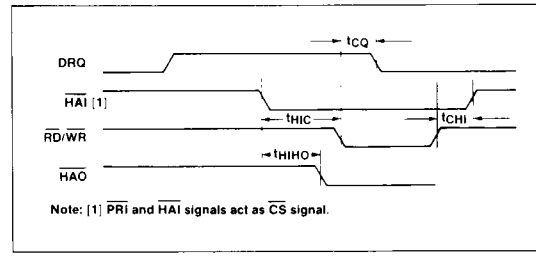
INTAK Cycle



Write Cycle

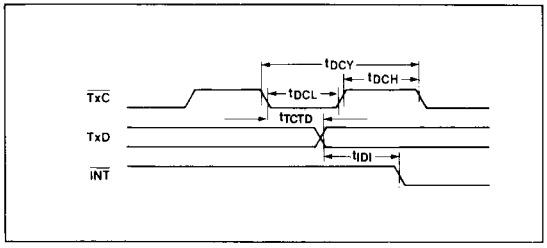


DMA Cycle

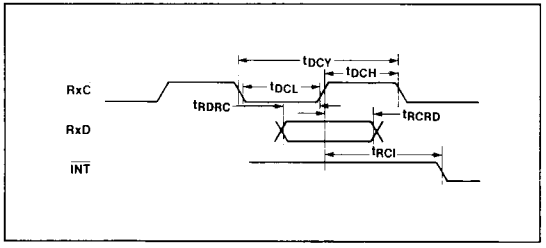


Timing Waveforms (cont)

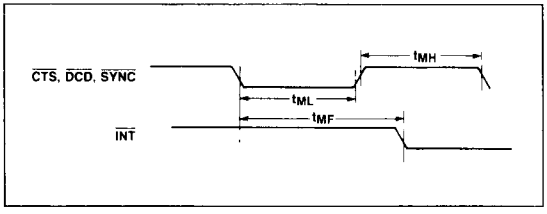
Transmit Data Cycle



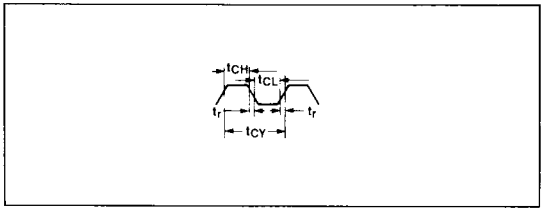
Receive Data Cycle



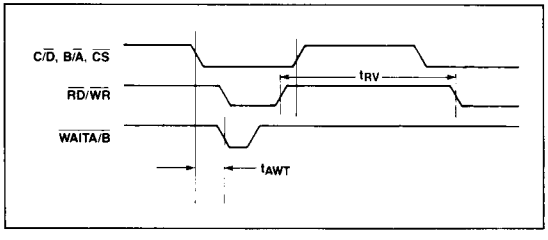
Other Timing



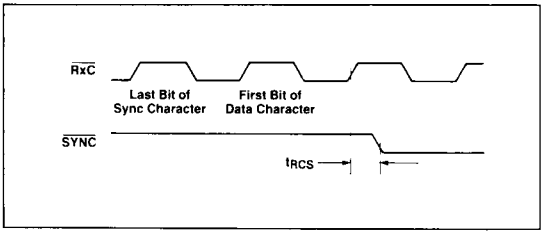
Clock



Read/Write Cycle (Software Block Transfer Mode)



Sync Pulse Generation (External Sync Mode)



Programming the MPSCC

Software operation of the MPSCC includes consistent register organization and high-level command structure to help minimize the number of operations required to implement complex protocol designs. The MPSCC also has extensive interrupt and status reporting capabilities to simplify programming.

The MPSCC Registers

The MPSCC interfaces to the system software with a number of control and status registers associated with each channel (see tables 1 and 2). Commonly used commands and status bits are accessed directly through control and status register 0. Other functions are accessed indirectly with a register pointer to minimize the address space that must be dedicated to the MPSCC.

All control and status registers except CR2 are separately maintained for each channel. Control and status register 2 are linked with the overall operation of the MPSCC and have different meanings when addressed through different channels.

Before intializing the MPSCC, first program control register 2A (2B if desired) to establish the MPSCC processor/bus interface mode. Each channel may then be programmed for separate use beginning with control register 4 to set the protocol mode for that channel. The remaining registers may then be programmed in any order.

Table 1. Control Registers

Control Register	Function
0	Frequently used commands and register pointer control
1	Interrupt control
2	Processor/bus interface control
3	Receiver control
4	Mode control
5	Transmitter control
6	Sync/address character
7	Sync character

Control Register 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CRC Control Command		Command			Register Pointer		

Register Pointer [D_0-D_2]

The register pointer specifies which register number is accessed at the next control register write or status register read. After a hardware or software reset, the register pointer is set to zero. Therefore, the first control byte goes to control register 0. When the register pointer is set to a value other than zero the next control or status ($C/\overline{D} = 1$) access is to the specified register. The pointer is then reset to 0 by setting the register pointer.

Commands [D_3-D_5]

Commands commonly used during the operation of the MPSCC are grouped in control register 0. They include the following:

Null [000]: This command has no effect and is used only to set the register pointer or issue a CRC command.

Send Abort [001]: When operating in the HDLC mode, this command causes the MPSCC to transmit the HDLC abort code by issuing 8 to 13 consecutive 1s. Any data currently in the transmitter or the transmitter buffer is destroyed. After sending the abort, the transmitter reverts to the idle phase (flags). When using the Tx byte count mode enable (D_6 of CR1), the send abort command is automatically issued when an underrun condition occurs.

Table 2. Status Registers

Status Register	Function
0	Buffer and "external/status" status
1	Received character error and special condition status
2 (Channel B only)	Interrupt Vector
3	Tx byte count register, low byte
4	Tx byte count register, high byte

Reset External Status Interrupt [010]: When the external/status change flag is set, the condition of bits D_3-D_7 of status register 0 are latched to capture the short pulses that may occur. The reset external/status interrupts command reenables the latches so that new interrupts may be sensed.

Channel Reset [011]: This command has the same effect on a single channel as an external reset at pin 2. A channel reset command to channel A rests the internal interrupt prioritization logic. This does not occur when a channel reset command is issued to channel B. All control registers associated with the channel to be reset must be reinitialized. After a channel reset, wait at least four system clock cycles before writing new commands or controls to that channel.

Enable Interrupt on Next Character [100]: Issue this command at any time when operating the MPSCC in an interrupt on first received character mode. This command must be issued at the end of a message to reenable the interrupt logic for the next received character (first character of the next message).

Reset Pending Transmitter Interrupt/DMA Request [101]: A pending transmitter buffer empty interrupt or DMA request can be reset without sending another character by issuing this command (typically at the end of a message). A new transmitter buffer empty interrupt or DMA request is not made until another character has been loaded and transferred to the transmitter shift register or when, if operating in synchronous mode, the first CRC character has been sent.

Error Reset [110]: This command resets a special receive condition interrupt. It also reenables the parity and overrun error latches that allow error checking at the end of a message.

End of Interrupt [111] [Channel A Only]: Once an interrupt request has been issued by the MPSCC, all lower priority internal and external interrupts in the daisy chain are held off to permit the current interrupt to be serviced while allowing higher priority interrupts to occur. At some point in the interrupt service routine (generally at the end), the end of the interrupt command must be issued to channel A to reenable the daisy chain and allow any pending lower priority internal interrupt requests to occur. The EOI command must be sent to channel A for interrupts that occured on either channel.

CRC Control Commands [D_6-D_7]

The following commands control the operation of the CRC generator/checker logic:

Null [00]: This command has no effect and is used when issuing other commands or setting the register pointer.

Reset Receiver CRC Checker [01]: This command resets the CRC checker to zero when the channel is in a synchronous mode. It resets to all 1s when in an HDLC mode.

Reset Transmitter CRC Generator [10]: This command resets the CRC generator to zero when the channel is in a synchronous mode. It resets to all 1s when in an HDLC mode.

Reset Idle/CRC Latch [11]: This command resets the idle/CRC latch so that when a transmitter underrun condition occurs (transmitter has no more characters to send), the transmitter enters the CRC phase of operation and begins to send the 16-bit CRC character calculated up to that point. The latch is then set so that if the underrun condition persists, idle characters are sent following the CRC. After a hardware or software reset, the latch is in the set state. This latch is automatically reset after the first character has been loaded into the Tx buffer in the HDLC mode.

Control Register 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Wait Function Enable	Tx Byte Count Mode Enable	Wait on Receive Transmitter	Receiver Interrupt Mode		Condition Affects Vector	Transmitter Interrupt Enable	Ext/Status INT Enable

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Low Byte							

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte							

External/Status Interrupt Enable [D_0]

When this bit is set to one, the MPSCC issues an interrupt whenever any of the following conditions occur:
- Transition of the DCD, CTS or SYNC input pin
- Entering or leaving synchronous hunt phase, break detection or termination
- HDLC abort detection or termination
- Idle/CRC latch set (CRC being sent)
- After ending flag is sent in the HDLC mode

Transmitter Interrupt Enable [D_1]

When this bit is set to one, the MPSCC issues an interrupt when the following conditions occur:
- A character currently in the transmitter buffer is transferred to the shift register (transmitter buffer becomes empty), or
- The transmitter enters the idle phase and begins transmitting sync or flag characters.
- The Tx byte count mode enable bit is set (D_6 of CR1 = 1). The 7201A will automatically issue a Tx interrupt or DMA request when the transmitter becomes enabled (D_3 of CR5 = 1).

Condition Affects Vector [D_2]

When this bit is set to zero, the fixed vector programmed in CR2B during MPSCC initialization is returned in an interrupt acknowledge sequence. When this bit is set to one, the vector is modified to reflect the condition that caused the interrupt. (Programmed in channel B for both channels).

Receiver Interrupt Mode [$D_3 \cdot D_4$]

This field controls how the MPSCC interrupt/DMA logic handles the character received condition.

Receiver Interrupts/DMA Request Disabled [00]: The MPSCC does not issue an interrupt or a DMA request when a character has been received.

Interrupt/DMA on First Received Character Only [01]: In this mode the MPSCC issues an interrupt only for the first character received after an enable interrupt/DMA on first character command (CR0) has been given. If the channel is in a DMA mode, a DMA request is issued for each character received, including the first. In general, use this mode whenever the MPSCC is in a DMA or block transfer mode. This will signal the processor that the beginning of an incoming message has been received.

Interrupt [and Issue a DMA Request] on All Received Characters [10] : In this mode an interrupt (and DMA request if the DMA mode is selected) is issued whenever there is a character present in the receiver buffer. A parity error is considered a special receive condition.

Interrupt [and Issue a DMA Request] on All Received Characters [11] : This mode is the same as the one above, except that a parity error is not considered a special receive condition. The following are considered special receive conditions:
— Receive overrun error
— Asynchronous framing error
— Parity error (if specified)
— HDLC end of message (final flag received)

Wait on Receiver/Transmitter [D_5]

If the wait function is enabled for block mode transfers, setting this bit to zero causes the MPSCC to issue a wait (WAIT output goes low) when the processor attempts to write a character to the transmitter while the transmitter buffer is full. Setting this bit to one causes the MPSCC to issue a wait when the processor attempts to read a character from the receiver while the receiver buffer is empty.

Tx Byte Count Enable [D_6]

Each channel has a 16-bit Tx byte count register used for automatic transmit termination. When this bit is set to one, the next two consecutive command cycle writes will be to the byte count register. The first byte is loaded into the lower 8 bits and the second to the upper 8 bits of the byte count register. The byte count register holds the number of transfers to be performed by the transmitter. A byte counter is incremented each time a transfer is performed until the value of the byte counter is equal to the value in the byte count register. When equal, interrupts or DMA requests will be stopped until the byte count enable bit is issued and a new byte count is loaded into the byte count register. If a transmit underrun occurs in the HDLC mode, and the byte count is not equal to the byte count register, an abort sequence will be sent automatically.

Also, when using the Tx byte count mode, a transmit interrupt or DMA request will automatically become active after issuing the TX enable command to CR5.

The Tx byte count mode can be cleared by either a channel reset command or a hardware reset.

Wait Function Enable [D_7]

Setting this bit to one enables the wait function selected by D_5 of CR1.

Control Register 2 (Channel A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Pin 10 SYNCB/ RTSB	Rx INT Mask	Interrupt Vector			Priority	DMA Mode Select	

DMA Mode Select [D_0 - D_1]

Setting this field determines whether channel A or B is used in a DMA mode [data transfers are performed by a DMA controller], or in a non-DMA mode where transfers are performed by the processor in either a polled, interrupt, or block transfer mode. The functions of some MPSCC pins are also controlled by this field. See table 3.

Priority [D_2]

This bit selects the relative priorities of the various interrupt and DMA conditions according to the application requirements. See table 4.

Interrupt Vector Mode [D_3 - D_5]

This field determines how the MPSCC responds to an interrupt acknowledge sequence from the processor. See table 5.

Rx INT Mask [D_6]

This option is generally used in the DMA modes. Enabling this bit inhibits the interrupt from occuring when the interrupt/DMA request on first received character mode is selected. In other words, only a DMA request will be generated when the first character is received.

Table 3. DMA Mode Selection

		Channel		Pin Function					
D_1	D_0	A	B	11	26	29	30	31	32
0	0	Non-DMA	Non-DMA	WAITB	DTRB	PRI	PRO	DTRA	WAITA
0	1	DMA	Non-DMA	DRQTxA	HAI	PRI	PRO	HAO	DRQRxA
1	0	DMA	DMA	DRQTXA	HAI	DRQRxB	DRQTxB	HAO	DRQRxA
1	1	DMA	DMA	DRQTxA	DTRB	DRQRxB	DRQTxB	DTRA	DRQRxA

Table 4. DMA/Interrupt Priorities

D_2	Mode		DMA Priority Relation	Interrupt Priority Relation
	Channel A	Channel B		
0	INT	INT		SRxA, RxA > TxA > SRxB, RxB > TxB > ExTA > ExTB
1	INT	INT		SRxA, RxA > SRxB, RxB > TxA > TxB > ExTA > ExTB
0	DMA	INT	RxA > TxA	SRxA, RxA > SRxB, RxB > TxB > ExTA > ExTB
1	DMA	INT	RxA > TxA	SRxA, RxA > SRxB, RxB > TxB > ExTA > ExTB
0	DMA	DMA	RxA > TxA > RxB > TxB	SRxA, RxA > SRxB, RxB > TxB > ExTB
1	DMA	DMA	RxA > RxB > TxA > TxB	SRxA, RxA > SRxB, RxB > ExTA, ExTB

Table 5. Interrupt Acknowledge Sequence Response

D_5	D_4	D_3	Mode	Status Register 2B and Interrupt Vector Bits Affected When Condition Affects Vector is Enabled
0	0	0	Nonvectored	$D_4D_3D_2$
0	0	1	Nonvectored	$D_4D_3D_2$
0	1	0	Nonvectored	$D_2D_1D_0$
0	1	1	Illegal	
1	0	0	8085 Master	$D_4D_3D_2$
1	0	1	8085 Slave	$D_4D_3D_2$
1	1	0	8086	$D_2D_1D_0$
1	1	1	8085/8259A Slave	$D_4D_3D_2$

Pin 10 $\overline{\text{SYNCB}}/\overline{\text{RTSB}}$ Select [D_7]

Programming a zero into this bit selects RTSB as the function of pin 10. A one selects SYNCB as the function.

Control Register 2 (Channel B)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector							

Interrupt Vector [D_0 · D_7]

When using the MPSCC in the vectored interrupt mode, the contents of this register are placed on the bus during the appropriate portion of the interrupt acknowledge sequence. Its value is modified if status affects vector is enabled. The value of SR2B can be read at anytime. This feature is useful in determining the cause of an interrupt when using the MPSCC in a nonvectored interrupt mode.

Control Register 3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Number of Received Bits per Character		Auto Enables	Enter Hunt Phase	Receiver CRC Enable	Address Search Mode	Sync Character Load Inhibit	Receiver Enable

Receiver Enable [D_0]

Setting this bit to one after the channel has been completely initialized allows the receiver to begin operation. This bit may be set to zero at any time to disable the receiver.

Sync Character Load Inhibit [D_1]

In the character synchronous modes, this bit inhibits the transfer of sync characters to the receiver buffer, thus performing a "sync-stripping" operation. When using the MPSCC's CRC checking ability, use this feature only to strip leading sync characters preceding a message, since the load inhibit does not exclude sync characters embedded in the message from the CRC calculation. Synchronous protocols using other types of block checking such as checksum or LRC are free to strip embedded sync characters.

Address Search Mode [D_2]

In the HDLC mode, setting this bit places the MPSCC in an address search mode. Character assembly does not begin until the 8-bit character (secondary address field) following the starting flag of a message matches either the address programmed into CR6 or the global address 11111111.

Receiver CRC Enable [D_3]

This bit enables and disables (1 = enable) the CRC checker in the character oriented protocol mode, allowing characters from the CRC calculation to be selectively included or excluded. The MPSCC has a one-character delay between the receiver shift register and the CRC checker so that the enabling or disabling takes affect with the last character transferred from the shift register to the receiver buffer. Therefore, there is one full character time in which to read the character and decide whether or not it should be included in the CRC calculation. In the HDLC mode, there is no 8-bit delay.

Enter Hunt Phase [D_4]

Although the MPSCC receiver automatically enters the sync hunt phase after a reset, there are other times when reentry is appropriate. This may occur when synchronization has been lost or, in an HDLC mode, to ignore the current incoming message. A one in this bit position at any time after initialization causes the MPSCC to reeneter the hunt phase.

Auto Enables [D_5]

Setting this bit to one causes the DCD and CTS inputs to act as enable inputs to the receiver and transmitter, respectively.

Number of Received Bits per Character [D_6 - D_7]

This field specifies the number of data bits assembled to make each character. The value may be changed while a character is being assembled and, if the change is made before the new number of bits has been reached, it affects that character. Otherwise, the new specifications take effect on the next character received. See table 6.

Control Register 4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Clock Rate		Sync Mode		Number of Stop Bits per Sync Mode		Parity Even/ Odd	Parity Enable

Parity Enable [D_0]

Setting this bit to one adds an extra data bit containing parity information to each transmitted character. Each received character is expected to contain this extra bit, and the receiver parity checker is enabled.

Table 6. Received Bits per Character

D_7	D_6	Bits per Character
0	0	5
0	1	7
1	0	6
1	1	8

Table 7. Stop Bits

D_3	D_2	Mode
0	0	Synchronous modes
0	1	Asynchronous 1 bit time (1 stop bit)
1	0	Asynchronous 1½ bit times (1½ stop bits)
1	1	Asynchronous 2 bit times (2 stop bits)

Parity Even/Odd [D_1]

Programming a zero into this bit when parity is enabled selects odd parity for the received character. Conversely, a one in this bit selects even parity generation and checking.

Number of Stop Bits or Sync Mode [D_2 - D_3]

This field specifies whether the channel is used in a synchronous or an asynchronous mode. In an asynchronous mode, this field also specifies the number of bit times used as the stop bit length by the transmitter. The receiver always checks for one stop bit. See table 7.

Sync Mode [D_4 - D_5]

When the stop bits/sync mode field is programmed for synchronous modes (D_2, D_3 = 00), this field specifies the particular synchronous format to be used. This field is ignored in an asynchronous mode. See table 8.

Clock Rate [D_6 - D_7]

This field specifies the relationship between the transmitter and receiver clock inputs (TxC, RxC) and the actual data rates at TxD and RxD. When operating in a synchronous mode, a 1x clock rate must be specified. In asynchronous modes, any of the rates may be specified. However, with a 1x clock rate, the receiver cannot determine the center of the start bit. In this mode, the sampling (rising) edge of RxC must be externally synchronized with the data. See table 9.

Table 8. Synchronous Formats

Sync Mode 1 D_5	Sync Mode 2 D_4	Mode
0	0	8-bit internal synchronization character (monosync)
0	1	16-bit internal synchronization character (bisync)
1	0	SDLC/HDLC
1	1	External synchronization (SYNC pin becomes an input)

Table 9. Clock Rates

Clock Rate 1 D_7	Clock Rate 2 D_6	Clock Rate
0	0	Clock Rate = 1x Data Rate
0	1	Clock Rate = 16x Data Rate
1	0	Clock Rate = 32x Data Rate
1	1	Clock Rate = 64x Data Rate

Control Register 5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DTR	Number of Transmitted Bits per Character		Send Break	Transmitter Enable	CRC Polynomial Select	RTS	Transmitter CRC Enable

Transmitter CRC Enable [D_0]

A one or a zero enables or disables (respectively) the CRC generator calculation. The enable or disable does not take effect until the next character is transferred from the transmitter buffer to the shift register, thus allowing specific characters to be included or excluded from the CRC calculation. By setting or resetting this bit just before loading the next character, it and subsequent characters are included or excluded from the calculation. If this bit is zero when the transmitter becomes empty, the MPSCC goes to the idle phase regardless of the state of the idle/CRC latch.

$\overline{RTS}$ [D_1]

In synchronous and HDLC modes, setting this bit to one causes the $\overline{RTS}$ pin to go low, while a zero causes it to go high. In an asynchronous mode, setting this bit to zero causes the $\overline{RTS}$ pin to go high when the transmitter is completely empty. This feature facilitates programming the MPSCC for use with asynchronous modems.

CRC Polynomial Select [D_2]

This bit selects the polynomial used by the transmitter and receiver for CRC generation and checking. A one selects the CRC-16 polynomial ($X^{16} + X^{15} + X^2 + 1$). A zero selects the CRC-CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$). In an HDLC mode CRC-CCITT must be selected. Either polynomial may be used in other synchronous modes.

Transmitter Enable [D_3]

After a reset, the transmitted data output (TxD) is held high (marking) and the transmitter is disabled until this bit is set.

In an asynchronous mode TxD remains high until data is loaded for transmission.

When the transmitter is disabled in an asynchronous mode, any character currently being sent is completed before TxD returns to the marking state.

If the transmitter is disabled during the data phase in a synchronous mode, the current character is sent. TxD then goes high (marking). In an HDLC mode, the current character is sent, but the following marking line is zero-inserted. That is, the line goes low for one bit time out of every five.

Never disable the transmitter during the HDLC data phase unless a reset follows immediately. In either case, any character in the buffer register is held.

Disabling the transmitter during the CRC phase causes the remainder of the CRC character to be bit-substituted with the sync (or flag). The total number of bits transmitted is correct and TxD goes high after they are sent.

If the transmitter is disabled during the idle phase, the remainder of the sync (flag) character is sent. TxD then goes high.

Send Break [D_4]

Setting this bit to one immediately forces the transmitter output (TxD) low (spacing). This function overrides the normal transmitter output and destroys any data being transmitted, although the transmitter is still in operation. Resetting this bit releases the transmitter output.

Transmitted Bits per Character [D_5 - D_6]

This field controls the number of data bits transmitted in each character. The number of bits per character may be changed by rewriting this field just before the first character is loaded. See table 10.

Normally each character is sent to the MPSCC right-justified and the unused bits are ignored. However, when sending five bits or less, the data should be formatted as shown below to inform the MPSCC of the precise number of bits to be sent. See table 11.

Table 10. Transmitted Bits per Character

Transmitted Bits per Character 1 D_6	Transmitted Bits per Character D_5	Bits per Character
0	0	5 or less (see below)
0	1	7
1	0	6
1	1	8

Table 11. Transmitted Bits per Character for 5 Characters or Less

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Number of Bits per Charater
1	1	1	1	0	0	0	D_0	1
1	1	1	0	0	0	D_1	D_0	2
1	1	0	0	0	D_2	D_1	D_0	3
1	0	0	0	D_3	D_2	D_1	D_0	4
0	0	0	D_4	D_3	D_2	D_1	D_0	5

$\overline{DTR}$ [Data Terminal Ready] [D_7]

When this bit is one, the $\overline{DTR}$ output is low [active]. When this bit is zero, $\overline{DTR}$ is high.

Control Register 6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Sync Byte 1							

Sync Byte 1 [D_0 - D_7]

Sync byte 1 is used in the following modes:

Monosync	8-bit sync character transmitted during the idle phase
Bisync	Least significant (first) 8 bits of the 16-bit transmit and receive sync character
External Sync	Sync character transmitted during the idle phase
HDLC	Secondary address value matched to secondary address field of the HDLC frame when the MPSCC is in the address search mode

Control Register 7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Sync Byte 2							

Sync Byte 2 [D_0 - D_7]

Sync byte 2 is used in the following modes:

Monosync	8-bit sync character matched by the receiver
Bisync	Most significant (second) 8 bits of the 16-bit transmit and receive sync characters
HDLC	The flag character 01111110 must be programmed into control register 7 for flag matching by the MPSCC receiver

Status Register 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Break/ Abort	Idle/ CRC	CTS	Sync Status	DCD	Tx Buffer Empty	INT Pending	Rec'd Char Available

Received Character Available [D_0]

When this bit is set, it indicates that one or more characters in the receiver buffer are available for the processor to read. Once the processor has read all the available characters, the MPSCC resets this bit until a new character is received.

Interrupt Pending [D_1 - Channel A Only]

The interrupt pending bit is used with the interrupt vector register (status register 2) to make it easier to determine the MPSCC's interrupt status. This is useful in a nonvectored interrupt mode where the processor must poll each device to determine the interrupt source. In this mode, interrupt pending is set when status register 2B is read, the PRI input is active (low), and the MPSCC requests interrupt service.

It is not necessary to read the status registers of both channels to determine if an interrupt is pending. If the status affects vector is enabled and the interrupt pending is set, the vector read from SR2 contains valid condition information.

In a vectored interrupt mode, interrupt pending is set during the interrupt acknowledge cycle (on the leading edge of the second INTAK pulse) when the MPSCC is the highest priority device requesting interrupt service (PRI is active). In either mode, if there are no other pending interrupt requests, interrupt pending is reset when the end of the interrupt command is issued.

Transmitter Buffer Empty [D_2]

This bit is set whenever the transmitter buffer is empty — except during the transmission of CRC. The MPSCC uses the buffer to facilitate this function. After a reset, the buffer is considered empty and transmit buffer empty is set.

External/Status Flags [D_3 - D_7]

The following status bits reflect the state of the various conditions that cause an external/status interrupt. The MPSCC latches all external/status bits whenever a change occurs that would cause an external/status interrupt, regardless of whether this interrupt is enabled. This allows transient status changes on these lines to be saved.

When operating the MPSCC in an interrupt-driven mode for external/status interrupts, read status register 0 when this interrupt occurs and issue a reset external/status interrupt command to reenable the interrupt and the latches. To poll these bits without interrupts, issue the reset external/status interrupt command to first update the status to reflect the current values.

$\overline{DCD}$ [D_3]: This bit reflects the inverted state of the $\overline{DCD}$ input. When $\overline{DCD}$ is low the $\overline{DCD}$ status bit is high. Any transition on this bit causes an external/status interrupt request.

Sync Status [D_4]: The meaning of this bit depends on the operating mode of the MPSCC.

Asynchronous mode: Sync status reflects the inverted state of the $\overline{SYNC}$ input. When $\overline{SYNC}$ is low, sync status is high. Any transition on this bit causes an external/status interrupt request.

External synchronization mode: Sync status operates in the same manner as in asynchronous mode. The MPSCC's receiver synchronization logic is also tied to the sync status bit in an external synchronization mode. A low-to-high transition ($\overline{SYNC}$ input going low) informs the receiver that synchronization has started and character assembly begins.

A low-to-high transition on the $\overline{SYNC}$ input indicates that synchronization has been lost. The sync status becomes zero and an external/status is generated. The receiver remains in the receive data phase until the enter hunt phase bit in control register 3 is set.

Monosync, bisync, HDLC modes: In these modes, sync status indicates whether the MPSCC receiver is in the sync hunt or receive data phase of operation. A zero indicates that the MPSCC is in the receive data phase, and a one indicates that the MPSCC is in the sync hunt phase (as in after a reset or when the enter sync hunt bit sets to 1). As in the other modes, a transition on this bit causes an external/status interrupt. Note that entering a sync hunt phase (when programmed) or a reset causes an external/status interrupt request which may be cleared immediately with a reset external/status interrupt command.

$\overline{CTS}$ [D_5]: This bit reflects the inverted state of the $\overline{CTS}$ input. When $\overline{CTS}$ is low, the $\overline{CTS}$ status bit is high. Any transition on this bit causes an external/status interrupt request.

Idle/CRC [D_6] [Tx Underrun/EOM]: This bit indicates the state of the idle/CRC latch used in the synchronous mode. After a hardware reset, this bit is set to one, indicating that the transmitter is completely empty. When the MPSCC enters idle phase, it automatically transmits sync or flag characters.

In the HDLC mode, the MPSCC automatically resets this latch after the first byte of a frame is written to the Tx buffer.

When the transmitter is completely empty, the MPSCC sends the 16-bit CRC character and sets the latch again. An external/status interrupt is issued when the latch is set, indicating that CRC is being sent. No interrupt is issued when the latch is reset.

Break/Abort [D_7]: In the asynchronous mode, this bit indicates the detection of a break sequence (a null character plus framing error that occurs when the RxD input is held low, spacing, for more than one character time). Break/abort is reset when RxD returns high (marking).

In the HDLC mode, break/abort indicates the detection of an abort sequence when seven or more ones are received in sequence. It is reset when a zero is received.

Any transition of the break/abort bit causes an external/status interrupt.

Status Register 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
End of SDLC Frame	CRC Framing Error	Over-run Error	Parity Error	SDLC Residue Code			All Sent

All Sent [D_0]

This bit is set when the transmitter is empty and reset when a character is present in the transmitter buffer or shift register. This feature simplifies the mode control software routines. In the bit synchronous mode, this bit sets when the ending flag pattern is sent.

Residue Code [D_1 · D_3]

Since the data portion of an HDLC message can consist of any number of bits and not necessarily an integral number of characters, the MPSCC has special logic to determine and report when the end of frame flag has been received (that is, the boundary between the data field and the CRC character in the last few data characters that were just read).

When the end of frame condition is indicated (D_7 of status register 1 = 1) and there is a special receive condition interrupt (if enabled), the last bits of the CRC character are in the receiver buffer. The residue code for the frame is valid in the status register 1 byte associated with that data character. (SR1 tracks the received data in its own buffer).

The meaning of the residue code depends upon the number of bits per character specified for the receiver. The previous character refers to the last character read before the end of frame, and so on. See table 12.

Table 12. Residue Codes

D_3	D_2	D_1	Previous Character	2nd Previous Character
8 Bits per Character				
1	0	0	C C C C C C C C	C C C C C D D D
0	1	0	C C C C C C C C	C C C C D D D D
1	1	0	C C C C C C C C	C C C D D D D D
0	0	1	C C C C C C C C	C C D D D D D D
1	0	1	C C C C C C C C	C D D D D D D D
0	1	1	C C C C C C C C*	D D D D D D D D*
1	1	1	C C C C C C C D	D D D D D D D D
0	0	0	C C C C C C D D	D D D D D D D D
7 Bits per Character				
1	0	0	C C C C C C C	C C C C C D D
0	1	0	C C C C C C C	C C C C D D D
1	1	0	C C C C C C C	C C C D D D D
0	0	1	C C C C C C C	C C D D D D D
1	0	1	C C C C C C C	C D D D D D D
0	1	1	C C C C C C C*	D D D D D D D*
0	0	0	C C C C C C D	D D D D D D D
6 Bits per Character				
1	0	0	C C C C C C	C C C C C D
0	1	0	C C C C C C	C C C C C D
1	1	0	C C C C C C	C C C D D D
0	0	1	C C C C C C	C C D D D D
1	0	1	C C C C C C	C D D D D D
0	0	0	C C C C C C	D D D D D D
5 Bits per Character				
1	0	0	C C C C C*	D D D D D*
0	1	0	C C C C D	D D D D D
1	1	0	C C C D D	D D D D D
0	0	1	C C D D D	D D D D D
0	0	0	C D D D D	D D D D D

Notes: C = CRC bit
D = Valid data
* = No residue

Special Receive Condition Flags

The status bits described below—parity error (if parity as a special receive condition is enabled), receiver overrun error, CRC/framing error, and end of HDLC frame—all represent special receive conditions.

When any of these conditions occur and interrupts are enabled, the MPSCC issues an interrupt request. In addition, if a condition affect vector mode is enabled, the vector generated (and the contents of SR2B for nonvectored interrupts) is different from that of a received character available condition. Therefore, it is not necessary to analyze SR1 with each character to determine if an error has occurred.

Also, the parity error and receiver overrun error flags are latched. That is, once one of these errors occurs, the flag remains set for all subsequent characters until reset by the error reset command. Therefore read SR1 only at the end of a message to determine if either of these errors occurred anywhere in the message. The other flags are not latched and follow each character available in the receiver buffer.

Parity Error [D_4]: This bit is set and latched when parity is enabled and the received parity bit does not match the sense (odd or even) calculated from the data bits.

Receiver Overrun Error [D_5]: This error occurs and is latched when the receiver buffer already contains three characters and a fourth character is completely received, overwriting the last character in the buffer.

CRC/Framing Error [D_6]: In the asynchronous mode a framing error is flagged (but not latched) when no stop bit is detected at the end of a character (RxD is low one bit time after the center of the last data or parity bit). When this condition occurs, the MPSCC waits an additional one-half bit time before sampling again so that the framing error is not interpreted as a new start bit.

In the synchronous mode, this bit indicates the result of the comparison between the current CRC result and the appropriate check value. It is usually set to one, since a message rarely indicates a correct CRC result until correctly completed with the CRC check character. Note that a CRC error does not result in a special receive condition interrupt.

End of HDLC Frame [EOF] [D_7]: This status bit is used only in the bit synchronous mode to indicate that the end of frame flag has been received and that the CRC error flag and residue code are valid. This flag can be reset at any time by issuing an error reset command. The MPSCC also automatically resets this bit when the first character of the next message is sent.

Status Register 2B

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector							

Interrupt Vector [D_0 - D_7 - Channel B Only]

Reading status register 2B returns the interrupt vector that is programmed into control register 2B. If a condition affects vector mode is enabled, the value of the vector is modified as shown in table 13.

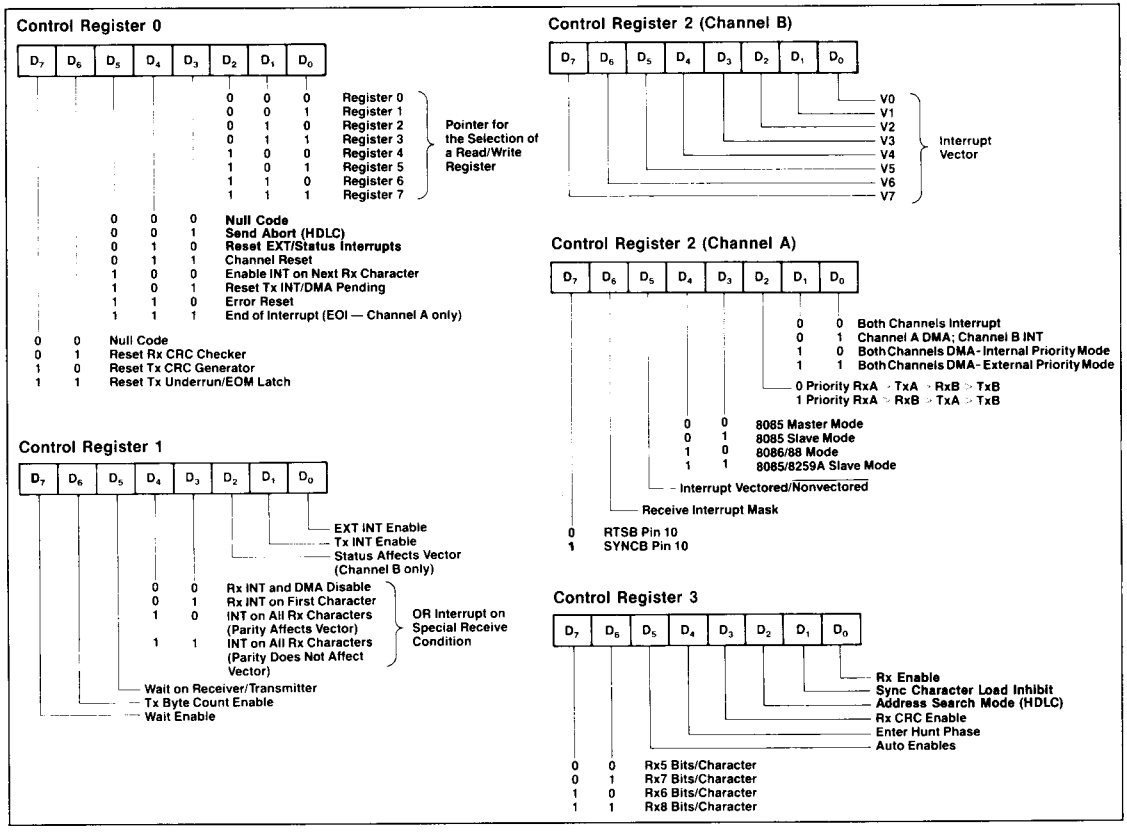
Code 111 can mean either channel A special receive condition or no interrupt pending. Examine the interrupt pending bit (D_1 of status register 0, channel A), to distinguish which it means. In a nonvectored interrupt mode, the vector register must be read first for the interrupt pending to be valid.

Table 13. Condition Affects Vector Modifications

Interrupt Pending (SR0, D_1 Channel A)	8085 Modes / 8086 Modes	D_4 / D_2	D_3 / D_1	D_2 / D_0	Condition
0		1	1	1	No interrupt pending
1		0	0	0	Channel B transmitter buffer empty
1		0	0	1	Channel B external/status Change
1		0	1	0	Channel B received character available
1		0	1	1	Channel B special receive condition
1		1	0	0	Channel A transmitter buffer empty
1		1	0	1	Channel A external/status change
1		1	1	0	Channel A received Character available
1		1	1	1	Channel A special receive condition

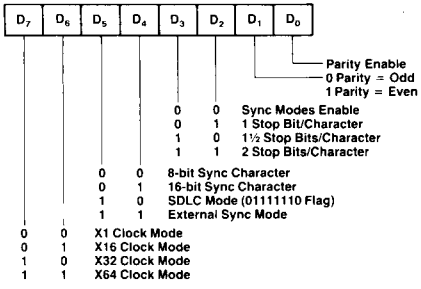
2

Status Register Bit Functions (Sheet 1 of 2)

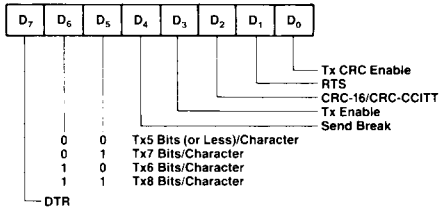


Status Register Bit Functions (Sheet 2 of 2)

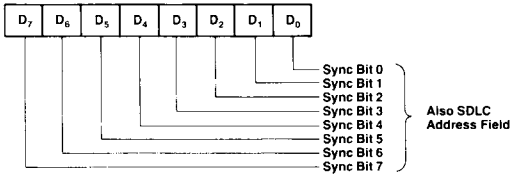
Control Register 4



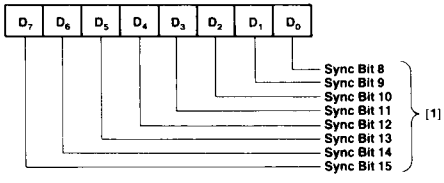
Control Register 5



Control Register 6



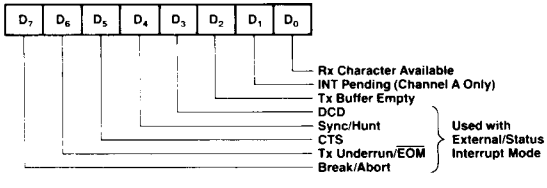
Control Register 7



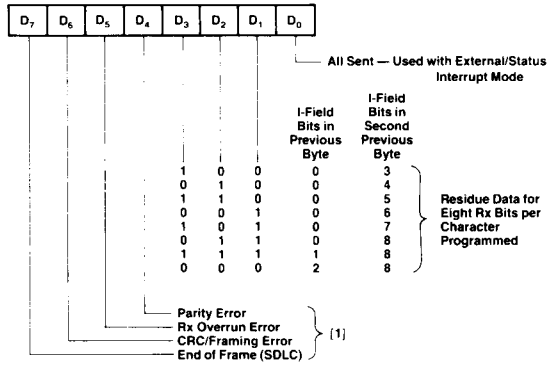
Note:

[1] For SDLC it must be programmed to 01111110 for flag recognition.

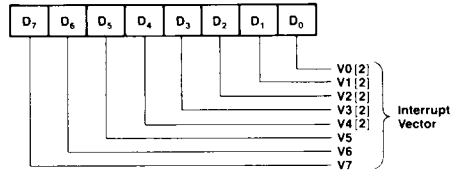
Status Register 0



Status Register 1



Status Register 2B

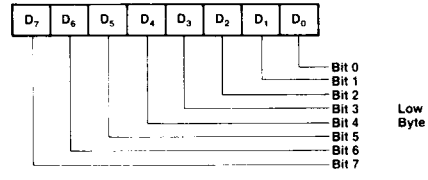


Note:

[1] Used with special receive condition mode.

[2] Variable if Status Affects Vector is programmed.

Status Register 3 (Tx Byte Count Register)



Status Register 4 (Tx Byte Count Register)